



PSMN030-60YS

N-channel LFPAK 60 V 24.7 mΩ standard level MOSFET

Rev. 02 — 25 October 2010

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in LFPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPAK provides maximum power density in a Power SO8 package

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

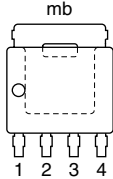
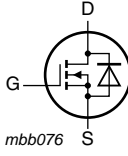
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	60	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1	-	-	29	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	56	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A};$ $T_j = 100\text{ °C};$ see Figure 12	-	-	39.5	mΩ
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A};$ $T_j = 25\text{ °C};$ see Figure 13	-	19.1	24.7	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 15\text{ A};$	-	3	-	nC
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30\text{ V};$ see Figure 14 ; see Figure 15	-	13	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LPAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN030-60YS	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}$; see Figure 1	-	21	A
		$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$; see Figure 1	-	29	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	116	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	56	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{slid(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	29	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	116	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 29\text{ A}; V_{sup} \leq 60\text{ V}; R_{GS} = 50\text{ }\Omega$; unclamped	-	23	mJ

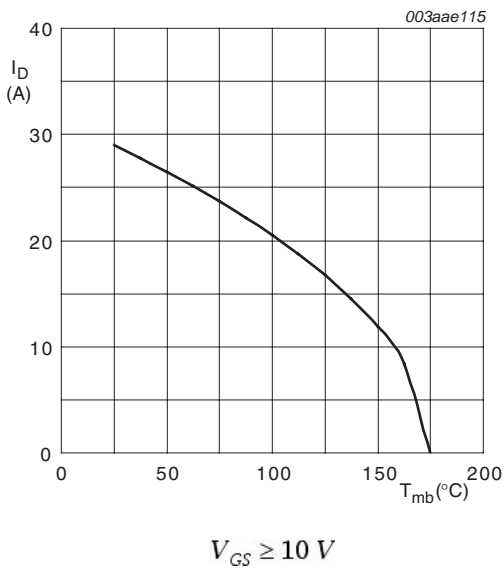


Fig 1. Continuous drain current as a function of mounting base temperature

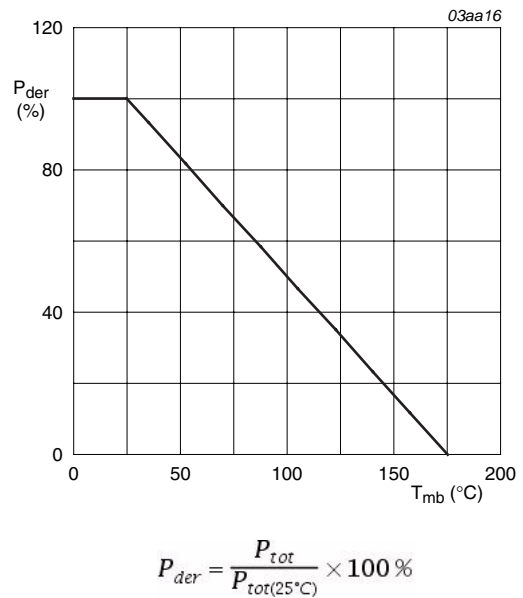
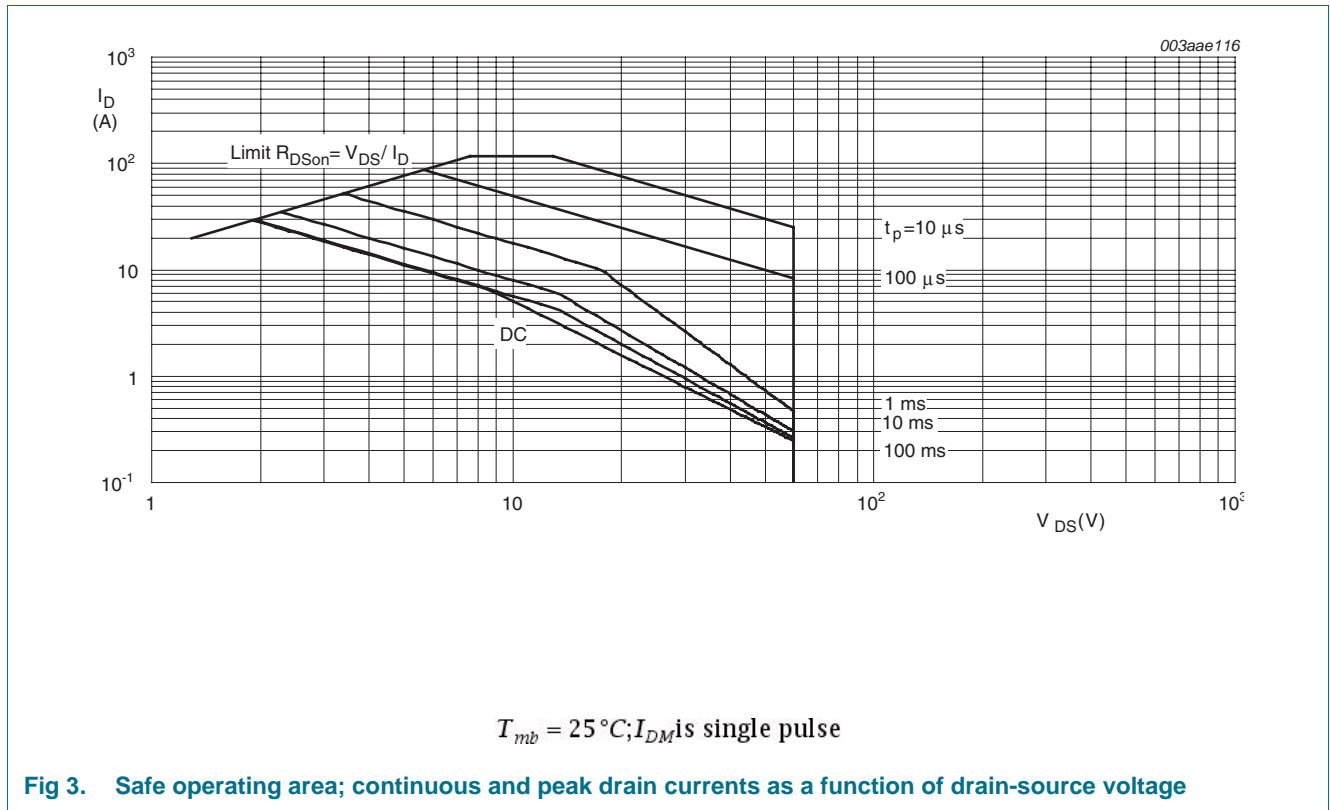


Fig 2. Normalized total power dissipation as a function of mounting base temperature



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2.7	K/W

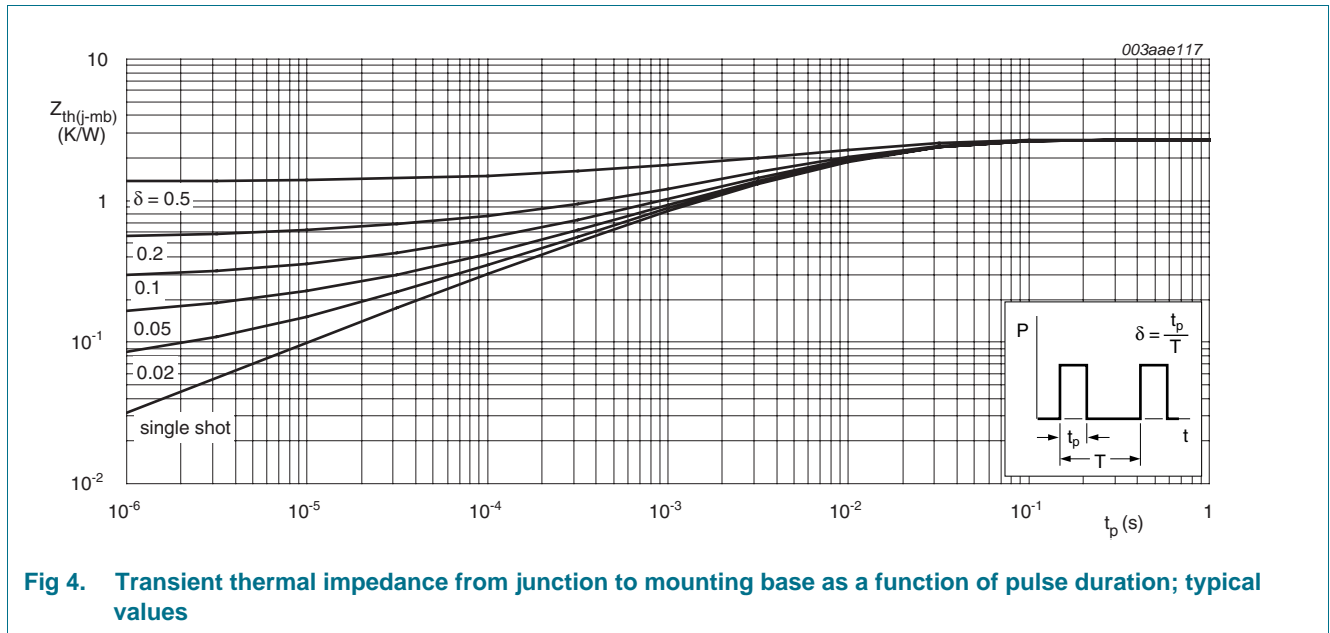


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

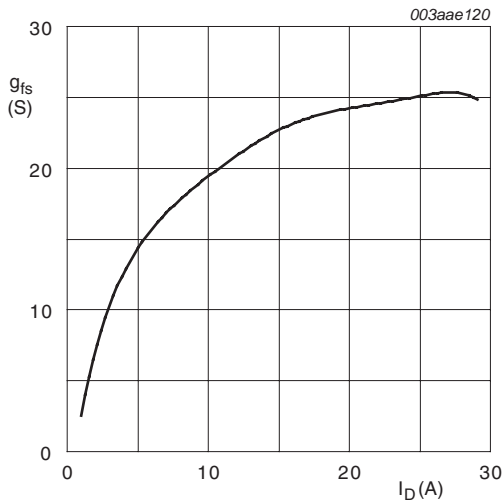
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	54	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11	2	3	4	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 11	-	-	4.7	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 11	1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	50	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 12	-	49.6	56.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see Figure 12	-	-	39.5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 13	-	19.1	24.7	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	0.98	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 15 \text{ A}; V_{DS} = 30 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15	-	13	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	10	-	nC
Q_{GS}	gate-source charge	$I_D = 15 \text{ A}; V_{DS} = 30 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14	-	4	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	2.2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.6	-	nC
Q_{GD}	gate-drain charge	$I_D = 15 \text{ A}; V_{DS} = 30 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15	-	3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 30 \text{ V};$ see Figure 14 ; see Figure 15	-	4.7	-	V
C_{iss}	input capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 16	-	686	-	pF
C_{oss}	output capacitance		-	109	-	pF
C_{rss}	reverse transfer capacitance		-	69	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 2 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 4.7 \text{ } \Omega$	-	10	-	ns
t_r	rise time		-	6	-	ns
$t_{d(off)}$	turn-off delay time		-	19	-	ns
t_f	fall time		-	5	-	ns

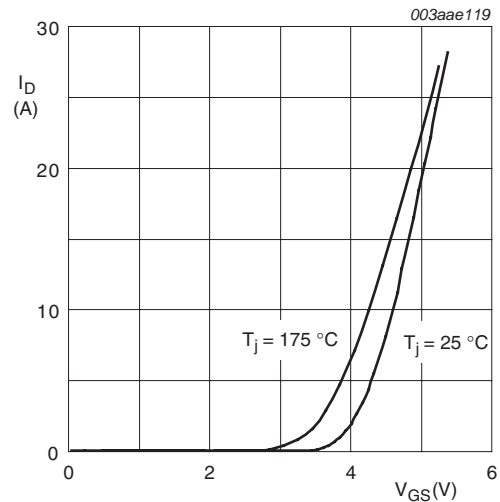
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 15\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17	-	0.87	1.2	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$;	-	25	-	ns
Q_r	recovered charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$	-	23	-	nC



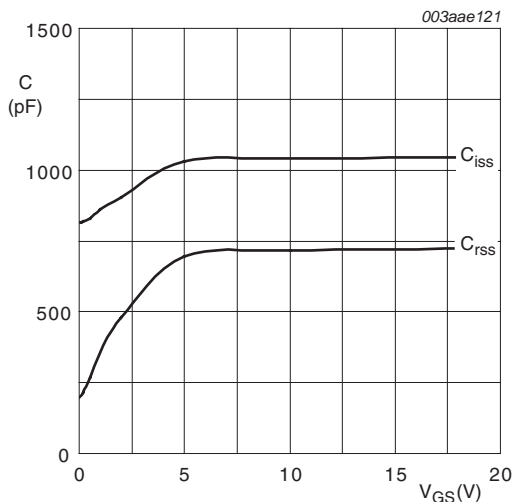
$T_j = 25\text{ °C}$; $V_{DS} = 10\text{ V}$

Fig 5. Forward transconductance as a function of drain current; typical values



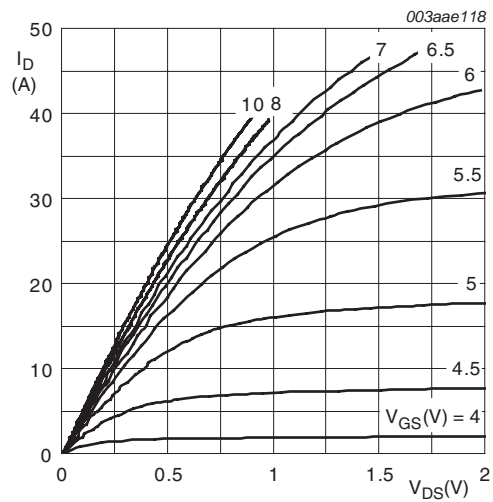
$V_{DS} > I_D \times R_{DS(on)}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



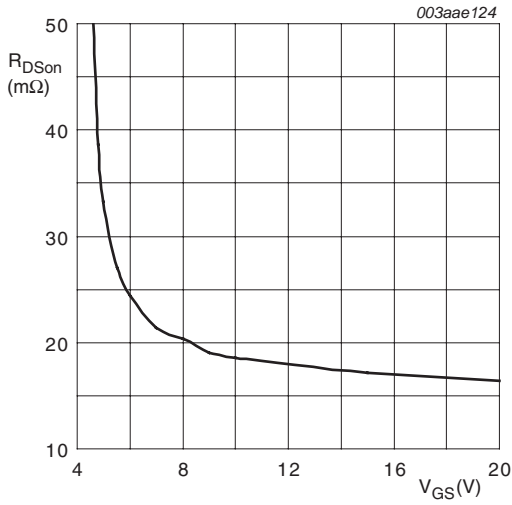
$V_{DS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



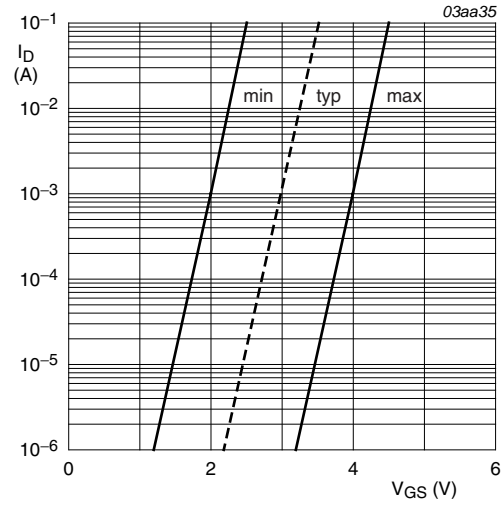
$T_j = 25\text{ °C}$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



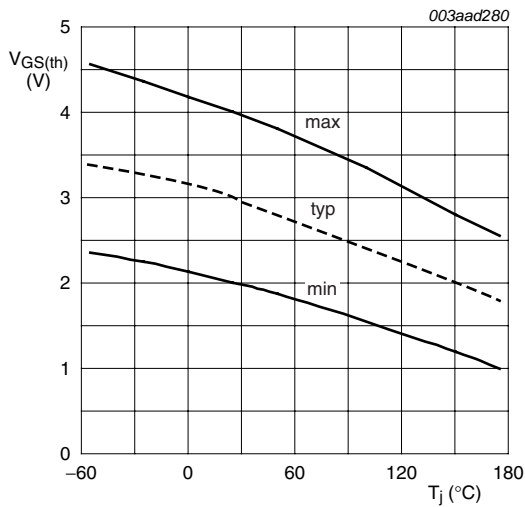
$T_j = 25^\circ\text{C}; I_D = 5\text{A}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values.



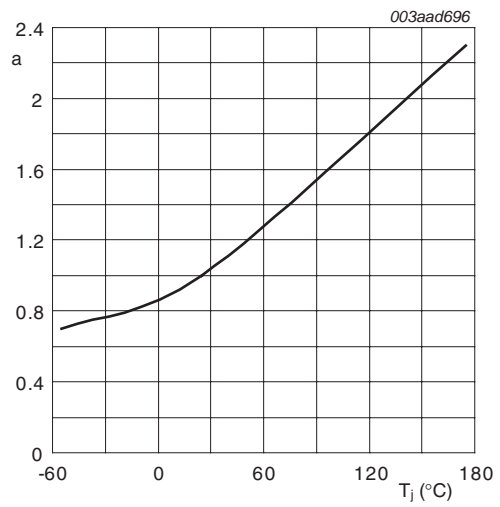
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature.

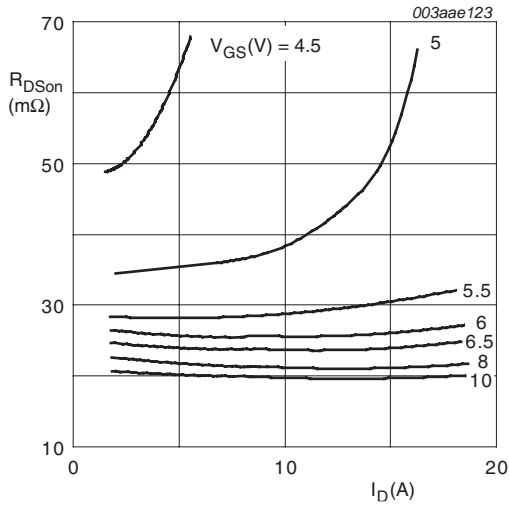


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

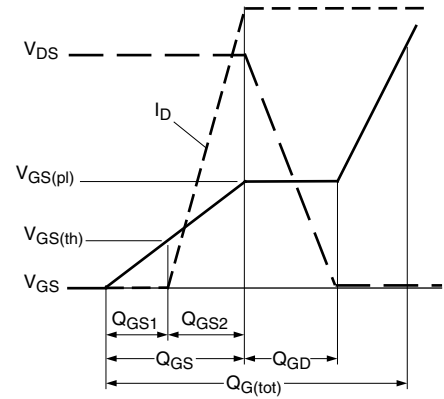


Fig 14. Gate charge waveform definitions

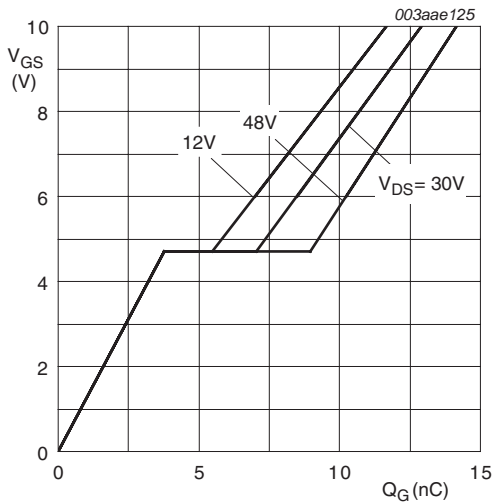


Fig 15. Gate-source voltage as a function of gate charge; typical values

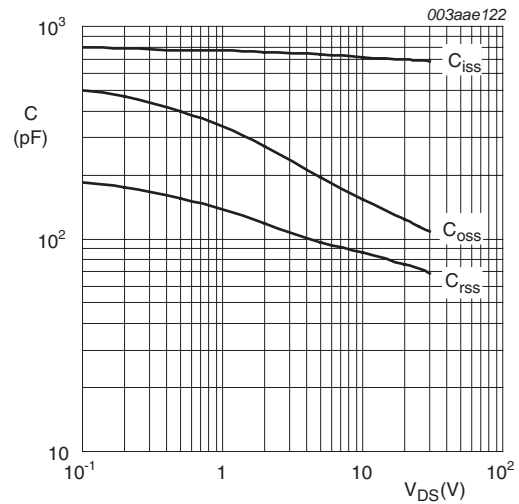


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

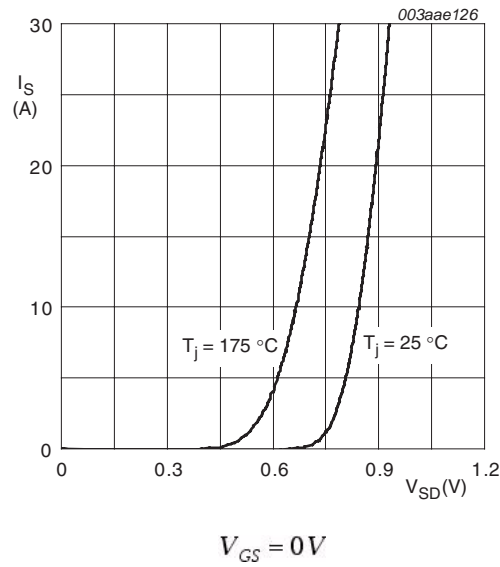


Fig 17. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

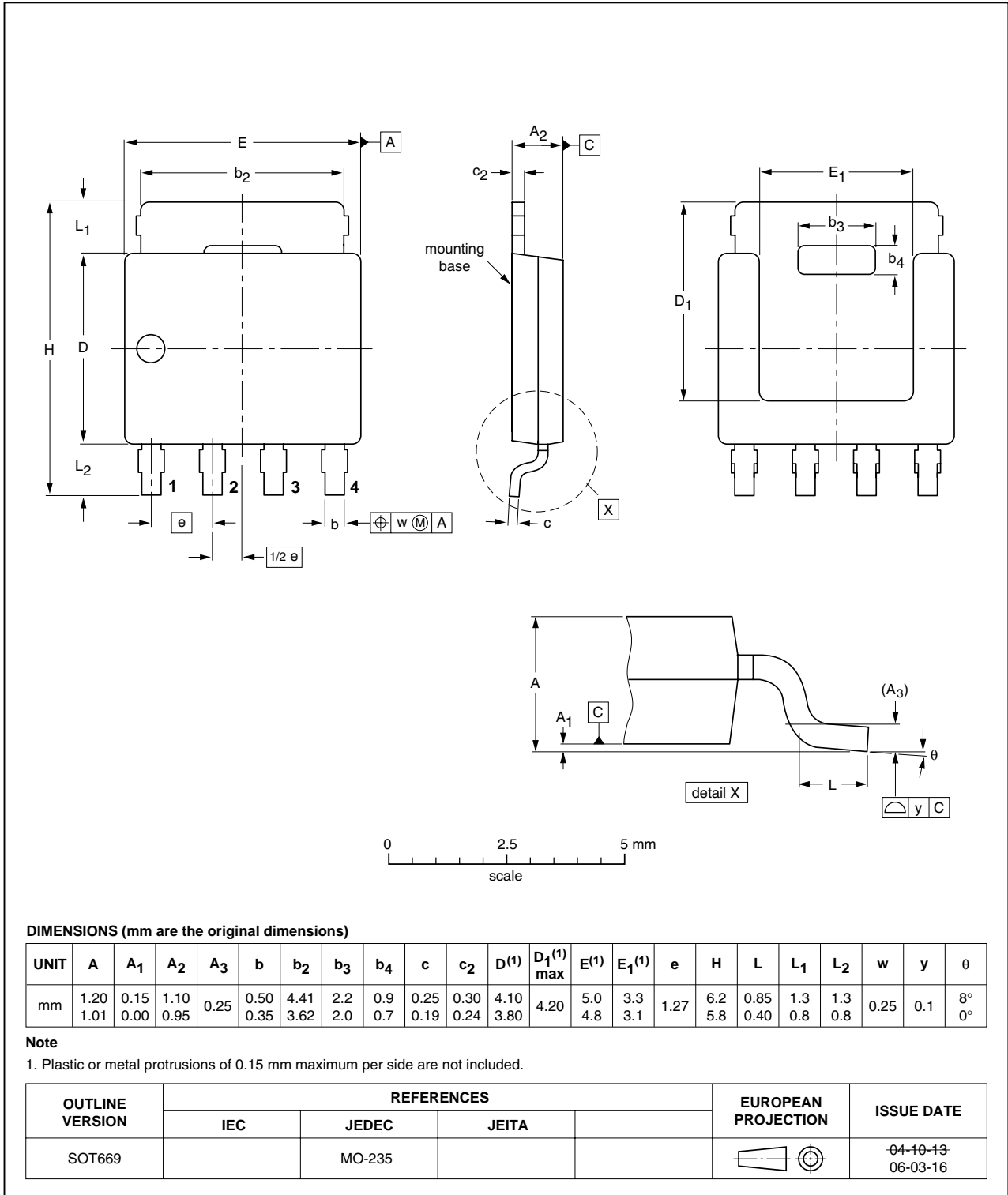


Fig 18. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN030-60YS v.2	20101025	Product data sheet	-	PSMN030-60YS v.1
Modifications:	<ul style="list-style-type: none">• Status changed from objective to product.• Various changes to content.			
PSMN030-60YS v.1	20100211	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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