General Description

The epc901 is a high-performance CCD line sensor capable of storing a total of 4 frames in the frame store elements for ultra high-speed image acquisition. The acquisition of the image is controlled by a control signal SHUTTER. The epc901 flags when a frame is ready for read-out by asserting the DATA_RDY signal. The transmission of the frame over the video amplifier is controlled by the external control signal READ. When a read-out is initiated by a pulse on the READ signal, it is sampled by a CDS stage. After a fixed delay the frame can be shifted out through the video amplifier by applying the appropriate amount of read clock edges.

The device offers various configuration options:

- Gain of the read-out stage selectable of 1, 2 or 4
- Transmission direction left to right and right to left
- Region of interest (ROI) center region (pixel 256 to 767)
- Binning of 2 or 4 pixels to reduce transmission time and noise
- Single- or multi-frame acquisition
- Clearing of frames stored and periodic flushing of pixel array to avoid blooming

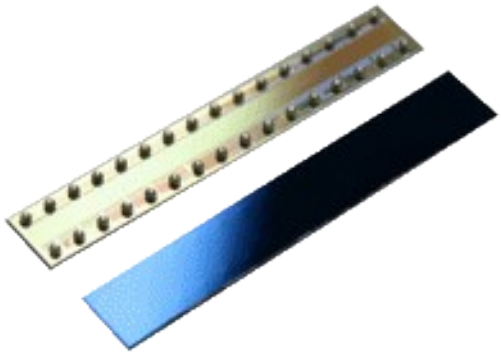


Figure 1: Backside illuminated CMOS/CCD imager

Features

- Photosensitive CCD array backside illuminated with 1024x1 pixel
- Very high frame rate
- Very high sensitivity due to 100% fill factor and ESPROS' unique OHC15L process technology
- Pixel size 7.5 x 120µm
- On-chip correlated-double sampling
- Single-ended or differential analog output
- Simple 5-pin control interface for acquisition and read-out
- I2C bus interface
- Internal clock source, trimmable
- Two on-chip temperature sensors
- Single supply voltage
- 32 Pin space saving CSP package
- Chip size L x W x T: 8.0 x 1.3 x 0.23 mm

Applications

- Linear and rotary encoder
- Triangulation light barrier / distance measurement
- Line sensor / camera
- Business card readers & portable scanners
- Multi-touch displays / electronic white boards
- Finger print readers
- Spectrometers
- Check & ticket readers
- Speed measurement
- Bar code readers

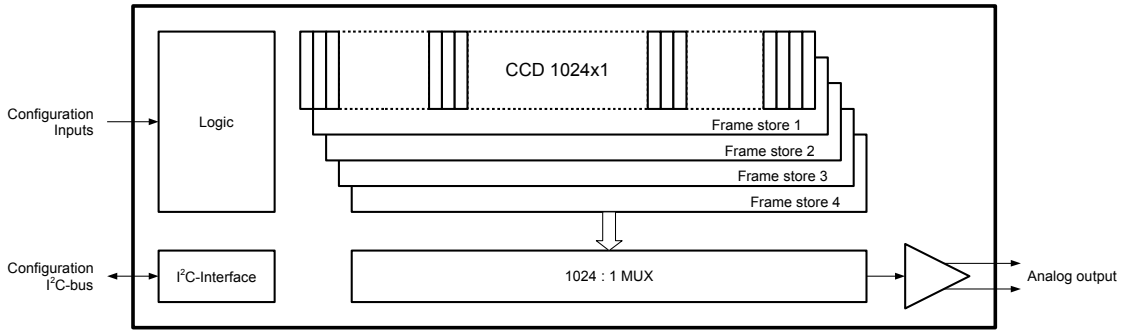


Figure 2: Block diagram

© 2020 ESPROS Photonics Corporation
Characteristics subject to change without notice

Table of Contents

1. Block diagram ... 3
2. Pin-out ... 3
2.1. Power domains ... 5
3. Electrical, optical and timing characteristics ... 6
3.1. Electrical and other characteristics ... 6
3.2. Temperature sensor characteristics ... 7
3.3. Timing parameters ... 7
3.4. Absolute maximum ratings ... 8
3.5. Optical characteristics ... 9
3.6. Frequency response ... 10
3.7. Video amplifier frequency response ... 10
4. Configuration ... 11
5. Imager operation ... 12
5.1. General remarks ... 12
5.2. Single frame acquisition ... 12
5.3. Multi frame acquisition ... 13
5.4. Image readout ... 13
5.5. ROI / binning read clock ... 14
5.6. Flush ... 14
6. Various features ... 15
6.1. Temperature sensor ... 15
6.2. Power-down ... 15
6.3. Oscillator clock trimming ... 15
6.4. Reset ... 15
7. I2C interface ... 16
7.1. I2C communication ... 16
7.1.1. Device addressing ... 16
7.1.2. Single-byte write ... 16
7.1.3. Multi-byte write ... 16
7.1.4. Single-byte read ... 17
7.1.5. Multi-byte read ... 17
7.1.6. Software reset ... 17
7.1.7. Device address sampling ... 17
7.1.8. Setup latency ... 17
7.2. I2C bus timing ... 18
8. Register description ... 19
8.1. Binning, amplifier gain, ROI, read direction ... 19
8.2. Video Amplifier bandwidth ... 20
8.3. Video amplifier bandwidth, noise and current consumption ... 20
8.4. Configuration control, video amplifier on/off ... 20
8.5. Video amplifier SE/Diff, charge pump on/off, 5V regulator on/off ... 21
8.6. Oscillator trimming (fine) ... 21
8.7. Oscillator trimming (coarse) ... 22
8.8. Temperature sensors read ... 22
8.8.1. Left temperature sensor ... 22
8.8.2. Right temperature sensor ... 22
8.9. Temperature sensors control ... 23
8.10. I2C error flag ... 23
8.11. Chip revision ... 23
9. Application information ... 24
9.1. Differential mode ... 24
9.2. Single ended mode ... 25
9.3. External components ... 25
9.4. Low noise operation ... 25
9.4.1. Charge pump noise ... 25
9.4.2. Video amplifier noise ... 25
9.4.3. Layout recommendations ... 26
10. Power consumption considerations ... 27
10.1. General considerations ... 27
10.2. Low power operation ... 27
11. Layout and packaging information ... 28
11.1. Mechanical dimensions ... 28
11.2. PCB design and SMD manufacturing process considerations ... 29
11.3. Tape & Reel Information ... 29
11.4. Soldering and IC handling ... 29
12. Self-test mode by fill-and-spill ... 30
13. Ordering Information ... 31
14. IMPORTANT NOTICE ... 32

© 2020 ESPROS Photonics Corporation
Characteristics subject to change without notice

1. Block diagram

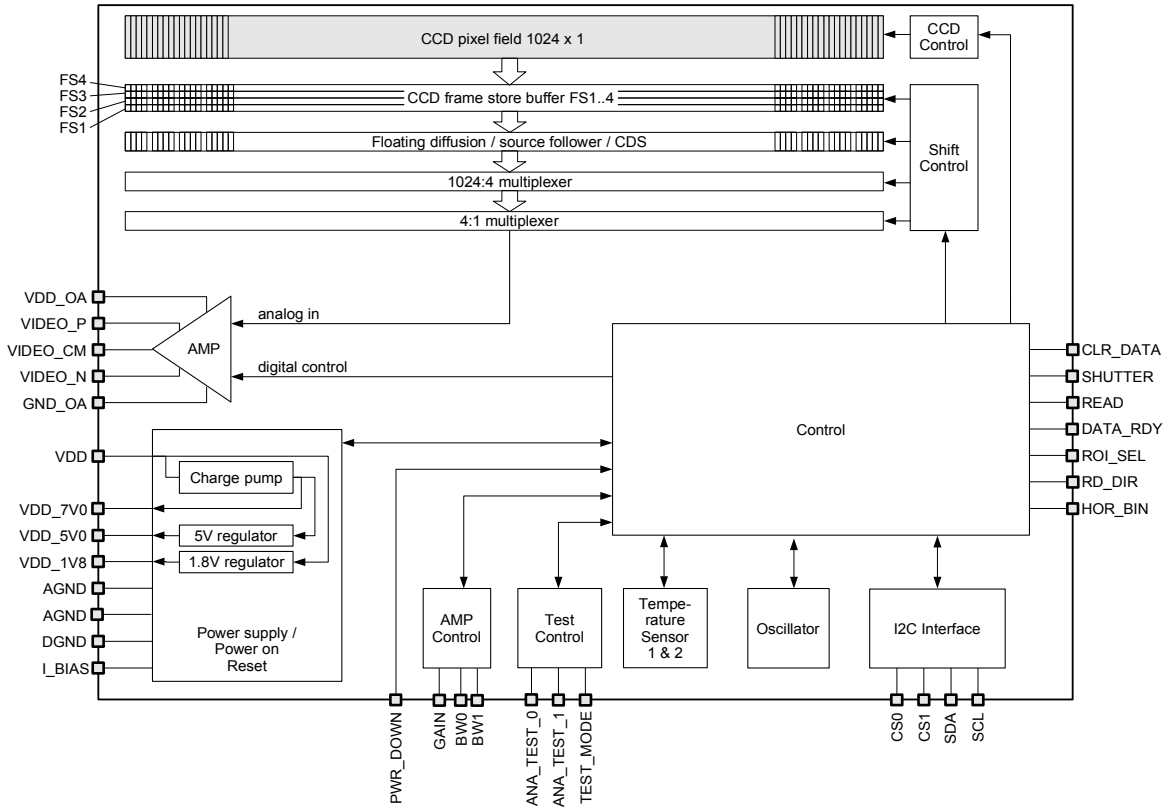


Figure 3: Block diagram

2. Pin-out

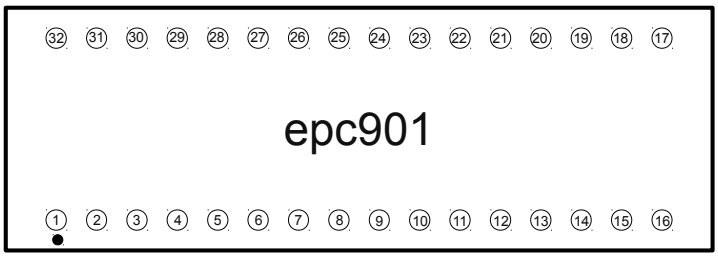


Figure 4: Pin-out, view to the photo-sensitive side (top-view)

Pin no.	Pin name	Pin type	Default [V]	Description
Digital pins				
2	PWR_DOWN	DI	0	Power-down mode enable
3	CLR_DATA	DI	0	Clear internal data memory controller
5	CLR_PIX	DI	0	Rising edge resets pixels and its controller
6	SHUTTER	DI	0	Exposure active when SHUTTER set
12	READ	DI	0	Read-out control and read clock
4	DATA_RDY	DO		Flag when data on video interface is ready. Used as a strap pin to turn on/off the charge pump
13	SDA	DIOD	VDD	I2C serial data (open drain)
14	SCL	DIOD	VDD	I2C serial clock (open drain)
15	ROI_SEL	DI	0	Region of interest selection
17	CS1	TER	VDD/2	I2C chip select 1
19	CS0	TER	VDD/2	I2C chip select 0
21	GAIN	TER	VDD/2	Select gain of read-out path
22	BW0	TER	VDD/2	LSB of bandwidth of video amplifier
23	BW1	TER	VDD/2	MSB of bandwidth of video amplifier
24	RD_DIR	DI	0	Read-out direction
25	HOR_BIN	TER	VDD/2	Horizontal binning selection
30	TEST_MODE	DI	0	Chip test
Analog pins				
8	VIDEO_N	AO		Negative terminal of video output
9	VIDEO_P	AO		Positive terminal of video output
11	VIDEO_CM	AI	VDD/2 or 0	Voltage to set video output common-mode
27	I_BIAS	AI		Bias current
28	ANA_TEST_1	AIO	0	Analog test in-/output 1
29	ANA_TEST_0	AIO	0	Analog test in-/output 0, rising edge indicates the last pixel in a frame
Supply pins				
26	VDD	Supply		Positive chip supply voltage
10	VDD_OA	Supply		Positive supply of video amplifier
32	VDD_1V8			Decoupling
18	VDD_5V0	AO / Supply		Decoupling / external 5V supply for low power consumption (refer to 10.2.)
20	VDD_7V0			Decoupling
16	AGND	Supply		Analog ground
1	AGND	Supply		Analog ground
7	GND_OA	Supply		Video amplifier ground
31	DGND	Supply		Digital ground

Definitions:

- DI: Digital input pin, with an internal pull-down resistor of approx. 100-250kΩ
- DO: Digital output pin
- DIOD: General purpose bidirectional digital pin with open-drain output, requires external pull-up resistor
- AO: Analog output
- AI: Analog input
- AIO: Analog input and output
- TER: Ternary input pin, with a pull-down and an equal pull-up resistor of approx. 100-250kΩ which tie the pin to the VDD/2 state.

2.1. Power domains

The epc901 chip has internally 5 different power domains and 3 ground references which are interconnected with ESD protection diodes. All pins are also equipped with ESD protection diodes. Figure 5 shows this functional circuit. The diodes have a breakthrough voltage of 0.3V. The designer has to take care that none of these diodes become conductive either at power-up, power-down or normal operation.

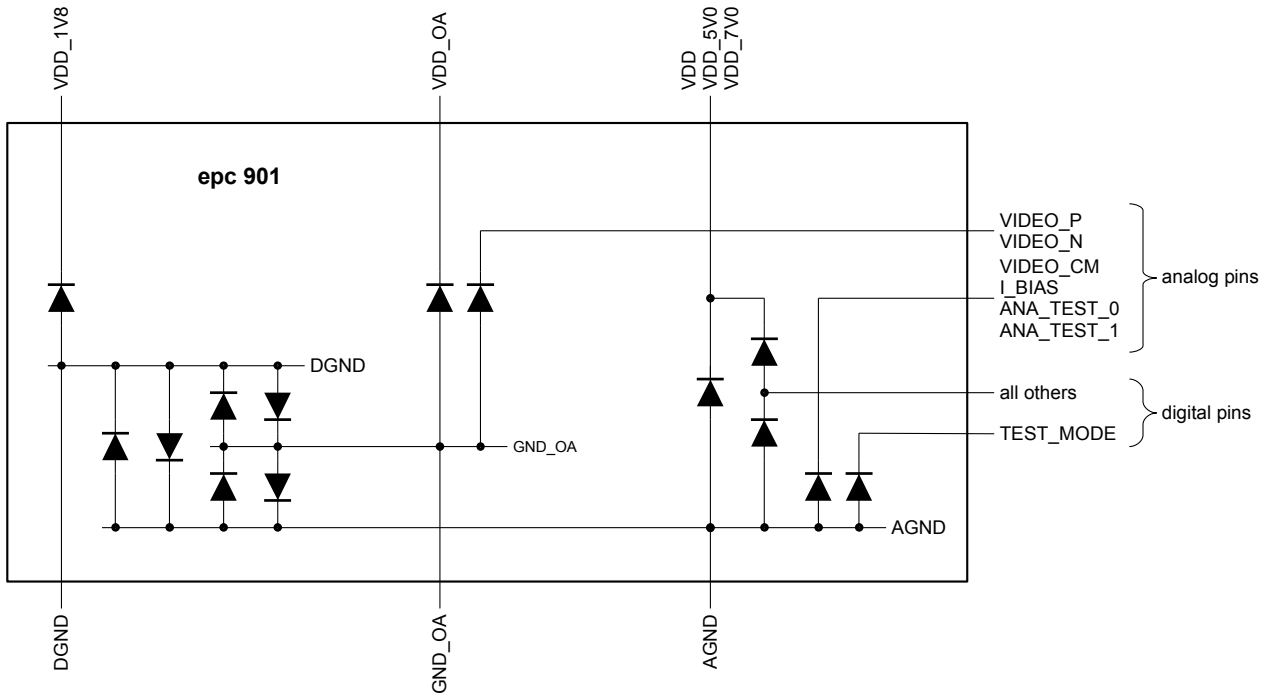


Figure 5: ESD protection diode circuit

3. Electrical, optical and timing characteristics

(T_A = 25°C, V_{DD} = 3.0V unless otherwise noted)

3.1. Electrical and other characteristics

Parameter	Description		Min	Typ	Max	Unit
$V_{DD\ Nominal}$	Nominal supply voltage on VDD and VDD_OA		2.70	3.00	3.45	V
	Supply voltage on VDD and VDD_OA with Read Clock of max. 1 MHz.		2.45			
PSRR	Power supply rejection ratio VDD and VDD_OA.	Differential		13		dB
		Single ended		9		dB
I_{DD}+I_{DD_OA} [1]	Total current consumption on pins VDD and VDD_OA (refer to section 10.)					
	Differential mode, full video bandwidth, 46kfps [2], Charge pump: ON Temperature sensors: ON	Idle mode (READ = L)		26	39	mA
		Peak, during read-out		48	72	mA
	Differential mode, full video bandwidth, 46kfps [2], external VDD5V0 supply [3] Charge pump: OFF Temperature sensors: OFF	Idle mode (READ = L)		10	15	mA
		Peak, during read-out		16	24	mA
	Differential mode, low video bandwidth, 1kfps [4], external VDD5V0 supply [3] Charge pump: OFF Temperature sensors: OFF	Idle mode (READ = L)		6.0	9.0	mA
		Peak, during read-out		6.0	9.0	mA
	Single-ended mode, low video bandwidth, 1kfps [4] Charge pump: ON Temperature sensors: ON	Idle mode (READ = L)		21	30	mA
		Peak, during read-out		40	60	mA
	Single-ended mode, low video bandwidth, 1kfps [4], external VDD5V0 supply [3] Charge pump: OFF Temperature sensors: OFF	Idle mode (READ = L)		5.0	10.0	mA
		Peak during read-out		5.0	10.0	mA
	Power-Save mode (POWR_DOWN = H, shutter still working), external VDD5V0 supply [3] Charge pump: OFF Temperature sensors: OFF			1.3	2	mA
	In-rush current at power-up during approximately 5ms Charge pump: ON			60	90	mA
	In-rush current at power-up during approximately 2ms, external VDD5V0 supply [3] Charge pump: OFF			50	75	mA
I_{DD_5V}	Current consumption on pin VDD_5V0 [3], Differential/single-ended mode, full video bandwidth, 46kfps [2] external VDD5V0 supply [3]) Charge pump: OFF			1.2	2.5	mA
V_{DIL}	Low voltage level on binary digital inputs [5] (Level L)				0.2*V_{DD}	V
V_{DIH}	High voltage level on binary digital inputs [5] (Level H)		0.5*V_{DD}			V
V_{DOL}, V_{TERIL}	Low voltage level on binary and ternary digital outputs (Level L)				0.2*V_{DD}	V
V_{DOH}, V_{TERIH}	High voltage level on binary and ternary digital outputs (Level H)		0.8*V_{DD}			V
V_{TERIM}	Centre voltage level on ternary digital inputs (Level M)		0.4*V_{DD}		0.6*V_{DD}	V
I_{DI}	Sink current at digital inputs				10	µA
R_{DI}	Internal pull-down resistor		100		250	kΩ
R_{TER}	Internal voltage dividing resistors which force the input to VDD/2		100		250	kΩ
I_{DO}	Sink / source current at digital outputs				3	mA
V_{VDD1V8}	Internally generated voltage on pin VDD1V8		1.62	1.8	1.98	V
V_{VDD5V0}	Internally generated voltage on pin VDD5V0		4.5	5.0	5.5	V
V_{VDD7V0}	Internally generated voltage on pin VDD7V0		6.0	6.5	7.0	V
$V_{VIDEO_P,N}$	Voltage range at output of video amplifier (@ gain 1)		0.25		V_{DD}-0.25	V
V_{CM_SE}	Voltage at VIDEO_CM to select single-ended mode				0.4	V

Parameter	Description		Min	Typ	Max	Unit
V_{CM_D}	Common-mode voltage in differential mode, set on pin VIDEO_CM. Note: For V_{CM_D}>1V, differential mode is detected automatically by default. For V_{CM_D}<1V, differential mode has to be enabled by setting bit AMP_OVR in register FORCE_ANA_CTRL_SIGS (see section 8.)		0.5	$V_{DD}/2$	$V_{DD}/2+0.1$	V
$R_{IN,CM}$	Input resistance of VIDEO_CM		100			kΩ
$CMRR_{CM}$	Common-mode rejection ratio on VIDEO_CM (f ≥ 100 kHz)	100kHz … 50MHz		17		dB
		100kHz … 10Mhz		24		dB
$V_{OFF,VIDEO,CM}$	Common-mode offset of video amplifier output				±50	mV
$V_{OFF,VIDEO,SIG}$	Signal offset of video amplifier output				±100	mV
C_{LVIDEO}	Load capacitance on video output	single ended	5		100	pF
		differential	5		25	pF
$R_{INT,VIDEO}$	Output resistance of the video amplifier	single ended		32	100	Ω
		differential		11	100	Ω
R_{LVIDEO}	Load resistance on video output		3			kΩ
$R_{th\ J\text{-}A}$	Thermal resistance junction - ambient			65		K/W

Notes:
[1] The current values change with the first Read Pulse after boot-up to these values
[2] Video amplifier BW = HIGH_BW, VIDEO_GBW_SEL_REG = 0x3
[3] VDD5V0 has only to be supplied externally in case the charge pump is configured to be off. See section 10.2.
[4] Video amplifier BW = LOW_BW, VIDEO_GBW_SEL_REG = 0x0.
[5] I2C pins SCL and SDA are according to I2C standards

3.2. Temperature sensor characteristics

Parameter	Description	Min	Typ	Max	Unit
T_{TEMP}	Temperature measurement range	-40		+85	ºC
$OFFSET_{TEMP}$	Temperature sensor offset		$-10.1 \cdot 10^3$		LSB
$GAIN_{TEMP}$	Temperature sensor gain. The typical measured temperature value of e.g. the left temperature sensor can be calculated from the value of the sensor output registers TEMP_SENS_L_MSB and TEMP_SENS_L_LSB as follows: $T_{TEMP_L} = \frac{TEMP_L[12:0] - OFFSET_{TEMP}}{GAIN_{TEMP}}$ [K] For accurate measurements measurements, calibration is required.	24	48	96	LSB/K
P_{TS}	Resolution of the temperature sensors		13		bits
N_{TEMP}	Noise		2	4	LSB
LIN_{TEMP}	Linearity of temperature sensors over the full temperature range		±2	±4	K
f_{TEMP}	Update rate of the temperature sensors (configurable)	0.1		10	Hz

3.3. Timing parameters

Parameter	Description		Min	Typ	Max	Unit
$T_{STARTUP}$	Start-up time after applying external supply/supplies (includes ramp-up of charge pump)				10	ms
T_{CP_UP}	Charge pump power-up time: time from changing the bit CP_PD from 1 to 0 until chip is operational (internal VDD5V)				5	ms
T_{WAKE_UP}	Wake-up time from Power-Save mode			7	12	µs
f_{OSC}	Oscillator clock frequency at nominal trim value (OSC_TRIM_REG at default value), refer to section 6.3.	room temperature	22.4	36	48	MHz
		-20°C < T_A < 65°C	18	36	50 [3]	MHz
R_{VIDEO}	Frame rate on video output		1	44	47 [4]	kfps
$T_{SU,CONF}$	Setup time of configuration pins with respect to rising edge of read pulse		50			ns

Parameter	Description	Min	Typ	Max	Unit
$T_{H,CONF}$	Hold time of configuration pins with respect to rising edge of read pulse	3			Oscillator clock cycles
$T_{SHUTTER}$	Pulse width of SHUTTER signal	5			Oscillator clock cycles
T_{FLUSH}	Flush period [1]	30		32	Oscillator clock cycles
T_{SHIFT}	Shift period [1]	24		26	Oscillator clock cycles
T_{RD_PULSE}	Pulse width of Read Pulse	3			Oscillator clock cycles
T_{CDS}	CDS operation			37	Oscillator clock cycles
T_{STORE}	Duration how long a frame may be stored in the frame-store	10			ms
f_{READ}	READ clock rate [2]	0.1		54	MHz
D	READ clock duty cycle @ f_{READ} max	45	50	55	%
$T_{H,VIDEO}$	Period during which the output of the video amplifier is held stable after the last read clock edge		50		µs
$T_{PERIOD,FLUSH}$	Periodicity of the periodic flush operation [5]		100		ms
T_{PULSE,CLR_DATA}	Pulse width on CLR_DATA	3			Oscillator clock cycles
$B_{3dB,VIDEO}$	3dB-bandwidth of video output @ C_{LVIDEO} = 40pF	10	11		MHz

Notes:
[1] The duration of the flush and shift periods can be calculated exactly by measurement of the clock oscillator frequency (see section 6.3.)
[2] To achieve the maximum clock frequency, the duty cycle of the read clock has to be 50% with a maximal tolerance of ±5%.
[3] The oscillator shall not be trimmed to a frequency higher than 50MHz.
[4] At max. f_{OSC}
[5] Refer to section 5.6. for more details.

3.4. Absolute maximum ratings

Description	Conditions
Power supply voltage (VDD)	-0.3V to +5V
Voltage to any Pin	-0.3 to VDD +0.3V
Operating and storage Temperature Range (T_S)	-40°C to +85°C
Relative humidity	0 to 95% non-condensing
ESD rating	all pins except VDD7V0 vs. VDD1V8: HBM class 2 (2kV to <4kV, JEDEC) Pin VDD7V0 vs. VDD1V8: HBM class 1B (500V to <1kV, JEDEC) Note: Pin VDD7V0 is in the final circuit loaded with 2.2µF low ESR capacitor.

3.5. Optical characteristics

(Gain 1, video bandwidth 1MHz, differential mode)

Parameter	Description		Min	Typ	Max	Unit
W_{PIX}	Width of pixels			7.5		µm
H_{PIX}	Height of pixels			120		µm
N_{PIX}	Number of pixels			1024		
N_{FS}	Number of frames stored on-chip (including the pixel array)			4		
FF	Optical fill factor in pixel array			100		%
CG	Conversion gain (standard version)		3	5	8	µV/e-
	Optical sensitivity (λ = 630 nm, gain = 1)			71		V/(Lux*s)
FW [4]	Full-well capacity per frame		400			ke-
N_{READ_D}	Read noise, differential mode, optimal settings [1]			700	1000	µVrms
N_{READ_SE}	Read noise, single ended mode, optimal settings [1]			500	700	µVrms
LIN	Linearity[2]	Differential mode		1.0	2.0	%
		Single-ended mode		2.0	4.0	%
I_{LAG}	Image lag @ max. Vpp and @ 400ke-	Single-frame acquisition (see section 5.2)			0.2	%
		Multi-frame acquisition (see section 5.3)		0.3	0.5	%
$\delta V_{DARK,PIX}$	Output voltage drift due to dark current in pixel area			1.0	10.0	V/s
$\delta V_{DARK,FS}$	Output voltage drift due to dark current in frame store area			0.3	0.6	V/s
Θ_{DARK}	Thermal drift of dark current		Doubles approx. every 8°K			
PRNU[3]	Photo response non-uniformity (@ 0.5*FW[4])			2	6	%
DSNU[3]	Dark pixel non-uniformity @ T_{EXP} = 100 µs			±0.3		% FW
M_{FW}	Irradiance to generate FW electrons per pixel in 1 ns (λ = 630 nm)			155		mW/mm^2
	Surface reflectivity (@ 550 to 860 nm, 0° incident angle)			2		%
	Surface reflectivity (@ 550 to 860 nm, 30° incident angle)			4		%
	Pixel cross-talk (@ 630nm, 0° incident angle)			20		%
	Cross-talk width @ 1σ			4		µm

Table 1: Optical specification

Notes:

[1] Charge pump off, temp sensor off, video amplifier BW=LOW_BW, VIDEO_GBW_SEL_REG=0x0 (minimum video amplifier bias current, Read Clock 1MHz).

[2] The linearity is defined as the maximum deviation of the pixel responses between 10% and 80% FW[4] from the straight line between 10% and 80% FW[4]. Pixels with high dark current excluded.

[3] Valid for Pixel 3 .. 1020.

[4] FW corresponds to 2V swing at the output in differential mode.

Figure 6 shows the typical quantum efficiency as a function of wavelength.

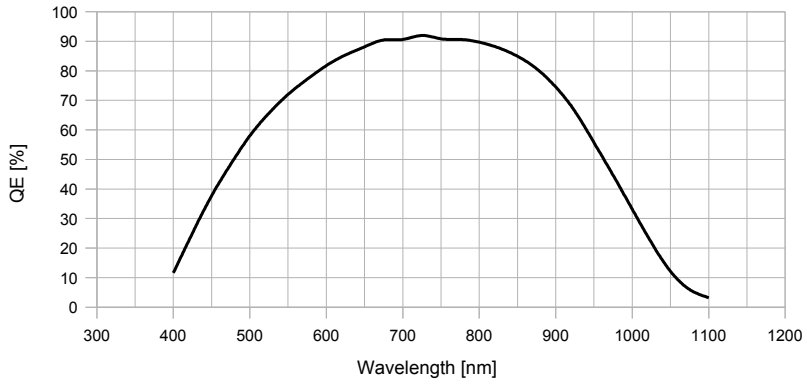
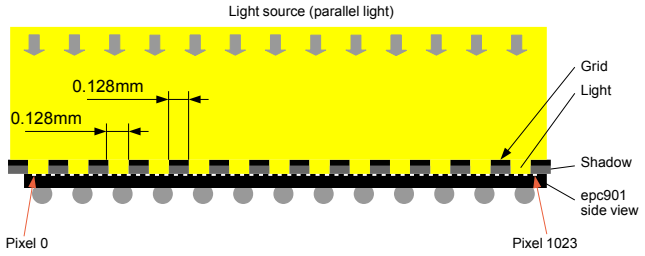


Figure 6: Typical quantum efficiency (QE) as a function of wavelength

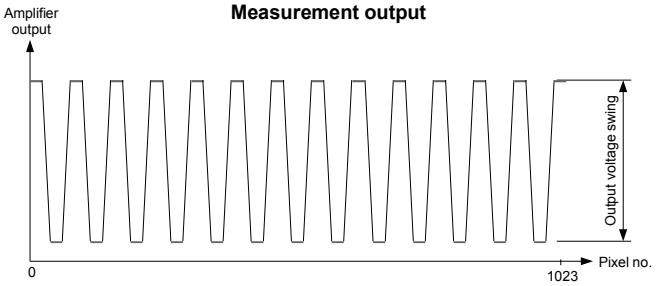
3.6. Frequency response

The signal amplitude at the output of the video amplifier is a function of the optical modulation and the read-out clock frequency. The optical modulation is defined as follows:

Test setup



Measurement output



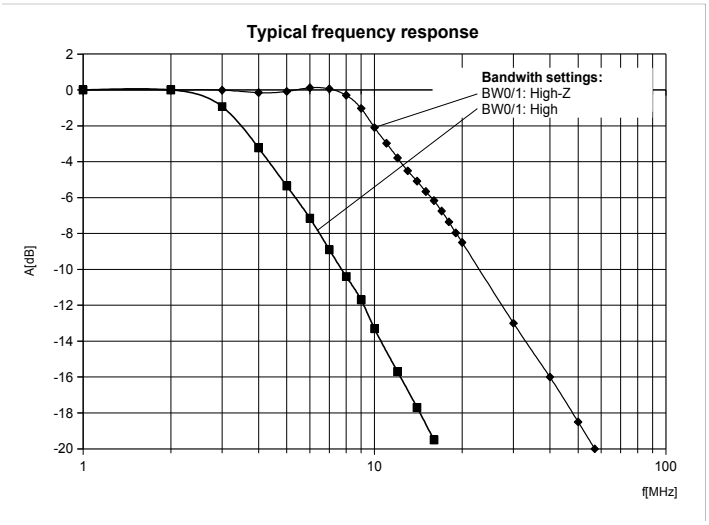
The amplitude at the video amplifier output as a function of the Read Clock frequency is as follows (temperature sensor off, differential mode):

Read Clock frequency	Mode	BW (video amplifier bandwidth setting)	VIDEO_GBW_SEL_REG	GAIN	Signal swing	SNR typ. (charge pump off)		SNR typ. (charge pump on)	
						min	typ	min	typ
1MHz	Differential	LOW_BW	0x0	1	2.0Vpp	66dB	70dB	65dB	67dB
10MHz	Differential	HIGH_BW	0x3	1	1.5Vpp	55dB	58dB	53dB	55dB
54MHz	Differential	HIGH_BW	0x3	1	0.5Vpp	46dB	49dB	44dB	46dB
54MHz	Differential	HIGH_BW	0x3	2	0.75Vpp	46dB	49dB	42dB	46dB
54MHz	Differential	HIGH_BW	0x3	4	1.25Vpp	46dB	49dB	42dB	46dB
1MHz	Single-ended	LOW_BW	0x0	1	1.6Vpp	67dB	70dB	N/A	N/A

Table 2: Useful video amplifier signal swing and SNR for different settings

3.7. Video amplifier frequency response

The following Bode plot shows the typical frequency response of the readout chain, according to the settings of the configuration pins BW0 and BW1, refer to section 4. and Table 9.



4. Configuration

The configuration pin status at power up and after reset define the operating parameters (hardware setting, refer to Table 3). The operation parameters can be changed during runtime over I2C (software setting, refer to 8.). Shaded field are used in typical applications.

Pin Name	Low (GND)	High-Z	High (VDD)	Comments
RD_DIR	Pixel 0 .. 1023		Pixel 1023 .. 0	
ROI_SEL	Pixel 0 .. 1023		Pixel 256 .. 767	Readout region of the pixel array
GAIN	2	1	4	Gain multiplier
HOR_BIN	2 pixel	1 pixel	4 pixel	Binning means averaging over 2 or 4 neighbor pixels in the voltage domain e.g. for HOR_BIN = H, pixels 0..3, 4..7, 8..11 etc. are averaged as follows $V_{BINNING_BY_4}[i]=\frac{V[i]+V[i+1]+V[i+2]+V[i+3]}{4}$, i = 0, 3, 7, .., 1020 Binning can be used to reduce the read-out time by the binning factor. Note: HOR_BIN = L is not applicable in single-ended mode.
VIDEO_CM	Single ended	Differential	n/a	Refer also to section 9.1.
DATA_RDY	Charge pump on	N/A	Charge pump off	Refer to Figure 8

BW0		X		16 MHz	The video bandwidth values are approximative only. The video bandwidth affects the current consumption and the noise at the output. The lower the bandwidth the lower the noise and the lower the current consumption. Recommendation: Keep the bandwidth as low as possible.
BW1		X			
BW0			X	8 MHz	
BW1	X				
BW0	X			4MHz	
BW1			X		
BW0			X	1MHz	
BW1			X		

Table 3: Configuration pin description (gray shaded cells are recommended, typical settings)

Notes:

- The configuration pins can be changed during runtime. Their status is read with the rising edge of the READ signal (Figure 7):

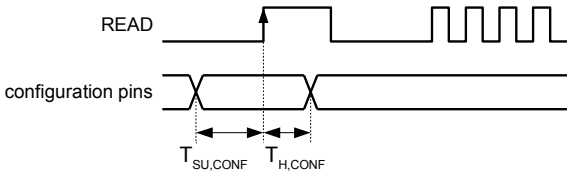


Figure 7: Status change of the configuration during runtime

  - VIDEO_CM and DATA_RDY are not read with the rising edge of the READ signal
  - RD_CONF_CTRL has to be at 0 (see Table 13).

- Enable/disable the charge pump:

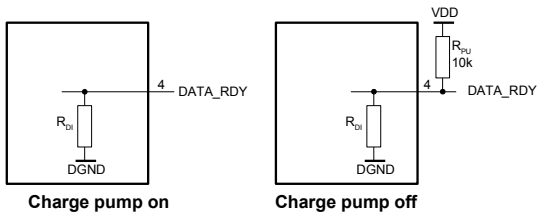


Figure 8: Charge pump operation

Important: Do not short DATA_RDY with VDD.

5. Imager operation

5.1. General remarks

The epc901 line imager chip is based on a backside illumination technology (BSI). The image is taken from the backside of the chip, whereas the electrical circuits and the pins are on the frontside. Thus, the chip must be flip-chip mounted to the PCB in order to expose the backside to the incoming light.

It is not possible with BSI to shield the photosensitive area with an integrated, electrically controlled shutter when there no light shall be detected. In other words, the pixel CCD is constantly photo-sensitive and collects charge generated by the detected photons (unwanted exposure). Thus, the CCD must be flushed or erased by the unwanted charge before an image can be acquired.

READ Pulse - The pulse applied to pin READ to initiate the read-out of a frame.
READ Clock - The clock applied to pin READ to read out the frame (after the Read Pulse).

5.2. Single frame acquisition

After the exposure time defined by the user, the charge collected in the CCD is shifted into an area which is not photo-sensitive. This area is called frame store. The following diagram shows this operation.

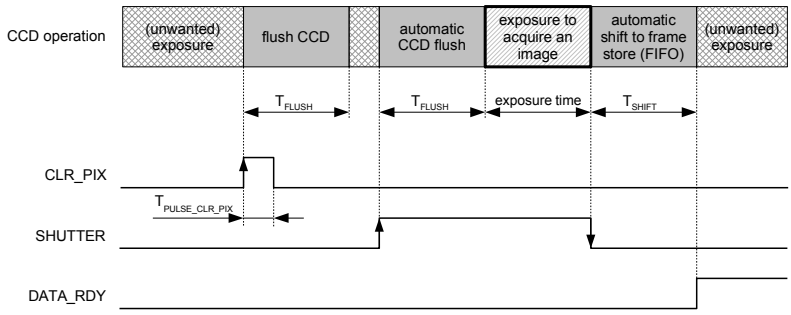


Figure 9: Image acquisition timing

The acquisition of a frame is controlled by a pulse on the SHUTTER pin (see Figure 9). The rising edge triggers the internal flush operation to erase the CCD from any unwanted electrons prior to the exposure. The exposure starts automatically after the flush operation is completed. The CCD collects electrons thereafter as long as the SHUTTER pin is high. Upon the falling edge of SHUTTER, the charge collected in the CCD pixel field is shifted to the CCD frame store which is an area which is not photo-sensitive (see (1) in Figure 10). As soon as the frame is ready for read-out, the signal DATA_RDY goes high. The image is ready to be readout as described in section 5.4.

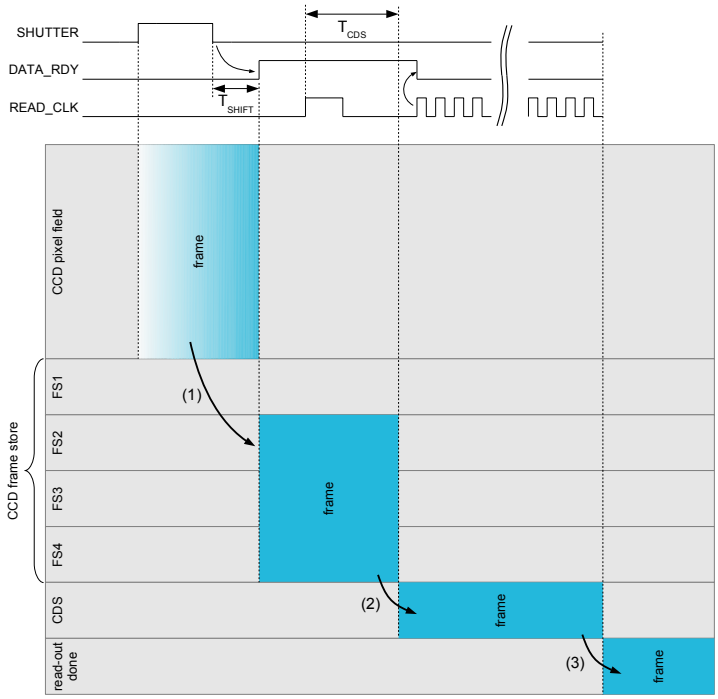


Figure 10: Example of single-frame acquisition and read-out

It is to note that the CCD continues to be photo-sensitive during the shift operation i.e. for a time T_{SHIFT} after the falling edge of SHUTTER.

5.3. Multi frame acquisition

Up to 4 images can be acquired and stored in the frame store in a fast sequence without intermediate read-out. The frame store is organized in 4 frame store elements (FS1-FS4), thereby each frame store element can store one frame/image. The first captured image initially occupies 3 frame store elements as for a single-frame acquisition (see section 5.2 and Figure 10). epc901 automatically detects a multi-frame acquisition when detecting the second SHUTTER signal without prior read-out. Upon the second shutter, the first image is shifted to a single frame store element (see (2) in Figure 11). The frames are shifted from the pixel field to the frame store as a FIFO: The first captured image is the first one to read out. The read-out is described in more detail in section 5.4. As soon as 4 frames have been captured without prior read-out, at least one read-out has to be issued prior the next shutter in order to make FS1 available again. Excessive shutter pulses are ignored.

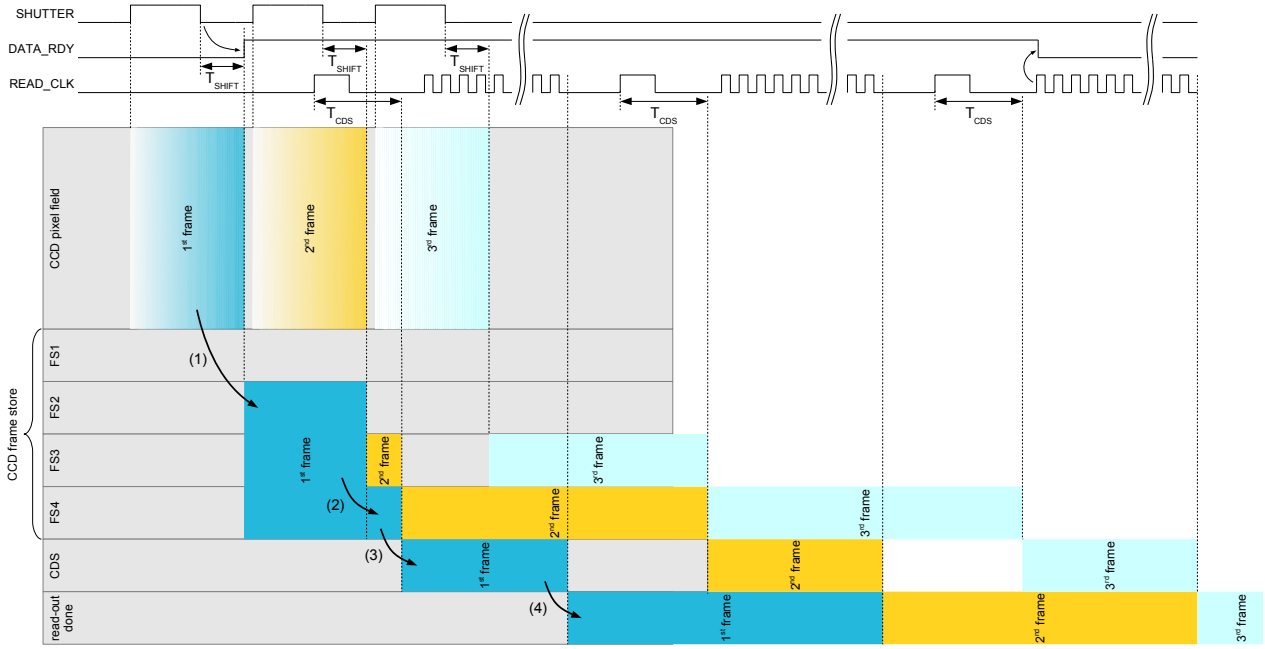


Figure 11: Multi-frame acquisition and read-out

5.4. Image readout

After one or more images have been captured, the first image (FIFO) can be read out through the interface on the pins VIDEO_P and VIDEO_N. The read-out is controlled by the READ pin. The following timing diagram shows its usage:

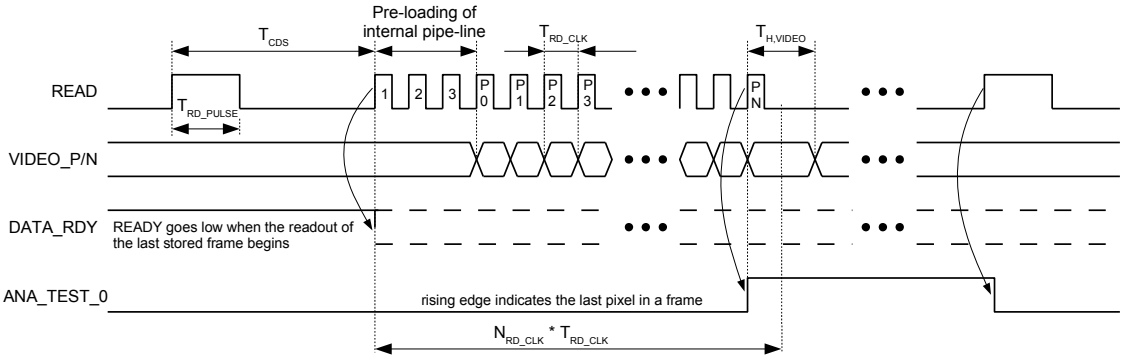


Figure 12: Image readout timing of one frame

The first pulse of a read sequence applied to pin READ is a Read Pulse and must have a duration of T_{RD_PULSE}. Upon this Read Pulse, the last frame in the frame store is converted pixel-wise from charge to voltage. This operation is called correlated double-sampling (CDS) and lasts for the time T_{CDS}. Following the Read Pulse, respecting a delay of at least T_{CDS}, Read Clock pulses are applied to the READ pin in order to transfer the pixel voltages to the VIDEO_P/N pins. The first 3 Read Clock pulses, designated with 1, 2 and 3 in Figure 12, are used to pre-load the pipeline. Thus the first 3 pixel voltage values on VIDEO_P/N can be ignored. The subsequent Read Clock pulses, designated with P0 ... PN in Figure 12, transfer the pixel voltage values through the video amplifier to the VIDEO_P/N pins.

After all pixels are read out, the output of the video amplifier is held stable for a time $T_{H,VIDEO}$ or until the next Read Pulse, whatever occurs first. The transmission of the last pixel is indicated by a high state of the pin ANA_TEST_0 upon the last Read Clock pulse rising edge. ANA_TEST_0 goes low again upon the following rising edge at READ.

Any subsequent pulse of duration T_{RD_PULSE} is interpreted as a Read Pulse and thus a new read-out sequence is initiated.

© 2020 ESPROS Photonics Corporation
Characteristics subject to change without notice

The signal DATA_RDY remains high as long as there is at least one frame stored in the CCD frame store. If no more frames are stored except the one that is currently read out, the signal DATA_RDY goes to low state on the first positive Read Clock edge (see Figure 12). If no frame is stored, the chip does nothing upon a Read Pulse.

IMPORTANT

- Differential mode only: The last pixel of the ROI, e.g. pixel 1023, is a dummy pixel and must be read for correct imager operation. Refer also to Table 1, note 3.
- It is important to sample the analog output signal of the video amplifier just before the rising edge of the next read pulse. This time point allows the readout circuits and the video amplifier to be fully settled. Also at this time point, the lowest possible readout noise can be achieved.
- The following time periods shall never overlap in any multi frame acquisition or by parallel reading during exposure: T_{FLUSH} with T_{CDS} and T_{SHIFT} with T_{CDS}. Refer for these signal to Figure 9 and Figure 12.
- At read clock frequencies above 20MHz, "ghost" signals in $pixel_{i+4}$ $pixel_{i+8}$ will become approximately as follows:

Read clock in MHz	Lag in % of illuminated pixel	
	4th Pixel	8th Pixel
20	10%	0%
40	35%	10%
50	45%	20%
54	50%	25%

Table 4: Image lag list

A software compensation algorithm is available to reduce this effect.

5.5. ROI / binning read clock

Read-out can be configured through configuration pins (see section 4.) and by register setting (see section 8.1.). Depending on binning and ROI selection, different numbers of pixels are available for read-out. E.g. if binning of 2 is selected, only 512 values can be read out because always two pixels are binned. Thus, 512 + 3 Read Clock pulses must be applied in this example. The following table shows the number of Read Clock pulses according to the configuration:

ROI_SEL	HOR_BIN	Number of Read Clock pulses	Frame read time with 54MHz read clock (w/o acquisition) [µs]	Max. frame rate with 54MHz read clock and 1µs integration time [fps]
L	L	512+3 = 515	9.54	76,600
L	M	1024+3 = 1027	19.2	44,300
L	H	256+3 = 259	4.8	120'000
H	L	256+3 = 259	4.8	120'000
H	M	512+3 = 515	9.54	76,600
H	H	128+3 = 131	2.43	167,600

Table 5: ROI_SEL/HOR_BIN settings

5.6. Flush

As explained in section 5.2., the imager is constantly photosensitive. So it constantly converts incoming light into charge. If the pixel field is not flushed periodically, excessive charge can be generated which may spill over from the pixel field to neighboring circuits, e.g. the frame store buffers. Thus, periodic flushing by applying a CLR_PIX pulse during the time no images are acquired is highly recommended, at least with a periodicity of $T_{PERIOD,FLUSH}$ (refer to section 3.3.). However, the need to do so depends on how much light is received and how long is the time between two SHUTTER pulses.

It is recommended to evaluate the setup first before the system software is implemented. During evaluation, one measure of the charge generated in the pixel by applying a SHUTTER signal with the length of the time between the intended acquisition of two images shall be executed. If the maximal pixel value exceeds 90% of full well (= 90% of output swing), it is highly recommended to place additional CLR_PIX pulses during the time where no image acquisition takes place to flush the pixel field and frame store.

A pulse on SHUTTER is ignored if it is issued within T_{FLUSH} after the rising edge of CLR_PIX. If a rising edge on CLR_PIX occurs while SHUTTER is high or during the subsequent internal shift period T_{SHIFT}, the pulse on CLR_PIX is ignored.

In power-down mode, the CCD is not photo-sensitive and therefore no charge is collected. The transition from power-down to operation flushes the CDD and the frame store automatically.

The frames stored in the pixel field and the frame store can be erased simultaneously by a pulse on CLR_DATA with a minimum pulse width of T_{PULSE,CLR_DATA}. The clear operation is triggered by the rising edge of CLR_DATA. After the frame store and the pixel field are cleared, the chip is ready to acquire new images.

A rising edge on CLR_DATA also aborts an on-going read-out and a new image acquisition can be initiated immediately. As long as DATA_RDY is not asserted (upon the new image acquisition), the read-out of the frame in the CDS can be continued without any impact on the frame (for multi-frame operation see section 5.3)

A rising edge of CLR_DATA during a shift operation might be ignored and thus shall be avoided. It is allowed to assert SHUTTER and CLR_DATA at the same time.

Please note that the frame store buffers also collect charge even if there is no operation with the CCD. This is due to dark current which can also flow into the frame store buffer elements. Thus, the frame store buffer should also be cleared (erased) regularly if there is no acquisition and readout within 100ms.

6. Various features

6.1. Temperature sensor

There are two temperature sensors on chip. One on each side of the pixel array. They are off by default and can be turned on through I2C (see Table 22). The temperature sensors provide uncalibrated values with an offset ($OFFSET_{TEMP}$) and a gain ($GAIN_{TEMP}$). Thus, calibration is needed to allow absolute temperature measurements. Calibration can take place during manufacturing of the system by applying one or two reference temperature/s and storing the calibration value in a non-volatile memory e.g. in the MCU.

The temperature sensors can be read through the I2C interface registers TEMP_SENSE_0/1 (refer to Chapter 8.8.).

6.2. Power-down

The chip can be forced into power-down mode to reduce the power consumption.

PWR_DOWN	Description
L	Operation
H	Power-down mode activated

If the chip is forced to power-down while frames are still stored on the IC, these frames are lost with power-down. When PWR_DOWN is asserted during an acquisition or transmission, the current operation is finished before the chip goes to power-down. When the power-down mode is de-activated, the IC needs T_{PWR_UP} to be back in functional mode. When PWR_DOWN goes to low state, the pixel array is automatically flushed. In power-down mode, no charge is collected by the CCD.

6.3. Oscillator clock trimming

The epc901 chip has an oscillator which controls the operation of the chip. The typical frequency is approx. 36MHz (refer to chapter 3.3). The internal clock oscillator frequency has an impact on the max. frame rate.

To measure this frequency in order to apply an optimized timing, the following procedure can be used:

1. Apply CLR_DATA
2. Apply SHUTTER for longer than T_{FLUSH}, e.g. 1µs
3. Measure the time from the falling edge of SHUTTER until the rising edge of DATA_RDY (T_{SHIFT})

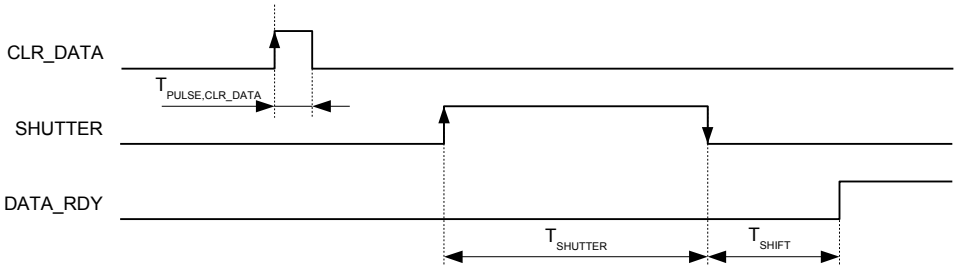


Figure 13: Sequence to measure internal clock frequency

Since T_{SHIFT} needs 24 to 26 clock cycles (n * ClockCycles), the frequency of the internal oscillator can be calculated according to the following formula:

$$F_{OSC} = \frac{n * ClockCycles}{T_{MEAS}}$$

E.g. if the measured time is 600ns, the oscillator frequency is between 40 and 43.3MHz. If the clock frequency shall be acquired more accurate, multiple measurements of T_{MEAS} shall be acquired and the average of these samples shall be used in the above formula. The clock frequency can be trimmed by setting a configuration register according to the description in Table 16 and 17.

6.4. Reset

The epc901 can be reset by the following mechanisms:

- Disconnecting and reconnecting the power supply
- Reset command through I2C (refer to section 7.1.6.)

© 2020 ESPROS Photonics Corporation
Characteristics subject to change without notice

7. I2C interface

The epc901 supports the following functions by using the I2C interface:

- Fast I2C (400 kBit/s)
- 7-bit addressing
- Slave (epc901 is always the slave)
- Supported functions are software reset, read, write, read the device address

Clock stretching and other uses of I2C bus are not supported. The register list which can be accessed by the I2C interface are listed in section 8. All described registers can be accessed directly.

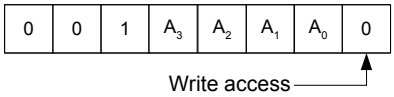
7.1. I2C communication

7.1.1. Device addressing

The MSBs of the device address are fixed to '001' internally, the LSBs A_3 to A_0 can be set by the two ternary input pins CS0 and CS1.

		CS0		
		L	M	H
CS1	L	0000	0001	0011
	M	0100	0101	0111
	H	1100	1101	1111

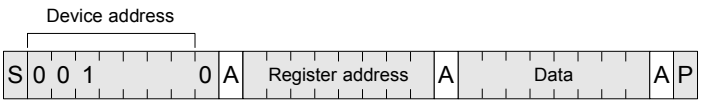
The LSB of the device addressing is used to select the communication direction:



The bus protocol in the following sections uses the following notation:

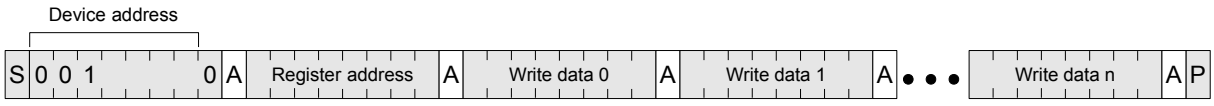
Symbol	Function
S	START
P	STOP
A	ACK
N	NACK
Shaded	Master
Unshaded	Slave (epc901)

7.1.2. Single-byte write



7.1.3. Multi-byte write

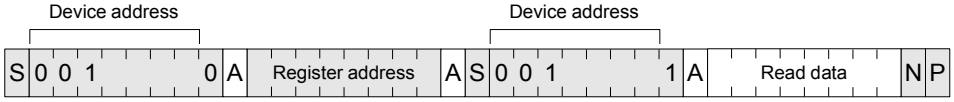
During a multi-byte write operation the master transmits the device address and the address of the first register to be written. All subsequent bytes until STOP are interpreted as write data packets.



Registers reside in a non-consecutive address space. Writing to a unused address will fail silently (no error feedback).

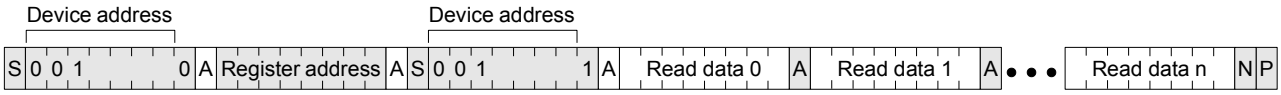
7.1.4. Single-byte read

During a single-byte read, only one register is read. After the device address is transmitted, the master has to transmit the register address. After addressing the epc901 IC with a read-command, it transmits the read data. The access is terminated with a NACK and a STOP by the master.



7.1.5. Multi-byte read

During a multi-byte read operation the master transmits the device address and the address of the first register to be read. Afterwards, the epc901 is addressed with a read command. It then transmits data bytes until the master applies NACK and a STOP.

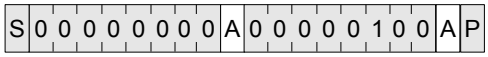


Registers reside in a non-consecutive address space. Reading to a unused address will return no useful data.

7.1.6. Software reset

A software reset has the same effect like a power-up reset. E.g. the chip uses the configuration as given by the configuration pins. Also, all trimming parameters are reset to the initial values.

7.1.7. Device address sampling



The device address pins CS0 and CS1 are sampled during power-up. They can be re-sampled by applying this command.

7.1.8. Setup latency

The new register value becomes active with the falling edge of the last bit transmitted.

7.2. I2C bus timing

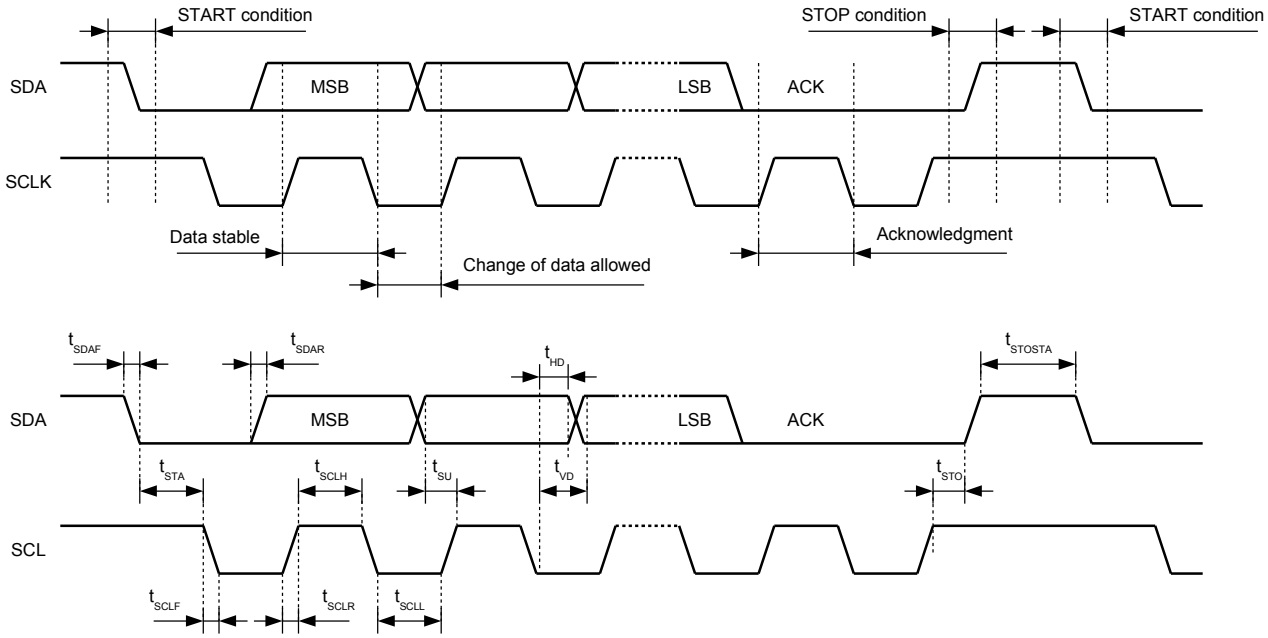


Figure 14: I²C bus timing, top: Basic communication sequence, bottom: Timing parameters

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	I²C data rate		400	kbit/s
t_{SCLL}	SCL clock low time	1.3		µs
t_{SCLH}	SCL clock high time	0.6		µs
t_{SU}	SDA setup time	100		ns
t_{HD}	Data hold time	0		ns
t_{VD}	Data valid time		900	ns
t_{SDAR} t_{SCLR}	SDA and SCL rise time		300	ns
t_{SDAF}, t_{SCLF}	SDA and SCL fall time		300	ns
t_{STA}	Start condition hold time	0.6		µs
t_{STO}	Stop condition setup time	0.6		µs
t_{STOSTA}	Stop to start condition time (bus free)	1.3		µs
C_b	Capacitive load for each bus line		400	pF
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter		50	ns

Table 6: I²C bus timing: Timing parameters (FM+)

8. Register description

Address	Register name	Ref.	Description
0x00	ACQ_TX_CONF_I2C	Table 8	Binning, amplifier gain, ROI, read direction
0x01	BW_VIDEO_CONF_I2C	Table 9	Video amplifier bandwidth
0x02	MISC_CONF	Table 12	Various settings
0x90	OSC_TRIM_REG	Table 16	Oscillator trimming (fine)
0x94	VIDEO_GBW_SEL_REG	Table 10	Video amplifier bandwidth, noise and current consumption
0xA0	TEMP_SENS_L_LSB	Table 19	LSB of left temperature sensor
0xA1	TEMP_SENS_L_MSB	Table 20	MSB of left temperature sensor
0xA2	TEMP_SENS_R_LSB	Table 21	LSB of right temperature sensor
0xA3	TEMP_SENS_R_MSB	Table 22	MSB of right temperature sensor
0xA4	TEMP_SENS_CONF	Table 23	Temperature sensor configuration
0xB0	I2C_ERROR_IND	Table 25	I2C error flag
0xD6	FORCE_ANA_CTRL_SIGS	Table 14	Analog control settings, e.g. power control
0xD7	OSC_TRIM_RANGE_REG	Table 18	Oscillator trimming (coarse)
0xFF	CHIP_REV_NO_REG	Table 26	Chip revision

Table 7: Register map accessible by the I2C interface

IMPORTANT NOTES:

1. “n/a” means “not applicable”. Do not modify these register bits. Thus, read first the register, modify the required bits and then write back the modified register value.
2. Do not write to other addresses than listed in Table 7. If accidentally a write has been occurred to a register address not in the list above, unexpected behavior can occur. A hardware reset brings the imager back to factory settings.
3. Default values are indicated as bold letters§
4. In the tables below, allowed operations are:
   R: Read
   W: Write
   WP: Write protected

8.1. Binning, amplifier gain, ROI, read direction

0x00	ACQ_TX_CONF_I2C							
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	HOR_BIN		GAIN		ROI_SEL	RD_DIR
Operation	n/a	n/a	R/W		R/W		R/W	R/W
Default	0	0	0	1	0	1	0	0

Table 8: Description of register ACQ_TX_CONF_I2C

HOR_BIN: Horizontal binning of the pixels:
00: Binning 2 pixels (in differential mode only, n/a in single ended mode)
01: No binning
10: Binning 4 pixels

GAIN: Video amplifier voltage gain
00: 2
01: 1
10: 4

ROI_SEL: Region of interest
0: All pixels (0 to 1023)
1: Inner half of the pixels (256 to 767)

RD_DIR: Read direction
0: From 0 to 1023
1: From 1023 to 0

8.2. Video Amplifier bandwidth

0x01	BW_VIDEO_CONF_I2C							
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	BW_VIDEO_1		BW_VIDEO_0	
Operation	n/a	n/a	n/a	n/a	R/W		R/W	
Default	0	0	0	0	0	1	0	1

Table 9: Description of register BW_VIDEO_CONF_I2C

BW_VIDEO_1/0: 1010: Video bandwidth 1 MHz
1000: Video bandwidth 4 MHz
0010: Video bandwidth 8 MHz
0101: **Video bandwidth 16 MHz**

Notes

1. Refer also to section 3.7.
2. The video bandwidth does not exactly match with the frequency values mentioned in Table 9. Please note that these values are approximative only.
3. Make sure MISC_CONF:RD_CONF_CTRL is set to 1
4. The settings of this register become active at the rising edge of a Read pulse
5. The use of this register overwrites the values set by the configuration pins (refer to Table 2 and Table 3)

8.3. Video amplifier bandwidth, noise and current consumption

0x94	VIDEO_GBW_SEL_REG							
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	n/a	n/a	GBW_SEL_DI	
Operation	n/a	n/a	n/a	n/a	n/a	n/a	R/W	
Default	0	0	0	0	0	0	0x3	

Table 10: Description of register VIDEO_GBW_SEL_REG

The bandwidth, noise and current consumption of the video amplifier is adjustable with this register as listed in Table 11. These settings regarding the video bandwidth are on top of the settings in Chapter 8.2. E.g. if the Video bandwidth is set to 4 MHz (in Table 9), and the GBW_SEL_DI is set to 0x01, the resulting bandwidth is 2 MHz. Please note that these values are approximative only.

VIDEO_GBW_SEL	Relative video amplifier bandwidth	Relative video amplifier current consumption	Relative read noise
00	25%	lowest	lowest
01	50%		
10	75%		
11	**100%**	**highest**	**highest**

Table 11: Bandwidth selection and bias current trimming (approx. values)

8.4. Configuration control, video amplifier on/off

0x02	MISC_CONF							
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	n/a	VIDEO_AMP_PD_OVR_EN	VIDEO_AMP_PD_OVR	RD_CONF_CTRL
Operation	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	1	0	0	1	1	0	0	0

Table 12: Description of register MISC_CONF

Register Name	Description	1	0
VIDEO_AMP_PD_OVR_EN	Enable/disable register bit VIDEO_AMP_PD_OVR	enabled	**disabled**
VIDEO_AMP_PD_OVR	Video amplifier power down. This bit is only effective if register bit VIDEO_AMP_PD_OVR_EN is set	Video amp off	**Video amp on**
RD_CONF_CTRL	Configuration control	By configuration registers	**By configuration pins**

Table 13: Description of register setting MISC_CONF

8.5. Video amplifier SE/Diff, charge pump on/off, 5V regulator on/off

0xD6	FORCE_ANA_CTRL_SIGS							
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	AMP_OVR_EN	AMP_OVR	VDD5V0_PD	CP_PD
Operation	R/WP	R/WP	R/WP	R/WP	R/WP	R/WP	R/WP	R/WP
Default	0	0	1	0	0	0	0	0

Table 14: Description of register FORCE_ANA_CTRL_SIGS

Bit Name	Description	1	0
AMP_OVR_EN	Control of the video amplifier mode selection AMP_OVR	enabled	**disabled**
AMP_OVR	Video amplifier mode selection (AMP_OVR_EN=1)	Differential	**Single-ended**
VDD5V0_PD	Power control of the 5V regulator	Regulator off	**Regulator on**
CP_PD	Power control of the charge pump	Charge pump off	**Charge pump on**

Table 15: Description of register setting FORCE_ANA_CTRL_SIGS

Notes
FORCE_ANA_CTRL_SIGS is write-protected (WP). The following example sequence turns the regulator and the charge pump off:

- Write address 0xD0: 0x4A //unlock register write protection
- Write address 0xD1: 0x66 //unlock register write protection
- Write Address 0xD6: FORCE_ANA_CTRL_SIGS = 0x23 //disable charge pump and 5V regulator

Notes:

- No other read or write access is allowed in between the sequence above
- After this sequence, the register FORCE_ANA_CTRL_SIGS is automatically locked

8.6. Oscillator trimming (fine)

0x90	OSC_TRIM_REG							
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	OSC_TRIM			
Operation	n/a	n/a	n/a	n/a	R/W			
Default	0	0	0	0	0x0			

Table 16: Description of register OSC_TRIM_REG

The trim range of OSC_TRIM is approx. 1.2 MHz per step:

Bit no.				Trim Value (MHz)
3	**2**	**1**	**0**	
1	0	0	0	-9.6
1	0	0	1	-8.4
1	0	1	0	-7.2
1	0	1	1	-6.0
1	1	0	0	-4.8
1	1	0	1	-3.6
1	1	1	0	-2.4
1	1	1	1	-1.2
0	**0**	**0**	**0**	**0.0**
0	0	0	1	+1.2
0	0	1	0	+2.4
0	0	1	1	+3.6
0	1	0	0	+4.8
0	1	0	1	+6.0
0	1	1	0	+7.2
0	1	1	1	+8.4

Table 17: Oscillator trimming

8.7. Oscillator trimming (coarse)

0xD7	OSC_TRIM_RANGE_REG							
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	n/a	n/a	n/a	OSC_TRIM_RANGE_UP
Operation	n/a	n/a	n/a	n/a	n/a	n/a	n/a	R/W
Default	0	0	0	0	0	0	0	0

Table 18: Description of register OSC_TRIM_RANGE_REG (available from revision number 0x14)

OSC_TRIM_RANGE_UP Defines oscillator trim range:
0: default oscillator trim range
1: oscillator frequency increased by 25%

8.8. Temperature sensors read

There are four registers which hold the current temperature values of the two temperature sensors. Once one of these addresses is read, all other temperature sensor registers are frozen until all four registers are read. The read sequence of these registers is not important.

The left temperature sensor is located near pixel 0, the right one near pixel 1023.

8.8.1. Left temperature sensor

0xA0	TEMP_SENSE_L_LSB							
Bit no.	7	6	5	4	3	2	1	0
Bit name	TEMP_L[7:0]							
Operation	R							
Default	0x0							

Table 19: Description of register TEMP_SENSE_L_LSB

0xA1	TEMP_SENSE_L_MSB							
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	TEMP_L[12:8]				
Operation	n/a	n/a	n/a	R				
Default	0	0	0	0x0				

Table 20: Description of register TEMP_SENSE_L_MSB

8.8.2. Right temperature sensor

0xA2	TEMP_SENSE_R_LSB							
Bit no.	7	6	5	4	3	2	1	0
Bit name	TEMP_R[7:0]							
Operation	R							
Default	0x0							

Table 21: Description of register TEMP_SENSE_R_LSB

0xA3	TEMP_SENSE_R_MSB							
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	TEMP_R[12:8]				
Operation	n/a	n/a	n/a	R				
Default	0	0	0	0x0				

Table 22: Description of register TEMP_SENSE_R_MSB

© 2020 ESPROS Photonics Corporation
Characteristics subject to change without notice

8.9. Temperature sensors control

0xA4	TEMP_SENS_CONF							
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	MEAS_RATE_CONF		ENABLE_R	ENABLE_L	PD_CONF_R	PD_CONF_L
Operation	n/a	n/a	R/W		R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	1

Table 23: Description of register TEMP_SENS_CONF

Register Name	Description	1	0
MEAS_RATE_CONF	Configure the measurement rate of the temperature sensors: **00: 10 measurements per second** 01: 1 measurement per second 10: 1 measurement every 10 seconds **Note:** A change of the measurement rate becomes effective after the temperature sensor has been disabled and enabled again		

ENABLE_R, ENABLE_L, PD_CONF_R, PD_CONF_L

ENABLE_R	ENABLE_L	PD_CONF_R	PD_CONF_L	Description
0	**0**	**1**	**1**	**Both sensors off**
1	1	0	0	Both sensors on
1	0	0	1	Only right sensor on
0	1	1	0	Only left sensor on

Table 24: Description of register setting TEMP_SENS_CONF

8.10. I2C error flag

0xB0	I2C_ERROR_IND							
Bit no.	7	6	5	4	3	2	1	0
Bit name	n/a	n/a	n/a	n/a	n/a	n/a	n/a	I2C_ERR
Operation	n/a	n/a	n/a	n/a	n/a	n/a	n/a	R
Default	n/a	n/a	n/a	n/a	n/a	n/a	n/a	0

Table 25: Description of register I2C_ERROR_IND

I2C_ERR This bit is set if the I2C controller fails to service a register operation. In error condition, the affected read operation may return wrong data or the affected write operation may be ignored. This bit is automatically reset after a read cycle.

8.11. Chip revision

0xFF	CHIP_REV_NO_REG							
Bit no.	7	6	5	4	3	2	1	0
Bit name	CHIP_REV_NO							
Operation	R							
Default	0	0	1	0	0	0	0	1

Table 26: Description of register CHIP_REV_NO_REG

9. Application information

Referring to Figure 15 and Figure 16, please note the following:

- The GND pins can be connected together, preferably to a plane / star connection. Refer also to section 9.4.3.
- The video amplifier has separate supply pins VDD_OA and GND_OA due to its fast switching currents. It is important to block this power supply pins with low ESR capacitors as close as possible to the chip in order to avoid noise at the video output due to supply voltage bouncing.
- The voltage level applied to VDD_OA must be the same as on pin VDD. Otherwise the IC can be damaged due to latch-up.
- If the pin VIDEO_CM is left open (not connected), the video amplifier operates in differential mode. If this pin is tied to ground, together with the pin VIDEO_N, the video amplifier operates in single ended mode.

Video amplifier operation mode	VIDEO_P	VIDEO_N	VIDEO_CM
Differential	Positive output	Negative output	(not connected)
Single ended	Output	GND	GND

9.1. Differential mode

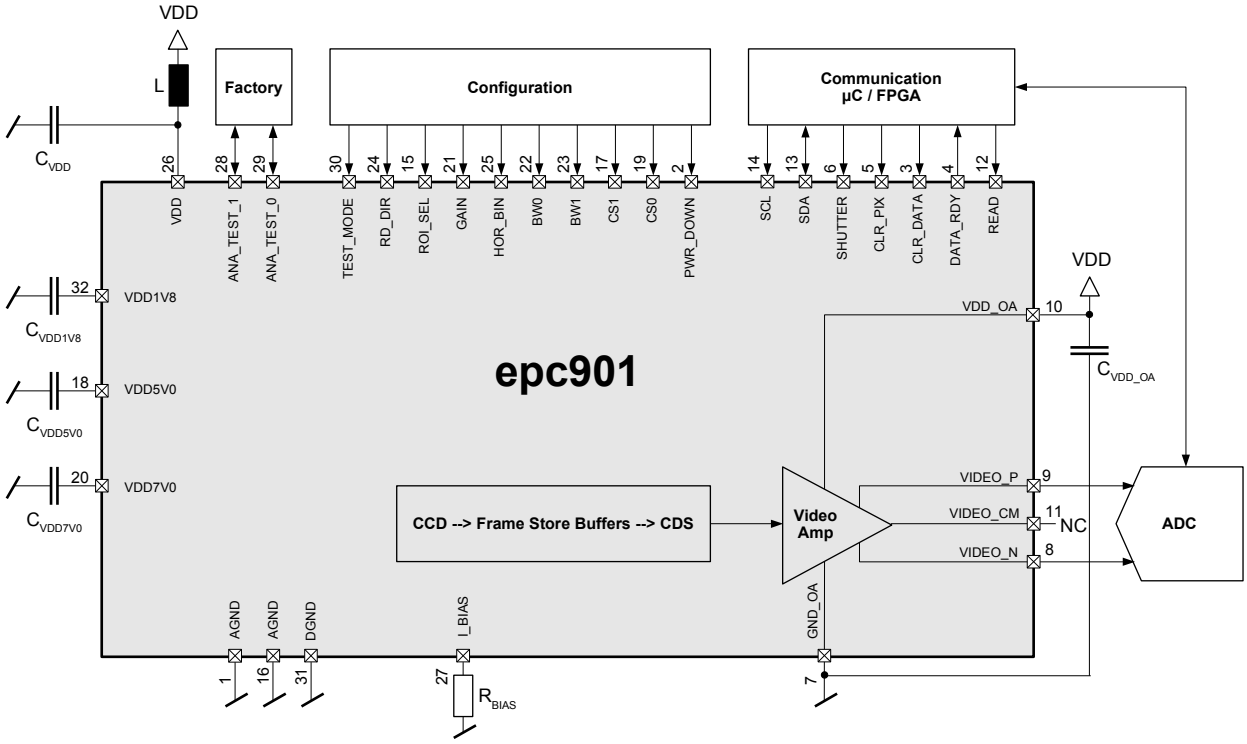


Figure 15: Differential mode application diagram

Pin 11 (VIDEO_CM) can be left open. The IC sets this pin to VDD/2 which is the offset voltage of the VIDEO_P and VIDEO_N signal. However, it is possible to apply a voltage source at VIDEO_CM to control the common mode voltage of the output signal. Make sure that this is a low noise/low ripple source and add a 1µF low ESR blocking capacitor as close as possible to pin 11. The voltage at VIDEO_CM must be as defined in the table under section 3.1. V_{CM_D}.

Illumination	VIDEO_N	VIDEO_P	VIDEO_P – VIDEO_N (typ.)
Dark voltage	V_{VIDEO_CM} + 0.4V	V_{VIDEO_CM} – 0.4V	-0.8V
Maximum video output	V_{VIDEO_CM} – 0.6V	V_{VIDEO_CM} + 0.6V	1.2

Table 27: Video amplifier output in differential mode

9.2. Single ended mode

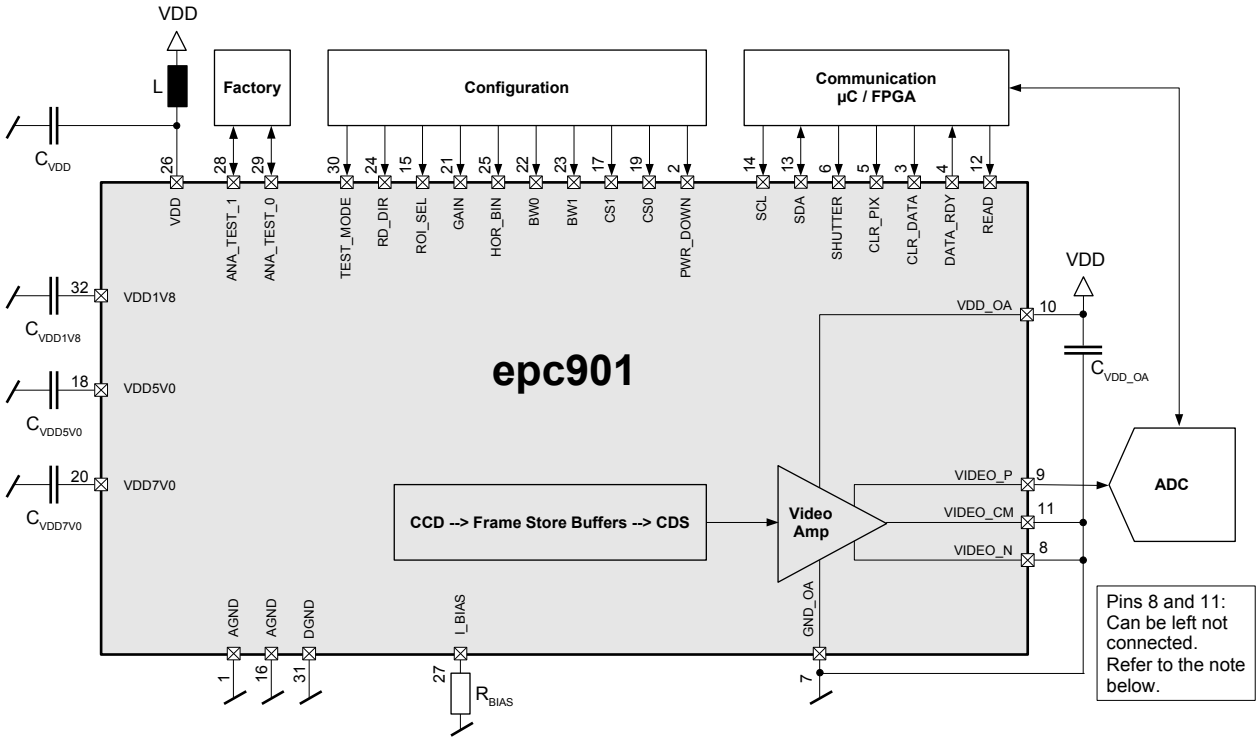


Figure 16: Single ended mode application diagram

If VIDEO_N and VIDEO_CM are tied to GND at power-up or RESET, single-ended mode is enabled. The output signal is available at VIDEO_P.

Note:
If the pins VIDEO_N and VIDEO_CM are not connected, the epc901 is in differential mode after power-up or RESET. In this case, single-ended mode can be selected via I2C register setting FORCE_ANA_CTRL_SIGS, bit AMP_OVR (see Table 14 and Table 15).

Illumination	VIDEO_P (typ.)
Dark voltage	0.4V
Maximum video output	2.0V

Table 28: Video amplifier output in single-ended mode

9.3. External components

The external components in Figure 15 and Figure 16 shall be as follows:

Parameter	Description	Value	Units	Tolerance	Comments
R_{BIAS}	Bias resistor	56k	kΩ	±1%	Temperature coefficient max. ±100ppm/K
C_{VDD1V8}	Decoupling capacitor	1.0	µF	±20%	low ESR
C_{VDD5V0}, C_{VDD7V0}	Decoupling capacitors	2.2	µF	±20%	low ESR
C_{VDD}, C_{VDD_OA}	Decoupling capacitors	1.0	µF	±20%	low ESR
L	Decoupling inductor	600	Ω		@100MHz, e.g. Taiyo Yuden BK1005HR601-T

9.4. Low noise operation

9.4.1. Charge pump noise

The internal charge pump generates some noise, especially in single-ended mode. The noise performance can be optimized by turning off the charge pump and supplying the chip with an external 5V supply. Refer to section 10.2.

9.4.2. Video amplifier noise

Another noise source is the video amplifier which can be used in two different modes. Single ended mode is the lower noise operation mode. Thus, use the chip in single ended mode for low noise applications. In addition, operate the video amplifier at lowest possible band-width and lowest current consumption. Refer to 8.2. and 8.3.

9.4.3. Layout recommendations

The epc901 line imager is a very high sensitivity analog/digital chip. Due to its high conversion gain, just a few electrons collected by coupling to signal lines close to the chip generate a significant voltage at the output. Thus, do not place any signal lines underneath the chip without shielding. It is highly recommended to place a stable AGND plane underneath the epc901 chip (on the top layer of the PCB) and not to place any signal tracks close to the chip.

Also very important is a clean noise-free power supply. Especially decouple the VDD from VDD_OA with capacitor so the output modulation of the video amplifier does not modulate the VDD of the chip. Make sure all the capacitors used for decoupling are low ESR types.

The READ signal line can also be a major source of noise or coupling to the output signal. Figure 17 shows a scope screen shot of such a coupling problem.

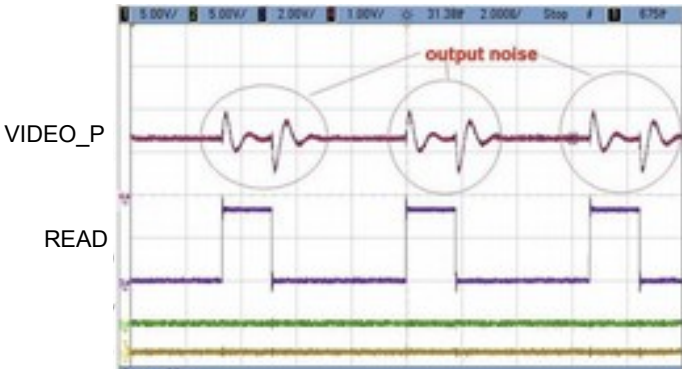


Figure 17: READ signal coupling to the output by a ground loop

The source of such problems is usually a ground loop. Especially if there is a significant distance 'd' as shown in Figure 18 (starting from a few cm only) between the video output of the epc901 chip and the input of the ADC. Care has to be taken that the layout of the GND lines is exactly like shown in Figure 18. **Make sure that the digital GND has a separate track as shown by the blue ground line!**

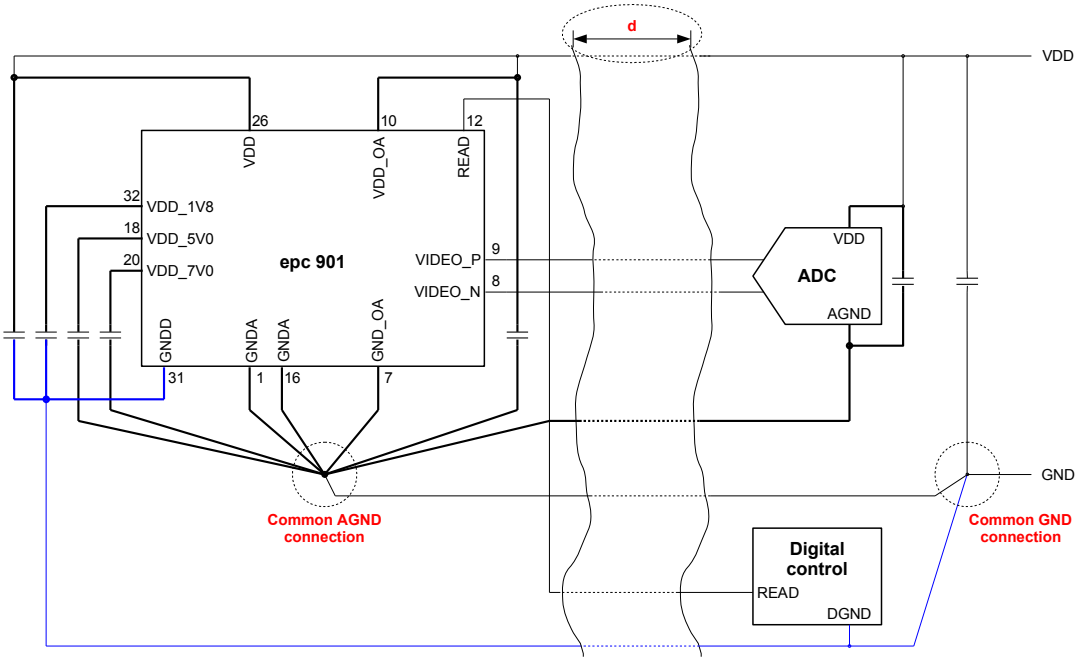


Figure 18: Recommended ground and power supply connections

Make also sure that the thick lines in Figure 18 are as short and as thick as possible.

10. Power consumption considerations

10.1. General considerations

There are several options to control the power consumption. However, a trade-off between performance and power consumption has to be considered. The following section describes the various options. The most power-consuming blocks are

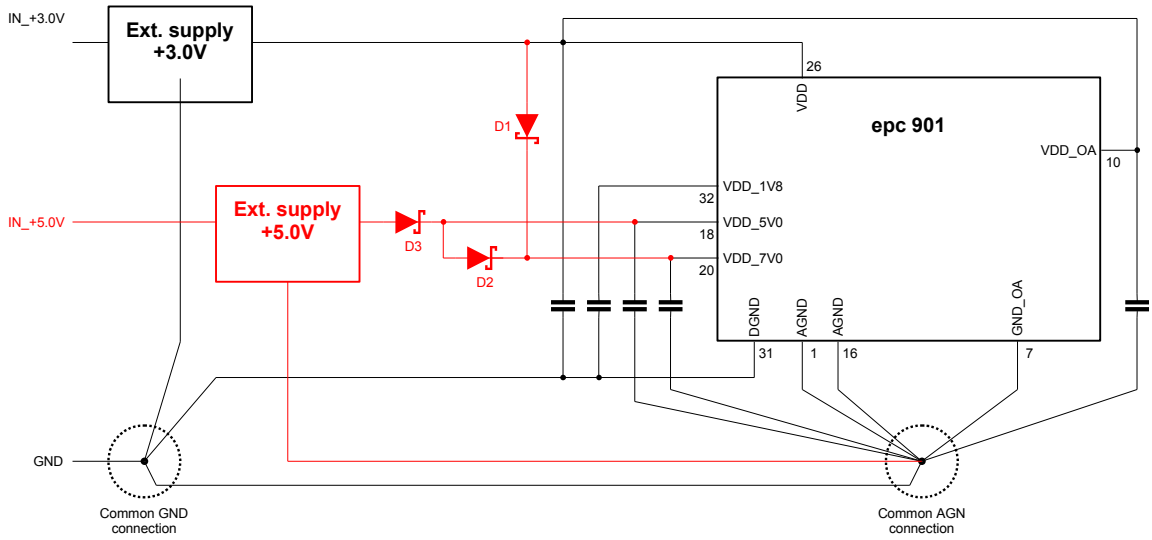
- Temperature sensors (approx. 3mA)
- Video amplifier (approx. 3.5mA)
- Charge pump and 5V regulator (approx. 13.5mA)

The wake-up time of the video amp is typ. 3µs only. Thus, in most applications it can be turned off during illumination in order to reduce the average power consumption.

10.2. Low power operation

The lowest possible power consumption of the epc901 can be achieved if it is supplied with 3V and 5V since the highest power consumption is the internal charge pump which generates the 5V from VDD. In this case, the chip-internal charge pump and the internal 5V regulator shall be turned off. The power consumption in this configuration is less than 20mW compared to 80mW in the standard mode. The following application information shows how this can be achieved. Follow carefully the instructions in order to avoid damage of the chip.

Use protection diodes according to circuit diagram below. The diodes have to be low voltage Schottky devices with a forward current of at least 100mA (i.e. BAT74).



Make sure that external 5V supply (VDD_5V0) is delayed by at least 100µs to the VDD.

1. Power up VDD (3V)
2. Wait for at least 100µs
3. Power up VDD_5V0

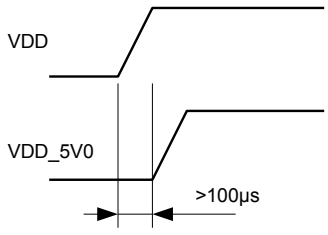
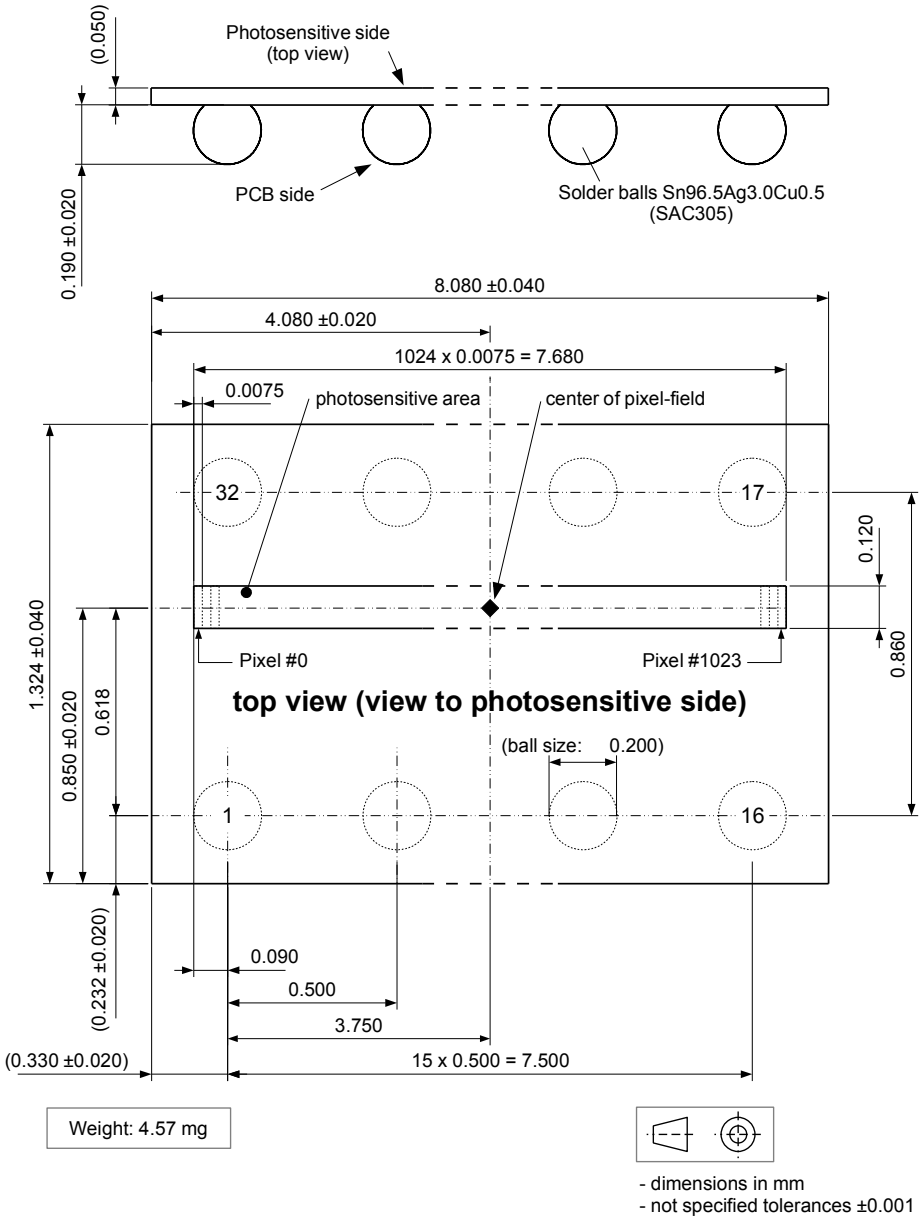


Figure 19: Power up sequence in low power configuration

11. Layout and packaging information

11.1. Mechanical dimensions

The packaging technology is a CSP with a uBGA. All measures which do not have an explicit tolerance are meant +/-0.001mm.



The photosensitive area is not marked neither on the front nor on the backside of the IC. As a visible reference, the metal ring of the IC can be used which is visible from the back side (solder ball side). Also from the front side (photosensitive area) it can be seen with a camera which is sensitive in the near infrared wavelength domain (950 .. 1150nm).

Figure 20 shows the epc901 chip from the bottom side with view to the solder balls. Please note the location of pin 1.

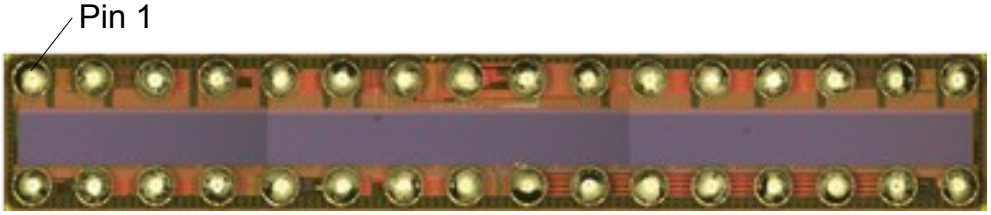


Figure 20: Bottom view

11.2. PCB design and SMD manufacturing process considerations

The epc901 chip comes in a very small 32 pin chip scale package, the PCB layout should be made with special care. The silicon chip is small and light weight compared to its solder balls. It is highly recommended that all tracks to the chip should come straight from the side. A consequent symmetrical PCB layout design is highly recommended to achieve high production yield.

The pads and the tracks should also have exactly the same width. The tracks shall be covered by a solder resist mask in order to avoid drain of the solder tin alloy to the track.

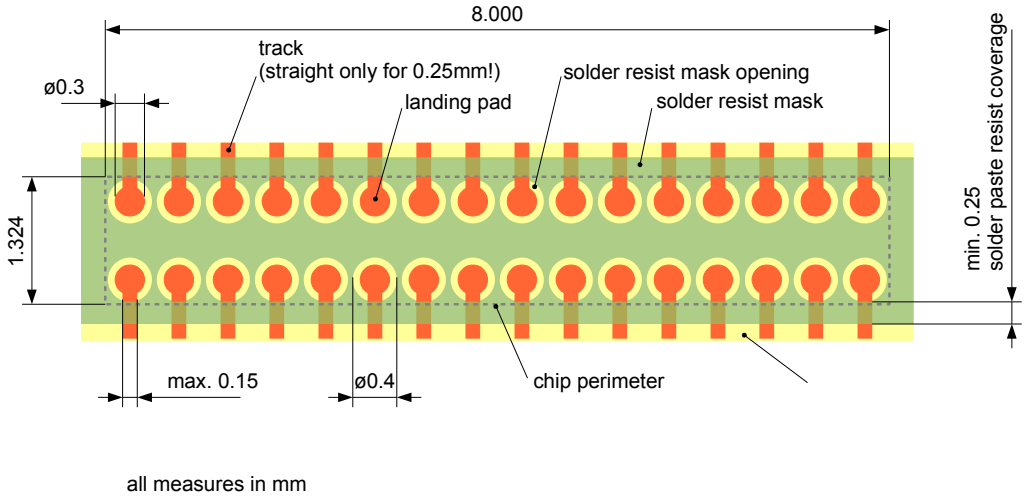


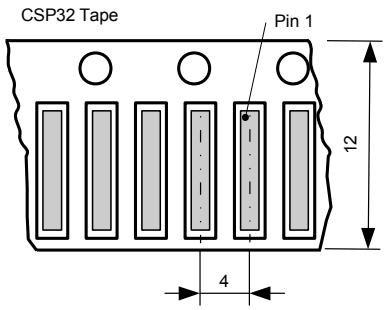
Figure 21: Recommended PCB layout

Underfill of the components reduces stress to the solder pads caused by e.g. temperature cycling or mechanical bending. The thermal and mechanical fatigue will be reduced and the longterm reliability will be increased. Underfill and underfill selection is application specific. It shall follow JEDEC-STD JEP150: Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface- Mount Components.

Please refer to the application note AN08_Process-Rules_CSP_Assembly. Please follow carefully the recommendations in this application note to achieve a high manufacturing yield.

11.3. Tape & Reel Information

The devices are packed in tape on reel for automatic placement systems. The tape is wound on 178 mm (7 inch) or 330 mm (13 inch) reels and individually packaged for shipment. General tape-and-reel specification data are available in a separate data sheet and indicate the tape sizes for various package types. Further tape-and-reel specifications can be found in the Electronic Industries Association (EIA) standard 481-1, 481-2, 481-3.



ESPROS does not guarantee that there are no empty cavities. Thus, the pick-and-place machine should check the presence of a chip during picking.

11.4. Soldering and IC handling

Since the chip is only 50µm thick and has a high aspect ratio (length to width), a careful handling during the surface mount assembly process shall be taken in order to avoid mechanical damage. In addition to that, careful PCB layout is needed in order to achieve reliable assembly results with a high yield. Please refer to the application note AN08_Process-Rules_CSP_Assembly which contains most up to date and comprehensive information to these topics. This application note can be downloaded at www.espros.com/application-notes.

© 2020 ESPROS Photonics Corporation
Characteristics subject to change without notice

12. Self-test mode by fill-and-spill

The CCD and the readout chain functionality of the epc901 chip can be tested without optical stimulation. This function is useful in a factory test of the final product or in safety applications. The concept is to inject electrically stimulated charge into the pixel instead of photon generated charge by the as-called fill-and-spill circuitry.

The basic behavior of the IC by the fill-and-spill circuitry is exactly the same as when the IC is illuminated. I.e. also when fill-and-spill is used, the acquisition is controlled by SHUTTER, the internal flush and shift operation are similar and the signal DATA_RDY is asserted at the end of the internal shift operation.

If the CCD is stimulated by the fill-and-spill, the on-chip test controller coordinates the operation of the fill-and-spill and the CCD.

Fill-and-spill procedure:

1. Select differential readout mode.
2. Apply the following voltages:

   TEST_MODE = VDD
   ROI_SEL = 0V or VDD
   RD_DIR = 0V or VDD

3. Access the test mode configuration registers. Write access remains available until next reset:

   Addr 0xD0: 0x4A
   Addr 0xD1: 0x66
   Addr 0xD2: 0x02
   Addr 0xD4: 0x20
   Addr 0xD5: 0x21

4. Select the pattern of pixels to be stimulated by writing to register Addr 0xD3 (see Table 29):

Bit select	Stimulation
7	not used
6	all odd pixels
5	pixels 2, 6, 10 etc.
4	pixels 4, 12, 20 etc.
3	pixels 0, 8, 16 etc.
2:0	Set these bits to 0x1

Table 29: Bit select description of register Addr 0xD3 in fill-and-spill test mode

5. Apply the following voltages to the test pins. Note that Vout varies from production lot to lot:

   ANA_TEST_0 = 1 VDC
   ANA_TEST_1 (VIDEO_P – VIDEO_N):
   - 3.0 VDC for Vout of approx. -0.3V
   - 3.6 VDC for Vout of approx. +0.5V

6. Wait 10 µs
7. Acquire a frame by using a 20µs SHUTTER signal. A different integration time is not allowed.
8. Read the frame as described in section 5.4.
9. Disconnect external voltage sources from pins ANA_TEST_0/1.
10. Configure test mode registers to their initial values:

    Addr 0xD4: 0x00
    Addr 0xD5: 0x01
    Addr 0xD2: 0x00
    Addr 0xD3: 0x00

11. Apply the following voltages:

    TEST_MODE = 0V
    ROI_SEL → application dependent
    RD_DIR → application dependent

Important notes:

- The chip does not operate correctly if the procedure and the write sequences described above are not exactly executed.
- ANA_TEST* are bi-directional pins, by default output pins. Thus, the voltages V_{IN} and V_{DC} may only be applied once the chip is in fill-and-spill mode. Otherwise, it can get damaged!

13. Ordering Information

Part Number	Part Name	Package	RoHS	Packaging Method
P100 401	epc901-CSP32-033	CSP32	Yes	Reel
P100 208	epc901 Evaluation Board V2	PCB 70.00 x 65.00 mm	Yes	Anti static bag
P100 209	epc901 Chip Carrier Board V2	PCB 36.00 x 42.75 mm	Yes	Anti static bag

Table 30: Ordering information

Application notes can be downloaded from the ESPROS website at www.espros.com/downloads/09_Application_notes.

14. IMPORTANT NOTICE

ESPROS Photonics AG and its subsidiaries (ESPROS) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to ESPROS' terms and conditions of sale supplied at the time of order acknowledgment.

ESPROS warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with epc's standard warranty. Testing and other quality control techniques are used to the extent ESPROS deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

ESPROS assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using ESPROS components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

ESPROS does not warrant or represent that any license, either express or implied, is granted under any ESPROS patent right, copyright, mask work right, or other ESPROS intellectual property right relating to any combination, machine, or process in which ESPROS products or services are used. Information published by ESPROS regarding third-party products or services does not constitute a license from ESPROS to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from ESPROS under the patents or other intellectual property of ESPROS.

Resale of ESPROS products or services with statements different from or beyond the parameters stated by ESPROS for that product or service voids all express and any implied warranties for the associated ESPROS product or service. ESPROS is not responsible or liable for any such statements.

ESPROS products are not authorized for use in safety-critical applications (such as life support) where a failure of the ESPROS product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of ESPROS products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by epc. Further, Buyers must fully indemnify ESPROS and its representatives against any damages arising out of the use of ESPROS products in such safety-critical applications.

ESPROS products are neither designed nor intended for use in military/aerospace applications or environments unless the ESPROS products are specifically designated by ESPROS as military-grade. Only products designated by ESPROS as military-grade meet military specifications. Buyers acknowledge and agree that any such use of ESPROS products which ESPROS has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

ESPROS products are neither designed nor intended for use in automotive applications or environments unless the specific ESPROS products are designated by ESPROS as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, ESPROS will not be responsible for any failure to meet such requirements.