



# PJA138K

## 50V N-Channel Enhancement Mode MOSFET – ESD Protected

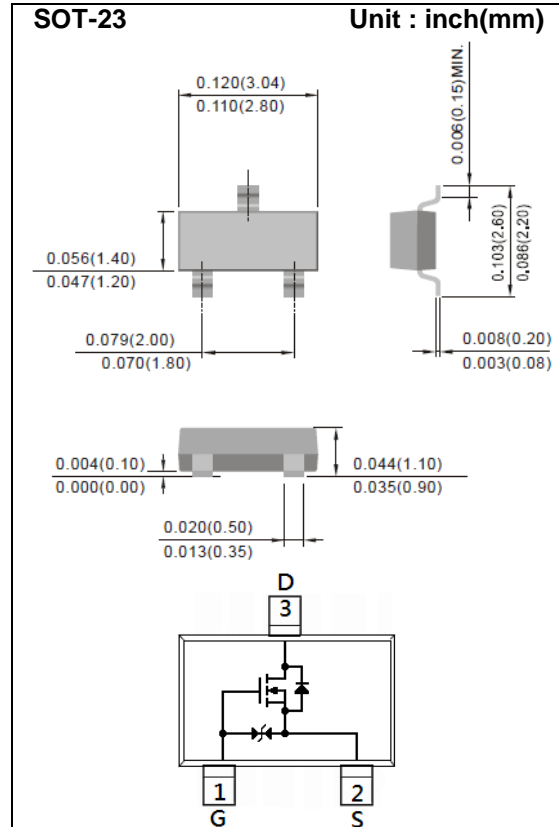
**Voltage** 50 V **Current** 500mA

### Features

- RDS(ON) , V<sub>GS</sub>@10V, I<sub>D</sub>@500mA<1.6Ω
- RDS(ON) , V<sub>GS</sub>@4.5V, I<sub>D</sub>@200mA<2.5Ω
- RDS(ON) , V<sub>GS</sub>@2.5V, I<sub>D</sub>@100mA<4.5Ω
- Advanced Trench Process Technology.
- Specially Designed for Battery Operated Systems, Solid-State Relays Drivers: Relay, Displays, Memories, etc.
- ESD Protected 2KV HBM
- Lead free in compliance with EU RoHS2.0 (2011/65/EU & 2015/865/EU directive)
- Green molding compound as per IEC61249 Std..(Halogen Free)

### Mechanical Data

- Case: SOT-23 Package
- Terminals: Solderable per MIL-STD-750, Method 2026



### Maximum Ratings and Thermal Characteristics (T<sub>A</sub>=25 °C unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage	V <sub>DS</sub>	50	V	
Gate-Source Voltage	V <sub>GS</sub>	+20	V	
Continuous Drain Current	I <sub>D</sub>	500	mA	
Pulsed Drain Current	I <sub>DM</sub>	1200	mA	
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C	500	mW
		Derate above 25°C	4	mW/°C
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55~150	°C	
Typical Thermal Resistance	R <sub>θJA</sub>	250	°C/W	
- Junction to Ambient <sup>(Note 3)</sup>				



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## Electrical Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.8	1.0	1.5	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=500mA$	-	0.96	1.6	$\Omega$
		$V_{GS}=4.5V, I_D=200mA$	-	1.25	2.5	
		$V_{GS}=2.5V, I_D=100mA$	-	2.73	4.5	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=50V, V_{GS}=0V$	-	0.01	1	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	$\pm 3.0$	$\pm 10$	
<b>Dynamic</b> (Note 4)						
Total Gate Charge	$Q_g$	$V_{DS}=25V, I_D=250mA,$ $V_{GS}=4.5V$ (Note 1,2)	-	0.63	1	nC
Gate-Source Charge	$Q_{gs}$		-	0.2	-	
Gate-Drain Charge	$Q_{gd}$		-	0.23	-	
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0MHz$	-	25	50	$\mu F$
Output Capacitance	$C_{oss}$		-	9.5	20	
Reverse Transfer Capacitance	$C_{rss}$		-	2.1	5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=25V, I_D=500mA,$ $V_{GS}=10V,$ $R_G=6\Omega$ (Note 1,2)	-	2.2	5	ns
Turn-On Rise Time	$t_r$		-	19.2	38	
Turn-Off Delay Time	$t_{d(off)}$		-	6.2	12	
Turn-Off Fall Time	$t_f$		-	23	50	
<b>Drain-Source Diode</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$	---	-	-	500	mA
Diode Forward Voltage	$V_{SD}$	$I_S=500mA, V_{GS}=0V$	-	0.86	1.5	V

**NOTES :**

1. Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. mounted on a 1 inch square pad of copper
4. Guaranteed by design, not subject to production testing.



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## TYPICAL CHARACTERISTIC CURVES

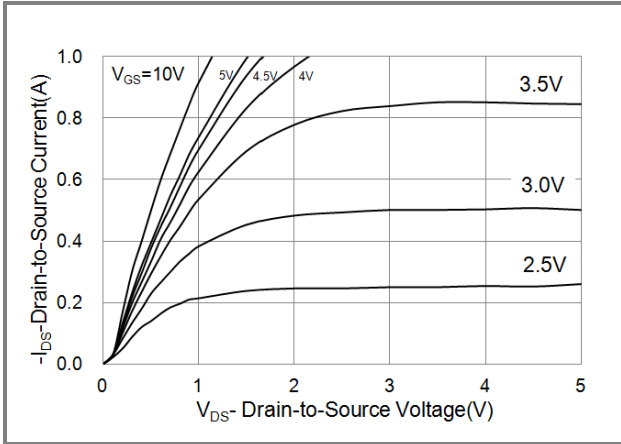


Fig.1 On-Region Characteristics

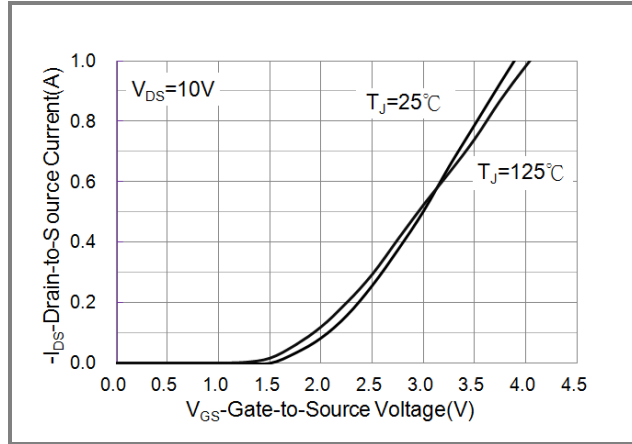


Fig.2 Transfer Characteristics

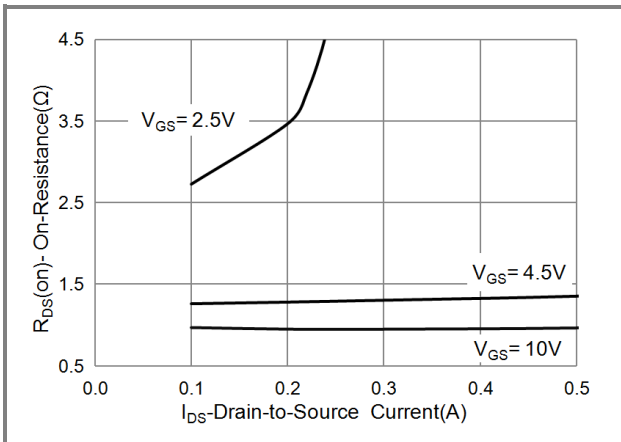


Fig.3 On-Resistance vs. Drain Current

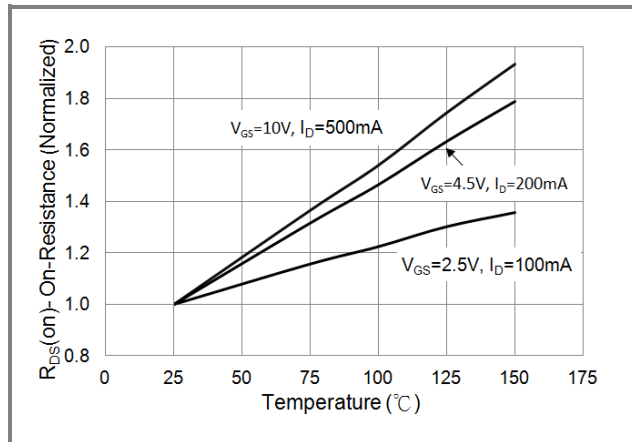


Fig.4 On-Resistance vs. Junction temperature

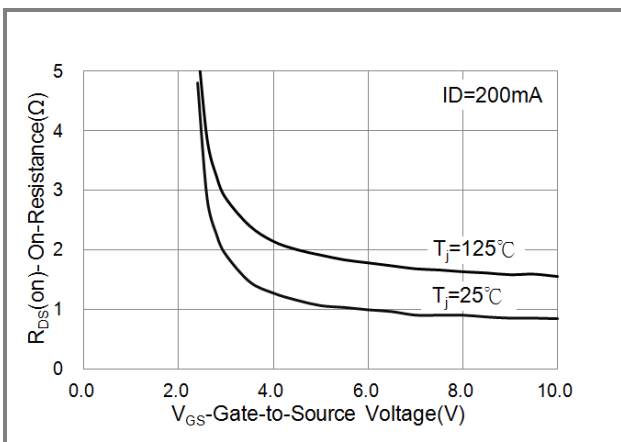


Fig.5 On-Resistance Variation with VGS.

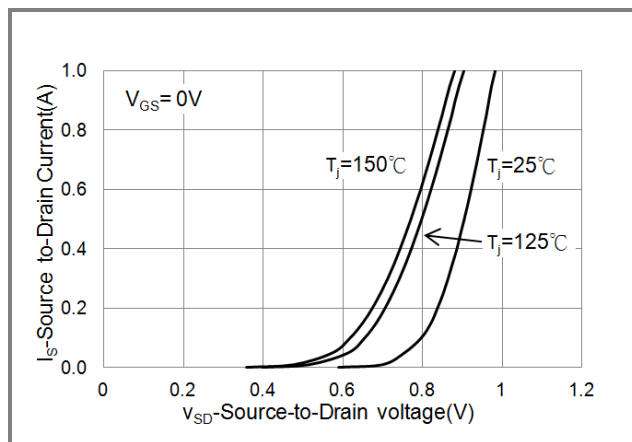


Fig.6 Body Diode Characteristics



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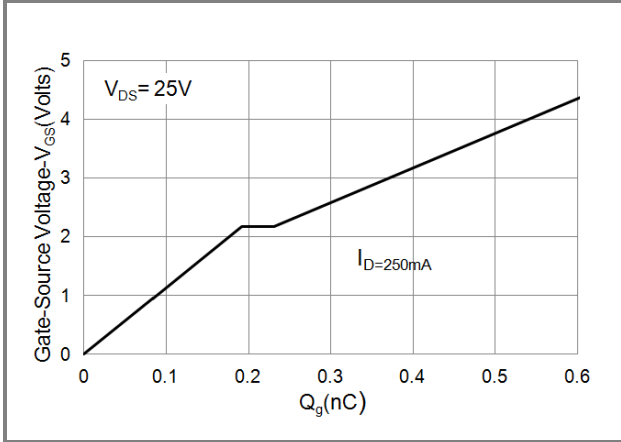


Fig.7 Gate-Charge Characteristics

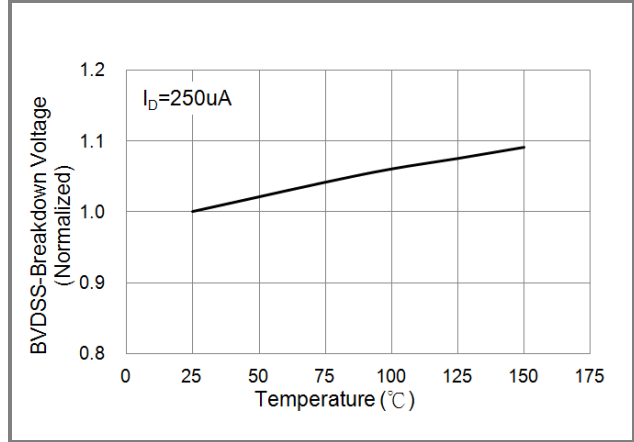


Fig.8 Breakdown Voltage Variation vs. Temperature

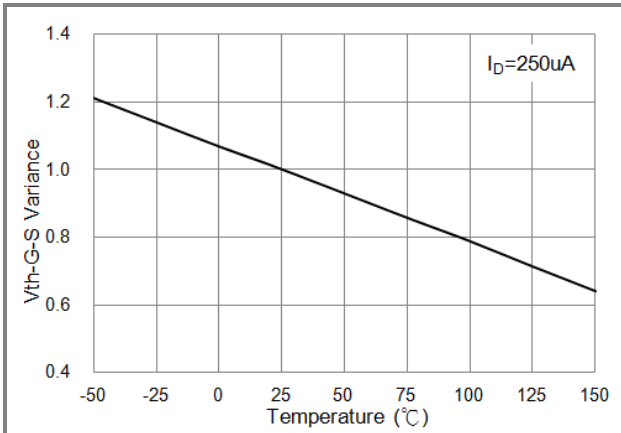


Fig.9 Threshold Voltage Variation with Temperature.

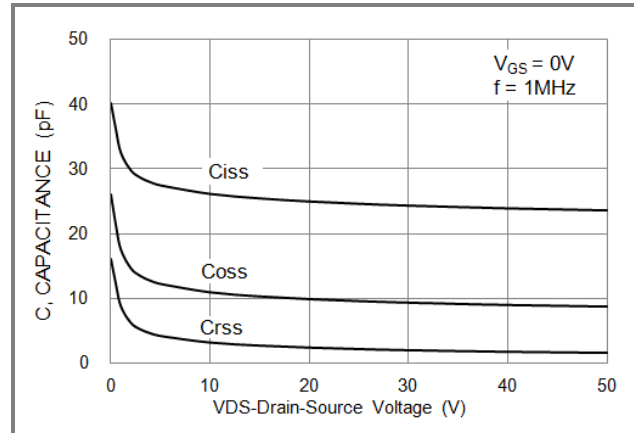


Fig.10 Capacitance vs. Drain-Source Voltage.

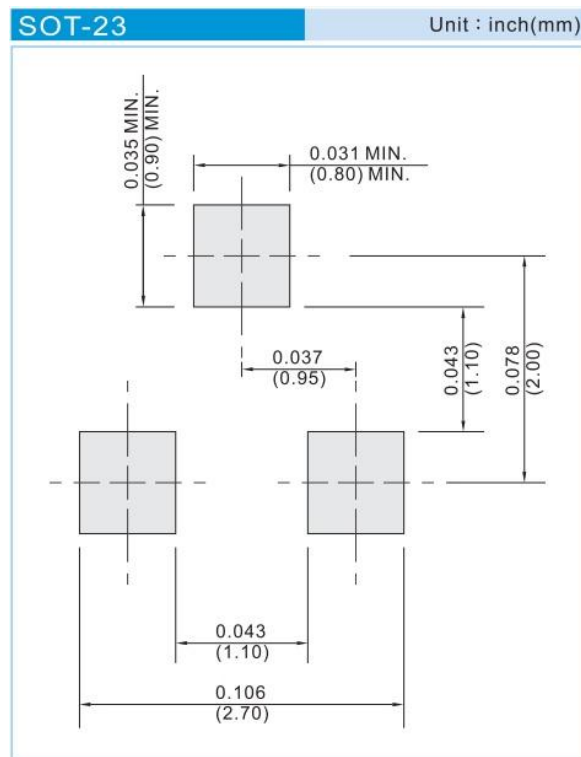


# PJA138K

## PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJA138K_R1_00001	SOT-23	3K pcs / 7" reel	8K3	Halogen free
PJA138K_R2_00001	SOT-23	12K pcs / 13" reel	8K3	Halogen free

## MOUNTING PAD LAYOUT





## PJA138K

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