# 1 Watt, GaAs pHEMT MMIC Power Amplifier, 27 GHz to 32 GHz

Data Sheet

# HMC1132

## FEATURES

**Saturated output power ($P_{SAT}$): 30.5 dBm at 22% power added efficiency (PAE)**
**High output IP3: 35 dBm**
**High gain: 22 dB**
**DC supply: 6 V at 600 mA**
**No external matching required**
**32-lead, 5 mm × 5 mm LFCSP package**

## APPLICATIONS

**Point-to-point radios**
**Point-to-multipoint radios**
**VSAT and SATCOM**
**Military and space**

## FUNCTIONAL BLOCK DIAGRAM

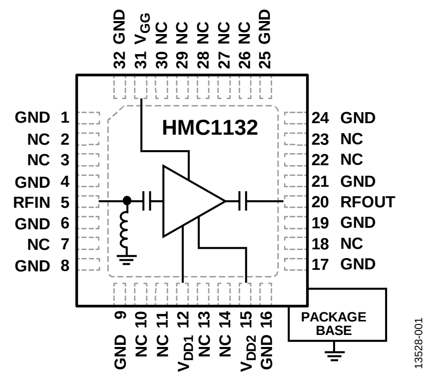


*Figure 1.*

## GENERAL DESCRIPTION

The HMC1132 is a four-stage, GaAs pHEMT MMIC, 1 watt power amplifier that operates between 27 GHz and 32 GHz. The HMC1132 provides 22 dB of gain and 30.5 dBm of saturated output power at 22% PAE from a 6 V power supply.

The HMC1132 exhibits excellent linearity and it is optimized for high capacity, point-to-point and point-to-multipoint radio systems. The amplifier configuration and high gain make it an excellent candidate for last stage signal amplification before the antenna.

The HMC1132 amplifier input/outputs (I/Os) are internally matched to 50 Ω. The device is supplied in a compact, leadless QFN, 5 mm × 5 mm surface-mount package.




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Technical Support www.analog.com

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## REVISION HISTORY

**7/2016—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL SPECIFICATIONS

$T_A$ = 25°C, $V_{DD}$ = $V_{DD1}$ = $V_{DD2}$ = 6 V, $I_{DD}$ = 600 mA.

**Table 1.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| FREQUENCY RANGE | | 27 | | 32 | GHz | |
| GAIN | | 20 | 22 | | dB | |
| Gain Variation over Temperature | | | 0.036 | | dB/°C | |
| RETURN LOSS | | | | | | |
| Input | | | 6 | | dB | |
| Output | | | 14 | | dB | |
| POWER | | | | | | |
| Output Power for 1 dB Compression | P1dB | 28 | 30 | | dBm | |
| Saturated Output Power | $P_{SAT}$ | | 30.5 | | dBm | |
| OUTPUT THIRD-ORDER INTERCEPT | IP3 | | 35 | | dBm | Measurement taken at 6 V at 600 mA, $P_{OUT}$ ÷ tone = 20 dBm |
| SUPPLY VOLTAGE | $V_{DD}$ | 4 | | 6 | V | |
| QUIESCENT SUPPLY CURRENT | $I_{DD}$ | 400 | | 700 | mA | |

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| Drain Voltage Bias | 6.5 V |
| RF Input Power (RFIN)[1] | 18 dBm |
| Channel Temperature | 175°C |
| Continuous $P_{DISS}$ (T = 85°C) (Derate 61 mw/°C Above 85°C) | 5.49 W |
| Thermal Resistance ($R_{TH}$) Junction to Ground Paddle | 16.4°C/W |
| Maximum Peak Reflow Temperature | 260°C |
| Storage Temperature Range | −40°C to +150°C |
| Operating Temperature Range | −40°C to +85°C |
| ESD Sensitivity (Human Body Model) | Class 0, passed 150 V |

[1] Maximum $P_{IN}$ is limited to 18 dBm or thermal limits constrained by maximum power dissipation (see Figure 31), whichever is lower.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

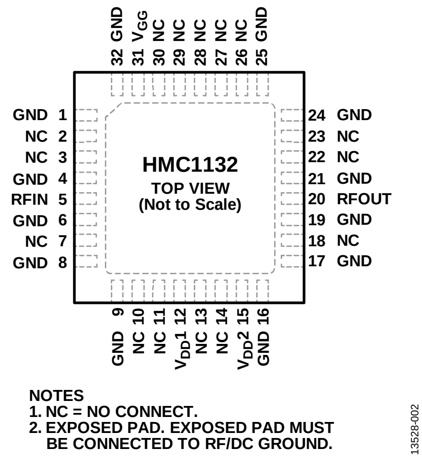


*Figure 2. Pin Configuration*

**Table 3. Pad Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 4, 6, 8, 9, 16, 17, 19, 21, 24, 25, 32 | GND | Ground. These pins are exposed ground paddles that must be connected to RF/dc ground. |
| 2, 3, 7, 10, 11, 13, 14, 18, 22, 23, 26 to 30 | NC | No Connect. These pins are not connected internally. However, all data was measured with these pins connected to RF/dc ground externally. |
| 5 | RFIN | RF Input. This pin is dc-coupled and matched to 50 Ω. See Figure 4 for the RFIN interface schematic. |
| 12, 15 | $V_{DD1}$, $V_{DD2}$ | Drain Bias Voltage. External by pass capacitors of 100 pF, 10 nF, and 4.7 µF are required. See Figure 5 for the $V_{DD1}$ and $V_{DD2}$ interface schematic. |
| 20 | RFOUT | RF Output. This pin is ac-coupled and matched to 50 Ω. See Figure 6 for the RFOUT interface schematic. |
| 31 | $V_{GG}$ | Gate Control for Amplifier. Adjust $V_{GG}$ to achieve the recommended bias current. External bypass capacitors of 100 pF, 10 nF, and 4.7 µF are required. See Figure 7 for the $V_{GG}$ interface schematic. |
| | EPAD | Exposed Paddle. The exposed pad must be connected to RF/dc ground. |

## INTERFACE SCHEMATICS

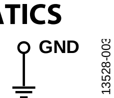


*Figure 3. GND Interface*

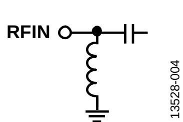


*Figure 4. RFIN Interface*

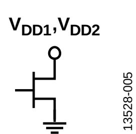


*Figure 5. $V_{DD1}$ and $V_{DD2}$ Interface*

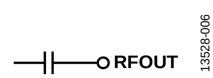


*Figure 6. RFOUT Interface*

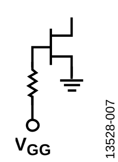


*Figure 7. $V_{GG}$ Interface*

# TYPICAL PERFORMANCE CHARACTERISTICS

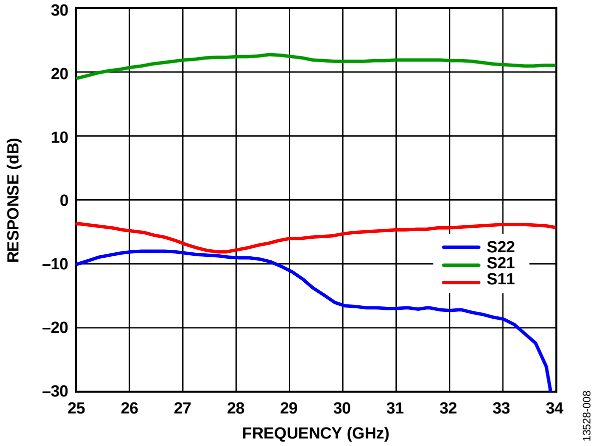


*Figure 8. Broadband Gain and Return Loss vs. Frequency*

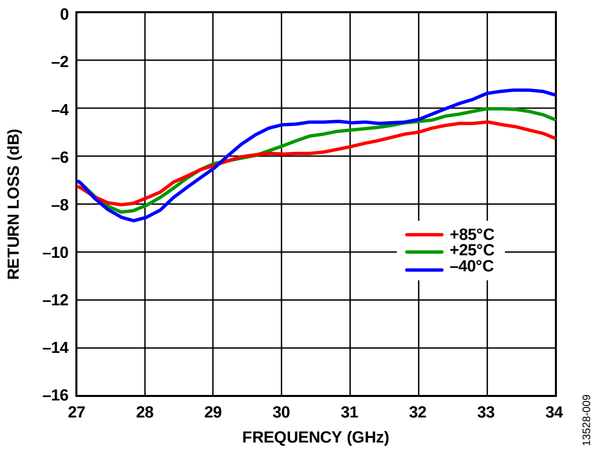


*Figure 9. Input Return Loss vs. Frequency at Various Temperatures*

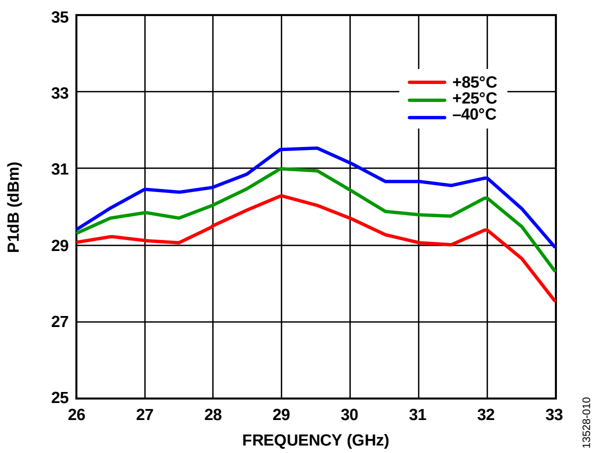


*Figure 10. P1dB vs. Frequency at Various Temperatures*

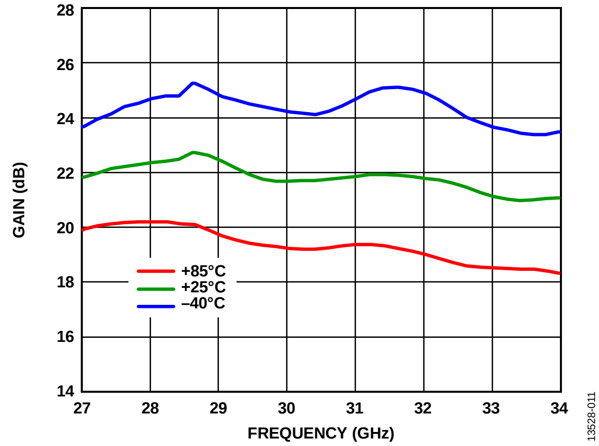


*Figure 11. Gain vs. Frequency at Various Temperatures*

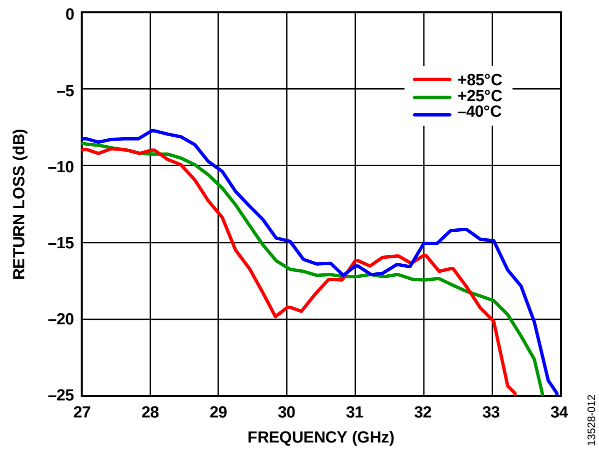


*Figure 12. Output Return Loss vs. Frequency at Various Temperatures*

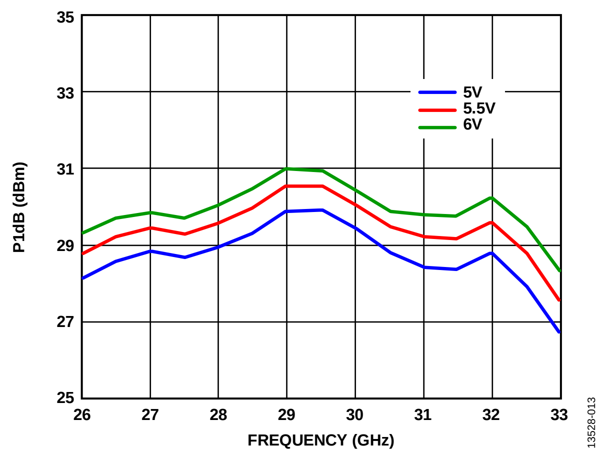


*Figure 13. P1dB vs. Frequency at Various Supply Voltages*

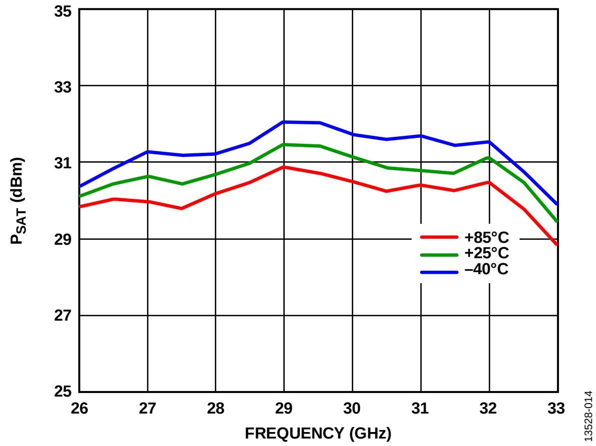


Figure 14. $P_{SAT}$ vs. Frequency at Various Temperatures

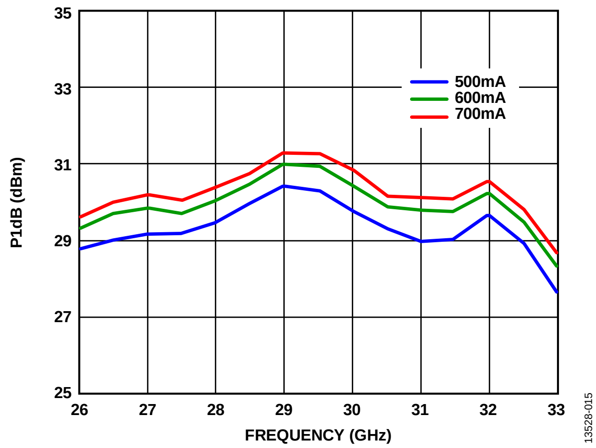


Figure 15. P1dB vs. Frequency at Various Supply Currents ($I_{DD}$)

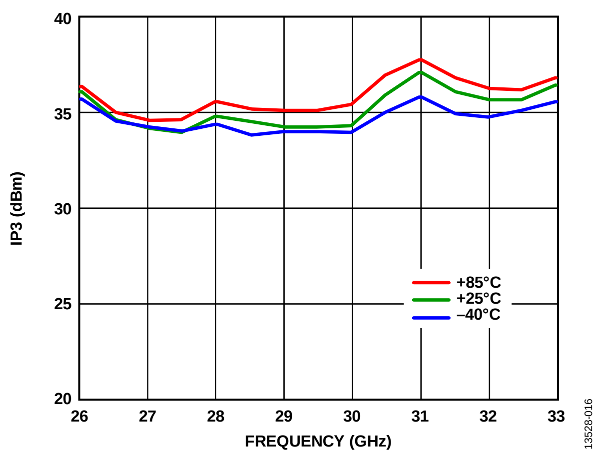


Figure 16. Output IP3 vs. Frequency at Various Temperatures, $P_{OUT}$/Tone = 20 dBm

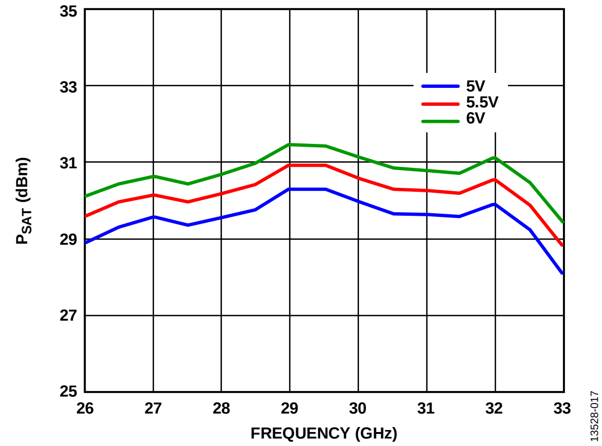


Figure 17. $P_{SAT}$ vs. Frequency at Various Supply Voltages

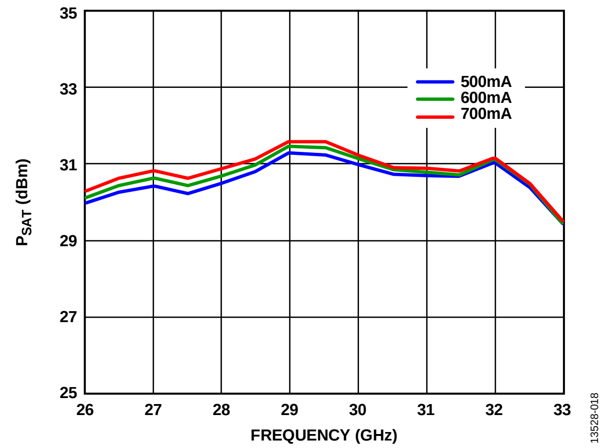


Figure 18. $P_{SAT}$ vs. Frequency at Various Supply Currents ($I_{DD}$)

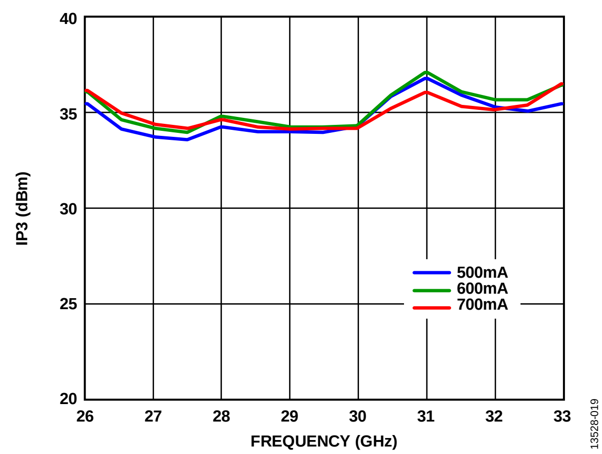


Figure 19. Output IP3 vs. Frequency at Various Supply Currents, $P_{OUT}$/Tone = 20 dBm

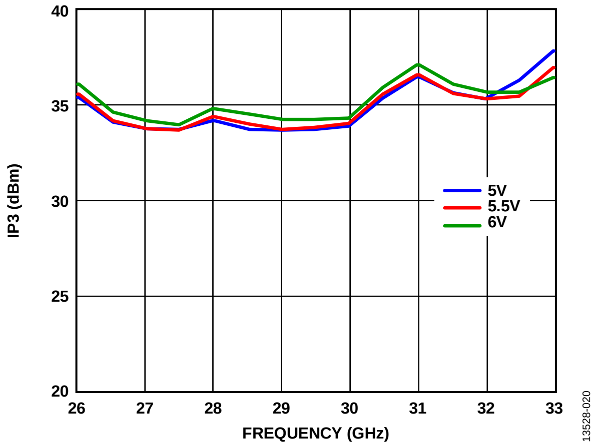


*Figure 20. Output IP3 vs. Frequency at Various Supply Voltages, $P_{OUT}$/Tone = 20 dBm*

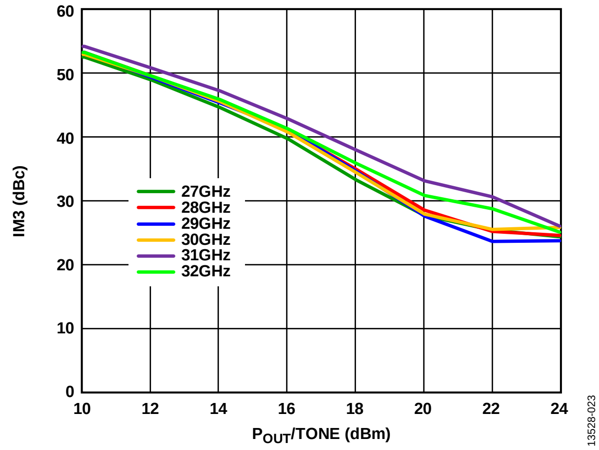


*Figure 23. Output IM3 at $V_{DD}$ = 5 V*

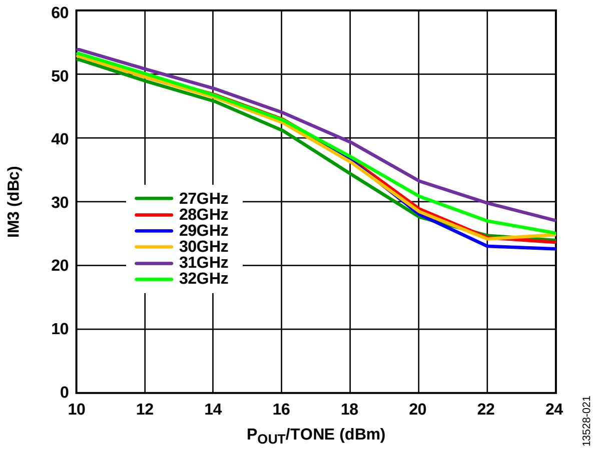


*Figure 21. Output Third-Order Intermodulation Distortion (IM3) at $V_{DD}$ = 5.5 V*

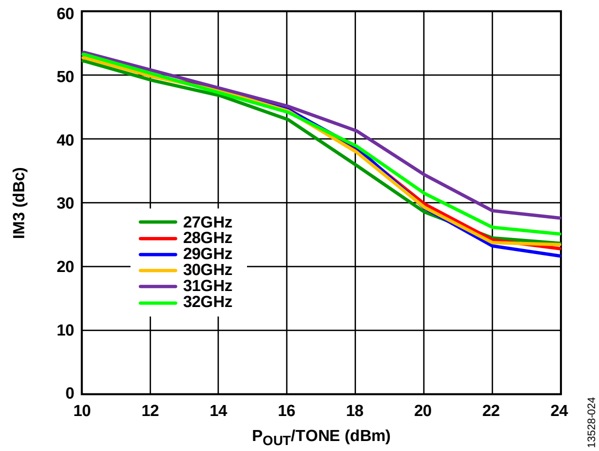


*Figure 24. Output IM3 at $V_{DD}$ = 6 V*

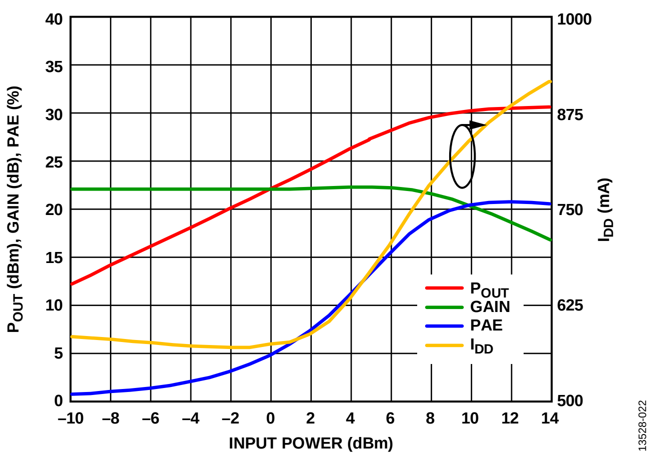


*Figure 22. Power Compression at 27 GHz*

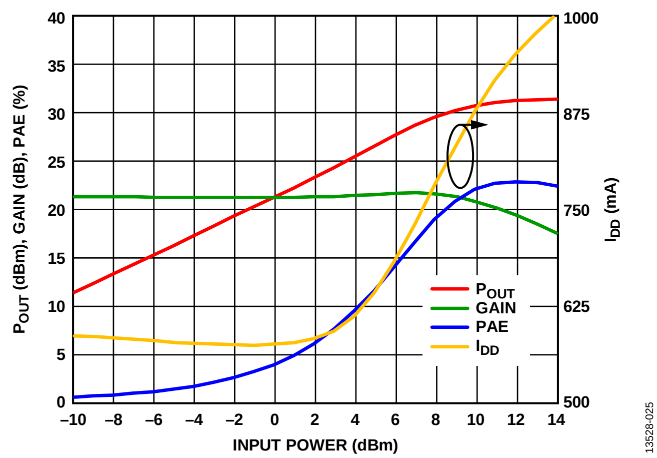


*Figure 25. Power Compression at 29.5 GHz*

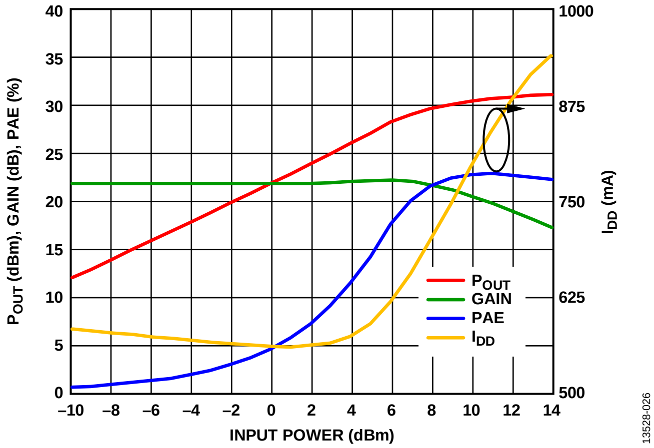


Figure 26. Power Compression at 32 GHz

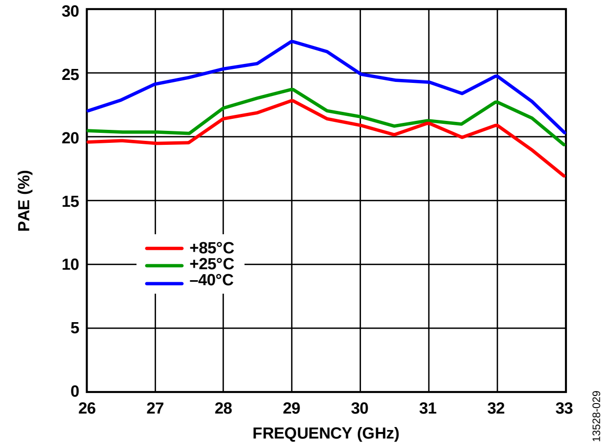


Figure 29. PAE vs. Frequency at Various Temperatures, $P_{IN}$ = 10 dBm

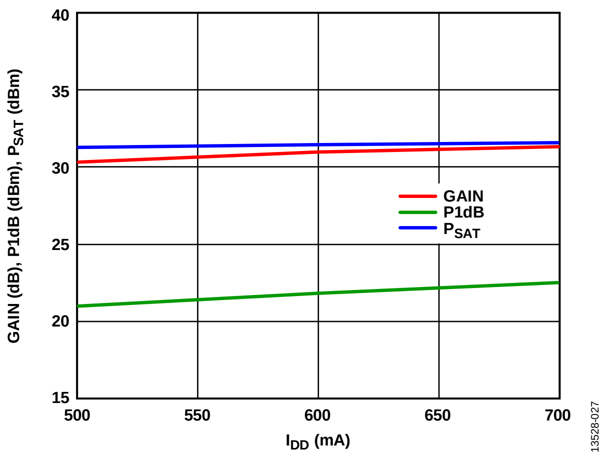


Figure 27. Gain and Power vs. Supply Current at 29.5 GHz

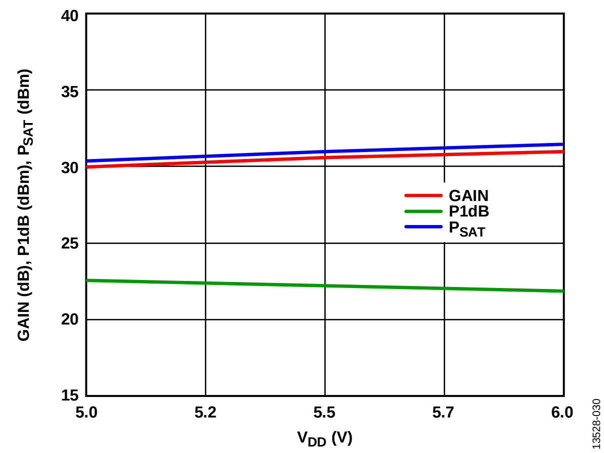


Figure 30. Gain and Power vs. Supply Voltage at 29.5 GHz

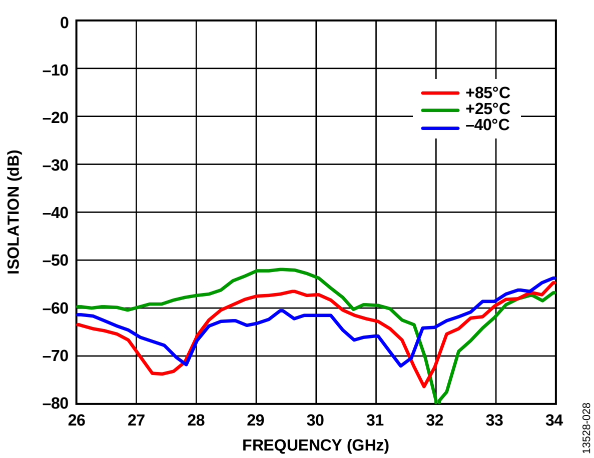


Figure 28. Reverse Isolation vs. Frequency at Various Temperatures

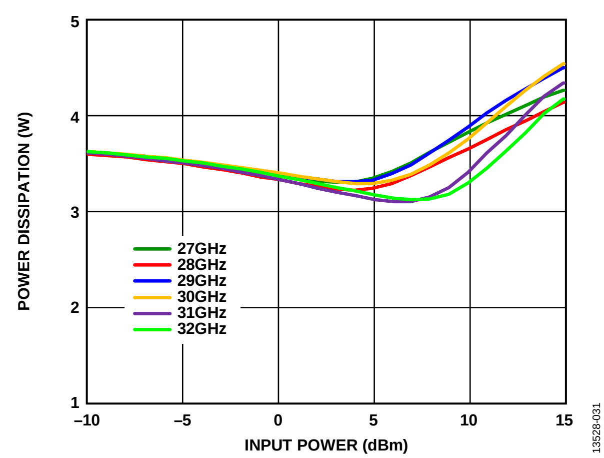


Figure 31. Power Dissipation at 85°C

# THEORY OF OPERATION

The architecture of the HMC1132 power amplifier is shown in Figure 32. The amplifier consists of a cascade of four, single-stage amplifiers. This approach provides a high P1dB as well as a high gain that is flat across the operating frequency range. $V_{DD1}$ provides drain bias to the first three gain stages, whereas $V_{DD2}$ provides drain bias to the fourth gain stage. $V_{GG}$ provides gate bias to all four gain stages, allowing control of the total quiescent drain current. RFIN and RFOUT provide dc paths to GND as a way of increasing the overall ESD robustness of the device.

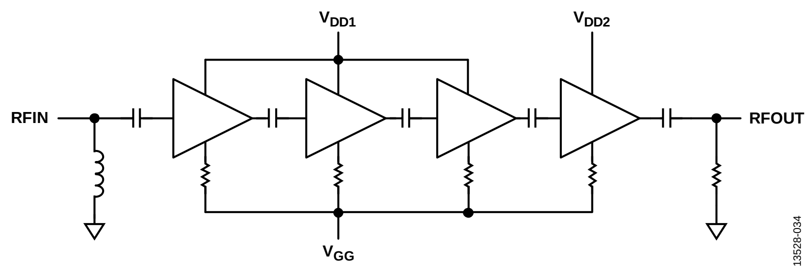


*Figure 32. Architecture and Simplified Block Diagram*

# APPLICATIONS INFORMATION

The HMC1132 is a GaAs, pHEMT, MMIC power amplifier. Capacitive bypassing is required for $V_{DD1}$ and $V_{DD2}$ as well as for $V_{GG}$ (see Figure 33). Drain bias voltage must be applied to both $V_{DD1}$ and $V_{DD2}$, and gate bias voltage must be applied to $V_{GG}$. Though the RFIN and RFOUT ports ac couple the signal, dc paths to GND are provided to increase the ESD robustness of the device. External dc blocking of RFIN and/or RFOUT is desirable when appreciable levels of dc are expected to be present.

All measurements for this device were taken using the typical application circuit shown in Figure 33, configured as shown on the evaluation printed circuit board (PCB).

The following is the recommended bias sequence during power-up:

1. Connect the evaluation board to ground.
2. Set the gate bias voltage to −2 V.
3. Set the drain bias voltages to 6 V.
4. Increase the gate bias voltage to achieve a quiescent $I_{DD}$ = 600 mA.
5. Apply the RF signal.

The following is the recommended bias sequence during power-down:

1. Turn off the RF signal.
2. Decrease the gate bias voltage to −2 V to achieve an $I_{DD}$ = 0 mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the gate bias voltage to 0 V.

The $V_{DD}$ = 6 V and $I_{DD}$ = 600 mA bias conditions are the operating points recommended to optimize the overall performance of the device. Unless otherwise noted, the data shown was obtained using the recommended bias condition. Operation of the HMC1132 at different bias conditions may provide performance that differs from what is shown in the Typical Performance Characteristics section. Biasing the HMC1132 for higher drain current typically results in higher P1dB, $P_{SAT}$, and gain, though at the expense of increased power consumption.

## APPLICATION CIRCUIT

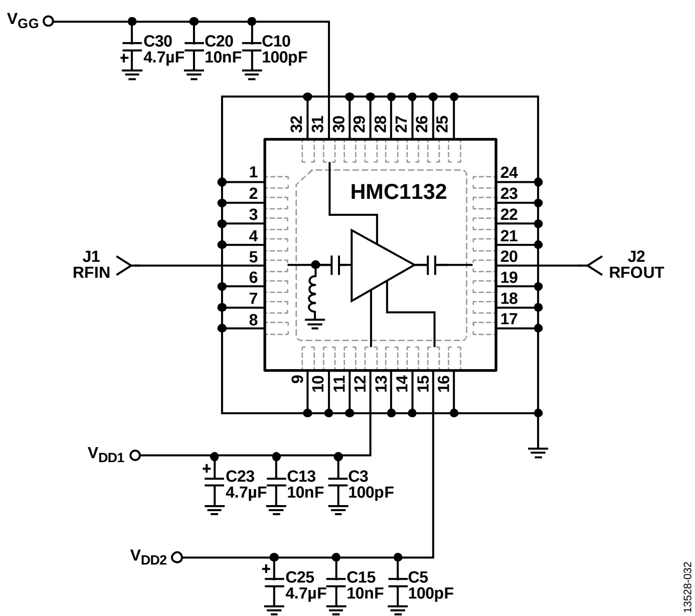


*Figure 33. Typical Application Circuit*

# EVALUATION BOARD

The HMC1132 evaluation board is a 2-layer board fabricated using Rogers 4350 and best practices for high frequency RF design. The RF input and RF output traces have a 50 Ω characteristic impedance. The circuit board is attached to a heat sink using SN96 solder and provides a low thermal resistance path. Components are mounted using SN63 solder allowing rework of the surface-mount components without compromising the circuit board to heat sink attachment.

The evaluation board and populated components are designed to operate over the ambient temperature range of −40°C to +85°C. During operation, to control the temperature of the HMC1132, attach the evaluation board to a temperature controlled plate. For proper bias sequence, see the Applications Information section.

The evaluation board schematic is shown in Figure 35. A fully populated and tested evaluation board (see Figure 34), is available from Analog Devices, Inc., upon request.

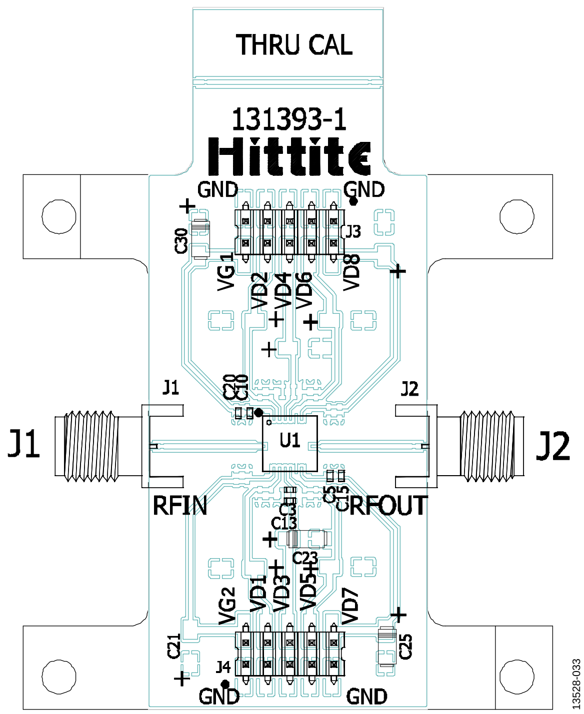


*Figure 34. Evaluation Printed Circuit Board (PCB)*

## BILL OF MATERIALS

**Table 4. Bill of Materials for Evaluation PCB EV1HMC1132LP5D**

| Item | Description |
|---|---|
| J1, J2 | Connector, SRI K connector. SRI PN 25-146-1000-92. |
| J3, J4 | DC pins. |
| J5, J6 | Connector, SRI K connector. Not populated. |
| C3, C5, C10 | 100 pF capacitors, 0402 package. |
| C13, C15, C20 | 10,000 pF capacitors, 0402 package. |
| C23, C25, C30 | 4.7 µF capacitors, Case A package. |
| U1 | HMC1132LP5DE amplifier. |
| Heat Sink | Used for thermal transfer from the HMC1132LP5DE amplifier. |
| PCB | 131393 evaluation board. Circuit board material: Rogers 4350. |

## EVALUATION BOARD SCHEMATIC

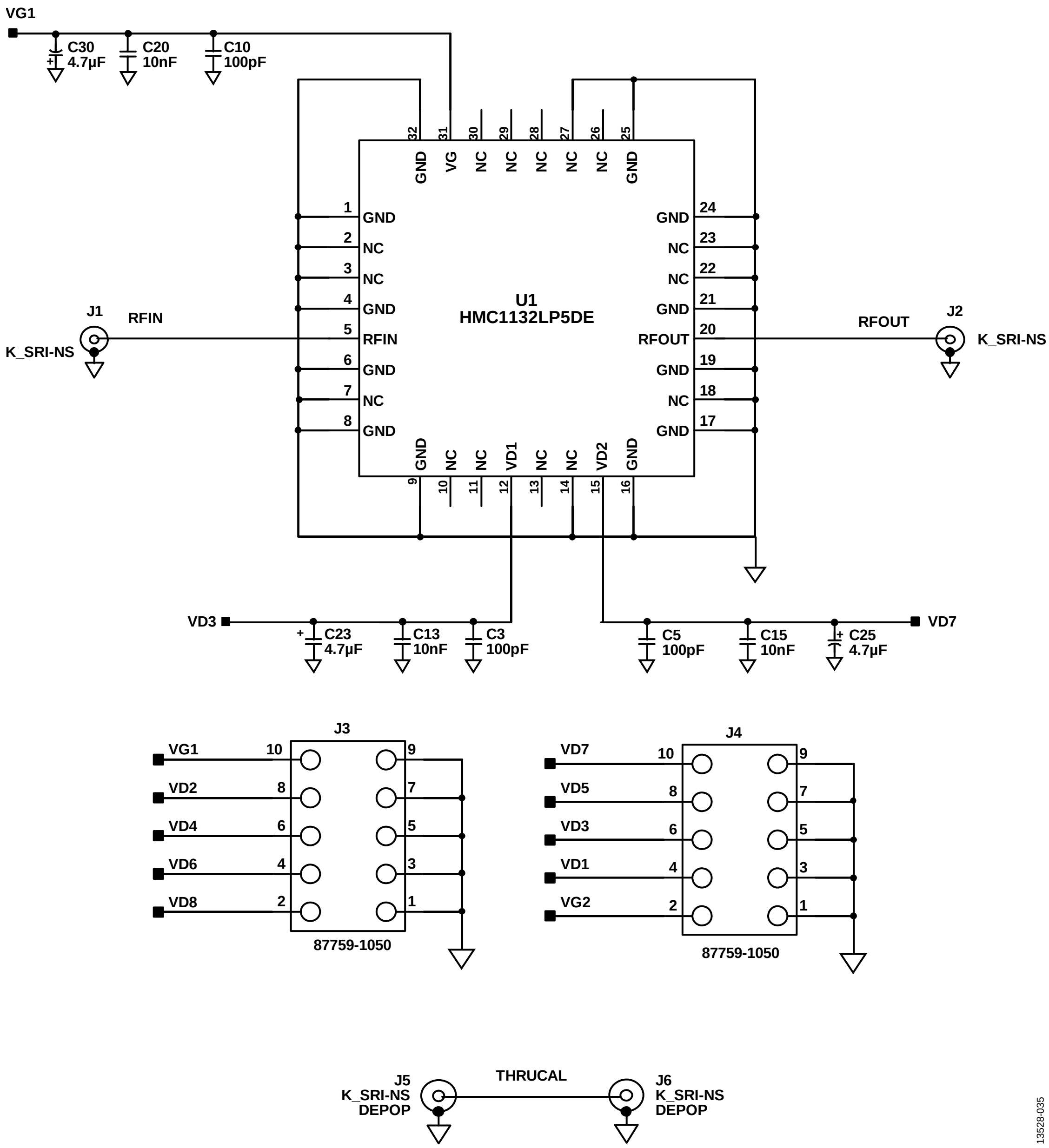


*Figure 35. Evaluation Board Schematic*

# OUTLINE DIMENSIONS

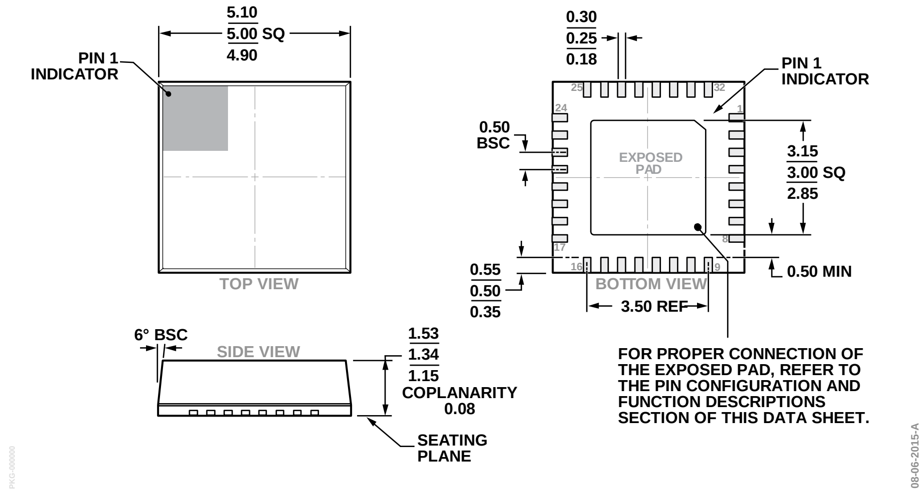


*Figure 36. 32-Lead Lead Frame Chip Scale Package [LFCSP]*
*5 mm × 5 mm Body and 1.34 mm Package Height*
*(HCP-32-2)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | MSL Rating[2] | Package Description[3, 4] | Package Option | Package Marking[5] |
|---|---|---|---|---|---|
| HMC1132LP5DE | −40°C to +85°C | MSL3 | 32-Lead Lead Frame Chip Scale Package [LFCSP] | HCP-32-2 | H1132 / XXXX |
| HMC1132LP5DETR | −40°C to +85°C | MSL3 | 32-Lead Lead Frame Chip Scale Package [LFCSP] | HCP-32-2 | H1132 / XXXX |
| EV1HMC1132LP5D | | | Evaluation board | | |

[1] When ordering the evaluation fixture only, reference the model number, EV1HMC1132LP5D.
[2] Maximum peak reflow temperature of 260°C.
[3] HMC1132LP5DE lead finish is NiPdAu.
[4] The HMC1132LP5DE is a premolded copper alloy lead frame.
[5] HMC1132LP5DE 4-digit lot number is represented by XXXX.