

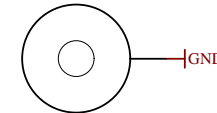
1

2

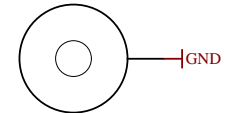
3

4

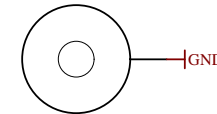
U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_REV_CH Revision_Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	
	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	



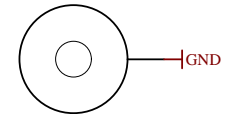
Mount.Hole 3.2mm für Unterlegscheibe



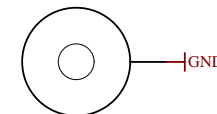
Mount.Hole 3.2mm für Unterlegscheibe



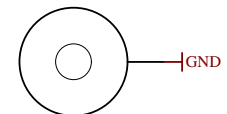
Mount.Hole 3.2mm für Unterlegscheibe



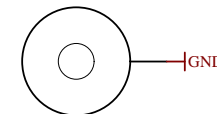
Mount.Hole 3.2mm für Unterlegscheibe



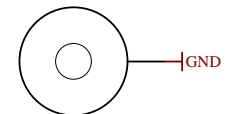
Mount.Hole 3.2mm für Unterlegscheibe



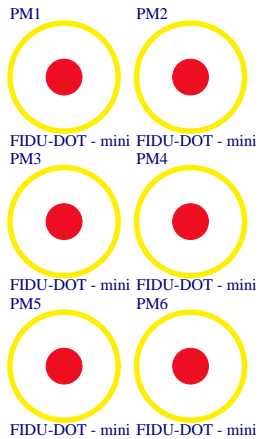
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe

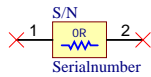


Mount.Hole 3.2mm für Unterlegscheibe



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serial
Serialnumber 6,3 x 6.3mm



	Title: TE0803	
	A4	Number: TE0803 03EG-1EB
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT
	Rev. 02	Page1 of 26
Filename: TE0803.SchDoc		

1

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A

A

B

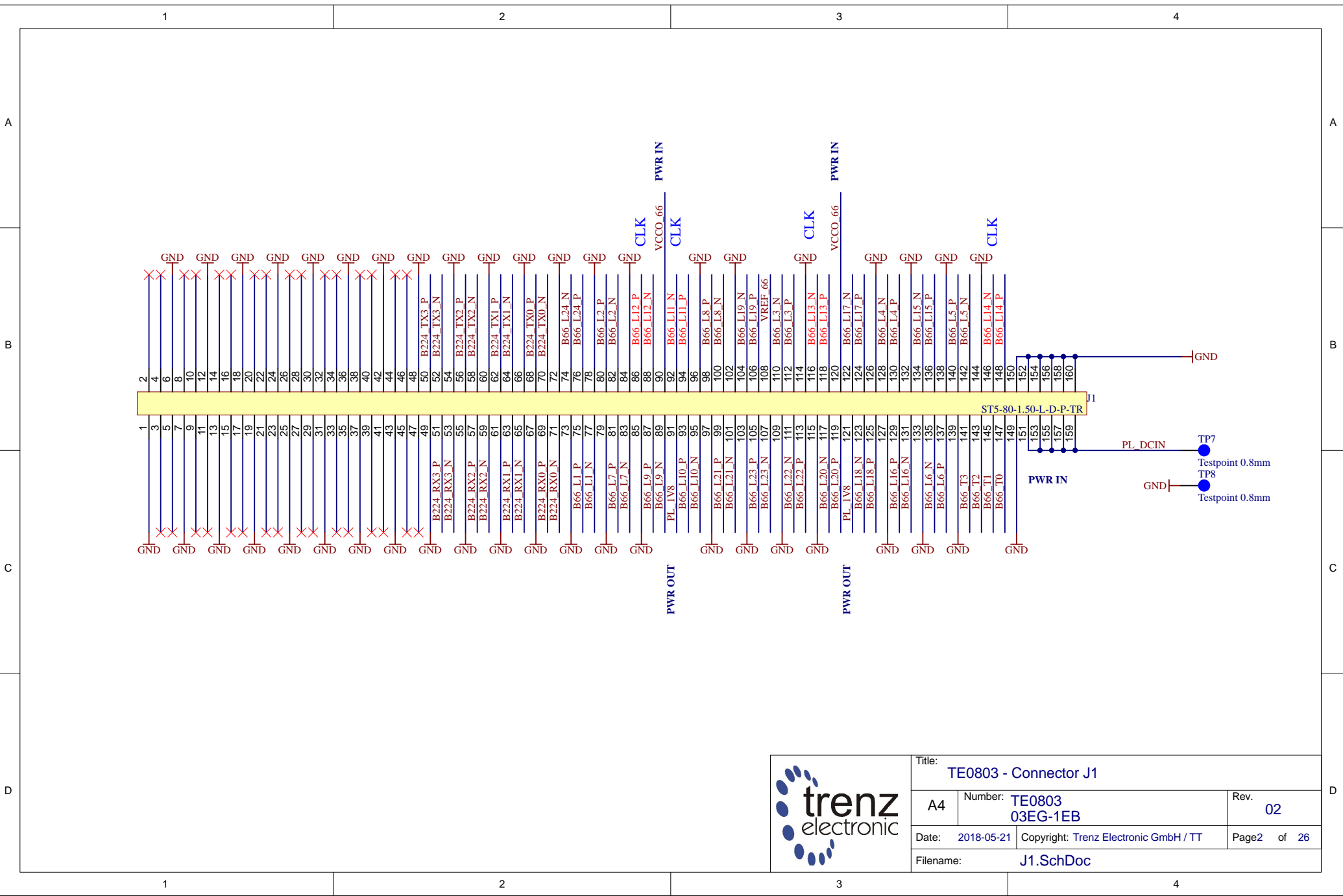

B

C

C

D

D

Title: TE0803 - Connector J1		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page2 of 26
Filename: J1.SchDoc		

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A

A

B

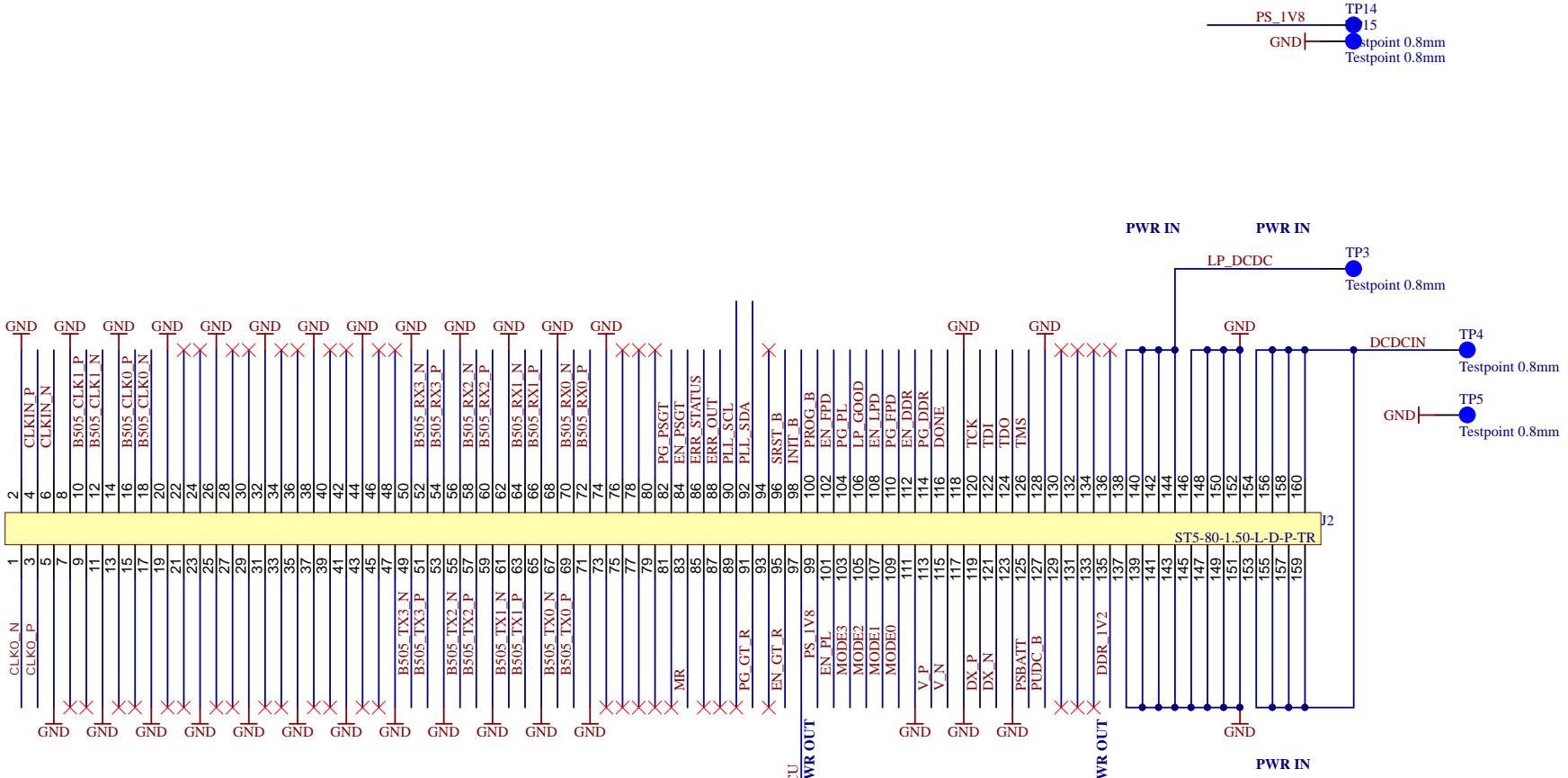
B

C

C

D

D



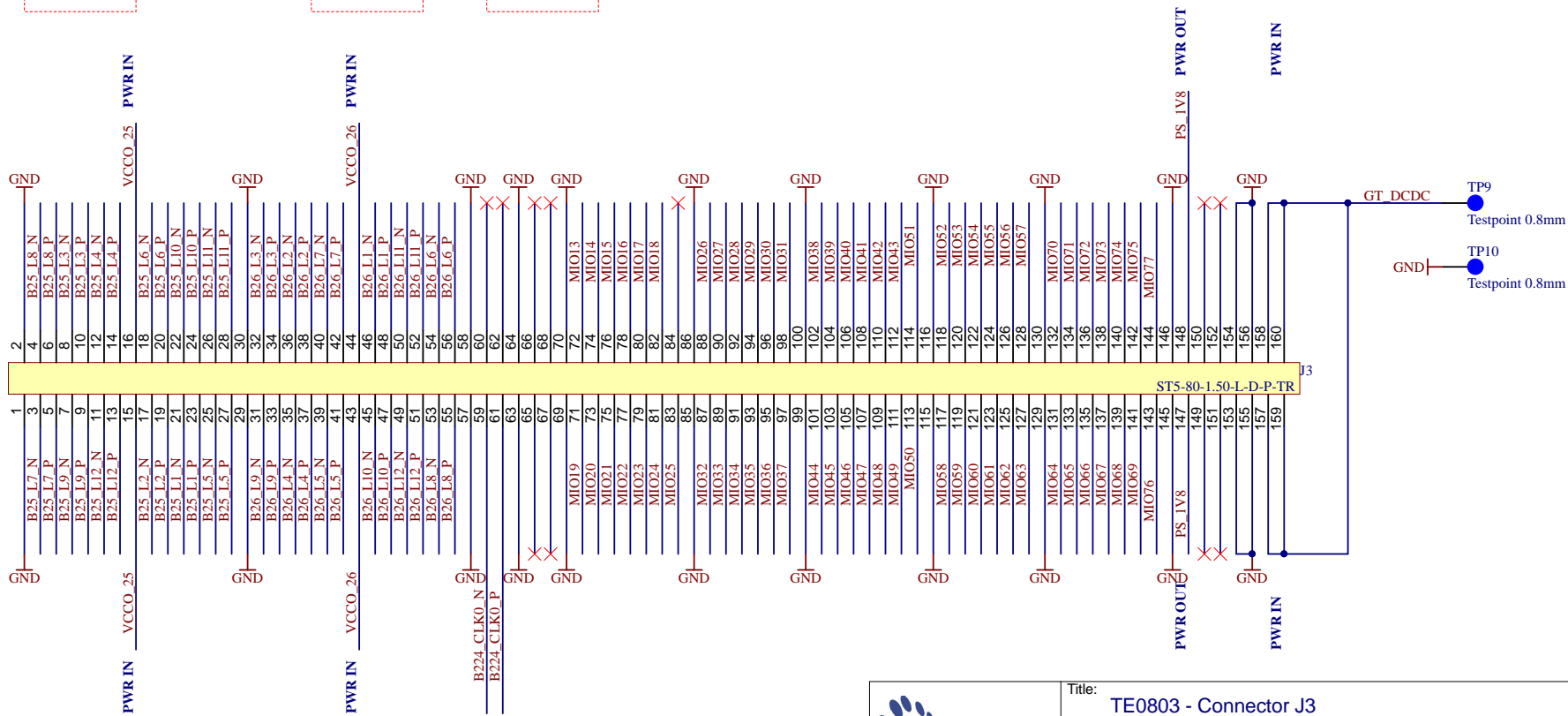
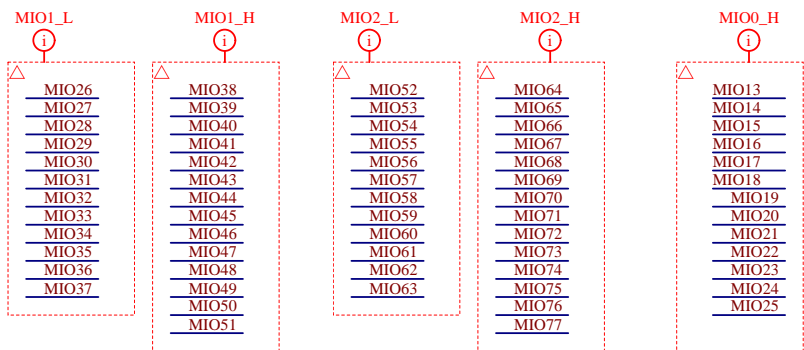
Title: TE0803 - Connector J2		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page3 of 26
Filename: J2.SchDoc		

1

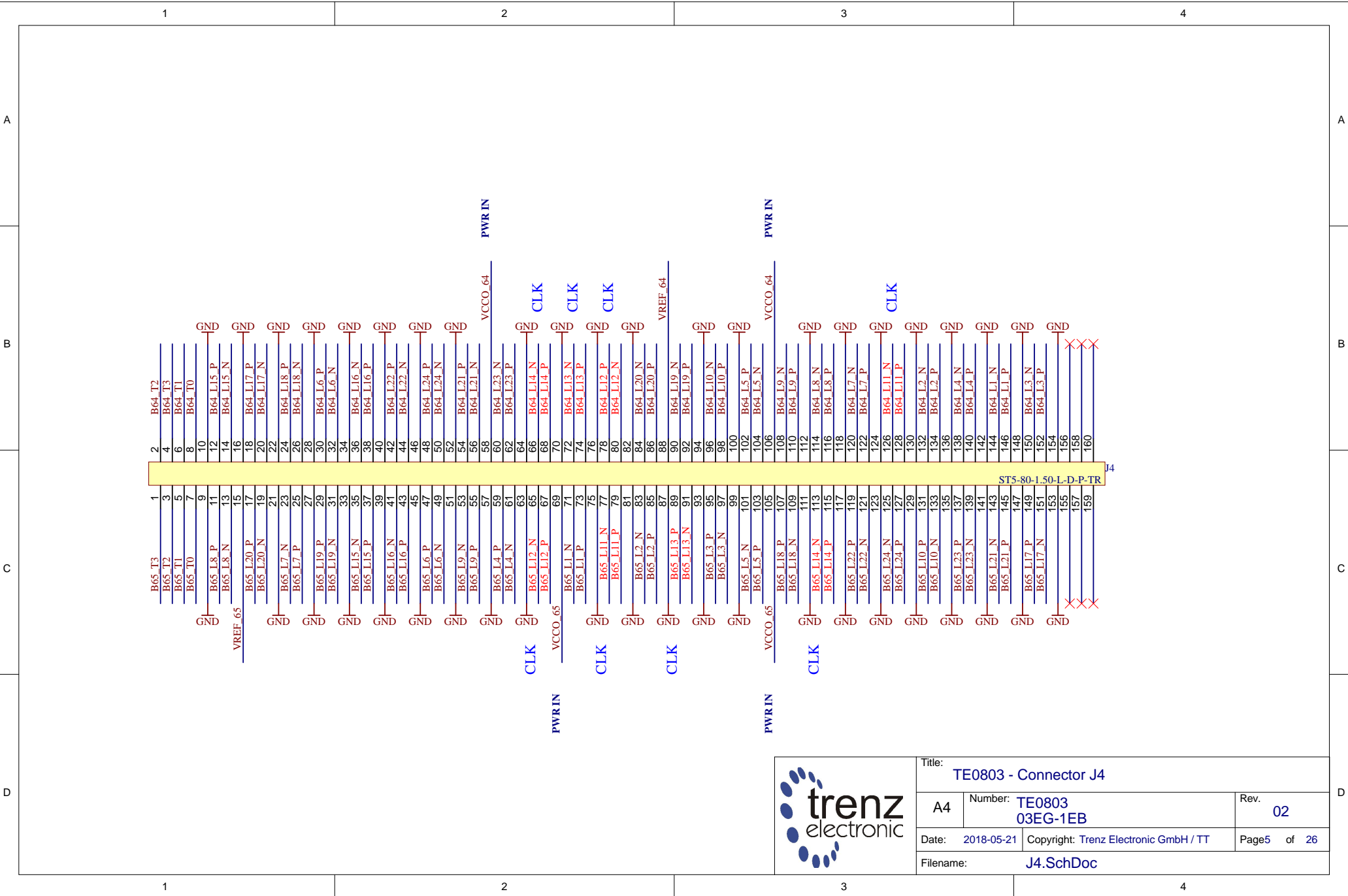
2

3

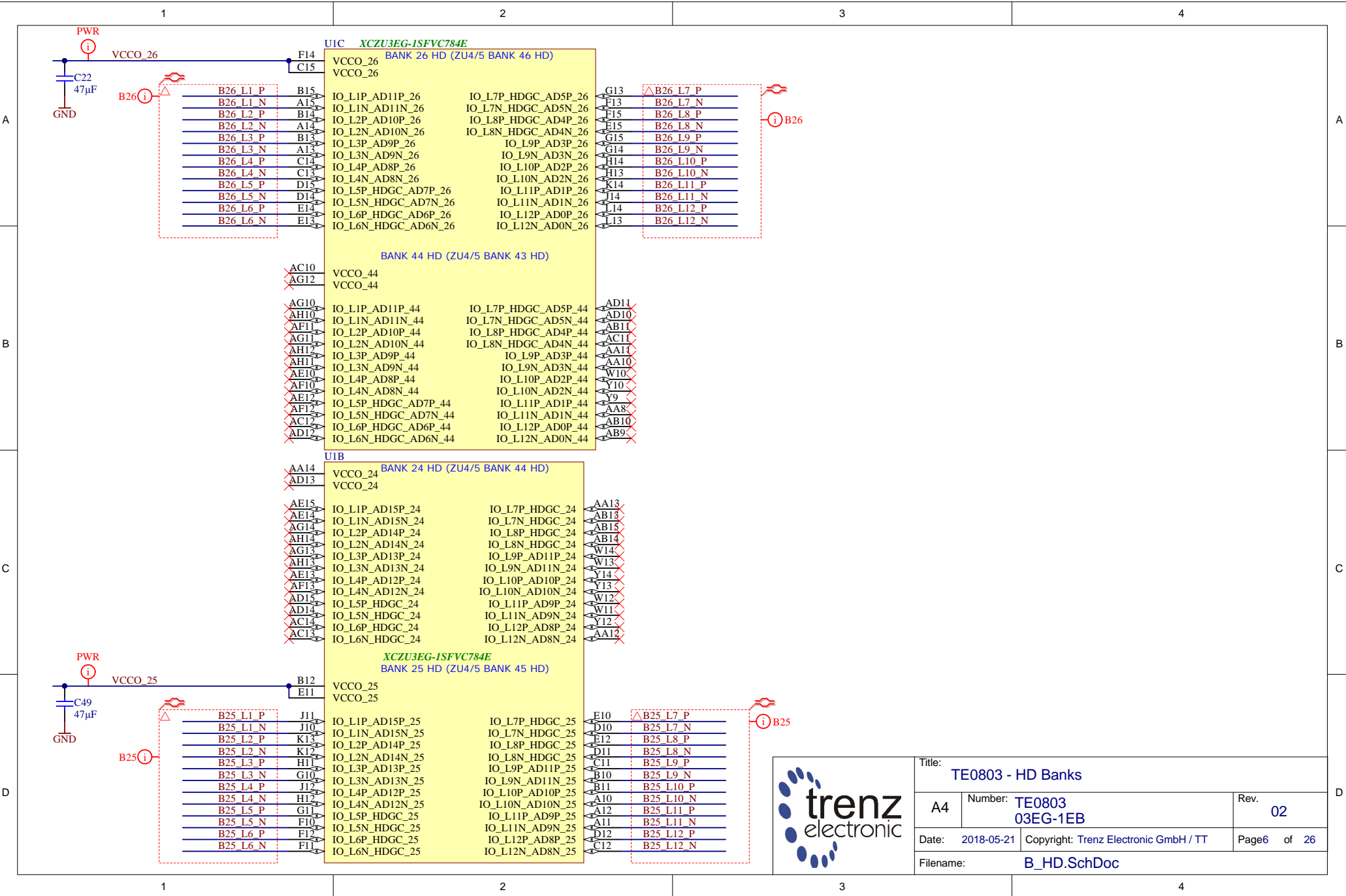
4



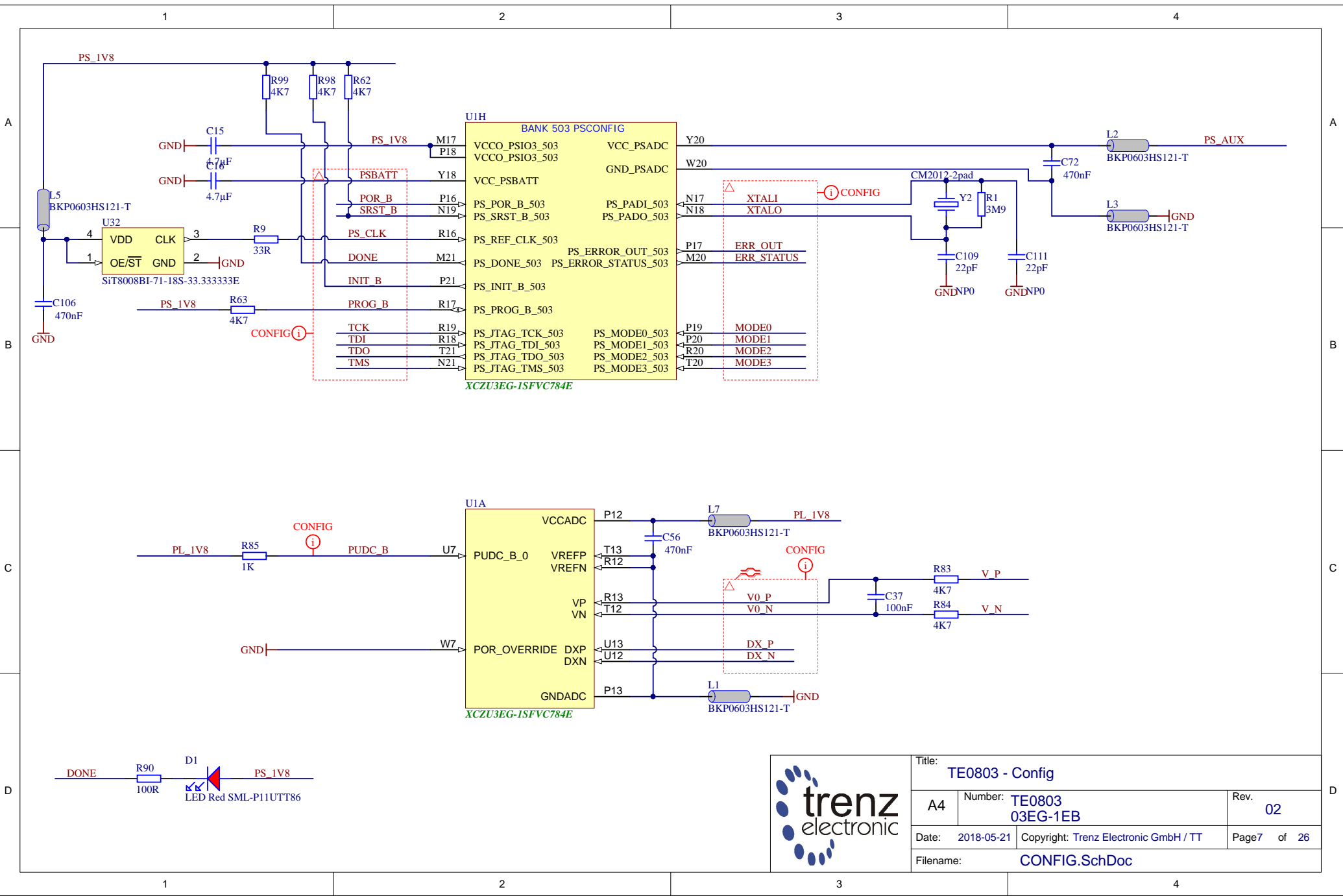
	Title: TE0803 - Connector J3	
	A4	Number: TE0803 03EG-1EB
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT
	Rev. 02	Page4 of 26
Filename: J3.SchDoc		



Title: TE0803 - Connector J4		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		



Title: TE0803 - HD Banks		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page6 of 26
Filename: B_HD.SchDoc		



U1H BANK 503 PSCONFIG

VCCO_PSIO3_503	VCC_PSADC	Y20	
VCCO_PSIO3_503	GND_PSADC	W20	
VCC_PSBATT			
POR_B	PS_PADI_503	N17	XTALI
SRST_B	PS_PADO_503	N18	
PS_CLK	PS_REF_CLK_503	P17	ERR_OUT
DONE	PS_ERROR_OUT_503	M20	
INIT_B	PS_DONE_503		
PS_ERROR_OUT_503	PS_ERROR_STATUS_503		
PS_INIT_B_503			
PROG_B	PS_PROG_B_503		
TCK	PS_JTAG_TCK_503	P19	MODE0
TDI	PS_JTAG_TDL_503	P20	MODE1
TDO	PS_JTAG_TDO_503	R20	MODE2
TMS	PS_JTAG_TMS_503	T20	MODE3
PS_MODE0_503			
PS_MODE1_503			
PS_MODE2_503			
PS_MODE3_503			

XCZU3EG-1SFVC784E

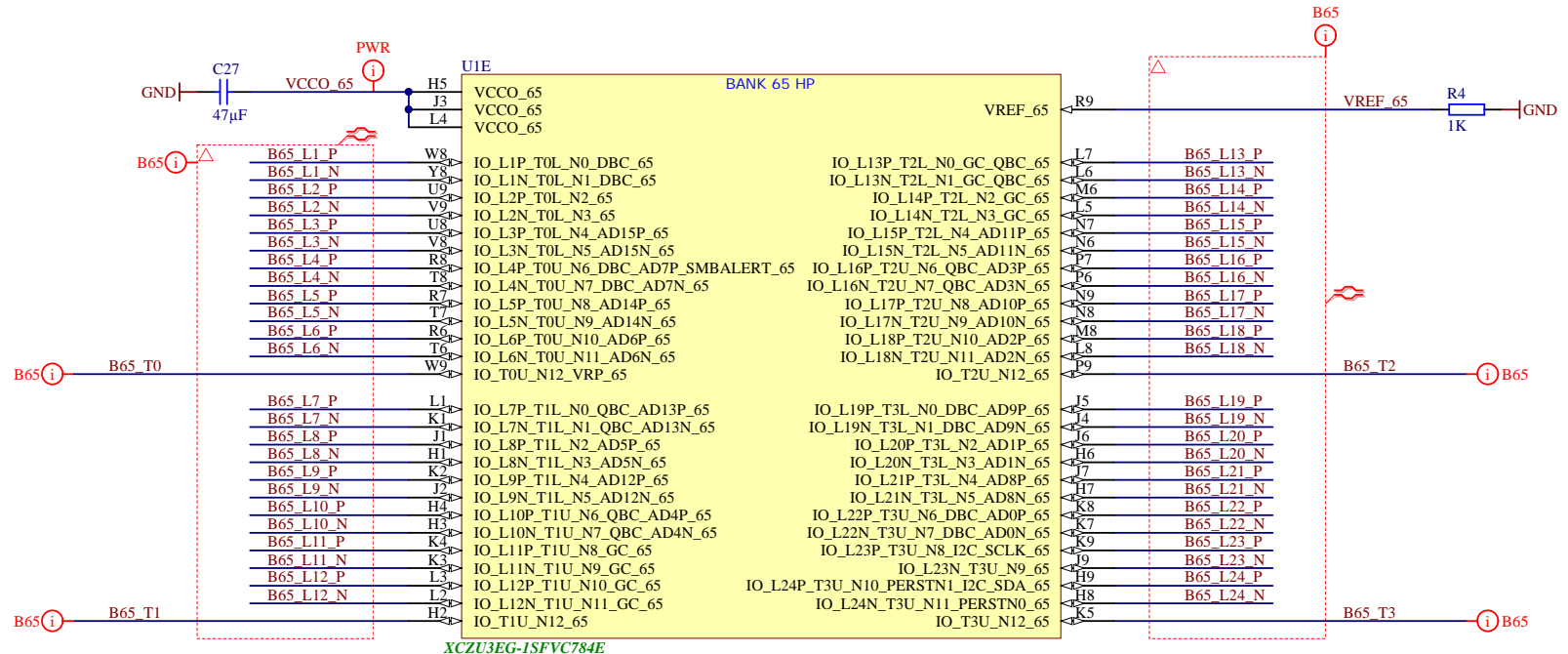
U1A

VCCADC	P12	
PUDC_B_0	T13	
VREFF	R12	
VREFN		
VP	R13	
VN	T12	
POR_OVERRIDE	U13	
DXP	U12	
DXN		
GNDADC	P13	

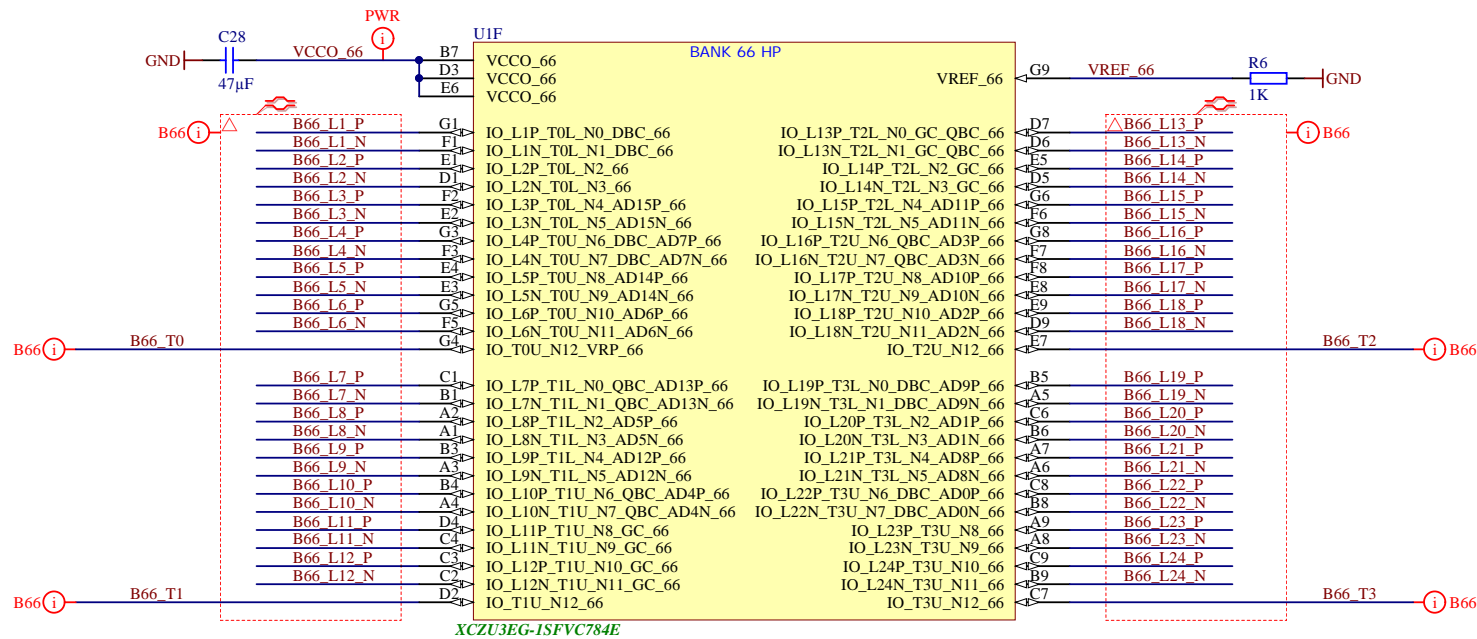
XCZU3EG-1SFVC784E

Title: TE0803 - Config		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page 7 of 26
Filename: CONFIG.SchDoc		

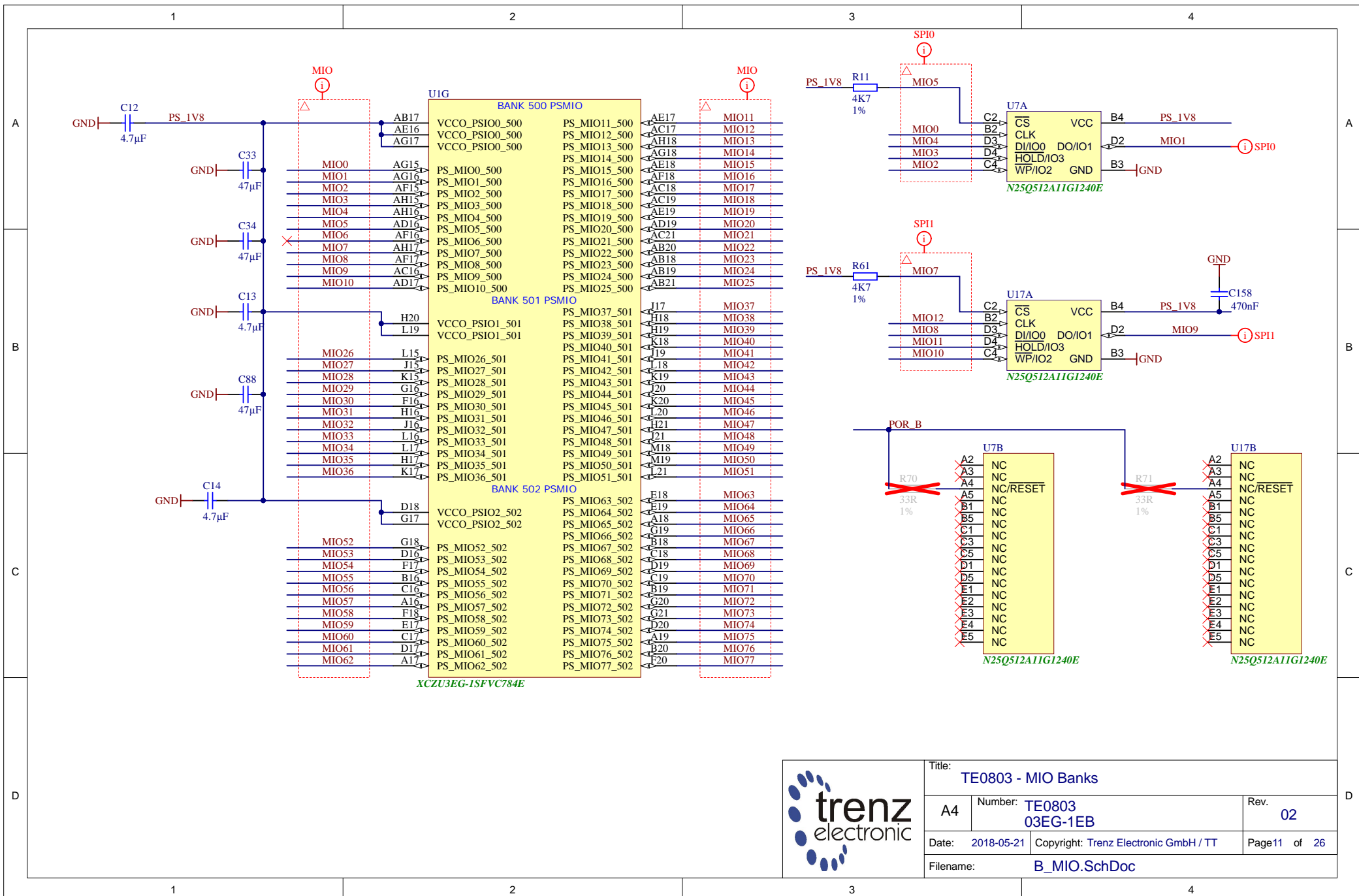




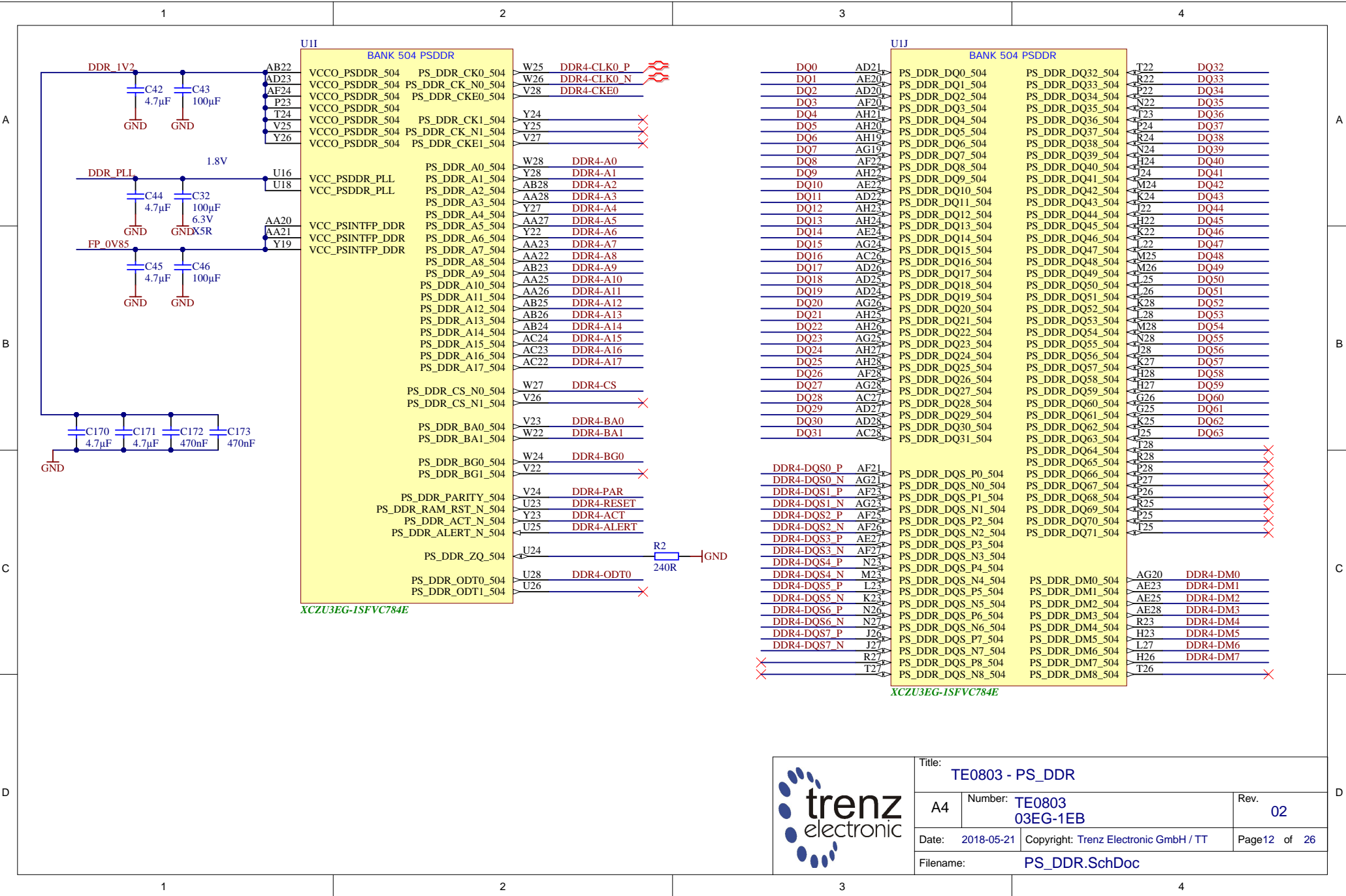
	Title: TE0803 - B65	
	A4	Number: TE0803 03EG-1EB
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT
	Filename: B65.SchDoc	Rev. 02 Page9 of 26



Title: TE0803 - B66		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page10 of 26
Filename: B66.SchDoc		



	Title: TE0803 - MIO Banks		
	A4	Number: TE0803 03EG-1EB	Rev. 02
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page 11 of 26
	Filename: B_MIO.SchDoc		



BANK 504 PSDDR

VCCO_PSDDR_504	PS_DDR_CK0_504
VCCO_PSDDR_504	PS_DDR_CK_N0_504
VCCO_PSDDR_504	PS_DDR_CKE0_504
VCCO_PSDDR_504	
VCCO_PSDDR_504	PS_DDR_CK1_504
VCCO_PSDDR_504	PS_DDR_CK_N1_504
VCCO_PSDDR_504	PS_DDR_CKE1_504
VCC_PSDDR_PLL	PS_DDR_A0_504
VCC_PSDDR_PLL	PS_DDR_A1_504
VCC_PSDDR_PLL	PS_DDR_A2_504
PS_DDR_A3_504	PS_DDR_A3_504
PS_DDR_A4_504	PS_DDR_A4_504
PS_DDR_A5_504	PS_DDR_A5_504
PS_DDR_A6_504	PS_DDR_A6_504
PS_DDR_A7_504	PS_DDR_A7_504
PS_DDR_A8_504	PS_DDR_A8_504
PS_DDR_A9_504	PS_DDR_A9_504
PS_DDR_A10_504	PS_DDR_A10_504
PS_DDR_A11_504	PS_DDR_A11_504
PS_DDR_A12_504	PS_DDR_A12_504
PS_DDR_A13_504	PS_DDR_A13_504
PS_DDR_A14_504	PS_DDR_A14_504
PS_DDR_A15_504	PS_DDR_A15_504
PS_DDR_A16_504	PS_DDR_A16_504
PS_DDR_A17_504	PS_DDR_A17_504
PS_DDR_CS_N0_504	
PS_DDR_CS_N1_504	
PS_DDR_BA0_504	
PS_DDR_BA1_504	
PS_DDR_BG0_504	
PS_DDR_BG1_504	
PS_DDR_PARITY_504	
PS_DDR_RAM_RST_N_504	
PS_DDR_ACT_N_504	
PS_DDR_ALERT_N_504	
PS_DDR_ZQ_504	
PS_DDR_ODT0_504	
PS_DDR_ODT1_504	

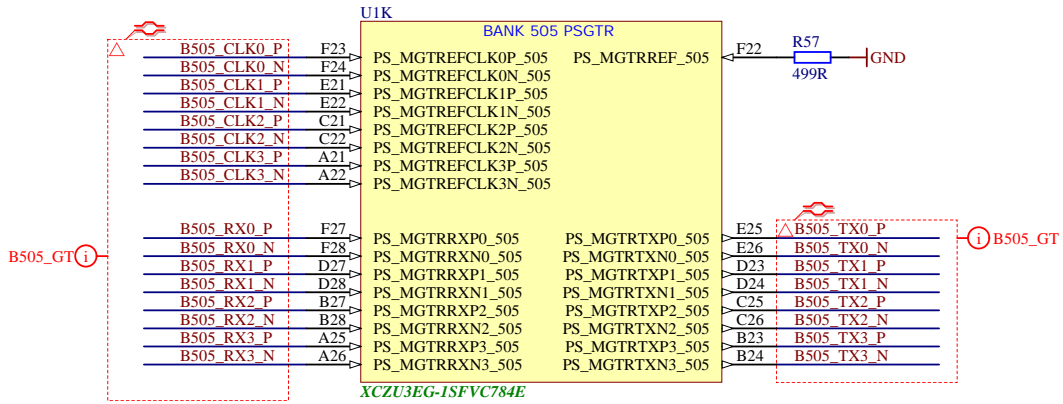
XCZU3EG-1SFVC784E


BANK 504 PSDDR

DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AF20	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AE22	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504
		PS_DDR_DQ64_504	
		PS_DDR_DQ65_504	
		PS_DDR_DQ66_504	
		PS_DDR_DQ67_504	
		PS_DDR_DQ68_504	
		PS_DDR_DQ69_504	
		PS_DDR_DQ70_504	
		PS_DDR_DQ71_504	
		PS_DDR_DQ8_504	
		PS_DDR_DM0_504	AG20 DDR4-DM0
		PS_DDR_DM1_504	AE23 DDR4-DM1
		PS_DDR_DM2_504	AE25 DDR4-DM2
		PS_DDR_DM3_504	AE28 DDR4-DM3
		PS_DDR_DM4_504	R23 DDR4-DM4
		PS_DDR_DM5_504	H23 DDR4-DM5
		PS_DDR_DM6_504	L27 DDR4-DM6
		PS_DDR_DM7_504	H26 DDR4-DM7
		PS_DDR_DM8_504	T26

XCZU3EG-1SFVC784E

	Title: TE0803 - PS_DDR	
	A4	Number: TE0803 03EG-1EB
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT
	Filename: PS_DDR.SchDoc	Rev. 02



	Title: TE0803 - PS_GT		
	A4	Number: TE0803 03EG-1EB	Rev. 02
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page13 of 26
	Filename: B_PS_GT.SchDoc		

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A

A

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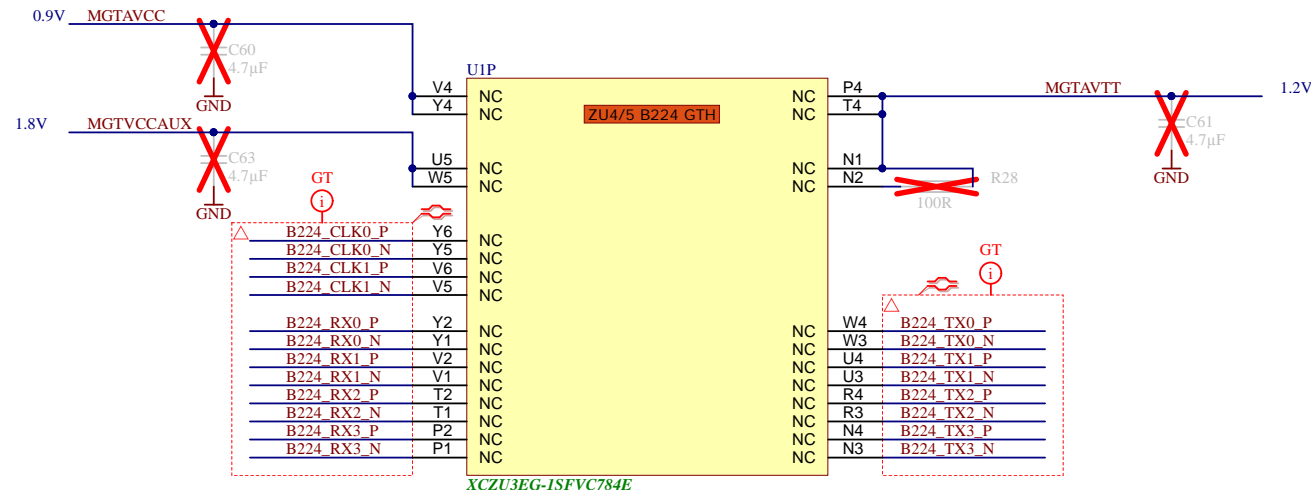
B

C

C

D

D



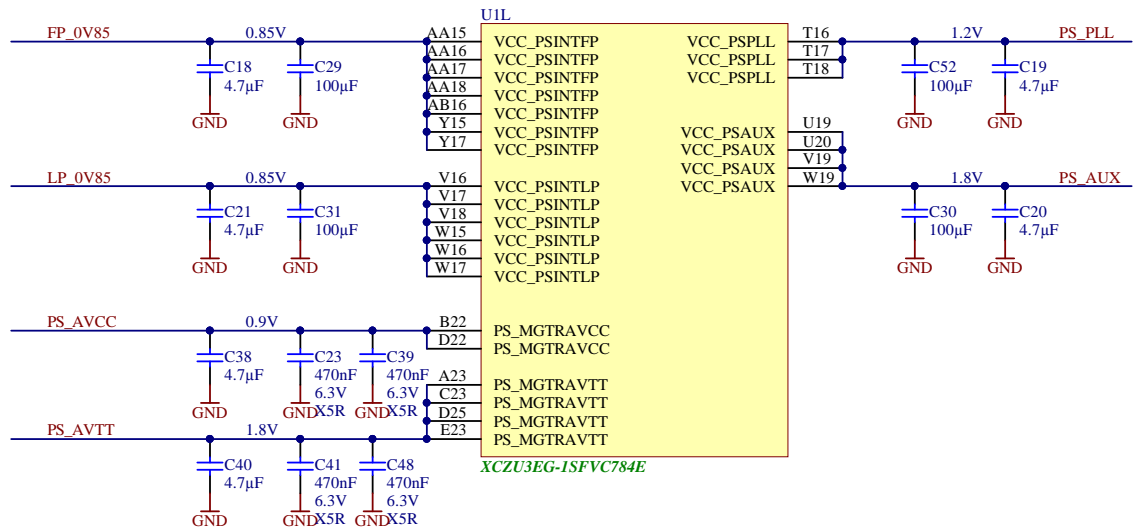
Title: TE0803 - B224GTH		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page 14 of 26
Filename: B_GT.SchDoc		

1

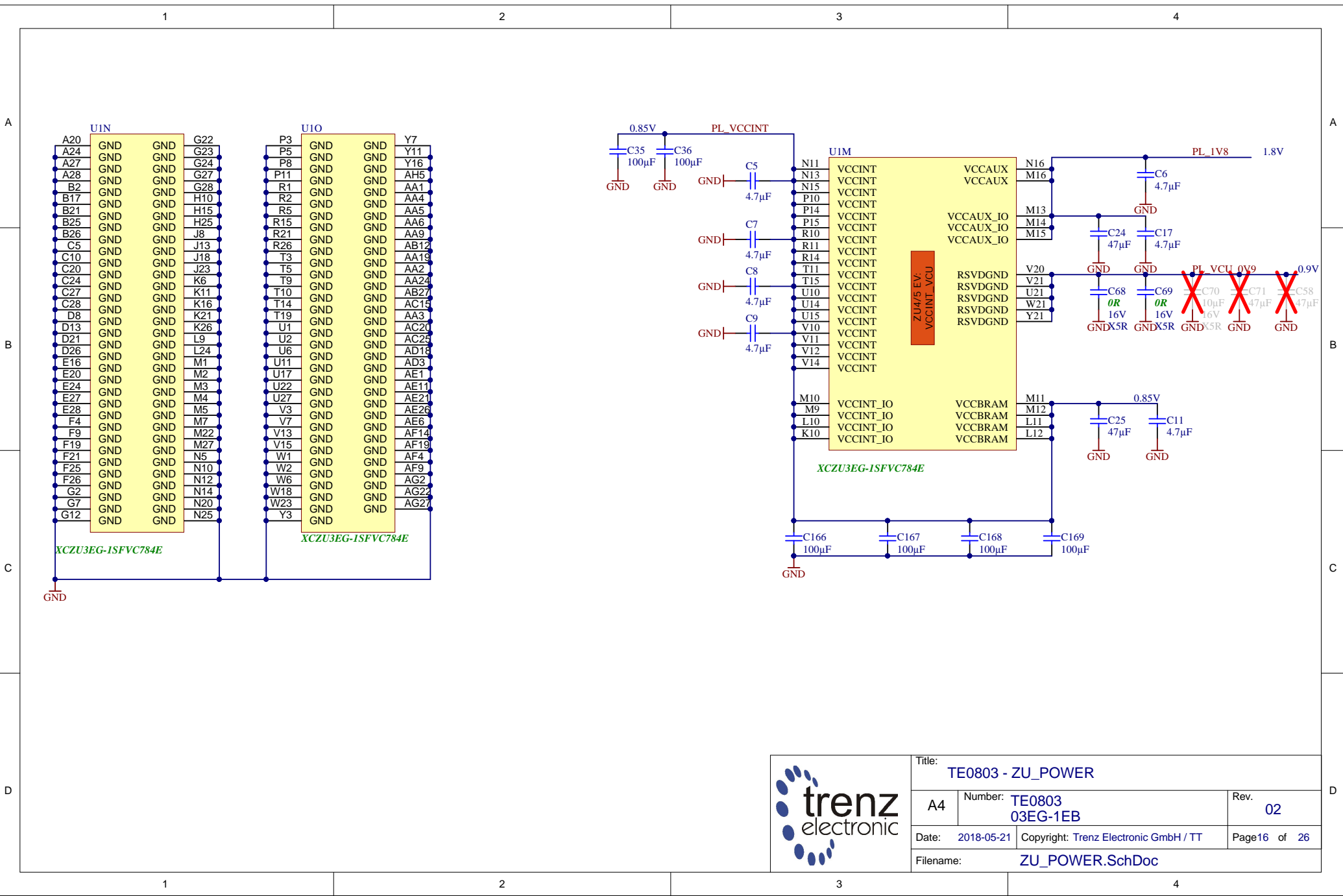
2

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Title: TE0803 - ZU_PS_POWER		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page15 of 26
Filename: ZU_PS_POWER.SchDoc		



	Title: TE0803 - ZU_POWER	
	A4	Number: TE0803 03EG-1EB
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT
	Filename: ZU_POWER.SchDoc	Page 16 of 26

1

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A

A

B

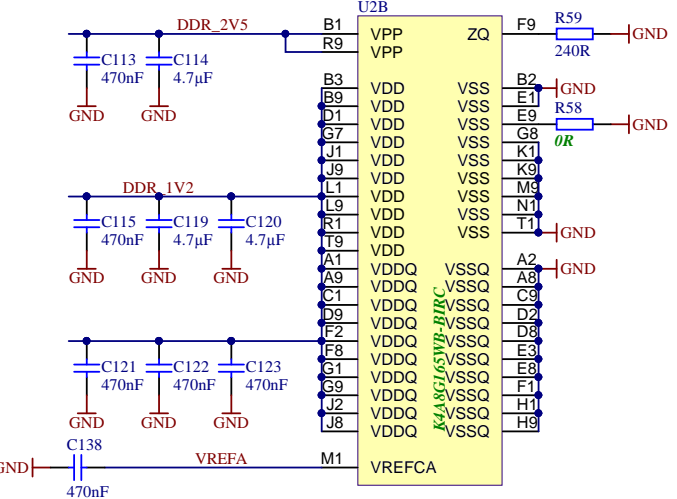
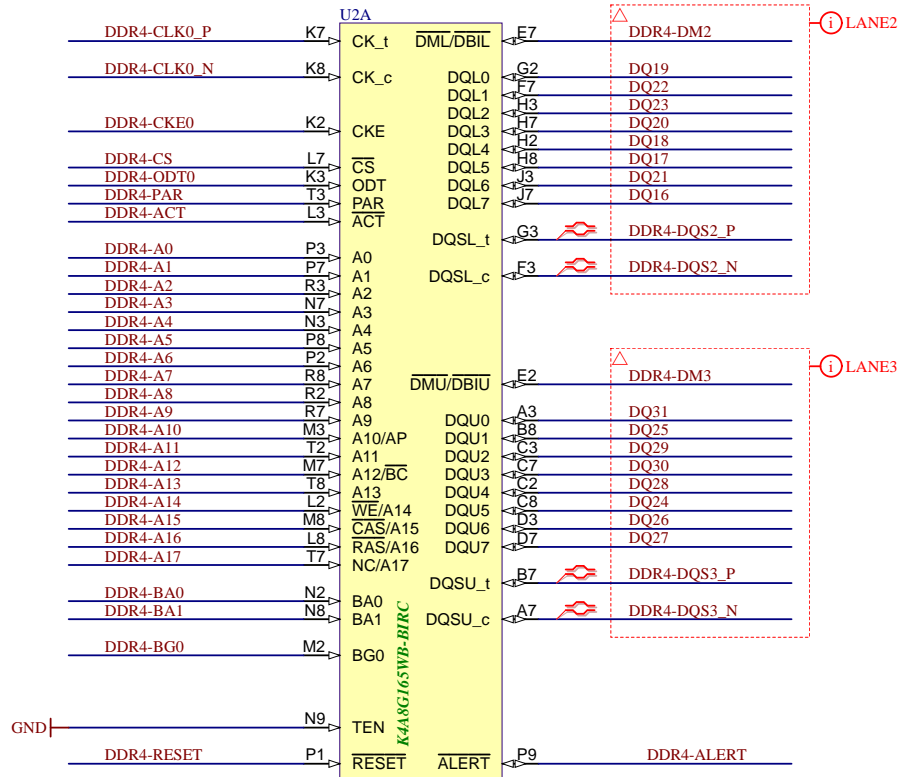
B

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D



Title: TE0803 - DDR4_1_RAM		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page17 of 26
Filename: DDR4-RAM.SchDoc		

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A

A

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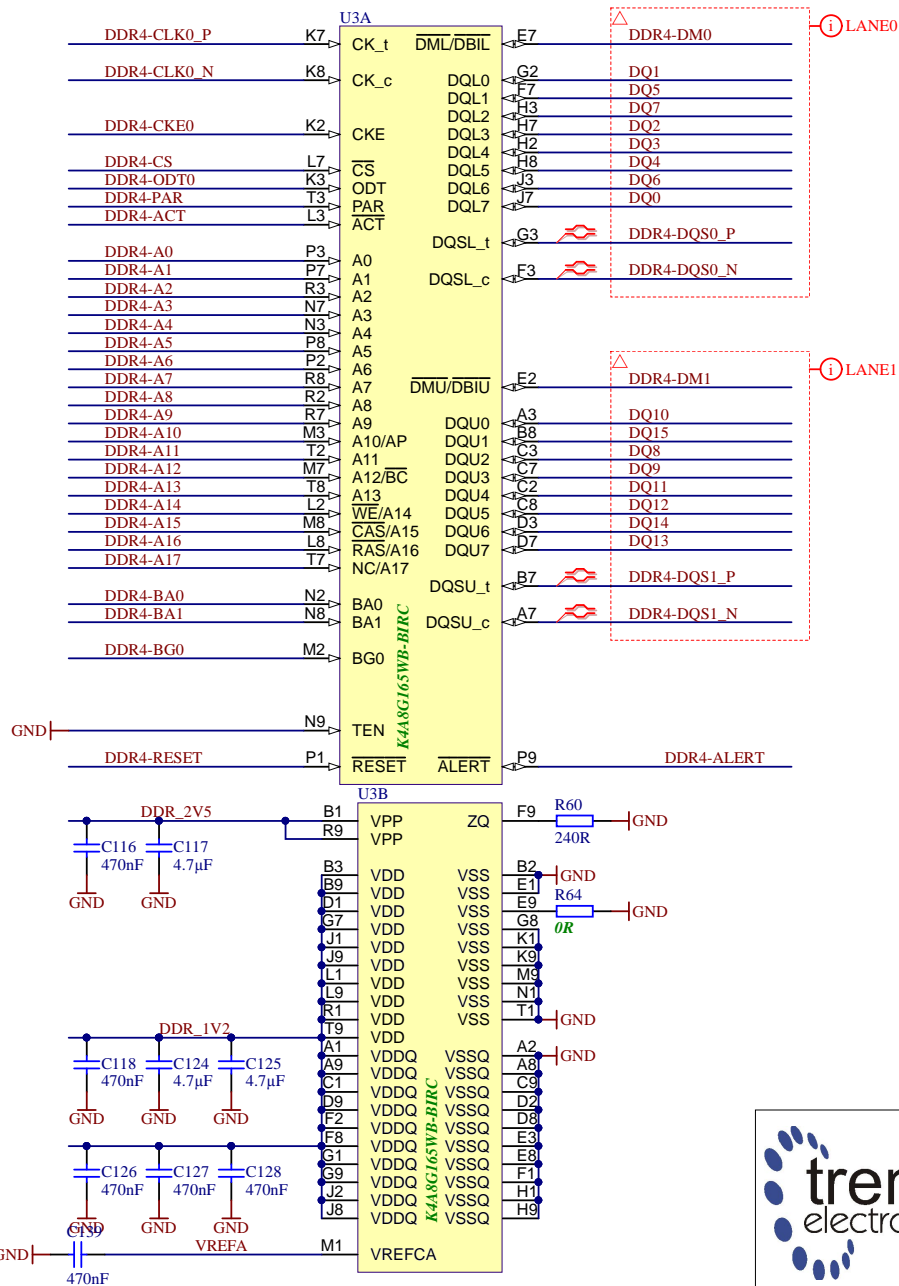
B

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C

D

D



Title: TE0803 - DDR4_2_RAM		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page 18 of 26
Filename: DDR4-RAM_2.SchDoc		

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A

A

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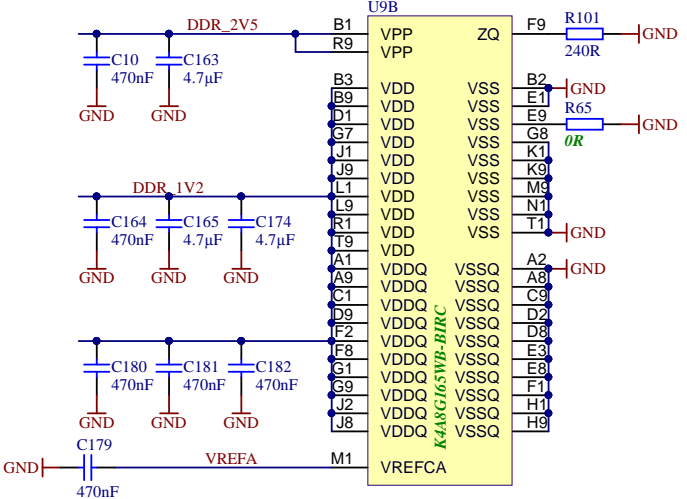
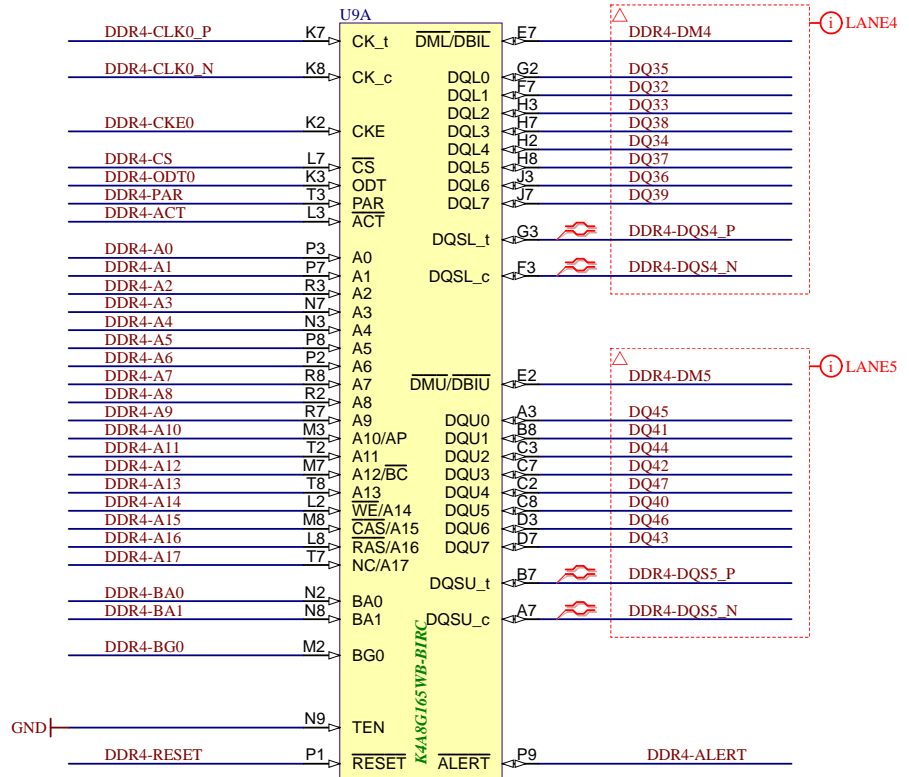
B

C

C

D

D



Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page 19 of 26
Filename: DDR4-RAM_3.SchDoc		

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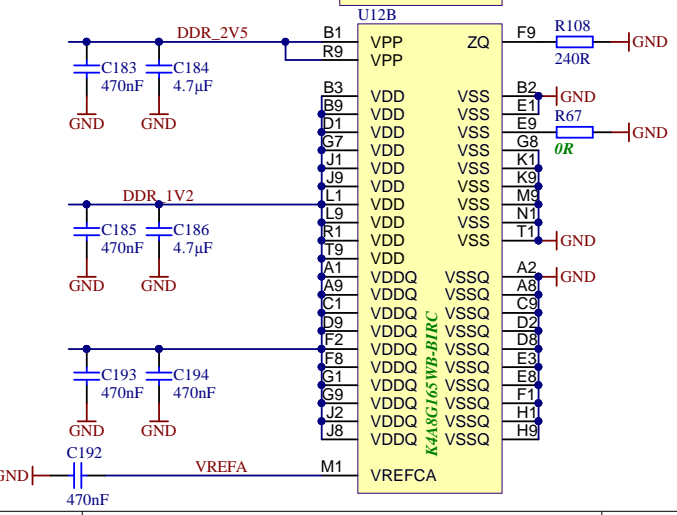
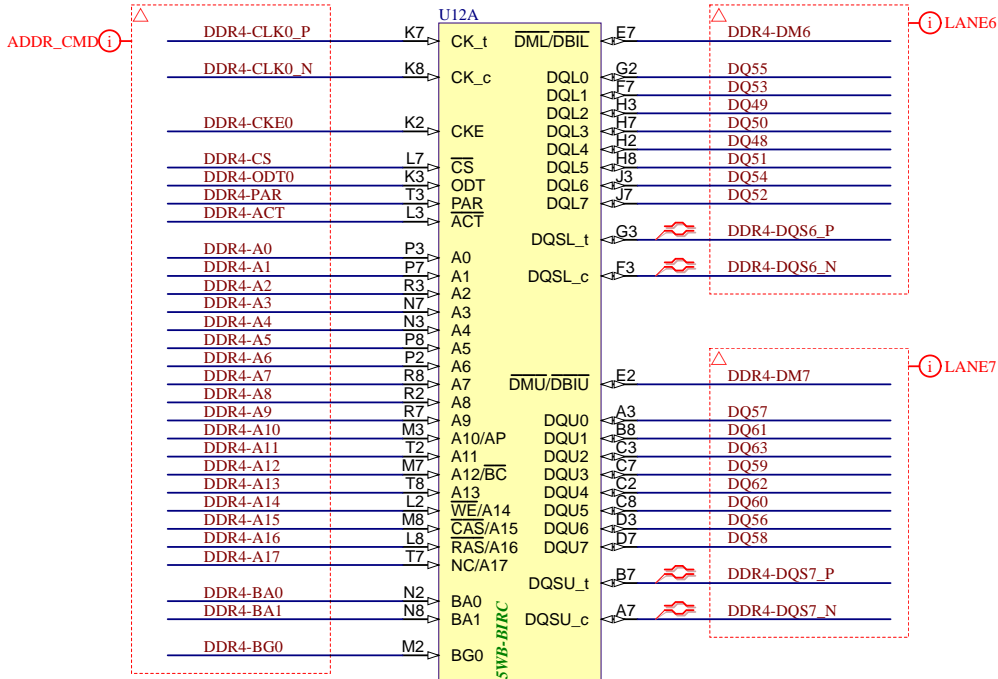
4

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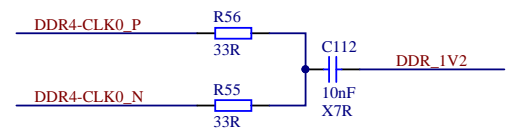
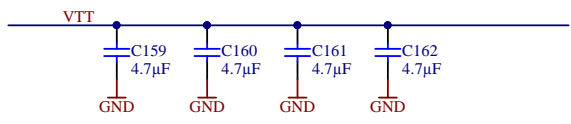
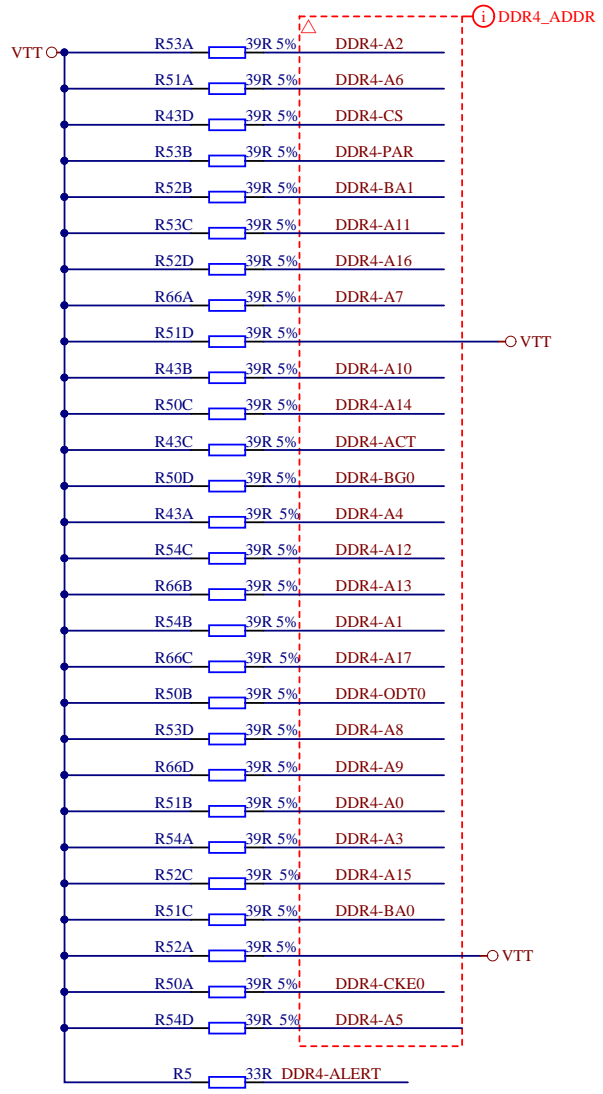
Title: TE0803 - DDR4_4_RAM		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page20 of 26
Filename: DDR4-RAM_4.SchDoc		

1

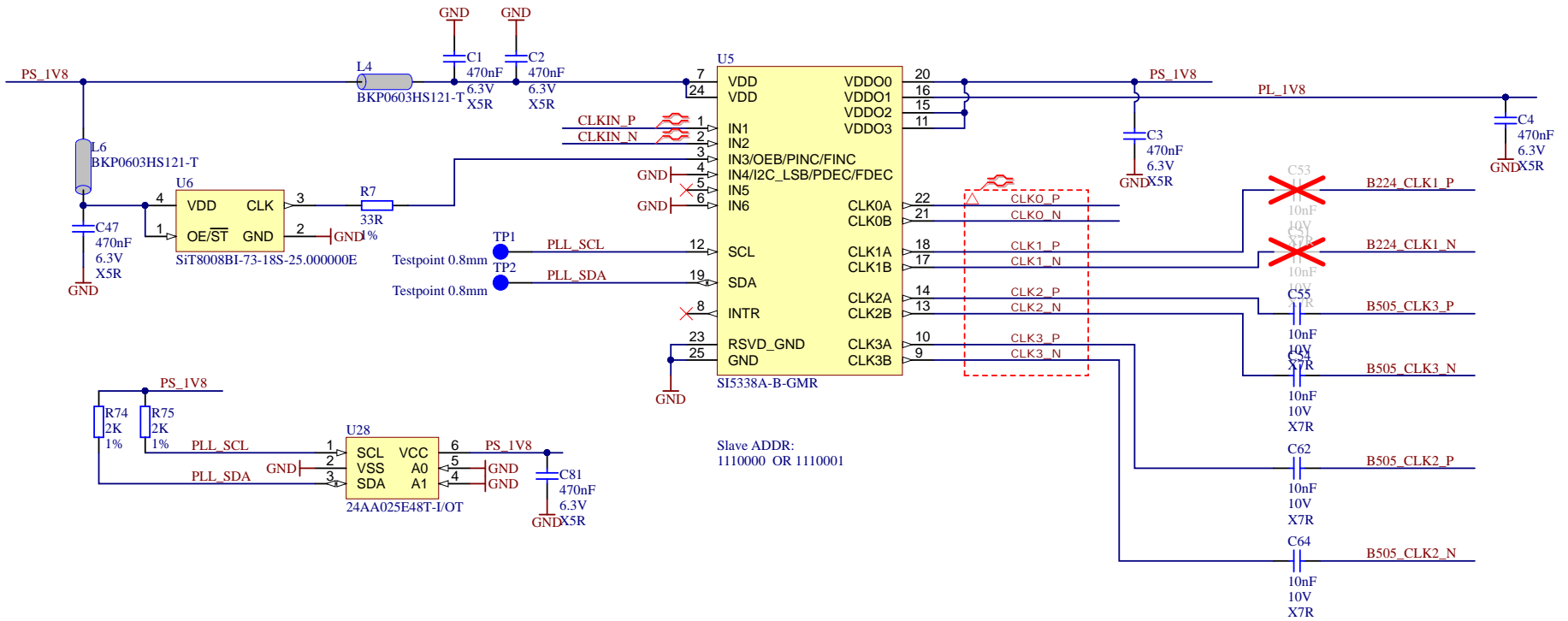
2


3

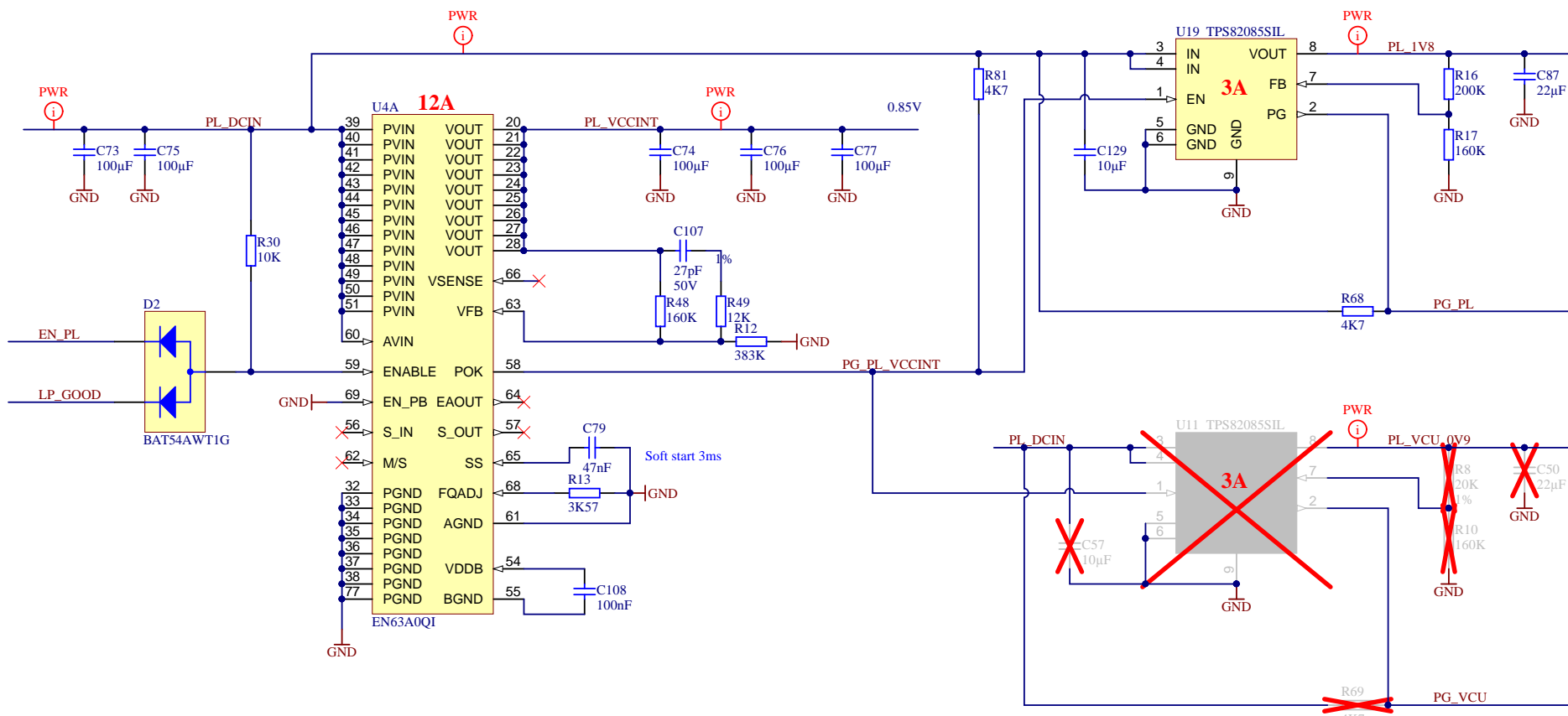
4



Title: TE0803 - DDR4_TERM		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page21 of 26
Filename: DDR4-TERM.SchDoc		



	Title: TE0803 - CLOCK		
	A4	Number: TE0803 03EG-1EB	Rev. 02
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page22 of 26
	Filename: Clock.SchDoc		



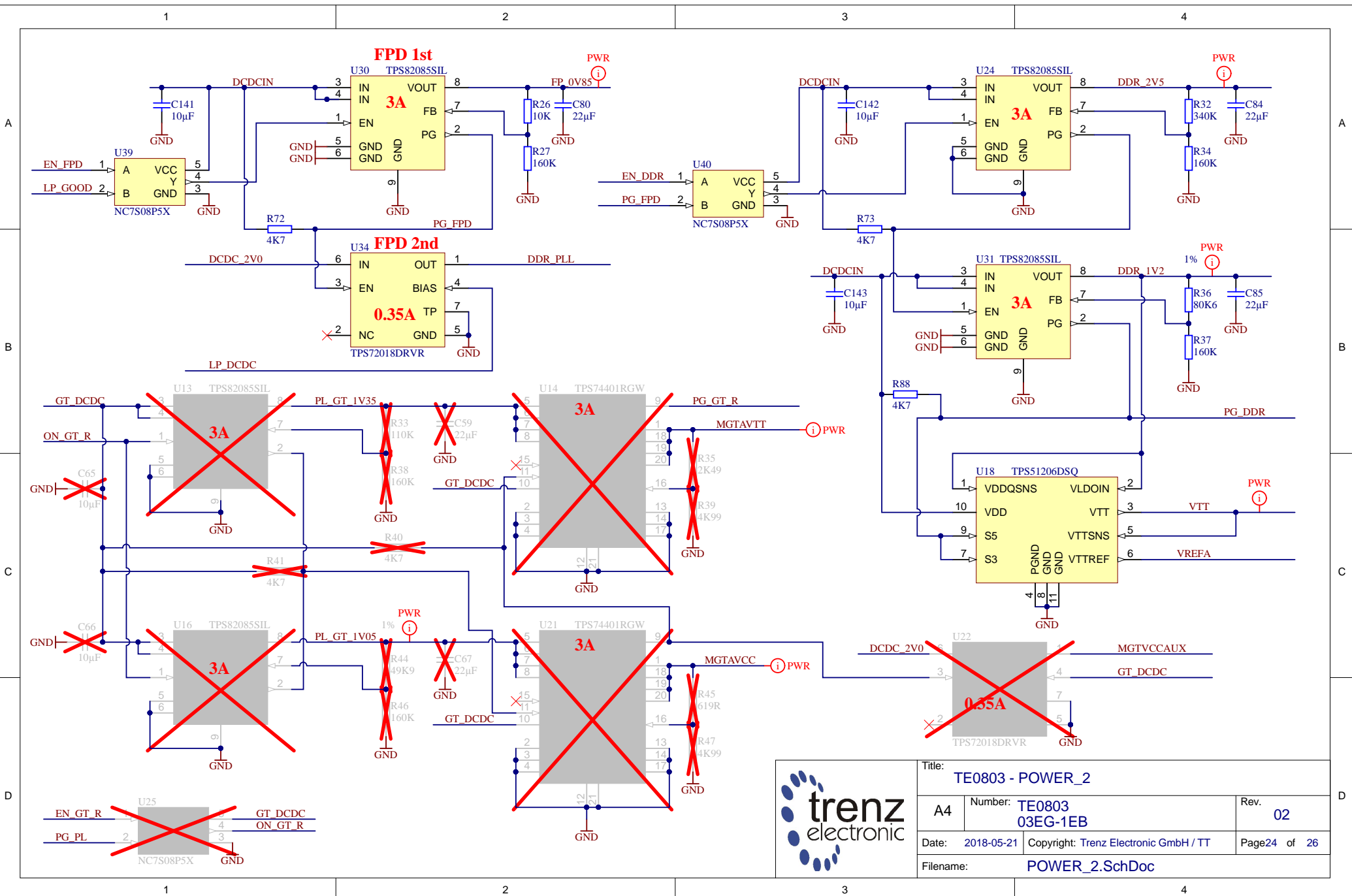
U4B

1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC(SW)	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

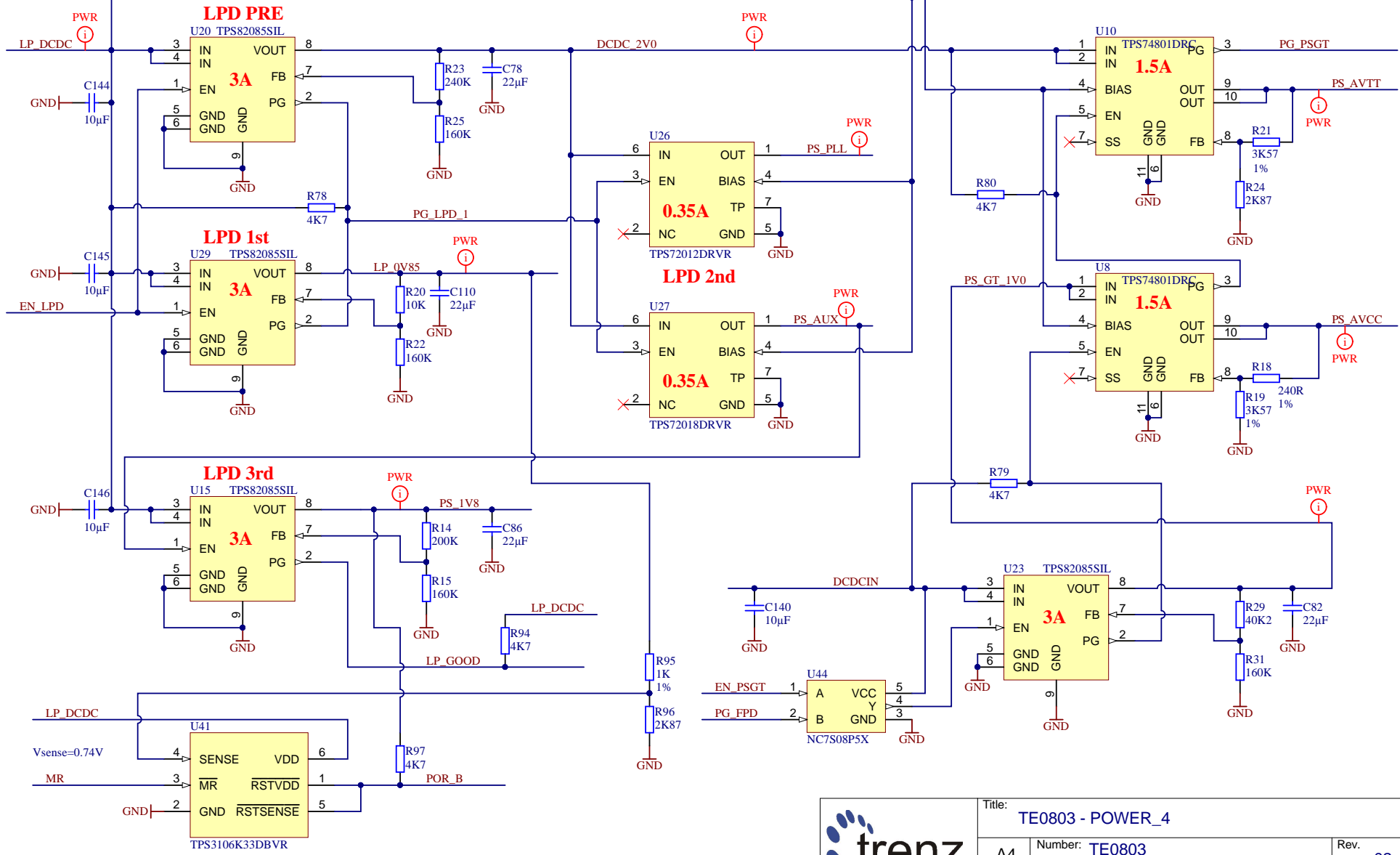
EN63A0QI




Title: TE0803 - POWER		
A4	Number: TE0803 03EG-1EB	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page23 of 26
Filename: POWER.SchDoc		



Title: TE0803 - POWER_2		
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CHANGES REV01a (20.11.2017):

1) VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR_PLL
- 2) All differential pairs wath length matched with tollerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

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