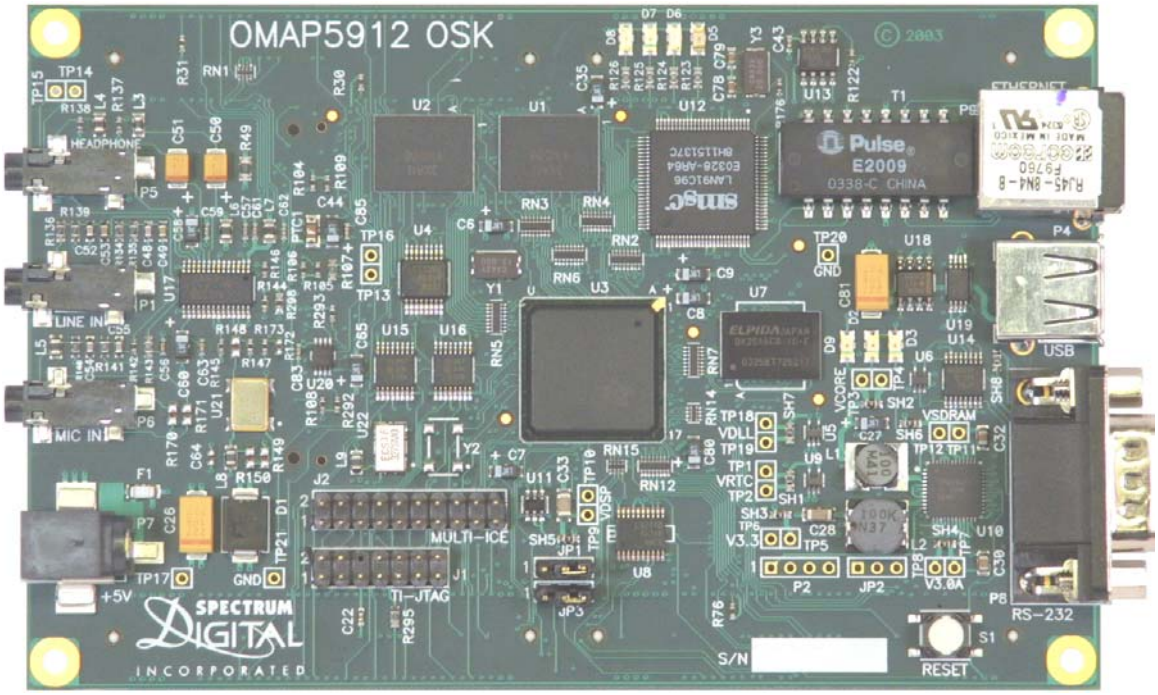


OMAP™ *Starter Kit(OSK)*
OMAP5912™ *Target Module*

Hardware Design Specification

Revision 2.3
July 26, 2004

Table of Contents

Figures

Tables

1.0 Overview

This document covers the design of the OMAP5912 Target Module (TM) to be used in the OMAP5912 Starter Kit (OSK). In covers in detail the design of each aspect of the TM. Sufficient detail is provided to show how each component interacts and what functions they are performing. Additional information will likely be required from the individual component datasheets of the components used.

The sections that make up this Design Specification include:

- Change History
- TM Requirements
- Detailed Design
- Expansion Connectors
- I/O Connectors
- Mechanical Specifications

2.0 Change History

The following table tracks the changes made for each revision of this document.

Table 1. Change History

Rev	Changes	Date	By
1.00	1. Release for revision 1.0 of the TM	12/18/03	GC RB
1.1	1. Fixed typos. Corrected pin numbering on Table 22.	1/13/04	GC
2.0	Changes made to reflect the Alpha2 version of the OMAP5912 OSK. 1. Changed Fig 32 for the Compact Flash to reflect changes made. Fixed buffer. 2. Changed Fig 26 and 27 for the Audio circuit to reflect changes made to the circuit. Corrected wiring error on the Microphone jack 3. Changed Fig 12 to reflect changes in the default core voltage. Added section to describe ability to set default voltage. 4. Changed Fig 33 to reflect new decode configuration. Added text to describe. Also changed Fig 38 and the text as required. 5. Removed CFLASH.DIS signal from Expansion Connector A. Replaced it with nEX_CS3. Changed pin 75 to nEX_CS4. 6. Changed Connector B to reflect changes for the UART1.CTS pin. 7. Added section to describe the ability to use either the CFLASH.IREQ pin or GPIO62 for the CFLASH.IREQ function. 8. Showed changes in the PWR_INT configuration. 9. Updated the USB to reflect new configuration and the dual mode option. 10. Removed references to Innovator and H2. 11. Cleaned up text to match current design	2/17/04	GC
2.1	Updated pictures to reflect the latest layout of the board.	3/8/04	GC
2.2	1. Table 3 was changed a) to show default mode of Flash as dual 16MB devices, 32MB total		

	b) Updated to show memory area can be used by activating the disable pin on the expansion connector. c) Corrected 16MB chip select address map for slot 2. d) Corrected address map on Compact Flash. Shows now as CS2. 2. Corrected Table to show dual 16MB mode as the default. 3. Minor updates on the schematic to reflect wrong values in the CD table on sheet 2. Does not affect the design of the board. 4. Added more detail on USB Client support. 5. Added information on power measurement feature being installed and how to use it, covered in Appendix C.	5/11/04	GC
2.3	1. Added clarification on the use of the external 32khz and the integrated crystal oscillator. 2. Added Appendix B to cover the board dimensions. The other two appendices were incremented. 3. Clarified text. Changed Table 2 title from Requirements to Specification. 4. Added reference to other OSs in section 4. 5. Section 5.4.1 Changed text to read dual 16MB devices is the standard configuration. 6. Section 5.5 Deleted reference to Micron 512Mb Mobile DDR throughout the entire section..	7/26/04	GC

3.0 Definitions, References, and Issues

3.1 Definitions

SDRAM-Synchronous Dynamic Random Access Memory
DDR- Dual Data Rate
SDR- Single Data rate
Flash-Nonvolatile memory
OTC-OMAP Technology Center
JTAG-Joint Test Access Group
USB-Universal Serial Bus
GP-General Purpose ROM
TM-Target Module
EM- Expansion Module

3.2 References

OMAP5910 Data Sheet
OMAP5910 Technical Reference Manual
OMAP GP Device Functional Specification
OMAP5912 Datasheet, SPRS231

4.0 OMAP5912 Target Module

The TM will contain the OMAP5912 processor. In order to keep the cost down, it will have limited functionality. However, it still must provide a certain level of functionality to be useful to the Linux and Microsoft development community and customers. It will also be able to support other OSs as allowed by the OMAP5912 processor. The OSK creates an opportunity to use the DSP and add various external peripherals to the OMAP5912 processor.

4.1 Product Requirements

The requirements for the OMAP5912 OSK Target Module are in **Table 2**.

Table 2. OMAP5912 OSK Target Module Specifications

Processor		
OMAP5912	GDY Package	1.0mm pitch
SDRAM		
32MB	Mobile DDR	1.8V Only
FLASH		
NOR Strata	32MB	Expandable to 64MB
NAND	via Expansion Card	
Power Management		
DC Input	DC Jack	Wall supply, 5V,3W, Regulated
Battery	Optional	Customer added
Status LEDs	Power good	User defined
Low Power Option		
Power on reset		
MPU Reset	Via switch	
Audio CODEC		
Audio CODEC	AIC23	
Line-In	3.5mm Jack	
Headphone Out	3.5mm Jack	
MIC In	3.5mm Jack	
Serial Ports		
RS232	DB9 Male	Tx, Rx
USB Host	250ma power	USB Type B
Ethernet	10Mb	RJ45, status LEDs
Expansion		
Compact Flash	Type I and Type II	Use integrated controller
Expansion Connectors	All signals except SDRAM	Support Expansion Cards
Debugging		
JTAG	14 Pin	
MultiICE	20 Pin	TRST polarity jumper
Form Factor		
Small as practical	Stackable	

5.0 Detailed Design

The following sections provide detailed description of the design of the OMAP5912 TM.

Figure 1 is the high level block diagram of the OMAP5912 TM design.

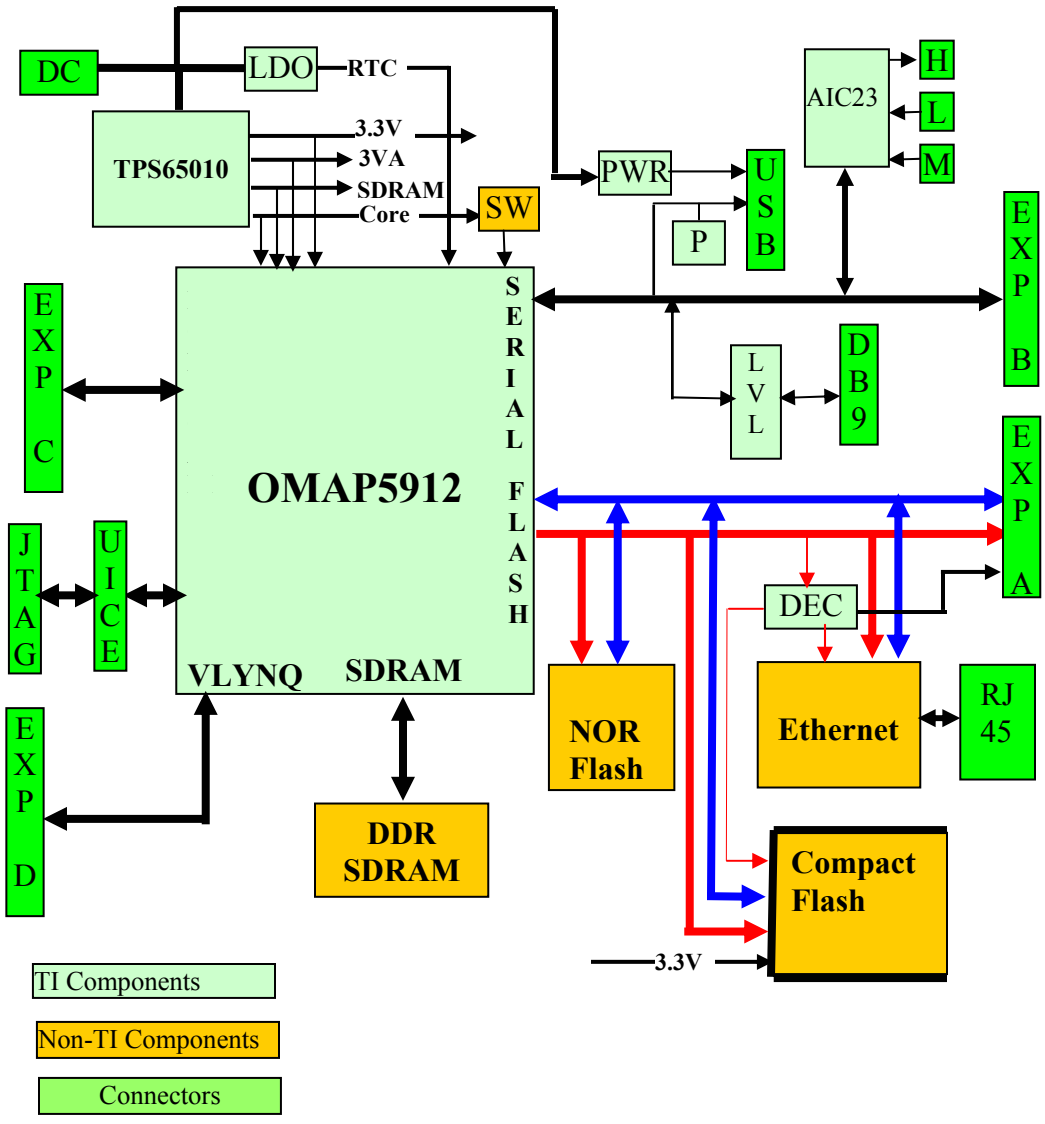


Figure 1. OMAP5912 Target Module Block Diagram

5.1 Memory Map

Covered in this section is the memory map of the 5912 TM.

5.1.1 Flash Memory Bus Memory Map

Table 3 defines the Flash bus or EMIFS (Expansion Memory Interface Slow) memory map. It should be noted that the Compact Flash interface has an option in the design to move the address space to the CS2 region. This is the default location. Refer to the Compact Flash section for more detail.

Table 3. Flash Bus Memory MAP

CS	Type	Start	End	Bytes	
CS1A	Not Used	0400 2000	047F FFFF	8M	Can be used on an expansion board.
"	Ethernet	0480 0000	04FF FFFF	8M	
"	Not Used	0500 0000	057F FFFF	8M	Can be used on an expansion board.
"	Not Used	0580 0000	05FF FFFF	8M	Can be used on an expansion board.
CS1B	Not Used	0600 0000	07FF FFFF	32M	Can be used on an expansion board.
CS2	CF Memory	0800 0000	0800 07FF	2K	When CF space is used, CS2 cannot be used for any other memory.
	CF Attrib	0800 0800	0800 0FFF	2K	When CF space is used, CS2 cannot be used for any other memory.
	CF I/O	0800 1000	0800 17FF	2K	When CF space is used, CS2 cannot be used for any other memory.
4 Possible Configuration					
4MB Mode, Supports 2 4MB Memory Parts, 8MB Total					
CS3	FLASH Slot 1	0C00 0000	0C3F FFFF	4M	Can be used on an expansion board via FLASH.DIS pin..
"	FLASH Slot 2	0C40 0000	0C7F FFFF	4M	Can be used on an expansion board via FLASH.DIS pin..
"	Not Used	0C80 0000	0FFF FFFF	56M	Can be used on an expansion board.
8MB Mode, Supports 2 8MB Memory Parts, 16MB Total					
CS3	FLASH Slot 1	0C00 0000	0C7F FFFF	8M	Can be used on an expansion board via FLASH.DIS pin..
"	FLASH Slot 2	0C80 0000	0CF8F FFFF	8M	Can be used on an expansion board via FLASH.DIS pin.
"	Not Used	0CD0 0000	0FFF FFFF	48M	Can be used on an expansion board.
16MB Mode, Supports 2 16MB Memory Parts, 32MB Total Default Mode					
CS3	FLASH Slot 1	0C000 0000	0CFF FFFF	16M	Can be used on an expansion board via FLASH.DIS pin..
"	FLASH Slot 2	0D00 0000	0DFF FFFF	16M	Can be used on an expansion board via FLASH.DIS pin..
"	Not Used	0E00 0000	0FFF FFFF	32M	Can be used on an expansion board.
32MB Mode, Supports 2 32MB Memory Parts, 64MB Total					
CS3	FLASH Slot 1	0C000 0000	0DFF FFFF	32M	Can be used on an expansion board via FLASH.DIS pin..
"	FLASH Slot 2	0E00 0000	0FFF FFFF	32M	Can be used on an expansion board via FLASH.DIS pin..

The TM supports multiple configurations of NOR FLASH that can be loaded with various devices to create the different configurations. For more information on the different configurations refer to the Flash memory section in Section 5.4.

5.1.2 SDRAM Memory Map

A single DDR SDRAM device is provided on the TM. Table 4 defines the memory map for the DDR SDRAM. The 32MB configuration is the default mode.

Table 4. SDRAM Memory MAP

Mode	Start	End	Bytes	
32MB	1000 0000	11FF FFFF	32M	Default configuration
64MB	1000 0000	13FF FFFF	64M	
Reserved	1800 0000	18FF FFFF		

5.2 OMAP5912 Processor

This section covers the part of the design that is specific to the OMAP5912 processor. Covered in this section will be:

- OMAP Processor
- Clock Interface
- Reset Circuitry
- Power connections
- Configuration pins

5.2.1 OMAP5912 Processor

There are two different packages available for the OMAP5912.

- ZDY Plastic BGA
- ZZG Plastic BGA

Both of these devices are 289 pins. The ZZG package is a much smaller package and has a finer pitch. The TM will use the ZDY package. Figure 2 shows the pin out of the ZZG package.

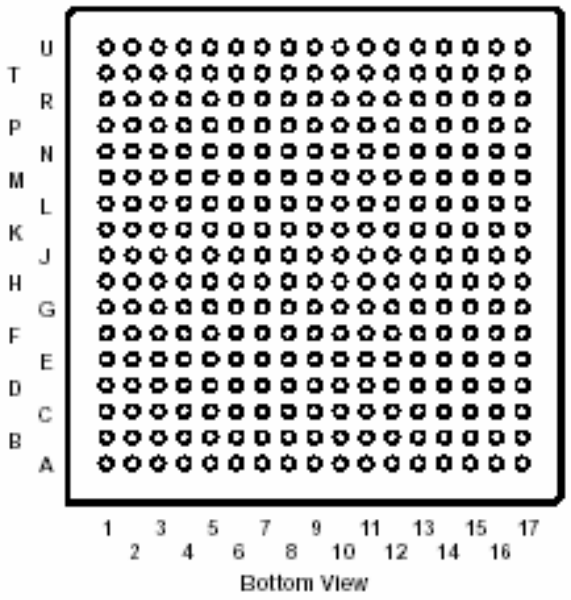


Figure 2. OMAP5912 Clock Inputs

The initial builds of the TM will use the revision 1.0 devices. Production is targeted for the 2.0 release.

5.2.2 Clock Interface

Figure 3 shows the design of the crystals for the OMAP5912TM.

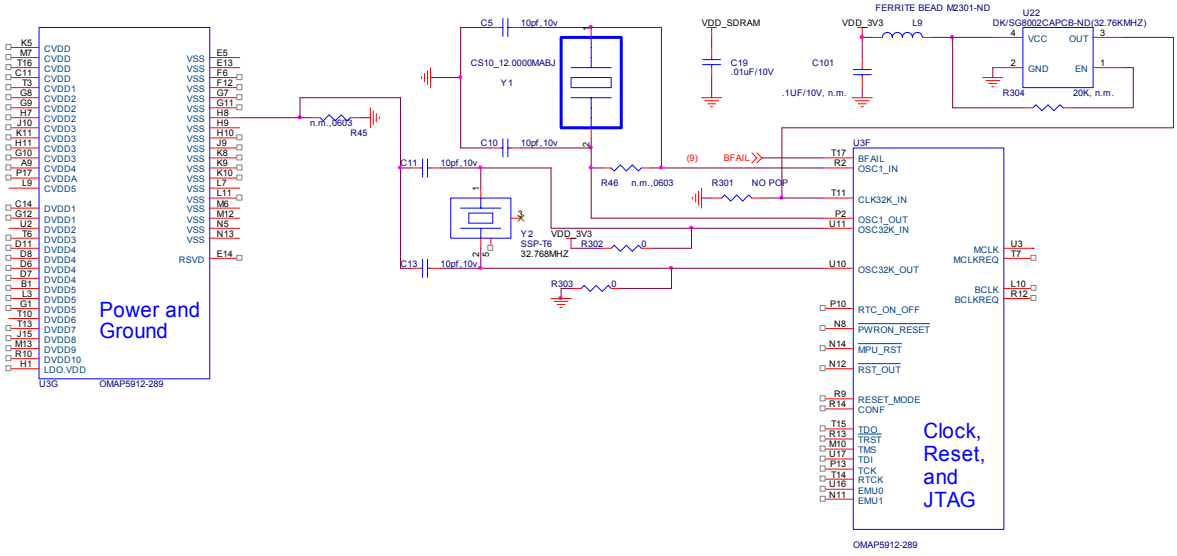


Figure 3. OMAP5912 Clock Inputs

The 32KHZ clock has two options provided on the board, crystal or external oscillator. While both are provided, there are issues with the current revision of the OMAP5912 that requires that the external oscillator be used. When the TMS version is used, both of these solutions are compatible with the TMS version

Both solutions are described in the following sections. In the final release, the crystal option will be used.

5.2.2.1 Crystal Configuration

In the crystal configuration for the 32KHZ clock, an external crystal, Y2, is used for the clock source. The crystal is connected across pins U10 and U11. Because the crystal is used, pin T11 must be grounded. Capacitors C11 and C13 terminate the crystal to ground. These capacitors must be connected directly to pin H8 of the OMAP5912, which is internally connected to ground. The length of this connection should be kept as short as possible. As an option, R45 is provided to provide a direct connection to ground if needed. It is not expected to be needed.

In this configuration, the following components are NOT to be installed:

- C101
- L9
- U22
- R304
- R302
- R303

5.2.2.2 Oscillator Configuration

In this configuration, U22 provides the 32KHZ clock. L9 and C101 provide filtering into the power rail of the oscillator. R304 provides a pull up to the enable pin of the oscillator. R302 and R302 provide the termination of the crystal pins on the OMAP5912 as required when using the external oscillator. In this configuration, the following components are NOT installed:

- C11
- C13
- Y2
- R301

5.2.2.3 12MHZ Clock

Crystal Y1 provides the 12MHZ function for the OMAP5912. Capacitors C5 and C10 provide termination for Y1. It is acceptable to use an external oscillator for the 12MHZ clock. This option is not supported in the TM design.

In addition, you may use a 13MHZ crystal in place off the 12 MHZ crystal. The OMAP5912 TM will not be supplied with this option, but the user could replace the crystal if desired based on their application.

5.2.3 Reset Interface

Figure 4 defines the use of the three pins that make up the reset functions on the OMAP5912.

The **nPWRON_RESET** is an input to the OMAP5912 that, when taken low, resets the entire OMAP5912.

The **MPU_RESET** signal is an input to the OMAP5912 that when taken low, resets the ARM core on the OMAP5912.

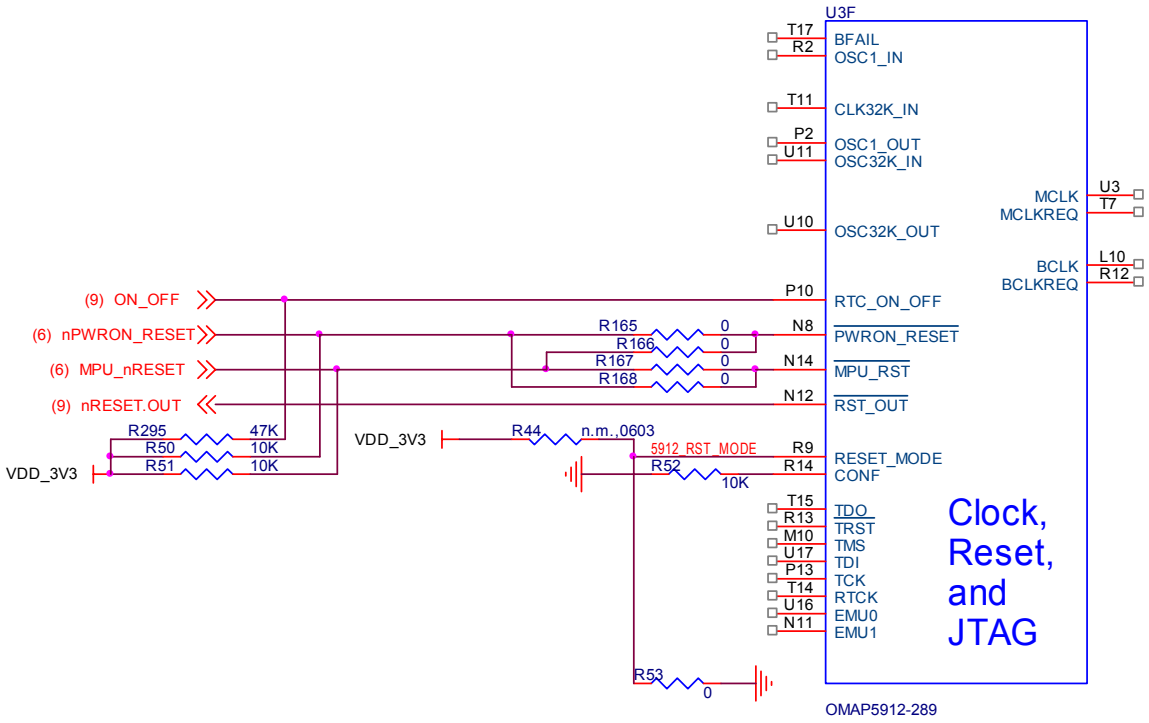


Figure 4. OMAP5912 Reset Interface

There is an issue with the current revision of the OMAP5912 processor. If the MPU_RESET signal is used, it may cause the EMIFS bus to lock. For this reason, it is not desirable to use MPU_Reset signal on the initial units. The current TM design takes care of this issue.

We have four resistors on the board, which based on the way they are loaded, gives us several options to configure the reset signals. The reset signals for the nPWRON_RESET and the nMPU_Reset are generated by the TPS65010 power management device. Both of these signals are open drain outputs. For more information on this refer to section on the TPS65010.

The following sections define how the design is intended to work for both the initial and production builds.

5.2.3.1 Initial Builds

In the current builds of the boards, we need both the nPWRON_RESET and nMPU_RESET to generate an nPWRON_RESET signal into the OMAP5912. The reset switch on the TPS65010 will only generate a nMPU_RST. Because we can only use the nPWRON_RESET signal on the OMAP5912, we need to make sure that both resets from the TPS65010 only generate the nPWRON_RESET signal. This is done by loading the resistors as follows:

- R165, connecting nPWRON_RESET to nPWRON_RESET of the OMAP5912
- R166, connecting nMPU_RST to the nPWRON_RESET of the OMAP5912.
- R167 and R168 are not installed.

This will allow both reset signals from the TPS65010 to only generate an nPWRON_RESET into the OMAP5912.

5.2.3.2 Final Builds

In the TMS version of the OMAP5912 build of the boards, it is expected that we will allow the resets to work such that the nPWRON_RESET and nMPU_RESET generate separate resets. In order to do this, load the resistors as follows:

- R165, connecting nPWRON_RESET to nPWRON_RESET of the OMAP5912
- R167, connecting nMPU_RESET to the nPWRON_RESET of the OMAP5912.
- R166 and R168 are not installed.

The **nRESET_OUT** signal is an output from the OMAP5912. The nRESET_OUT signal is connected to pin 60 of the B expansion connector.

The **RESET_MODE** pin is controlled by the loading of one of two resistors. R53 is the default configuration. It is not envisioned that the other mode, where R44 is loaded instead, will ever be used. There are no plans to support this mode at all. However, it was decided to support both modes just in case we needed it someday.

5.2.4 Power Connections

Figure 5 shows the power connections on the OMAP5912 processor. Each of these is discussed in the following paragraphs.

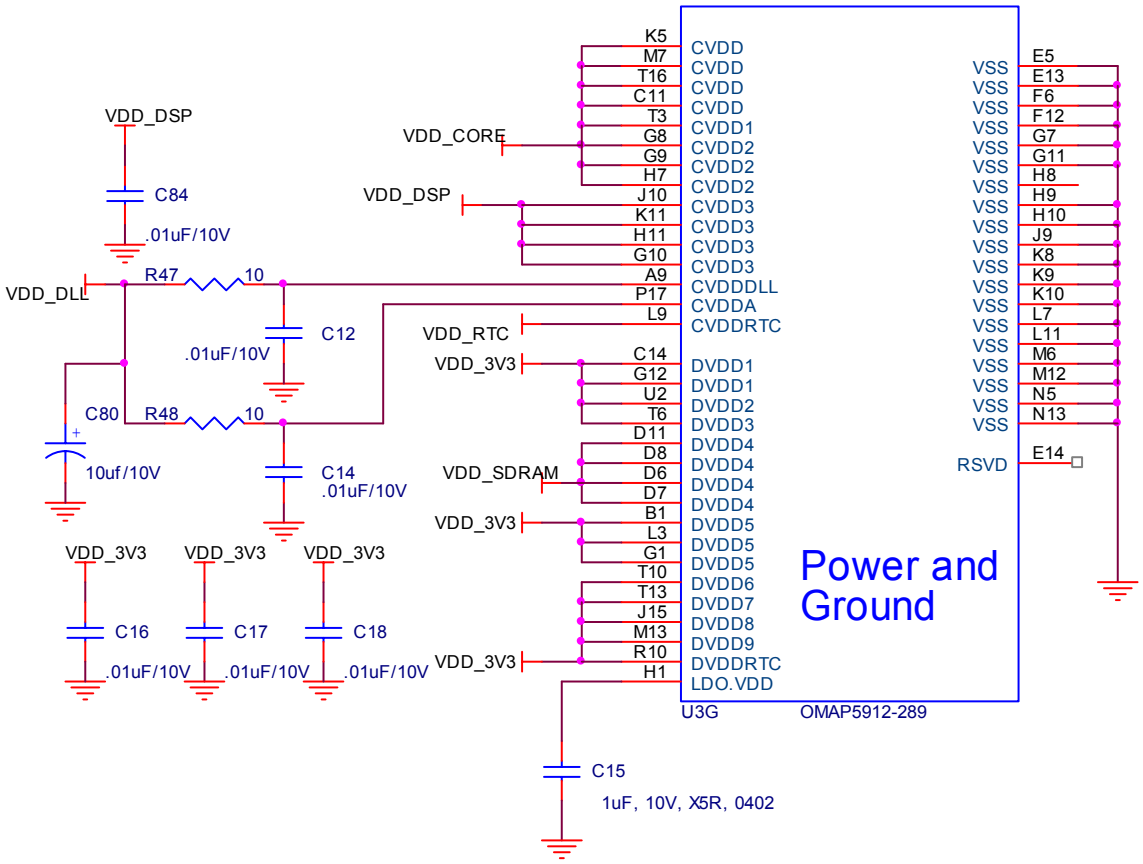


Figure 5. OMAP5912 Power Connections

The **VDD_DLL** power on the OMAP5912 can be sensitive to noise. For this reason a couple of RC circuits are used to provide enhanced noise immunity. R47 and C12 provide a filter for the CVDDLL pin, which is the core voltage supply pin for the DLL. R48 and C14 perform the same function for the CDDDA pin, which provides the power

to the DLL itself. Capacitor C80 provides low frequency filtering for the DLL supply. Power for the DLL is supplied by a separate LDO, U5. Information on this can be found in the Power Management section.

VDD_CORE is the main supply to the internal core voltages of the OMAP5912 and is a nominal 1.6V but can be set to 1.1V-1.5 V under SW control via the TPS65010. Refer to the Power Management section for more details. Filtering of the voltage is supplied by the bypass and filter capacitors.

VDD_DSP is the supply pins for the DSP in the OMAP5912. Power for the DSP is supplied through U11. U11 should be placed as close as possible to the OMAP5912 in the layout process. U11 can be disabled by taking GPIO4 of the TPS65010 low.

VDD_RTC supplies power to the Real Time Clock inside the OMAP5912. Power is supplied by U9. Refer to **SVDD_RTC Section** for a more detailed description.

VDD_3V3 is the 3.3V supply for the OMAP5912. This supplies power to the various I/O function pins as well as the FLASH bus.

VDD_SDRAM supplies voltage to the output pins for the SDRAM interface.

Pin H1 on the OMAP5912 Processor is the output of a regulated supply that is delivered by an embedded LDO to the DPLL macros. The regulated supply is available on the OMAP5912 at pad H1. A decoupling capacitor of 1 µF must be connected externally between LDO.FILTER and ground.

All power is connected to a common ground. All leads from the ground pins on the OMAP5912 to the actual ground plane should be kept as short as practical.

5.2.5 Configuration Pins

There are a group of pins that are used to configure the OMAP5912 processor based on each individual application. **Figure 6** shows these pins.

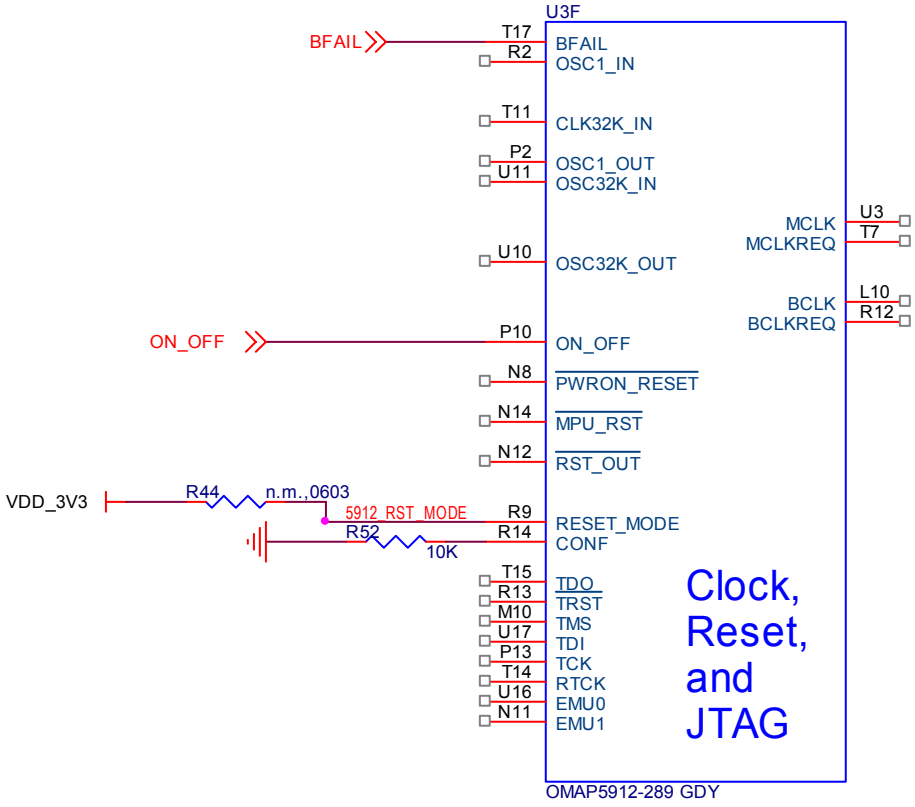


Figure 6. OMAP5912 Configuration Pins

BFAIL is the battery power failure and external FIQ interrupt input. BFAIL can be used to gate certain input pins when battery power is low or failing. The pins that can be gated are configured via software. This pin can also optionally be used as an external FIQ interrupt source to the MPU. The function of this pin is configurable via software.

On the TM, this pin connects to pin 54 of expansion connector B. It is not used by any circuitry on the TM and is free to be used by an expansion card.

On_OFF controls the internal RTC. When pulled low, the RTC is disabled. A resistor insures that the RTC is enabled by pulling the pin to VDD_RTC. This pin also connects to pin 56 of expansion connector B for use by expansion cards as needed either as a way to disable the internal RTC or to be used as one of its optional features. Refer to the OMAP5912 Datasheet for more detail on how the pin can be used.

CONF must be tied low through a 10K ohm resistor to put the OMP5912 in the operational mode. Pulling this pin Hi puts the device in the test mode. The test mode is not used on the TM design.

5.3 Power Management

This section covers the design of the power management circuitry for the OMAP5912 TM. Covered in this section will be:

- Block Diagram
- Power Budgets
- TPS65010
- DC Input
- SDRAM Voltage
- VDD_3V3 Supply
- VDD_3V Supply

5.3.1 Block Diagram

Figure 7 is the high level block diagram of the Power Management Circuitry.

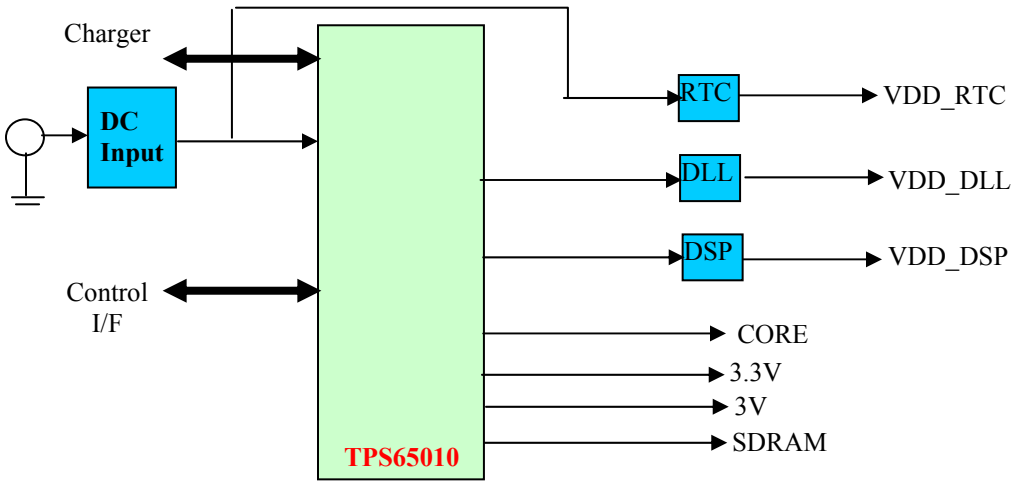


Figure 7. Power Management Block Diagram

The **TPS65010** is the power management device used.

The **DC Input** block is the interface to the external DC power supply.

The **SDRAM** rail provides power to the SDRAM device on the board.

The **3.3V** rail is the main power rail to the 3.3V bus on the board including the FLASH memory devices.

The **3V** rail supplies power to the AIC23 audio CODEC.

The **control interface** contains the setting of the configuration pins and the I2C interface through which the OMAP51912 communicates to the TPS65010.

The **RTC** block provides power to the Real Time Clock voltage input of the OMAP5912.

The **DLL** block provides a separate power rail to the internal DLL power of the OMAP5912.

The **DSP** block provides for the ability to control the power to the DSP block of the OMAP5912.

The **Core** voltage rail supplies power to the core components in the OAMP5912 processor.

Each of these blocks is discussed in more detail in the following sections.

5.3.2 Power Budget

Table 5 defines the estimated power budget for each sections of the TM. The design of the power circuitry has been based on these parameters. These are very rough worst case estimates with a lot of head room allowed. Actual power consumption will depend on clock speed and applications that are being run.

Table 5. TM Power Budgets

Capacity (Ma)------>		2500	400	1000			200	200	
		DC_IN	CORE	3V3	RTC	DLL	3V	SDRAM	Comments
Device	Voltage		1.6V	3.3V	1.8V	1.8V	3.0V	1.8V	
TPS65010(Ma)	VINMAIN	932.3							
TPS65010(Ma)	VINCORE	206							
TPS65010(Ma)	VIN1	23							
TPS65010(Ma)	VIN2	75							
TPS65010(Ma)	AC	500							Only when battery connected
OMAP5912(Ma)			206		5	5			Estimated
OMAP5912(Ma)				85					I/O Voltage
AIC23(Ma)							23		
Flash (2) (Ma)				160					Worst case all Devices
DDR SDRAM(Ma)								75	Estimated

Capacity (Ma)------>		2500	400	1000			200	200	
		DC_IN	CORE	3V3	RTC	DLL	3V	SDRAM	Comments
Device	Voltage		1.6V	3.3V	1.8V	1.8V	3.0V	1.8V	
SN74LVC139(Ma)				2					Conservative est.
SN74CBTLV3257(Ma)				0.3					
LEDS (4) (Ma)				40					
LAN91C96(Ma)				64					
AT93C46(Ma)				2					
MAX3221(Ma)				10					Estimated
SN74AHC1G04DCKR(Ma)				10					
SN74LVC244AGQN(Ma)				24					Estimated
Compact Flash(Ma)				400					Limited to 500mA. Spec @ 400ma
Expansion Slot(Ma)		500		125(1)					
USB Host(Ma)		250							Shuts down @ 440ma. Spec @ 250ma
(Ma)	Totals	2486.3	206	922.3	5	5	23	75	
(Ma)	Remaining	13.7	194	67.7			177	125	

(1)The 3.3V expansion supply is limited to 125ma and is for running a single expansion card. If more power is needed, the DC input should be used.

5.3.3 TPS65010

The TPS65010 is a power management device specifically designed for use with the OMAP Family of processors. Its features are:

- Linear Charger Management for Single Li-Ion Li-Polymer Cells
- Dual Input Ports for Charging From USB or From Wall Plug,
  - Handles 100-mA / 500-mA USB Requirements
- Charge Current Programmable Via External Resistor
- 1 A, 95% Efficient Step-Down Converter for I/O and Peripheral Components (VMAIN)
- 400 mA, 90% Efficient Step-Down Converter for Processor Core (VCORE)
- 2x 200-mA LDOs for I/O and Peripheral Components, LDO Enable via Bus
- Serial Interface Compatible With I2C,
  - Supports 100 kHz, 400-kHz Operation
- LOW_PWR Pin to Lower or Disable Processor Core Supply Voltage in Deep Sleep Mode
- 70-µA Quiescent Current
- 1% Reference Voltage
- Thermal Shutdown Protection
- HBM and CDM Capabilities of 1 kV at VIB, PG, and LED2 pins

The **TPS65010** is an integrated power and battery management IC for applications powered by one Li-Ion or Li-Polymer cell, and which require multiple power rails. Both step-down converters enter a low power mode at light load for maximum efficiency across the widest possible range of load currents.

The **LOW_PWR** pin allows the core converter to lower its output voltage when the application processor goes into deep sleep. The TPS65010 also integrates two 200-mA LDO voltage regulators, which are enabled via the serial interface. Each LDO operates with an input voltage range between 1.8 V and 6.5 V, allowing them to be supplied from one of the step-down converters or directly from the battery.

The TPS65010 also has an integrated and flexible Li-Ion linear charger and system power management. It offers integrated ac-adapter supply management with autonomous power-source selection, power FET and current sensor, high accuracy current and voltage regulation, charge status, and charge termination. The USB mode is for the charger and is not used in this particular design. In the ac-adapter configuration an external resistor sets the maximum value of charge current. The battery is charged in three phases: conditioning, constant current and constant voltage. Charge is normally terminated based on minimum current. An internal charge timer provides a safety backup for charge termination. The TPS65010 automatically restarts the charge if the battery voltage falls below an internal threshold. The charger automatically enters sleep mode when the DC supply is removed.

NOTE: While the battery can be added to the OSK, it is not supported with the OSK. The user will need to add a battery as needed.

The serial interface can be used for dynamic voltage scaling, for collecting information on and controlling the battery charger status, for optionally controlling 2 LED driver outputs, masking interrupts, or for disabling and setting the LDO output voltages. The interface is compatible with the fast/standard mode I2C specification allowing transfers at up to 400 kHz.

5.3.4 DC Input

Figure 8 shows the design of the DC input portion of the board.

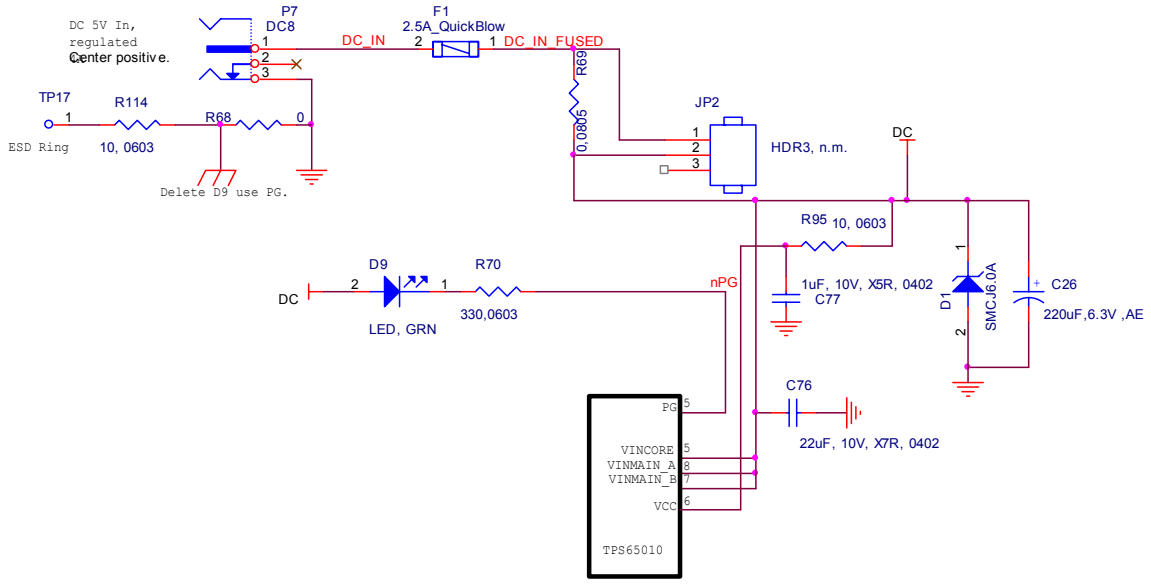


Figure 8. DC Input Design

P7 is the main power jack for the external DC supply. The external supply is specified to be a regulated 5V. A regulated 5V is required for the USB interface. In series with the DC input is a 2.5A quick blow fuse in a 1206 package. This fuse is intended as a protection device in the case that the external +5V supply does not shut down properly. Diode **D1** provides for an additional protection function that insures that the input DC voltage cannot get over 6V. **C26** provides for the filtering of the DC input. **C76** is required by the TPS65010 and should be placed as close to the device as possible.

JP2 is an option jumper that is not normally installed. Its purpose is to allow for the selection of either the DC input mode or the battery mode. In the battery mode the battery is used as the main DC input. This is described further in the Battery section of this document. The standard configuration is the loading of the **R69**, a 1206 sized 0 ohm resistor. You may also replace **R69** with a .01 ohm or larger resistor to allow for the measurement of the total board current consumption by using an oscilloscope to measure the voltage drop across **R69**.

D4 is an LED that is connected to the **PG** (Power Good) output of the TPS65010. This will be the main power LED for the OSK. The open-drain **PG** output indicates when a valid power supply is present for the charger on the ac adapter input. The output turns ON when a valid voltage is detected. A valid voltage is detected whenever the voltage

rises above the voltage on **VBAT** plus 100 mV. This output is turned off in the sleep mode. The PG output can also be programmed via the LED1_ON and LED1_PER registers in the serial interface of the TPS65010. It can then be programmed to be permanently on, off, or to blink with defined on- and period-times. PG is controlled per default via the charger.

Due to the nature of the TPS65010 design, the main DC input can exhibit noise. For this reason, the VCC input of the TPS65010 must be filtered. This is done via an RC circuit comprised of **R95** and **C77**. The supply current of the VCC rail for the TPS65010 is specified at 50uA.

You will also notice a single point ground connection. This is the point in which the Frame ground and signal ground connect at a single point via **R68** which is not actually required but is intended mainly to insure that the ground buses stay separated and that the PCB layout software does not try to interconnect the ground planes anywhere other than at this single point. This point should be as close to the DC input ground pin as possible. In addition there is an ESD ring that goes around the board that also connects to this single point via **R111** which is used to lower the current of the discharged voltage.

5.3.5 SDRAM Voltage

The SDRAM voltage bus has a dedicated voltage supply which minimizes noise on the bus. Figure 9 covers the portion of the design that comprises the SDRAM voltage supply.

The SDRAM and the OMAP5912 voltage pins use LDO1 of the TPS65010. Resistors R82 and R83 are supplied to allow for the voltage to be offset back into the sense input of the TPS65010. This allow for the voltage to be adjusted for voltage drops experienced by the layout. The default configuration is to set the voltage at 1.8V which is done by making R82 a 243K and R83 a 93.1K into the sense input.

LDO1 will deliver up to 200ma. The requirement for the SDRAM is 75ma. The voltage on LDO1 can be adjusted via software, however the default setting is external adjust. The optional settings under SW control will not be used. Refer to the TPS65010 Datasheet for more detail.

Capacitor **C32** provides filtering for the voltage rail. Power for the VLDO1 is supplied by the main DC voltage input rail. Capacitor C31 is required to minimize ripple into the LDO which can be generated by the TPS65010 back onto the main DC rail.

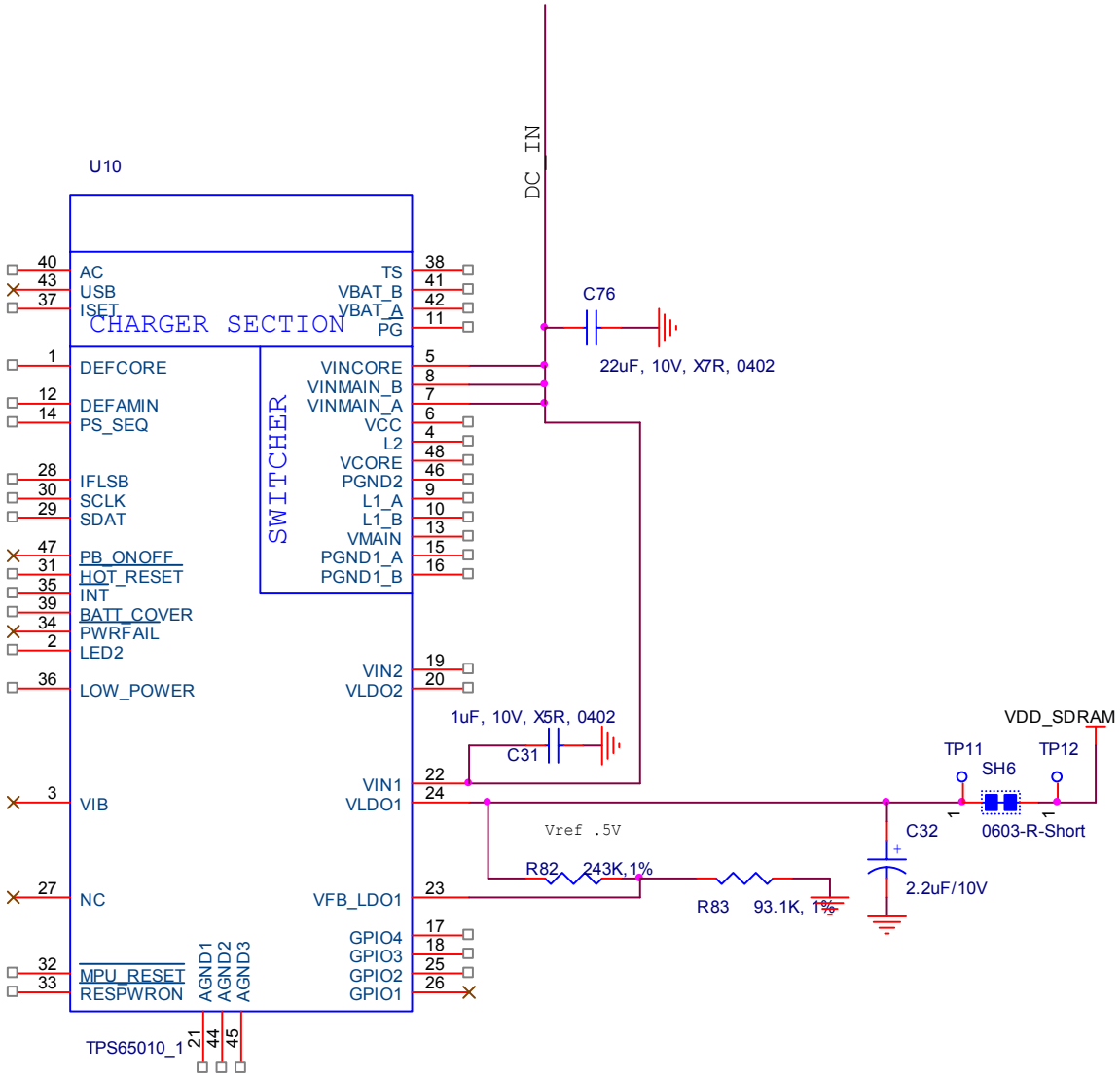


Figure 9. SDRAM Power Design

The current consumption of the VDD_SDRAM voltage rail can be measured across **SH6** using test points **TP11** and **TP12** by using a scope to measure the voltage drop across the .01 ohm resistor in **SH6**. Refer to **Appendix C** for a description of the current measuring procedure.

5.3.6 3.3V Supply

Figure 10 below defines the design of the 3.3V voltage rail on the TM. The 3.3V supply is the main power supply for most of the circuitry on the board including the Flash and Ethernet devices.

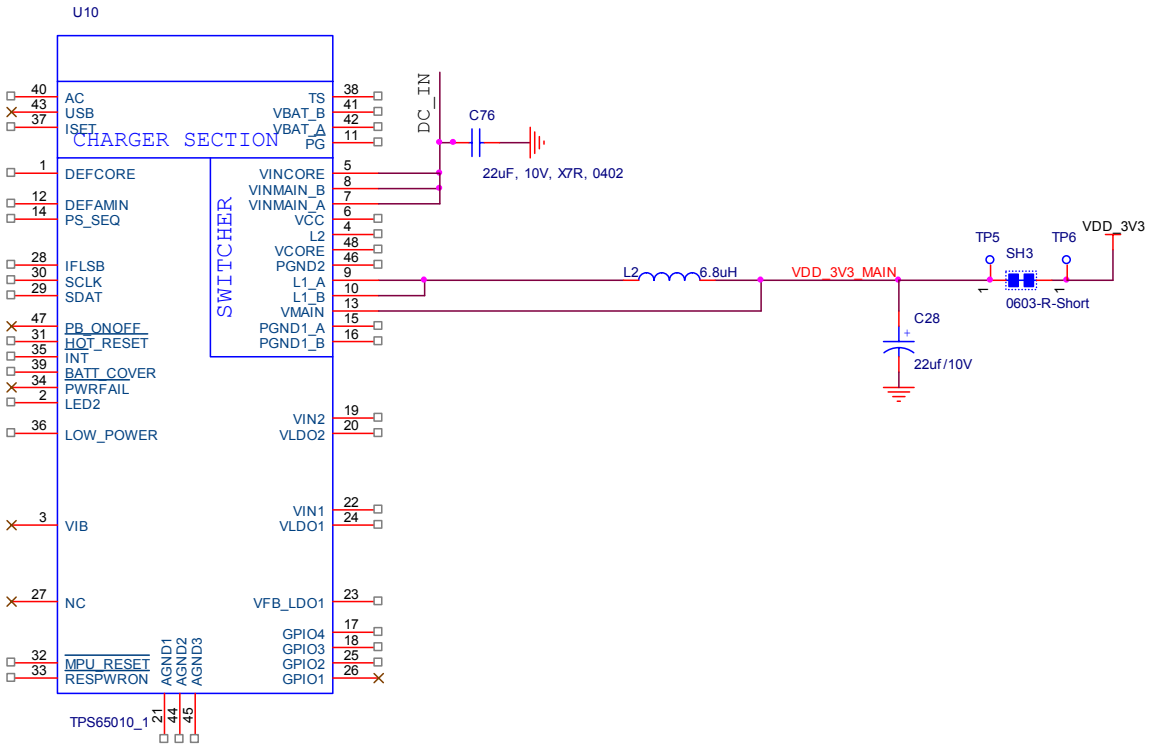


Figure 10. 3.3V Power Design

The 3.3V supply is supplied by the main switcher in the TPS65010 which incorporates a synchronous step-down converters operating typically at 1.25 MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converters automatically enter power save mode and operate with pulse frequency modulation (PFM). The 3.3V converter is capable of delivering 1A output current. The converter output voltages are programmed via the VDCDC1 and VDCDC2 registers in the serial interface. The 3.3V converter defaults to 3.3-V output voltage because the DEFMAIN configuration pin is tied to VCC. The 3.3V output voltage can subsequently be reprogrammed after start-up via the serial interface.

Inductor **L2** is required for the switcher in the TPS65010. Capacitor **C28** provides filtering for the voltage rail. Power for the 3.3V supply is supplied by the main DC voltage input rail. Capacitor C76 is required to minimize ripple into the switcher.

The current consumption of the VDD_3V3 voltage rail can be measured across **SH3** using test points **TP5** and **TP6** by using a scope to measure the voltage drop across the .01 ohm resistor in **SH3**. Refer to **Appendix C** for a description of the current measuring procedure.

5.3.7 3V Supply

Figure 11 shows the design of the 3V power supply which is dedicated for use by the AIC23 CODEC on the board.

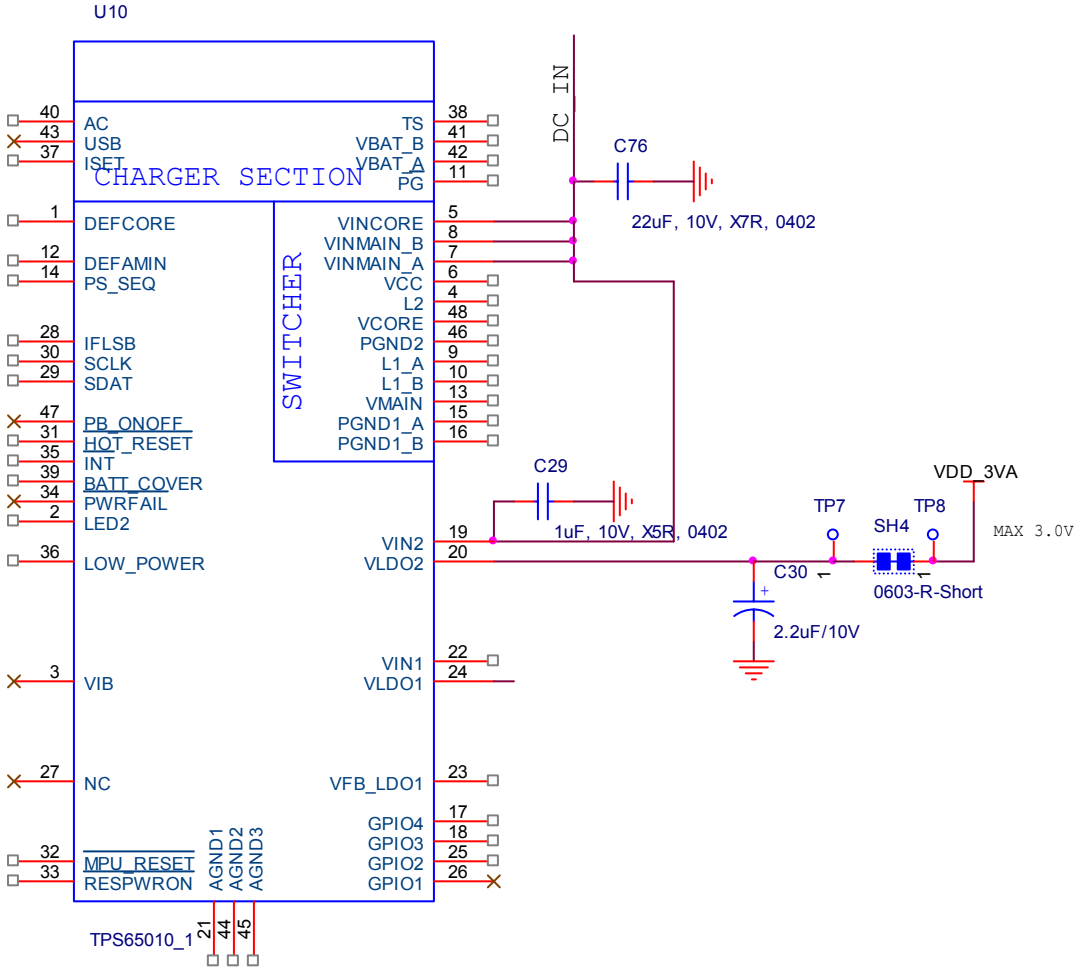


Figure 11. 3V Power Design

The 3V voltage supply use LDO2 of the TPS65010. LDO2 will deliver up to 200ma. The requirement for the AIC23 is 25ma. The voltage on LDO2 can be adjusted via software while there is no external adjustment mechanism on VLDO2. The maximum voltage on VLDO2 is 3.0V. Refer to the TPS65010 Datasheet for more detail.

Capacitor **C30** provides filtering for the voltage rail. Power for the VLDO2 is supplied by the main DC voltage input rail. Capacitor **C29** is required to minimize ripple into the LDO which can be generated by the TPS65010 back onto the main DC rail.
The current consumption of the VDD_3VA voltage rail can be measured across **SH4** using test points **TP7** and **TP8** by using a scope to measure the voltage drop across the .01 ohm resistor in **SH4**. Refer to **Appendix C** for a description of the current measuring procedure.

5.3.8 Control Interface

Figure 12 is the control interface portion of the TSP65010 device.

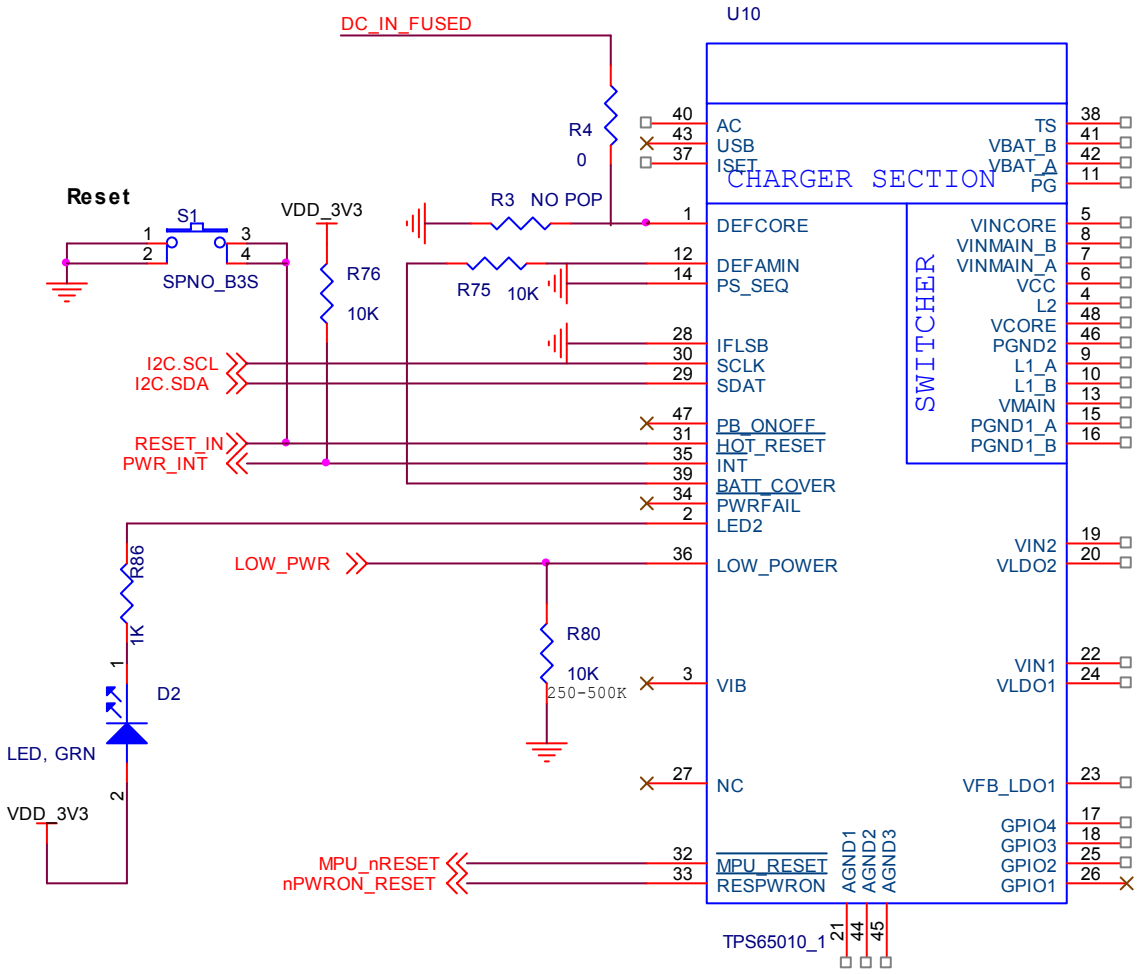


Figure 12. TPS65010 Control Interfaces

5.3.8.1 Default Core voltage

Resistors R3 and R4 set the default core voltage on power up. With R4 populated and R3 not populated, which is the default configuration, the core voltage is 1.6V at power up. With R3 populated and not R4, the default voltage is 1.6V or as determined by the loading of R3 and R4.

5.3.8.2 SW1

SW1 connects to the **HOT_RESET** input and is used to generate an **MPU_RESET** signal for the ARM processor. **HOT_RESET** is de-bounced internally by the TPS65010 and has a typical de-bounce time of 56 ms. The *RESET_IN* signal connects to the

Expansion Connector B pin 59 to allows the ADM or expansion cards to generate a **MPU_RESET** if needed. It can also be used to exit **LOW POWER MODE**, in this case the TPS65010 waits until the VCORE voltage has stabilized before generating the **MPU_RESET** pulse. The **MPU_RESET** pulse is active low for 100 usec. **HOT_RESET** has an internal 1M pullup to VCC.

NOTE: Refer to the Reset Section for an updated description on the use of the nMPU_RST signal.

5.3.8.3 LED D2

The **LED2** output is connected to **D2** and can be programmed to blink or be permanently on or off. The LED2_ON and LED2_PER registers are used to control the blink rate. For **LED2**, the minimum blink on time is 10 ms and this can be increased in 127 10 ms-steps to 1280 ms. The minimum blink period is 100 ms and this can be increased in 127 100-ms steps to 12800 ms. Software applications are free to use this as needed.

5.3.8.4 LOW_POWER Input

The low_power state is entered via the processor setting the ENABLE_LP bit in the serial interface and then raising the **LOW_PWR** pin. The TPS65010 actually uses the rising edge of the internal signal formed by a logical AND of the LOW_PWR and ENABLE LP signals to enter low power mode.

The VMAIN switching converter remains active, but the VCORE converter may be disabled in low power mode via the serial interface by setting the LP_COREOFF bit in the VDCDC2 register. If left enabled, the VCORE voltage is set to the value predefined by the CORELP0/1 bits in the VDCDC2 register. The LDO1OFF/nSLP and LDO2OFF/nSLP bits in the VREGS1 register determine whether the LDOs are turned off or put in a reduced power mode (transient speed-up circuitry disabled in order to minimize quiescent current) in low power mode.

All TPS65010 features remain addressable via the serial interface. TPS65010 can exit this state either due to an under-voltage condition at VCC, due to an OVERTEMP condition, by the processor deasserting the **LOW_POWER** pin or by the user activating the **HOT_RESET** pin or the PB_ONOFF pin.

5.3.8.5 Interrupt Output

The open drain **INT** pin is used to combine and report all possible conditions via a single pin to the OMAP5912. INT can also be activated if any of the regulators are below the regulation threshold. The PWR_INT signal connects to MPUIO1 on the OMAP5912.

5.3.8.6 I2C

The **SDA** and **SCL** pins form the I2C interface that connects to the OMAP5912 Processor to allow applications on the OMAP5912 to control the functions of the TPS65010 device.

The **I2C** serial interface is compatible with the standard and fast mode I2C specifications, allowing transfers at up to 400 kHz. The interface enables most functions to be programmed to new Register contents remain intact as long as VCC remains above 2 V.

The TPS65010 has a 7-bit address with the LSB set by the IFLSB pin which is tied to ground. The 6 MSBs are 100100. Attempting to read data from register addresses not listed in this section results in FFh being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS65010 device generates an acknowledge bit after the reception of each byte.

The OMAP5912 must generate an extra clock pulse that is associated with the acknowledge bit. The TPS65010 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account.

During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS65010 device must leave the data line high to enable the master to generate the stop condition.

5.3.9 RTC Power

The RTC section provides power to the separate Real Time Clock input of the OAMP5912 Processor. **Figure 13** provides the design of the circuit.

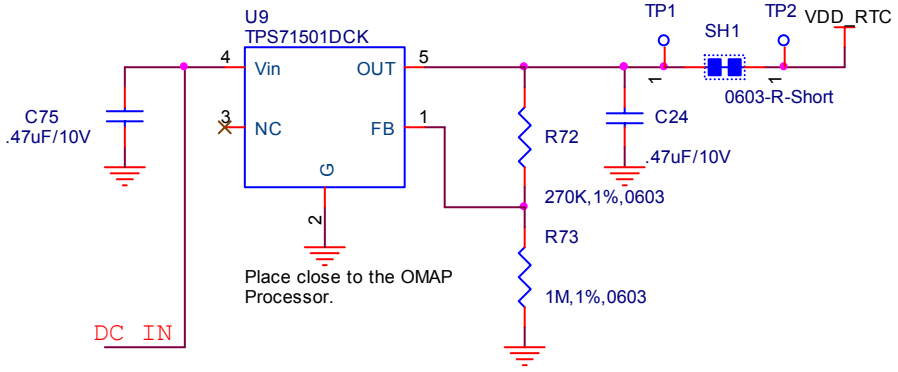


Figure 13. RTC Power Design

The RTC power regulator is separate from the TSP6510 and is fed directly by the main DC supply. This insures that power can be fed continuously from the external supply or the battery, when installed. Even though the TPS6510 can power down, the voltage to the RTC will always be supplied.

U9 is a TPS71501 LDO regulator. The features of this regulator include:

- 50-mA Low-Dropout Regulator
- Available in 2.5 V, 3.0 V, 3.3 V, 5.0 V, and Adjustable
- 24-V Maximum Input Voltage
- Low 3.2-µA Quiescent Current at 50 mA
- 5-Pin SC70/SOT-323 (DCK) Package
- Stable With Any Capacitor (>0.47 µF)
- Over Current Limitation
- –40°C to 125°C Operating Junction Temperature Range

The TM design uses the adjustable version of the regulator which allows the voltage to be set by changing **R72** and **R73**. This insures that no matter how the layout is done, that we can be sure that exactly 1.8V is on the OMAP5912 processor pins.

In the Figure 13 resistors R1 and R2 should be chosen for approximately 1.5-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases VO. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using the information in **Figure 14**:

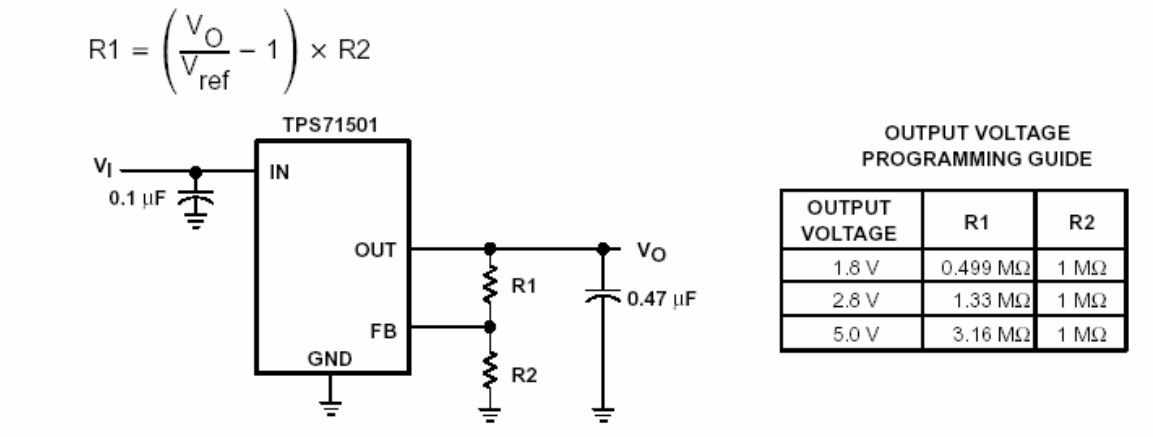


Figure 14. RTC Voltage Adjustment

The current consumption of the VDD_RTC voltage rail can be measured across **SH1** using test points **TP1** and **TP2** by using a scope to measure the voltage drop across the .01 ohm resistor in **SH1**. Refer to **Appendix C** for a description of the current measuring procedure.

There is no separate external battery backup on the RTC. This requires that the battery be installed and the OMAP5912 processor be put into deep sleep mode.

5.3.10 DSP Voltage Control

The OMAP5192 has the ability to have the DSP power removed to conserve power. **Figure 15** shows the control circuitry for this function.

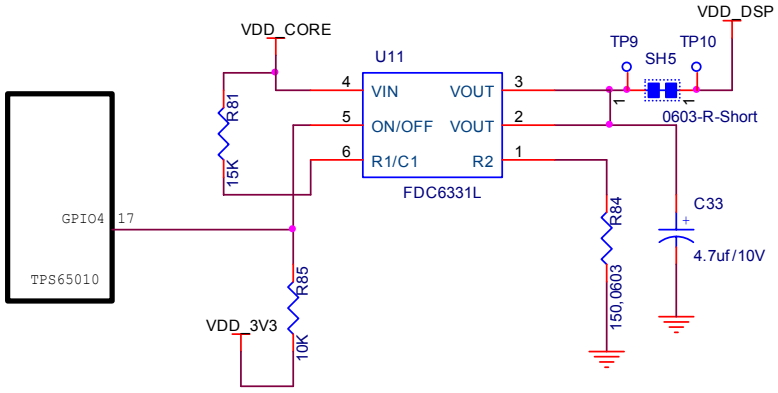


Figure 15. DSP Voltage Control

U11 is a FDC6331L integrated power switch from Fairchild. This device is a FET switch that allows the voltage on the DSP to be completely removed by taking pin 16 of the TPS6501 low. This load switch integrates a small N-Channel power MOSFET that drives a large P-Channel power MOSFET (Q2) in one tiny 6 package. Access to the GPIO pin is via the I2C bus between the TPS6501 and the OMAP5912.

The current consumption of the VDD_DSP voltage rail can be measured across **SH5** using test points **TP9** and **TP10** by using a scope to measure the voltage drop across the .01 ohm resistor in **SH5**. Refer to **Appendix C** for a description of the current measuring procedure.

5.3.11 DLL Voltage

Figure 16 shows the dedicated LDO regulator for DLL power supply.

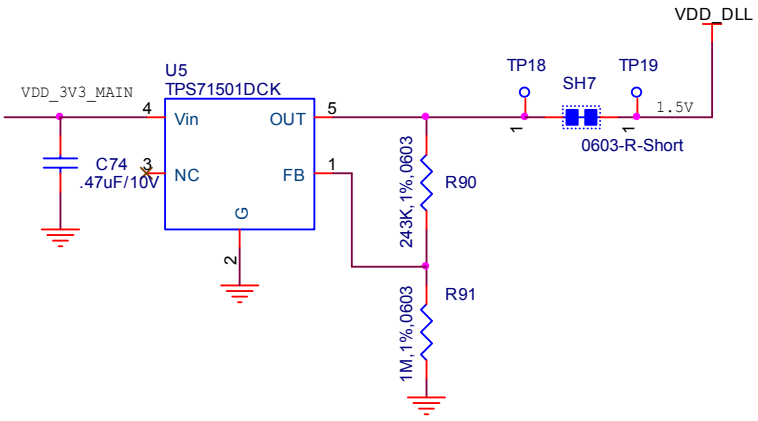


Figure 16. DLL Voltage Circuit

The DLL power regulator is separate from the TSP6510 and is fed directly by the 3.3V supply from the TPS65010.

U5 is a TPS71501 LDO regulator. The features of this regulator include:

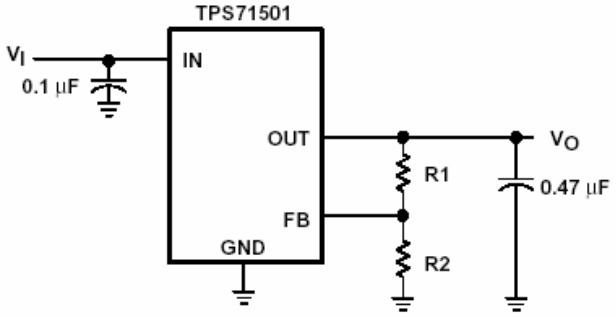
- 50-mA Low-Dropout Regulator
- Available in 2.5 V, 3.0 V, 3.3 V, 5.0 V, and Adjustable
- 24-V Maximum Input Voltage
- Low 3.2-µA Quiescent Current at 50 mA
- 5-Pin SC70/SOT-323 (DCK) Package
- Stable With Any Capacitor (>0.47 µF)
- Over Current Limitation
- –40°C to 125°C Operating Junction Temperature Range

The TM design uses the adjustable version which allows the voltage to be set by changing **R90** and **R9**1. This insures that no matter how the layout is done, that we can be sure that exactly 1.5V is on the DLL power pins.

NOTE: During the layout process, all of the components from **C74** forward, need to be placed as close to the OMAP5912 as possible.

Figure 17 shows that resistors R1 and R2 should be chosen for approximately 1.5-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases VO. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 µA, and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2
1.8 V	0.499 MΩ	1 MΩ
2.8 V	1.33 MΩ	1 MΩ
5.0 V	3.16 MΩ	1 MΩ

Figure 17. DLL Voltage Adjustment

The current consumption of the VDD_DLL voltage rail can be measured across **SH7** using test points **TP18** and **TP19** by using a scope to measure the voltage drop across the .01 ohm resistor in **SH7**. Refer to **Appendix C** for a description of the current measuring procedure.

5.3.12 Core Voltage

The Core voltage output of the TPS6510 provides power for the core circuitry inside the OMAP5912. **Figure 18** shows the external components on the TPS6510.

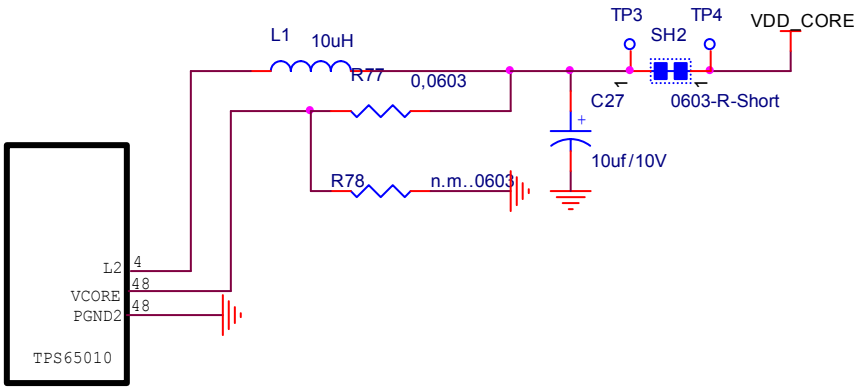


Figure 18. Core Voltage Circuit

The VCORE converter is always enabled in a typical application. The VCORE output voltage can be disabled or reduced from 1.6 V to a lower, preset voltage under processor control. When the processor enters the sleep mode, a high signal on the LOW_PWR pin initiates the change. When the processor is in sleep or low power mode, the VCORE voltage can be programmed to lower voltages without a problem.

In order to insure that the voltage is exactly at the correct value on the OMAP5912 pins, **R77** and **R78** have been added to allow the VCORE to be set as needed. In the default configuration **R78** is not installed and R77 is a zero ohm resistor. If however during the prototype phase a need arises to set this voltage, it can be done by installing **R78** and setting **R77** and **R78** to the required values.

The exact core voltage for the OMAP5912 is set at 1.6V. This may change at later date as testing progresses. This design allows the voltage level to be changed as needed.

The current consumption of the VDD_CORE voltage rail can be measured across **SH2** using test points **TP3** and **TP4** by using a scope to measure the voltage drop across the .01 ohm resistor in **SH2**. Refer to **Appendix C** for a description of the current measuring procedure.

5.3.13 Battery Mode

An optional Li-ION battery can be connected by using header **J4**. The selection of this battery is the responsibility of the user of the TM, and is not supplied with the TM or the OSK. Refer to the TPS65010 datasheet for information on selecting the appropriate battery. In order for the circuit to operate properly, the temperature sense lead must be connected on the battery.

Figure 19 is the section of the design that concerns the battery mode of operation.

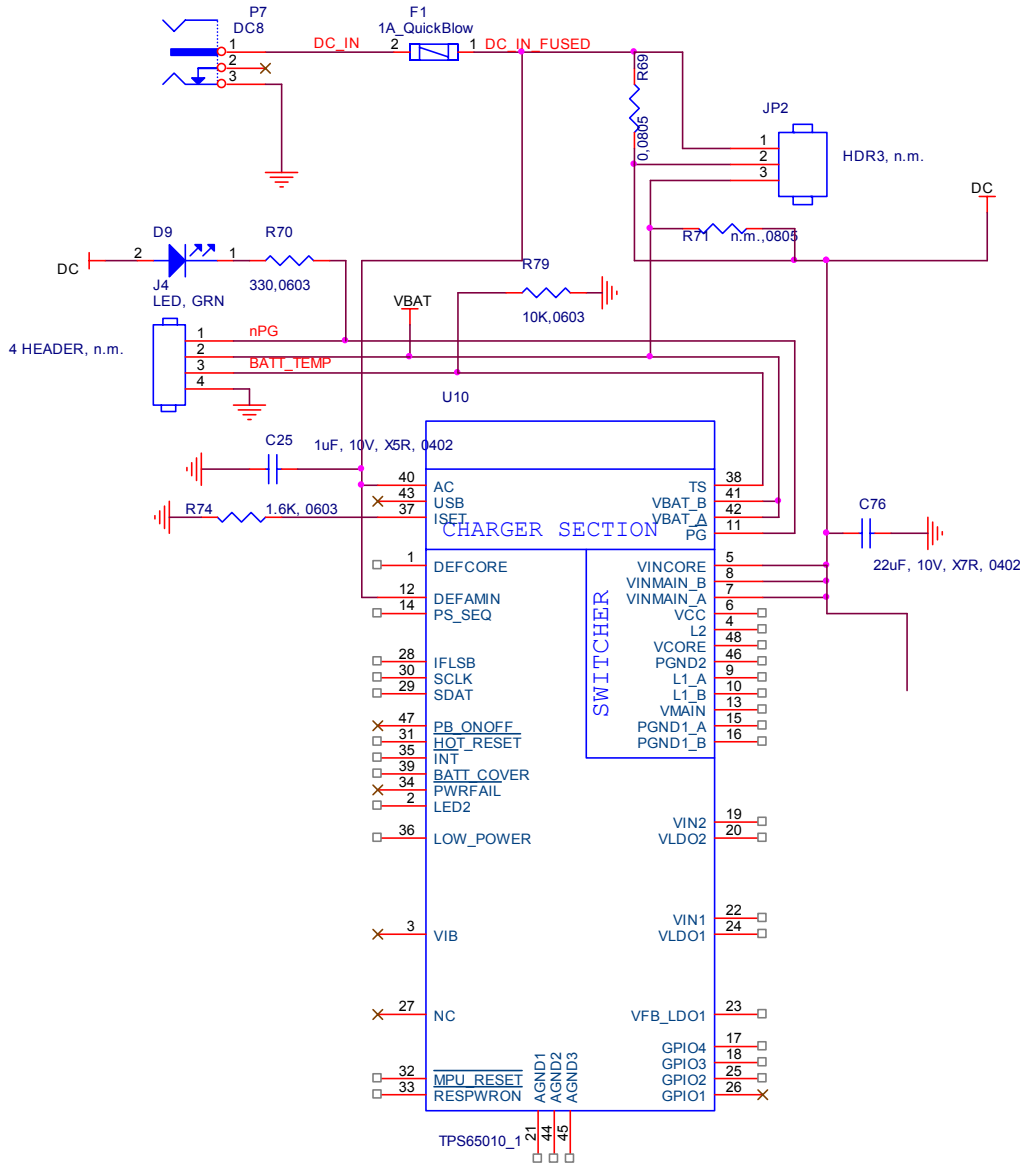


Figure 19. Optional Battery Configuration

In order for the TPS65010 to operate correctly in the Non-Battery mode, resistor **R79** must be installed to insure that the temperature detection circuitry in the TPS65010 is kept happy. When in the battery mode of operation, **R79** MUST is removed.

JP2 can be used to attach the battery to the Circuitry by placing it so that pins 2 and 3 are shorted. For this to work, **R69** and **R7**1 must be removed. Optionally, **R69** can be removed and **R71** installed.

This places the battery as the main voltage source and uses the DC input only as a supply to the charger circuit of the TPS65010. **C25** is a filter for the input of the battery charger circuit in the TPS65010. **R74** sets the default charge current for the battery.

5.4 Flash Memory

The TM supports two NOR FLASH devices and can be configured in several ways to obtain a range of Flash densities as needed. It also provides for a mechanism whereby the FLASH can be disabled by an expansion board and that expansion board is then the provider of the FLASH devices.

The following sections provide a description of the FLASH circuitry on the OMAP5912 TM.

5.4.1 Supported Configurations

Table 6 defines the supported FLASH memory configuration on the TM. The standard configuration is the dual 16MB devices for a total of 32MB.

Table 6. FLASH Configurations

Size	Slot 1	Slot 2
4Mb	4Mb	-
8Mb	4Mb	4MB
8Mb	8Mb	-
16Mb	8Mb	8Mb
16Mb	16Mb	-
32Mb	16Mb	16Mb
32Mb	32Mb	
64Mb	32Mb	32Mb

5.4.2 Supported FLASH Devices

The Flash design will support the devices specified in Table 7.

Table 7. Supported FLASH Devices

Manufacturer	Part Number	Size
Micron	MT28F320J3	32Mb
Intel	RC28F320J3A110	32Mb
Micron	MT28F640J3	64Mb
Intel	RC28F640J3A120	64Mb
Micron	MT28F128J3FS-12	128Mb
Intel	RC28F128J3C150	128Mb
Micron	MT28F128K3	128Mb
Intel	RC28F128K3C115	128Mb
Micron	MT28F256K3	256Mb
Intel	RC28F256K3C120	256Mb

Only the NOR flash devices are supported on the TM. Two Micron MT28F128J3 devices is the base configuration. The Micron QFlash^{TM} devices are SW compatible with the Intel Strata Flash devices. It is offered in a version with a Micron ID or an Intel ID.

5.4.3 FLASH Circuit Design

Figure 20 is the interconnection between the OMAP5912 and the FLASH devices. Only one FLASH device is shown. The differences in connections required for the second FLASH device is contained in the text.

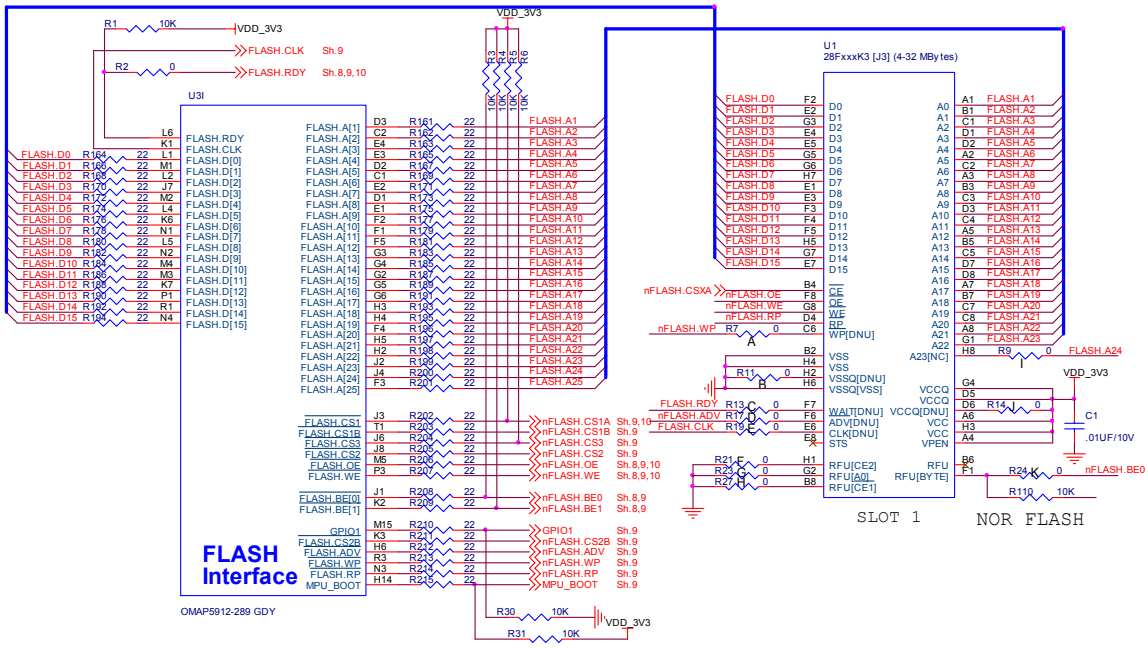


Figure 20. FLASH Circuitry Design

5.4.4 Address Bus

The OMAP5912 has 24 address lines, A1-A25. Only address lines 1-24 are used for the largest device. Even though all of the address lines are connected to the devices, not all of the pins may be used depending on which device is installed.

5.4.5 Data Bus

The data bus from the OMAP5912 is 16 bits wide. All of the data bits are connected to each of the Flash devices.

5.4.6 Control Signals

All signals are the same for both slots except the CS signal. Slot 0 uses the **CSXA** while Slot 1 uses **CSXB**. Depending on the type of memory used, some of the signals may not be connected. This is handled by the populating or unpopulating of certain resistors.

The signal **GPIO1** is used to set the configuration of the Flash bus. To be compatible with the TM design, this pin must be tied to ground. The **MPU_BOOT** signal should be tied Hi for the TM application.

5.4.7 Address Decode Logic

Figure 21 is the design of the decode logic for the FLASH devices.

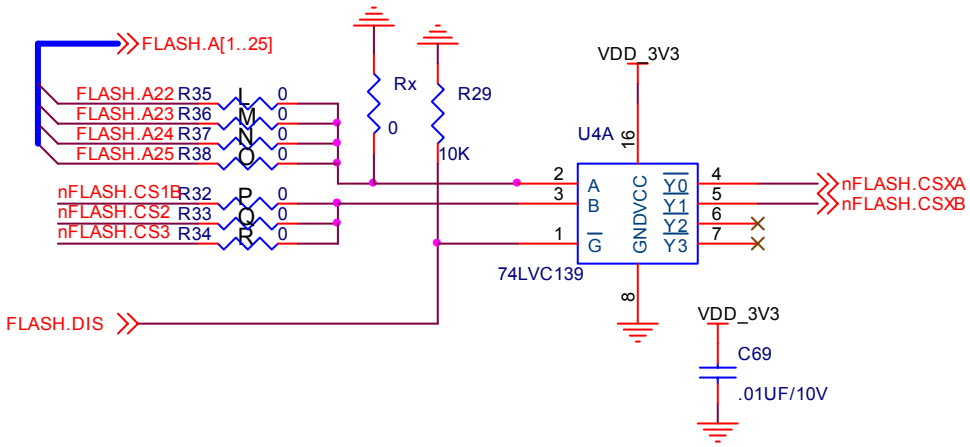


Figure 21. FLASH Decode Logic

Table 8 below defines how the resistors are to be loaded for each of the supported memory size configurations. In order to support contiguous memory between the two memory device slots, the address decoding for the second block must be moved. This is done by placing the A bit of the '139 decoder to the appropriate address line at the beginning of the Slot 2 address range. Highlighted is the default value of the TM design.

Table 8. Flash Address Decode Resistor Options

Devices	Size	L	M	N	O	Address line used
1	4MB	x				A22
2	8MB	x				A22
1	8MB		x			A23
2	16MB		x			A23
1	16MB			x		A24
2	32MB			x		A24
1	32MB				x	A25
2	64MB				x	A25
1	64MB					None

In the event a single 64MB device is used, Rx in **Figure 21** must be installed to insure that the full 64MB range is valid for the CS.

The base address range can also be moved between chip selects. Table 9 defines how this can be done. The moving of the chip select is not impacted by whether or not there is one or two memory devices used.

Table 9. Flash Chip Select Resistor Options

Chip Select	Size	P	Q	R
CS1B	32MB	x		
CS2	64MB		x	
CS3	64MB			x

Note that if CS1B is to be used, it is limited to 32MB of address space. Insure that the desired memory configuration will work with CS1B. CS3 is the default configuration.

5.4.8 GP Mode Support

The GP (General Purpose) device is a production device that offers other capabilities in the boot code which enable the user to boot and flash without authentication and run-time security environment. Boot code for GP device consists in an enhancement of the boot code that is used for a High Security device. GP device boot code implementation is based on ES1.2 boot code (boot code release 6.8) of OMAP5912 High Security device. GP device is different from a High Security device because Production ID bits [30:31] are not the same for a GP device.
The initial builds of the TM may not support the full GP device functionality, but hardware support is required.

GP device allows two new different ways of booting/flashing in the boot code:

- GP Full Boot:

  The device boots without authentication. This is neither for booting, nor for flashing. Run-time security is disabled (secure mode entry is disabled).

- GP Fast Boot:

  The device boots skipping the main boot code process that consists in booting (memories detection) and flashing (interfaces polling), and jumps directly to CS3. Run-time security is disabled (secure mode entry is disabled). Interrupts are disabled and ARM is in Supervisor mode.

In order to select between these modes, GPIO_13 is tested. If GPIO_13 is LO, then GP Fast Boot is selected. If it is HI, then GP full boot is selected. In order to allow the user to select the desired mode, a jumper is provided to allow the setting of GPIO_13 either HI or LO. In the current design, this jumper is designated as JP3.

5.5 DDR SDRAM

This section covers the design of the SDRAM section of the TM. While the OMAP5912 does support SDR (Single Data Rate) SDRAM, this design will use the DDR (Dual Data Rate) SDRAM devices. Only a single DDR SDRAM device will be used and chosen from one of four devices:

- Samsung 128Mb Mobile DDR
- Samsung 256Mb Mobile DDR
- Elpida 246 Mb Mobile DDR EDK2516CBBH

Most likely, the Elpida device will be used.

Only Mobile DDR devices are supported by the OMAP5912. Mobile provides for low current operation and supports only 1.8V voltage rails and interfaces. The OMAP5912 will support up to 256Mb of DDR SDRAM. Due to the limitation of the single device, the maximum memory is limited by the single devices that are on the market.

5.5.1 DDR SDRAM Circuit Design

Figure 22 is the design of the DDR SDRAM interface on the OMAP5912 TM.

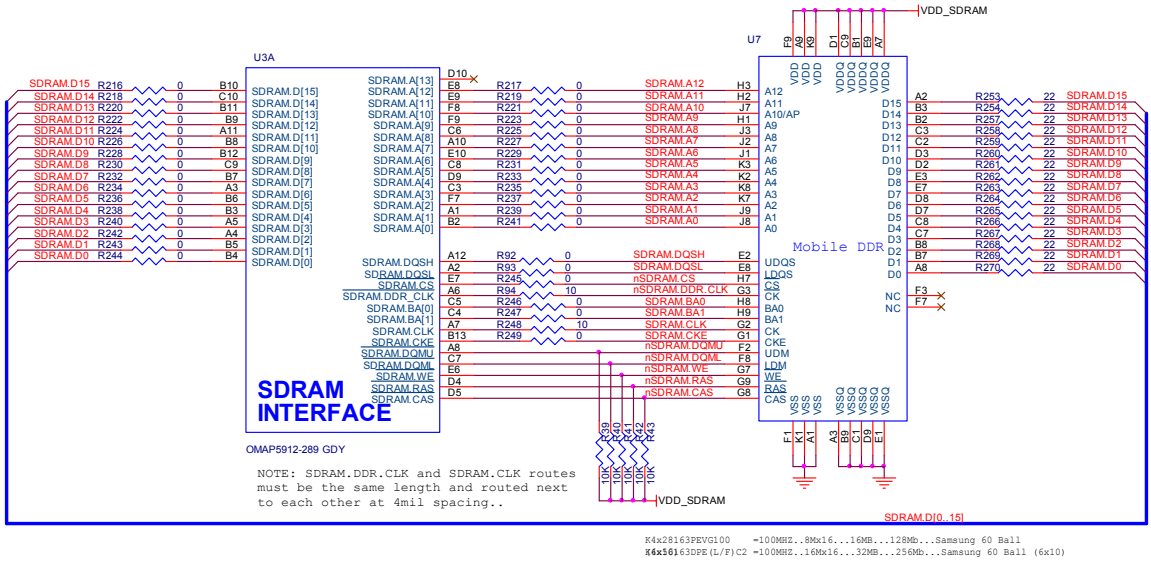


Figure 22. Mobile DDR SDRAM Design

5.5.2 Micron DDR Device

Micron is due to come out with a new mobile DDR device in the Q2 of 2004. The design has been set up to use this device. It is pin compatible with the Samsung device, but is slightly larger in overall size. The PCB design must take into account the larger size of the Micron device.

The initial Micron device will be the 512Mb device followed by a 256 Mb device. Once the devices are available, it will be qualified before being used on the TM design.

5.5.3 Samsung DDR Device

The features of the Samsung memory include:

- 1.8V power supply, 1.8V I/O power
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Four banks operation
- Differential clock inputs(CK and CK)
- MRS cycle with address key programs
  - CAS Latency (3)
  - Burst Length (2, 4, 8)
  - Burst Type (Sequential & Interleave)
  - Partial Self Refresh Type (1, 2, 4 Banks)
  - Temperature Compensated Self Refresh
- All inputs except data & DM are sampled at the positive going edge of the system clock(CK).

- Data I/O transactions on both edges of data strobe, DM for masking.
- Edge aligned data output, center aligned data input.
- No DLL; CK to DQS is not synchronized.
- LDM/UDM for write masking only.
- 7.8us auto refresh duty cycle.
- 100MHZ operating Frequency (DDR200 device)

The definition of the pins on the Samsung device is provided in Table 10.

Table 10. Samsung DDR Pin Definitions

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	Input	Clock : CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Internal clock signals are derived from CK/$\overline{CK}$.
CKE	Input	Clock Enable : CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE , are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
$\overline{CS}$	Input	Chip Select : $\overline{CS}$ enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
*1LDM,UDM	Input	Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-DQ7 ; UDM correspons to the data on DQ8-DQ15.
BA0, BA1	Input	Bank Addres Inputs : BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A [n : 0]	Input	Address Inputs : Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 determines which mode register (mode register or extended mode register) is loaded during the MODE REGISTER SET command.
*1DQ	I/O	Data Input/Output : Data bus
*1LDQS,UDQS	I/O	Data Strobe : Output with read data, input with write data. Edge-aligned with read data, centered in write data. it is used to fetch write data. For the x16, LDQS corresponds to the data on DQ0-DQ7 ; UDQS corresponds to the data on DQ8-DQ15.
NC	-	No Connect : No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply : +1.8V ± 0.1V.
VSSQ	Supply	DQ Ground.
VDD	Supply	Power Supply : +1.8V ± 0.1V .
VSS	Supply	Ground.

Refer to the Samsung datasheet for more detailed information on the device.

5.5.4 Elpida DDR Device

The features of the Elpida device include:

- Low voltage power supply
  - VDD: 1.8V ± 0.15V
  - VDDQ: 1.8V ± 0.15V
- Wide temperature range (.25°C to 85°C)
- Programmable Partial Array Self Refresh
- Programmable Driver Strength
- Auto Temperature Compensated Self Refresh by built-in temperature sensor.
- Deep power down mode
- Small package (60-ball FBGA)
- FBGA package is lead free solder (Sn-Ag-Cu)
- Data rate: 200Mbps/IO(max)
- Double Data Rate architecture: two data transfers per one clock cycle
- Bi-directional, data strobe (DQS) is transmitted received with data, to be used in capturing data at the receiver.
- 1.8V LVCMOS interface
- Command and address signals refer to a positive clock edge
- Quad internal banks controlled by BA0 and BA1
- Data mask (DM) for write data
- Wrap sequence = Sequential/ Interleave
- Programmable burst length (BL) = 2, 4, 8
- Automatic precharge and controlled precharge
- Auto refresh and self refresh
- 8,192 refresh cycles/64ms (7.8µs maximum average periodic refresh interval)
- Burst termination by Burst stop command and
- Precharge command

5.5.5 Device Compatibility

The Micron, Elpida, and Samsung devices are pin compatible with each other. **Figure 23** below shows the pin arrangement for each device. The Elpida device has a different orientation than the Samsung device.

Samsung

60Ball(6x10) CSP						
	1	2	3	7	8	9
A	Vss	DQ15	Vssq	Vddq	DQ0	Vdd
B	Vddq	DQ13	DQ14	DQ1	DQ2	Vssq
C	Vssq	DQ11	DQ12	DQ3	DQ4	Vddq
D	Vddq	DQ9	DQ10	DQ5	DQ6	Vssq
E	Vssq	UDQS	DQ8	DQ7	LDQS	Vddq
F	Vss	UDM	N.C.	N.C.	LDM	Vdd
G	CKE	CK	$\overline{CK}$	$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
H	A9	A11	A12	$\overline{CS}$	BA0	BA1
J	A6	A7	A8	A10/AP	A0	A1
K	Vss	A4	A5	A2	A3	Vdd

Elpida

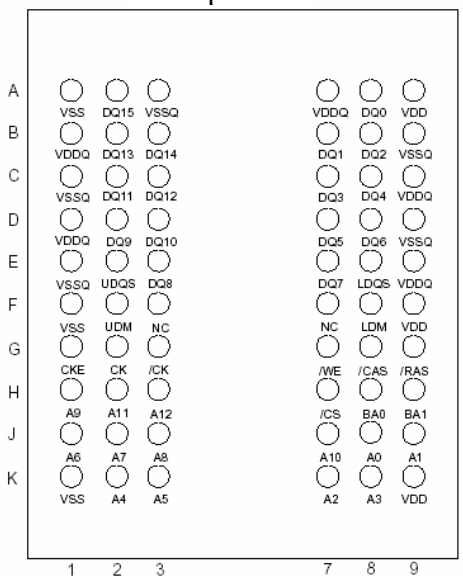
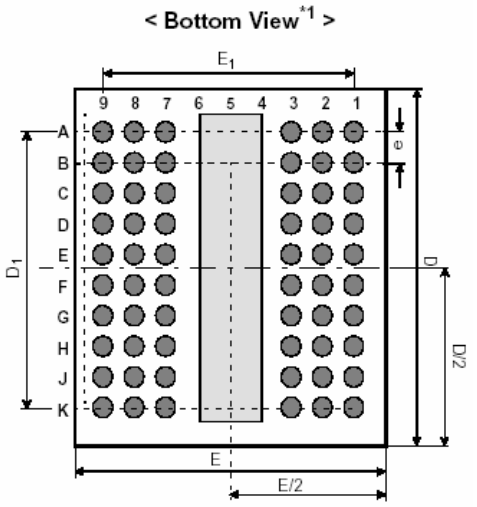


Figure 23. DDR SDRAM Pin outs

. Figures 24 and 25 show the mechanicals of each of the memory devices.



[Unit:mm]

Symbol	Min	Typ	Max
A	0.90	0.95	1.00
A_1	0.30	0.35	0.40
E	-	11.5	-
E_1	-	6.4	-
D	-	9.0	-
D_1	-	7.2	-
e	-	0.80	-
jb	0.40	0.45	0.50
z	-	-	0.10

Figure 24. Samsung DDR Mechanical

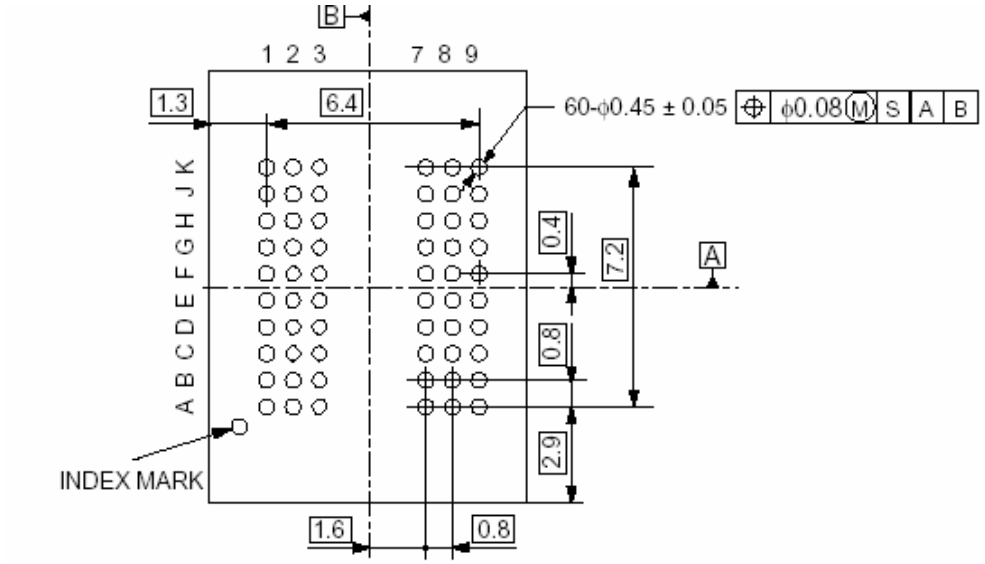


Figure 25. Elpida DDR Mechanical

The Alpha units were built with the 256 Mb Samsung devices and the Beta units will use the Elpida device. The determination of if and when to move to the Micron device will be made once those devices are qualified and the schedule information has been received.

5.6 Audio Codec

An AIC23 audio CODEC is provided on the OMAP5912 TM to provide. The design of the audio circuit is described in this section.

5.6.1 Audio CODEC Design

Figure 26 is the design of the audio CODEC circuit on the TM.

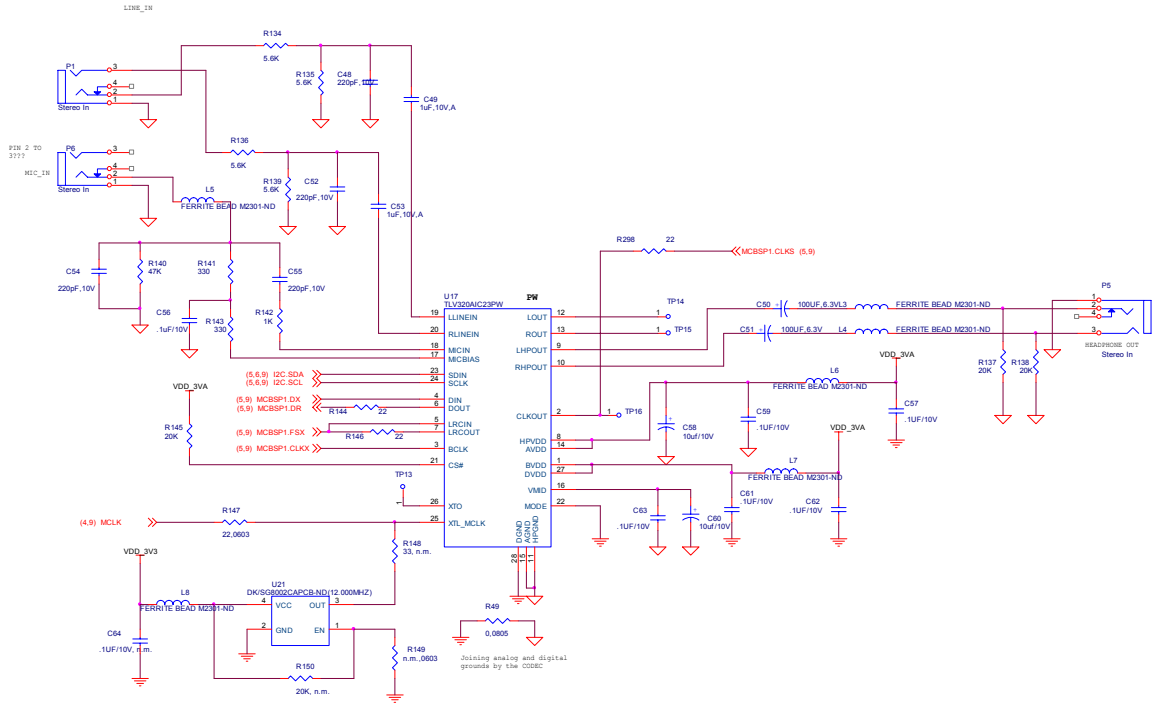


Figure 26. AIC23 Audio CODEC Design

5.6.2 Audio Inputs

The audio circuit has two stereo audio inputs. **Figure 28** shows the audio inputs.

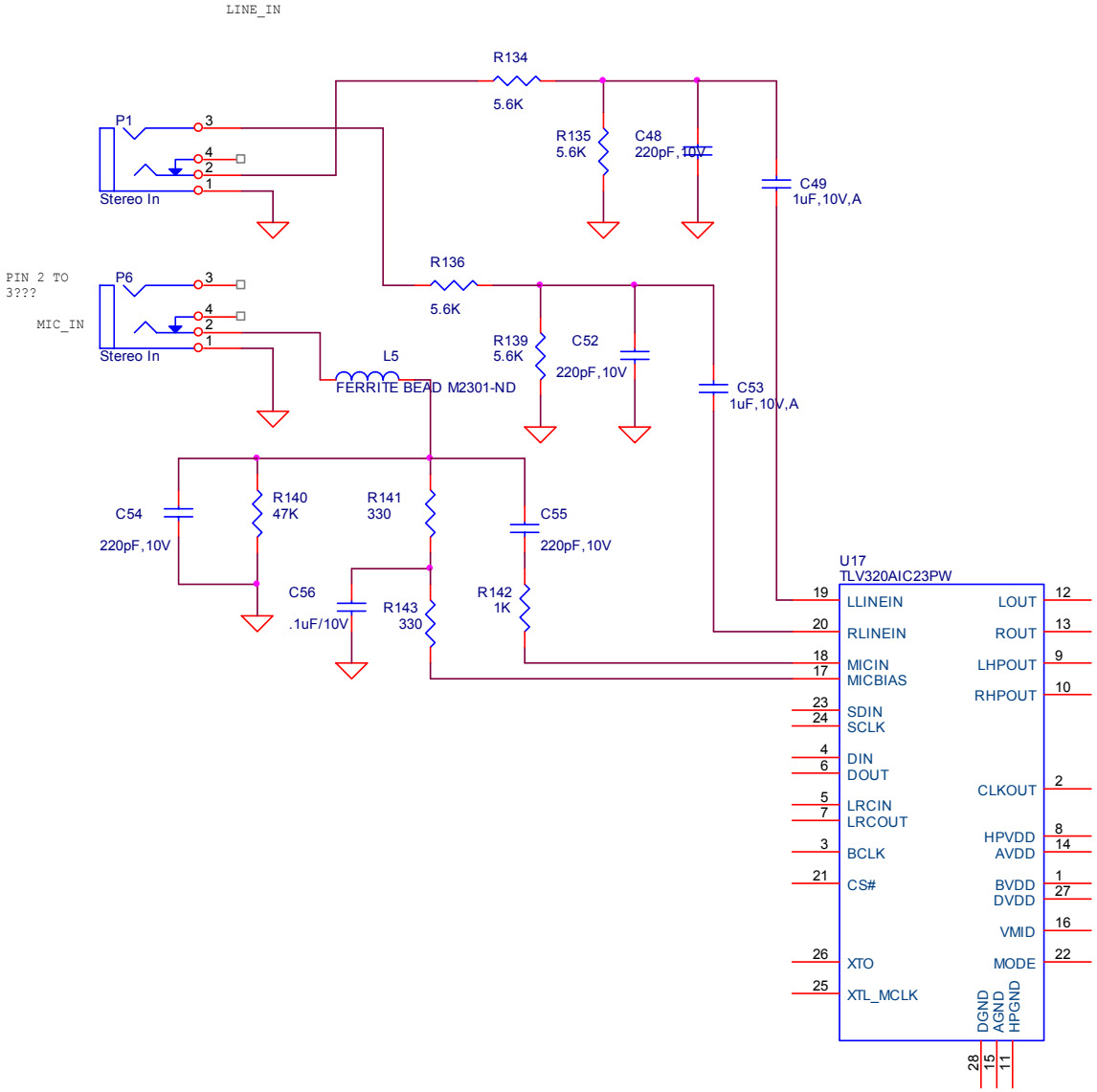


Figure 27. AIC23 Audio Inputs

The TLV320AIC23 has line inputs for the left and the right audio channels (RLINEIN and LLINEIN). Access to these signals is gained through connector **P1**, a 3.5mm audio jack. Both line inputs have independently programmable volume controls and mutes. The gain is independently programmable on both left and right line-inputs.

R134 and **C48** create a high pass filter for the audio input on the left channel. **R136** and **C52** do the same for the right channel. Resistors **R139** and **R136** are used to insure the line inputs are terminated when no signal is present at **P1**.

Connector **P6** is a 3.5mm jack that is used to connect the microphone input to the AIC23. MICIN is a high-impedance, low-capacitance input that is compatible with a wide range of microphones. It has a programmable volume control and a mute function. Active and passive filters prevent high frequencies from folding back into the audio band.

The MICBIAS output provides a low-noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. The maximum source current capability is 3 mA. This limits the smallest value of external biasing resistors that safely can be used. The MICBIAS output is not active in standby mode.

5.6.3 Audio Outputs

Figure 29 defines the design of the stereo headphone output of the AIC23 Audio CODEC.

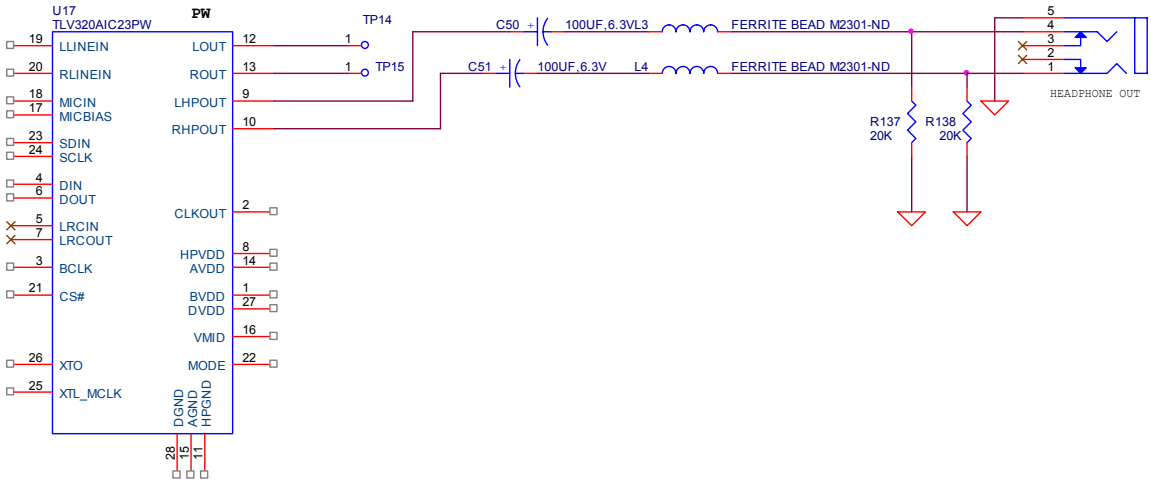


Figure 28. AIC23 Audio Outputs

Access to the headphone outputs is via a single 3.5mm stereo jack. While suitable for driving a headphone, the output is not suitable for driving a set of speakers unless those speakers are powered. The audio is coupled to the left and right channels through C30 and C31. Each channel has a ferrite bead and resistor circuit to help minimize transmissions out the audio jack.

5.6.4 Clocking

The AIC23 requires an external 12MHZ clock to drive the internal components. **Figure 30** shows that there are two ways of accomplishing this.

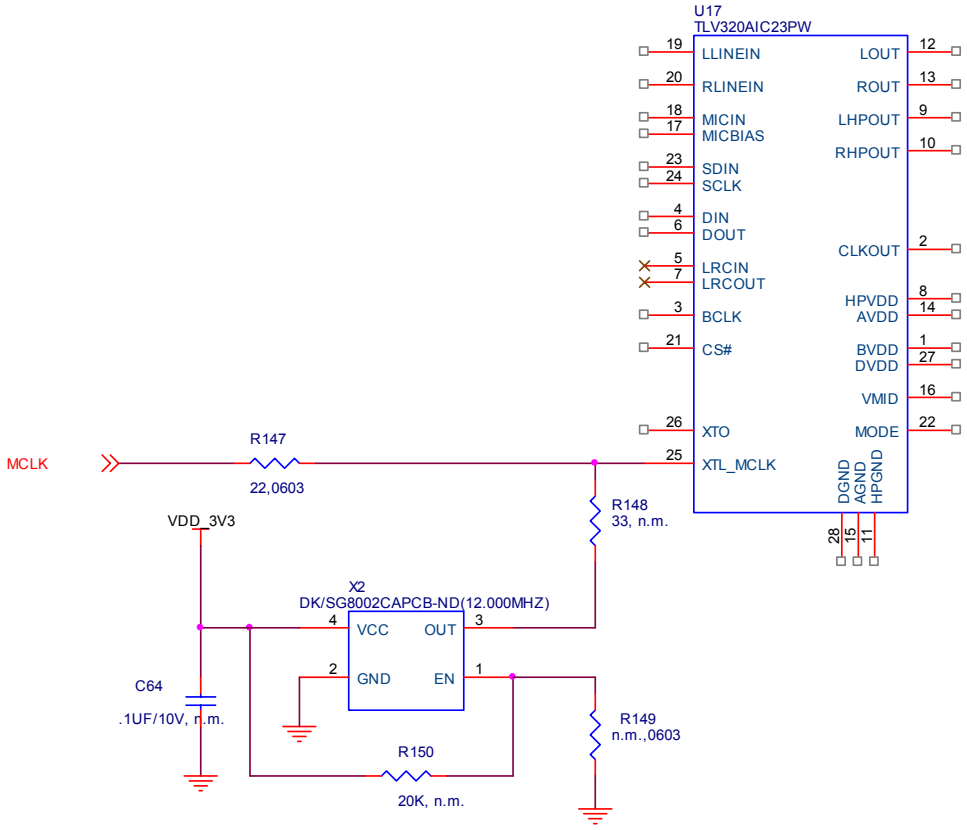


Figure 29. AIC23 Clocking Options

X2 is an external 12MHZ crystal oscillator that can provide the 12MHZ clock when installed. **R3** must be mounted to make the connection. At this time, **X2** is not installed and the primary clock source option for providing the clock is used.

The primary clock source is the **MCLK** signal from the OMAP5912. This can be set to 12MHZ and fed directly into the AIC23. This is the primary option planned for the TM. In this option X2, R150, R149, R148, and C64 are not installed.

5.6.5 Power

Figure 31 describes the power design for the AIC23.

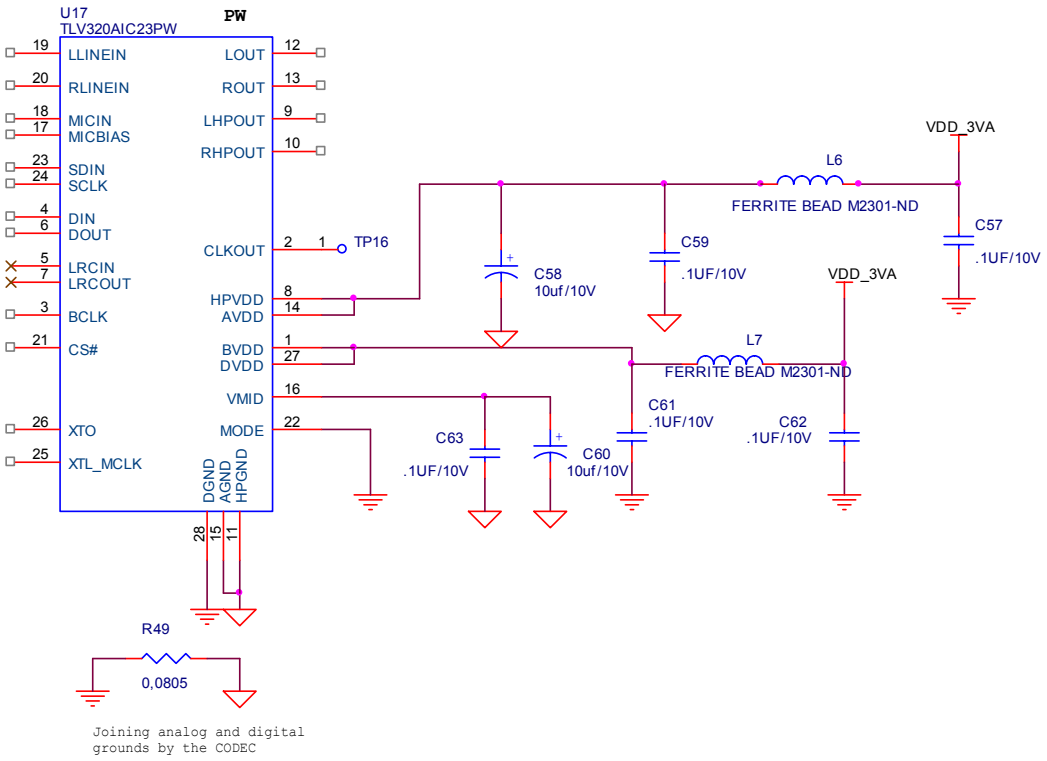


Figure 30. AIC23 Power Section

Each of the power inputs are heavily filtered to minimize the affect noise may have on the audio component. The power rails are actually split into analog and digital rails. **BVDD** and **DVDD** are digital rails for the **AIC23**. **HPVDD** and **AVDD** are the analog rails. The LC circuits minimize any high frequency noise form entering the **AIC23** whose harmonics could potentially cause noise in the audio.

Resistor **R49** allows for the grouping of the grounds for the AIC23 such that they connect at a single point to the system ground. This technique is used to insure that the PCB layout software does not allow the ground to be connected on a common ground plane.

5.6.6 OMAP5912 Interface

Figure 32 is the design of the interface between the OMAP5912 and the AIC23 CODEC.

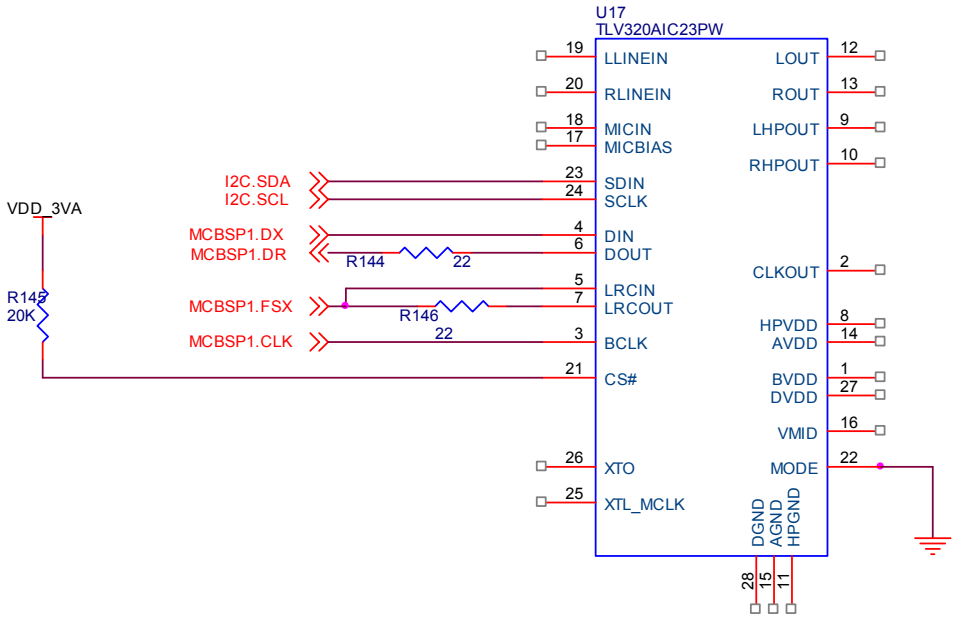


Figure 31. AIC23 OMAP5912 Interface

The mode of the AIC23 control interface is controlled by the **MODE** pin. If the mode pin is tied low, then the interface is a two wire interface, or I2C. If the mode pin is tied high, then it is in the SPI mode. In the TM design, the interface is set to two wire mode. In 2-wire mode, the data transfer uses **SDIN** for the serial data and SCLK for the serial clock. The start condition is a falling edge on **SDIN** while SCLK is high. The seven bits following the start condition determine which device on the 2-wire bus receives the data. R/W determines the direction of the data transfer. The TLV320AIC23 is a write only device and responds only if R/W is 0. The device operates only as a slave device whose address is selected by setting the state of the **CS#** pin as defined in Table 11.

Table 11. AIC23 I2C Address Definition

CS State	Address
0	0011010
1	0011011

In the TM design, this signal is pulled high via R145. The I2C bus is used to setup all control functions on the AIC23.

McBSP1 is used from the OMAP5912 as the audio channel interface for the AIC23. The McBSP1 is setup as an I2S interface. McBSP1 is used because in the OMAP5912 the DSP has direct access to McBSP1.

The AIC23 is setup as the master. This means that the AIC23 provides the frame sync and clock to the OMAP5912. **McBSP1.DX** is the input path to the AIC23 while **MCBSP1.DR** is the output path. **McBSP1.CLK** is the clock output from the AIC23. **McBSP1.FSX** is the frame clock for the data signal.

5.7 Compact Flash

The TM has a Compact Flash interface that supports both Type I and II cards**. Figure 33** details the design of the interface.

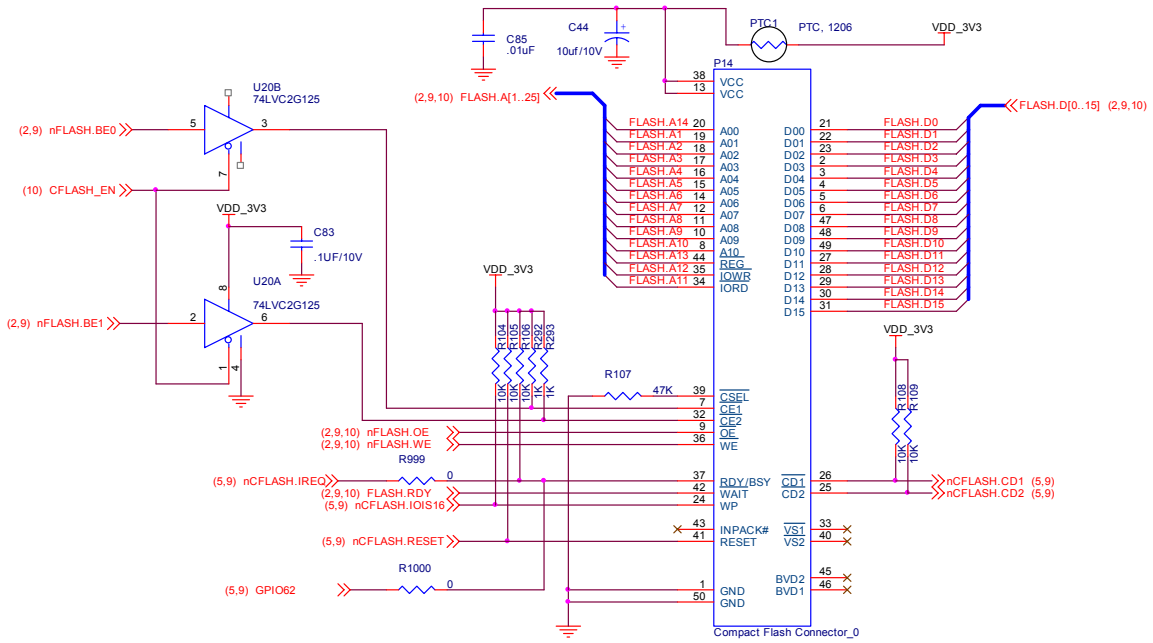


Figure 32. Compact Flash Socket Design

5.7.1 Integrated Interface

The OMAP5912 has an integrated control interface that allows for a Compact Flash device to be connected directly to the OMAP5912. The Compact Flash controller (CFC) interfaces a Compact Flash and a classical memory interface. Control signals from memory interface are processed through the CFC to drive a Compact Flash card, and

control signals from Compact Flash are processed to perform a data transfer to the memory interface.

5.7.2 Compact Flash Interface Signals

Signals on the OMAP5912 are converted to Compact Flash control signals when the Compact Flash is accessed. Table 12 defines how the signals functions change when the Compact Flash is accessed.

Table 12. OMAP5912 Compact Flash Interface

Name	I/O	Compact Flash Name	Compact Flash Description
FLASH.A[10-1]	OUT	A10-A1	Address bus
FLASH.A[14]	OUT	A0	Address bus
FLASH.A[13]	OUT	REG	Attribute memory select
FLASH.A[12]	OUT	IOWR	I/O data write
FLASH.A[11]	OUT	IORD	I/O data read
FLASH.RDY	IN	WAIT	Wait
FLASH.WE	OUT	WE	Strobe
FLASH.BE[1]	OUT	CE2	Card enable
FLASH.BE[0]	OUT	CE1	Card enable
FLASH.D[15:0]	I/O	D15-D0	Data bus
FLASH.OE	OUT	OE	Output enable
CFLASH.IOIS16	IN	WP IOIS16	Write protect 8/16 bits selection
CFLASH.RESET	OUT	RESET	Reset
CFLASH.CD1	IN	CD1	Card detect
CFLASH.CD2	IN	CD2	Card detect
CFLASH.IREQ	IN	RDY/BSY IREQ	Ready for new data

5.7.3 CFLASH.IREQ

Currently, we are unable to get the CFLASH.IREQ to work properly as defined. For this reason we have a provided the ability to connect the CFLASH.IREQ to either the predefined CFLASH.IREQ pin or to GPIO62. The default configuration uses GPIO62, although this could change in the future.

5.7.4 Address Decode Logic

Within OMAP, the CF interface can be placed at CS0-CS3 by setting a register in the OMAP5912. The TM design recognizes either CS1 or CS2 only in its design. CS2 is the default selection in order not to interfere with the Ethernet controller which is located at CS1.

No external CS signal is needed as this is generated on the BE0 and BE1 pins from the OMAP5912. However, **BE0** and **BE1** when not being used to access the CF card can still be active during other memory accesses which could lead to false enables being sent to the CF card. For this reason the **BE0** and **BE1** must be qualified with an external CS

signal called **CFLASH_EN**. This signal is used to activate two buffers SN74LVC2G125 buffers. When qualified with the CFLASH_EN signal, the BE0 and BE1 signals are allowed to pass to the CF interface. Resistors R292 and R293 are set at 1K to allow for a fast rise time when the CFLASH_EN signal is driven high because this causes the buffers to tri-state. CFLASH_EN is connected to CS2.

Figure 34 shows the decode logic for the CFLASH_EN signal.

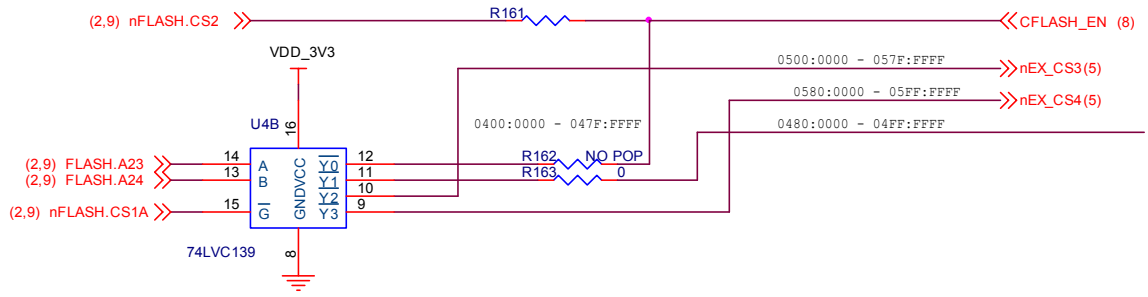


Figure 33. Compact Flash Decode Logic

U4B is half of a SN74LVC139 decoder. The **CFLASH_EN** signal enables the CE buffers for the CF Interface as mentioned earlier. This CF Interface can reside in either CS1 or CS2. CS2 is the default configuration, meaning R161 is loaded and R162 is not loaded.

The CF interface will be active for the entire CS range selected. Depending on what specific addresses are selected, the CF Interface will take on the characteristics of a specific CF mode. The Compact Flash card supports the following access modes:

- Common memory
- Attribute memory
- I/O

The controller manages access to the different modes of the Compact Flash (access protocol in these modes follows the Compact Flash standard). Table 13 shows what address ranges create implement which access mode for the CF interface.

Table 13. Compact Flash Memory Mapping

Space Name	Start Address and CS Address	Stop Address	Size
CF memory space	0000:0000	0000:07FF	2K bytes
CF attribute space	0000:0800	0000:0FFF	2K bytes
CF I/O space	0000:1000	0000:17FF	2K bytes

5.7.5 Databus Interface

The databus is connected to the CF Interface and is used as with any normal memory device interface.

5.7.6 Power interface

Power to the CF Interface is supplied by the 3.3V supply. **PTC1** is a self healing current limiting device. This is provided in lieu of a fuse device. When the current exceeds 1A max, the resistance of the PTC will go up, limiting the current to the CF Interface. The hold current, is specified at 500ma.

5.8 JTAG/MultiICE Interface

A single standard 14 pin JTAG connector is provided on the design to allow access to the JTAG interface of the OMAP

5.8.1 JTAG/MultiICE Features

The JTAG/MultiICE interface provides the following features:

- JTAG port Buffer
- Standard 14 pin JTAG connector
- 20 Pin MultiICE Connector
- Ability to reset the ARM processor for the Multi ICE interface
- Strappable JTAG reset nTRST pull down
- Disable pin for ADM shutdown

5.8.2 Design Description

Figure 35 is the design of the JTAG interface on the TM.

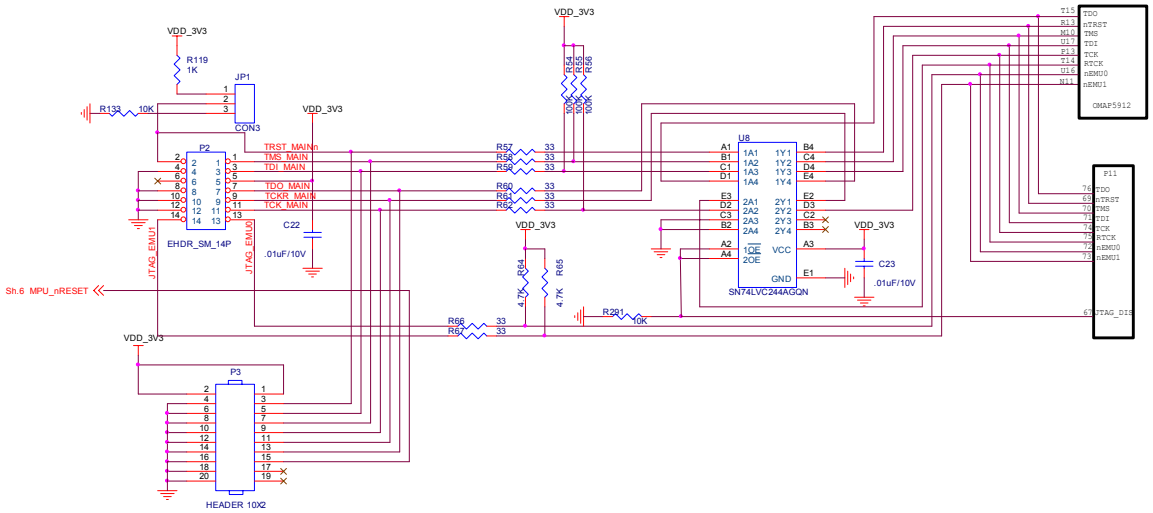


Figure 34. JTAG Interface Design

The OMAP5912 provides the signals for the JTAG interface. The JTAG interface is routed through **U8** which is a SN74LVC244AGQN buffer. Series resistors **R57-62** and **R66-67** are intended to control the over and undershoot of the signals. Resistors **R54-56** and **R64-65** provide additional pull up current for the signals as needed. These values may be adjusted during the testing phase of the board.

Connector **P2** is the connection for the 14 pin JTAG connector. Pin 6 is removed and acts as a polarization key for the standard JTAG connector. **JP1** is used to set the default termination of the **nTRST** signal to either being pulled down, for the standard JTAG, or pulled up, for the MultiICE interface.

P3 is the connector for the MultiICE cable. The polarity of the nTRST signal is different on the MultiICE than it is on the standard JTAG.

The buffer **U8** is normally enabled via the pull down resistor **R291**. When the TM is plugged into the ADM, this signal is pulled HI. This disables the interface by disabling the buffer. The signals that connect to **P11** are then used to provide access to the circuitry on the ADM. At this point, both of the connectors on the TM are isolated from the signals on **P11** and cannot be used.

5.9 USB Port

A standard USB Host port interface is provided via a standard Type A connector. This can be used to connect such devices as:

- Keyboard
- Mouse
- Digital cameras

The design does support the configuring of the USB port to provide client side capabilities. That will be discussed in the following sections.

5.9.1 USB Features

The OMAP5912 USB host controller (HC) communicates with USB devices at the USB low-speed (1.5M bit-per-second maximum) and full-speed (12M bit-per-second maximum) data rates. It is compatible with the *Universal Serial Bus Specification Revision 2.0* and the *Open HCI—Open Host Controller Interface Specification for USB,* Release 1.0a, available through the Compaq Computer Corporation web site.

A single USB Type B connector is provided on the OMAP5912 TM. Power is provided by the OMAP5912 TM through this connector to power external devices.

5.9.2 Design Description

Figure 36 is the design diagram of the USB interface.

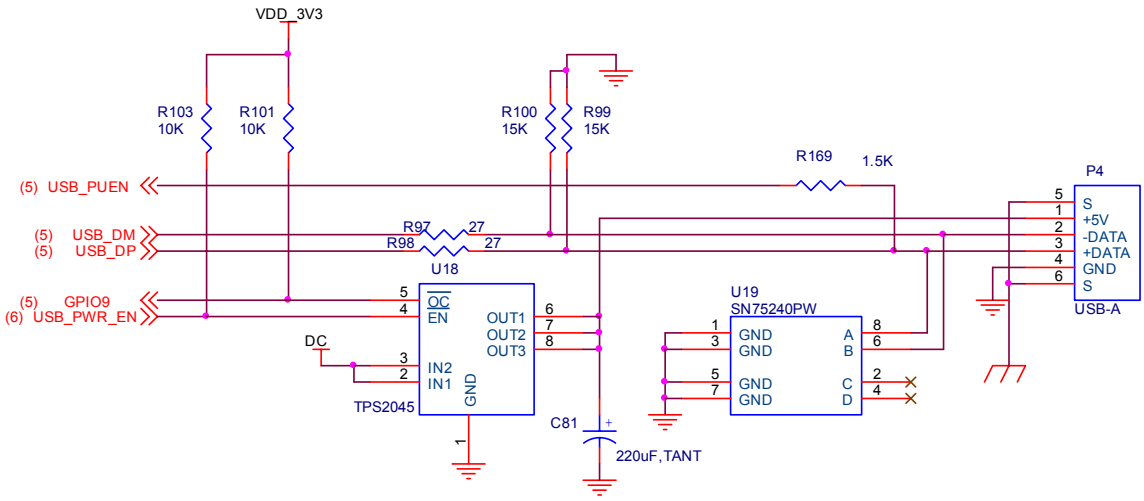


Figure 35. USB Host Design

5.9.2.1 Host Operation

Three signals are used on the OMAP5912 to implement the USB host interface**. USB.DM** and **USB.DP** provide the plus and minus polarity of the interface signals directly to the USB connector **P4** via a pair of 27ohm resistors. Proper initialization of the OMAP5912 device to support this mode of operation requires proper setting of the top-level pin multiplexing for pins USB.DP and USB.DM and selection of an HMC_MODE value, which routes a host controller port to pin group 0. OTG_SYSCON_1.USB0_TRX_MODE must be set to 3 to allow proper operation of the integrated USB transceiver. OMAP5912 integrated pull downs for pins USB.DP and

USB.DM do not meet the USB specifications for D+ and D– pull downs. The external 15K pull down resistors, **R199** and **R100**, are implemented to meet this requirement. USB.PUEN is used in the GPIO mode to detect the over current mode. Proper initialization of the OMAP5912 device to support this mode of operation on pin **P4** requires proper setting of the top-level pin multiplexing.

Resistor **R169** is not required for the Host mode of operation, which is the default mode of the design. If Client mode is required, an external adapter can be purchased that will connect to **P4** and convert it to the client gender (See section 7.1.11). **R169** is used to signal the host that it is active and wishes to be identified. This does not interfere with host operation as the **USB.PUEN** is not activated via software.

To select USB Host, GPIO9 needs to be high (default selection), and ball P4 on OMAP5912 (USB.PUEN) needs to be placed into high Z state (by setting FUNC_MUX_CTRL_D[5:3] = 100) in order to negate the impact of the 1.5k ohm resistor pull up on the D+ signal.

To select USB Client(Function) (with the use of an external adapter), GPIO9 must be low, and the USB.PUEN signal must be muxed onto the P4 ball (set FUNC_MUX_CTRL_D[5:3] = 000).

U16 is a TPS2014 is a power distribution switch. The TPS2014 power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The high-side switch is a 95-mW n-channel MOSFET. The switch is controlled by a logic enable that is compatible with 3-V logic. Gate drive is provided by an internal charge pump designed to control the power switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 4 V. When the output load exceeds the current-limit threshold or a short is present, the TPS2014 limits the output current to a safe level by switching into a constant-current mode, and the over current logic output is set to low. Continuous heavy overloads and short circuits will increase the power dissipation in the switch and cause the junction temperature to rise. A thermal protection circuit is implemented, which shuts the switch off to prevent damage when the junction temperature exceeds its thermal limit. An under voltage lockout is provided to ensure the switch is in the off state at start-up. The TPS2014 is designed to limit at 1.2 A. **C81** is a low ESR capacitor required for the output of the TPS2014.

U19 is a USB port transient protection device. The SN75240 is a dual transient voltage suppressors designed to provide additional electrical noise transient protection to two USB ports. Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the OMAP5912 if they are of sufficient magnitude and duration. The SN75240 significantly increase the port ESD protection level and reduce the risk of damage to the large and expensive circuits of the USB port.

U10 is the TPS65010 power management device. In order to save as many GPIO pins on the OMAP5912 as possible, the GPIO pin on the TPS65010 was used as the enable pin for the TPS2014. A high on EN turns off the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 mA. A logic zero input restores bias to the drive and control circuits and turns the power on. To access the GPIO pin on the TPS65010, the I2C interface is used to communicate to the GPIO pin.

Access to the USB.DM, USB.DP, and USB.PUEN (GPIO58) can be obtained via the B connector **P10** if use by the expansion cards or ADM is desired. In order for this to happen, the nothing can be plugged into the USB connector **P4**.

5.9.2.2 Client Operation

With the use of an adapter, the USB interface can be converted for use as a client interface. Refer to **Figure 36**. Resistor R169 is connected to the USB_PUEN signal. This is required to activate the client interface. In the host mode, this pin is left tri-stated. By default U18 is not enabled. This must be left disabled in the client mode.

The adapter is defined in the pin out section of the document.

5.10 Serial Port

Access to a single serial port with an RS232 level driver via a DB9 connector will be provided. This will be used for downloading and connection to a serial debugger or terminal device.

5.10.1 Features

Features of the serial interface are:

- OMAP5912 UART1 connection default
- OMAP5912 UART3 connection optional
- 240K Baud Max speed
- DB9 Male Connector
- Disable pin accessible via the expansion connectors
- TX,RX signals
- Ground

5.10.2 Design Description

Figure 37 is the design diagram of the serial interface.

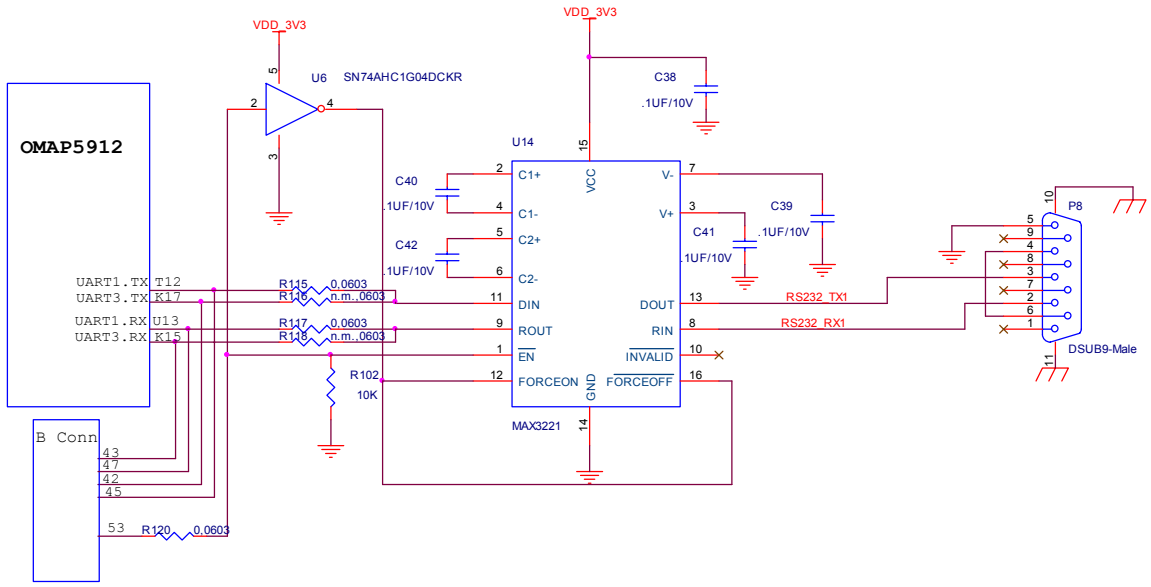


Figure 36. Serial Port Interface

Serial port UART1 is the default serial port used from the OMAP5912. The option is there to switch the port to UART3 by removing **R115** and **R117** and installing **R116** and **R118**. **R116** and **R118** are not populated on the board.

The UART1 and UART3 signals from the OMAP5912 are also available on expansion connector B for use by the expansion cards. If the use of these signals is needed, pin 53 on the B Connector can be pulled Hi and the RS232 driver is disabled through the SN74AHC1G04 inverter.

The RS232 driver function is performed by **U14**, a TI MAX3221 which converts the signals from the OMAP5912 to the required RS232 levels. It should be noted that the output levels of the MAX3221 swing +3V and -3V. While this is more than adequate to drive a terminal or PC located in the area, it may not be adequate to drive over long distances. If long distance is a requirement, the signals will need to be boosted to higher levels.

Pins 4 and 6 are looped back on each other to allow for the detection of the TM by the applications running on the PC.

5.11 Ethernet

The TM is equipped with a 10Mb Ethernet port. This section describes the Ethernet interface and how it connects to the OMAP5912 Processor.

5.11.1 Ethernet Circuit Design

Figure 38 is the design of the Ethernet interface on the TM.

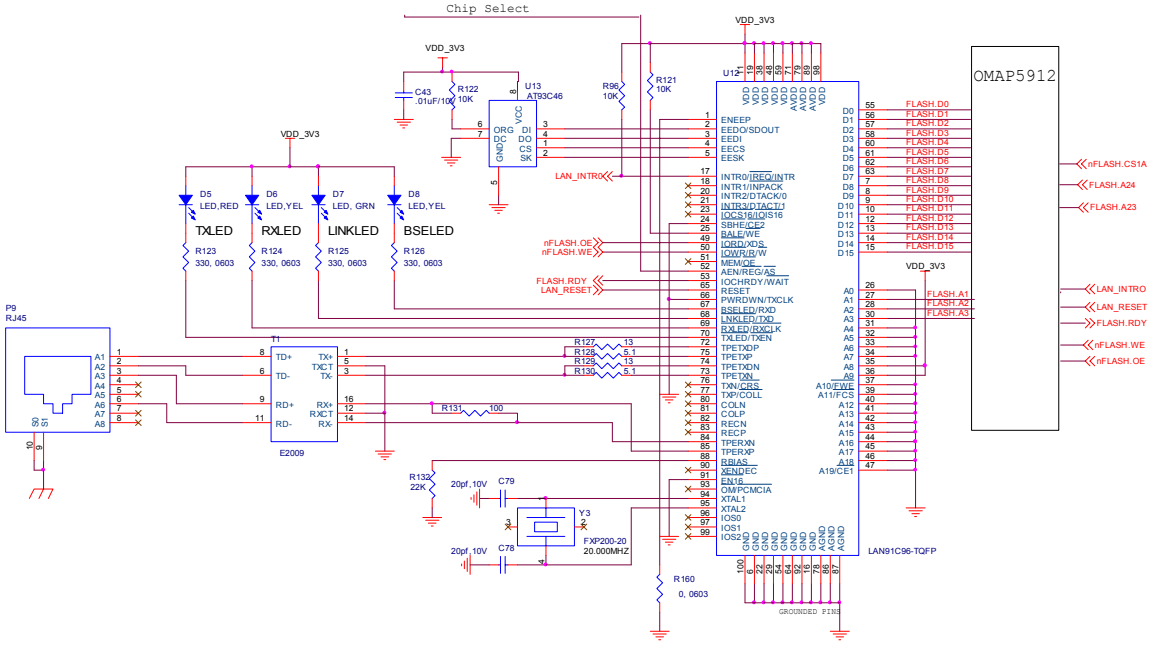


Figure 37. 10Mb Ethernet Design

The following sections break down the design and provide detailed description of each section. Included in the descriptions will be:

- Interrupt
- Memory Address Decode
- LAN91C96
- Crystal Circuit
- Output Section
- EEPROM
- Status LEDS

5.11.2 Interrupt

The interrupt line from the LAN91C96 device connects to GPIO0 on the OMPA5912. Pin 93 "nROM/nPCMCIA" is open, which puts the LAN91C96 in Local Bus mode. In this mode the LAN_INTR0 is a active HIGH line. You will note on the schematic that the signal LAN_INTR0 is shown to be active High.

5.11.3 Memory Address Decode

The second half of **U4**, a 74LVC139, is used to create the address decode for the Ethernet controller and the Compact Flash**. Figure 39** is the design of the decode circuit.

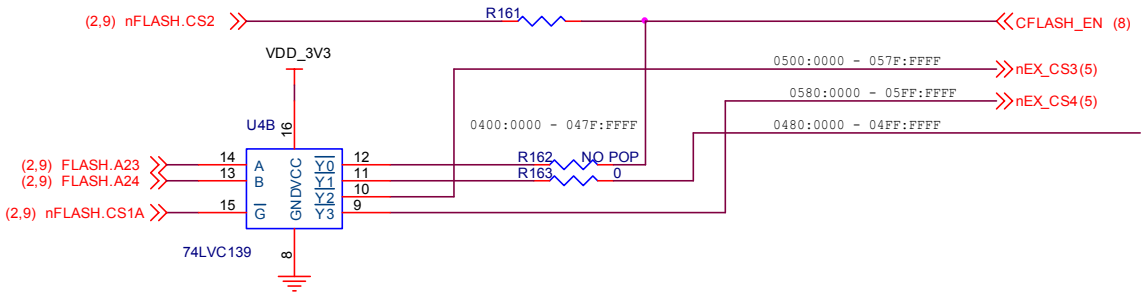


Figure 38. Ethernet Address Decode Logic

CS1A may be shared with the Compact Flash circuit or the Compact Flash circuit may have its own address chip select. There are two different scenarios that are supported by this design:

- Compact Flash and Ethernet share CS1A
- Compact Flash uses CS2 and Ethernet uses CS1A

The default configuration is that the Compact Flash occupies CS2.

5.11.3.1 Chip Select Shared

CS1A from the OMAP5912 is used as the primary chip select. Address lines A24 and A23 from the OMAP5912 are also used to minimize the amount of the CS1A block that is being used by the LAN91C96. Address lines A24 must be low and A23 must be high to select the LANC9196 device. This results in an effective address range of 0480:0000-04FF:FFFF for the Compact Flash. Use address 0490:0000 as the base address for the LAN91C96 in this scenario.

5.11.3.2 CF CS2 and Ethernet CS1A

The compact Flash will be mapped to CS2 and the Ethernet mapped to CS1A as the default configuration.

5.11.3.3 Expansion Chip Selects

Two signals are provided for use by the Expansion Cards. These are nEX_CS3 and nEX_CS4. These signals are brought out onto the expansion connectors.

5.11.4 LAN91C96

The LAN91C96 Ethernet Transceiver from SMSC provides the interface for the Ethernet function on the OMAP5912 TM. The features of the LAN91C96 are:

- ISA/PCMCIA Single-Chip Ethernet Controller
- A Subset of Motorola 68000 Bus Interface Support
- Fully Supports Full Duplex Switched Ethernet
- Supports Enhanced Transmit Queue Management
- 6K Bytes of On-Chip RAM
- Supports IEEE 802.3 (ANSI 8802-3) Ethernet Standards
- Automatic Detection of TX/RX Polarity Reversal
- Simultasking Early Transmit and Early Receive Functions
- Enhanced Early Transmit Function
- Receive Counter for Enhanced Early Receive
- Hardware Memory Management Unit
- Optional Configuration via Serial EEPROM Interface (Jumperless)
- Supports single +3.3V VCC Designs
- 6 Bit Data and Control Paths
- Fast Access Time (40ns)
- Pipelined Data Path
- Handles Block Word Transfers for any Alignment
- High Performance Chained ("Back-to-Back") Transmit and Receive
- Dynamic Memory Allocation Between Transmit and Receive
- Flat Memory Structure for Low CPU Overhead
- Buffered Architecture, Insensitive to Bus Latencies (No Overruns/Underruns)
- Integrated 10BASE-T Transceiver Functions:
  - Driver and Receiver
  - Link Integrity Test
  - Receive Polarity Detection and Correction
- 10 Mb/s Manchester Encoding/Decoding and Clock Recovery
- Automatic Retransmission, Bad Packet Rejection, and Transmit Padding
- External and Internal Loopback Modes
- Four Direct Driven LEDs for Status/ Diagnostics

5.11.5 Crystal

An external 20MHZ crystal is used to supply the clock source for the LAN91C96. The crystal was chosen as a lower cost option.

5.11.6 Output Section

Figure 40 shows the design of the output section of the Ethernet circuitry.

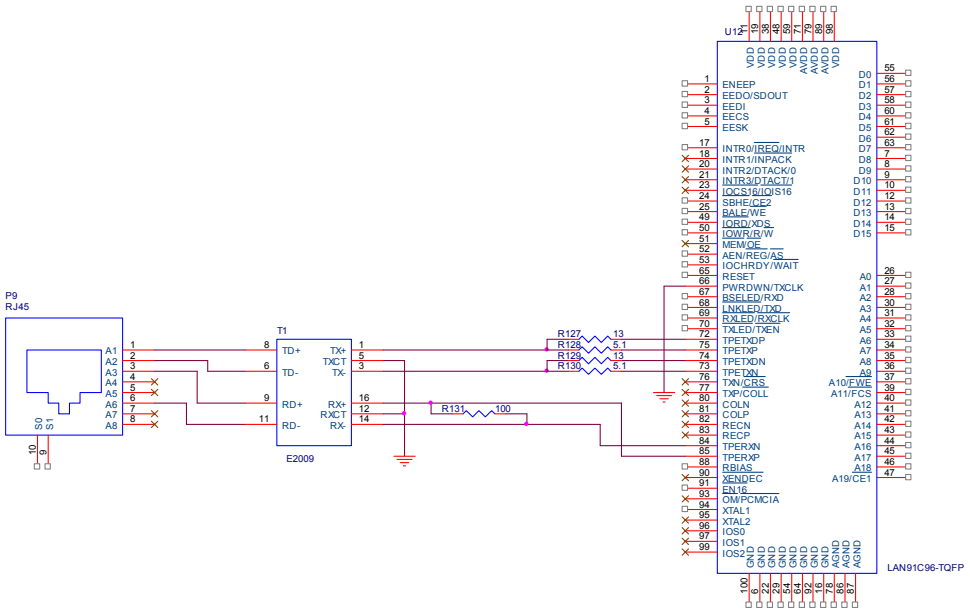


Figure 39. Ethernet Output Section

5.11.7 EEPROM

Figure 41 is the interface between the EEPROM and the LAN91C96 Ethernet Controller.

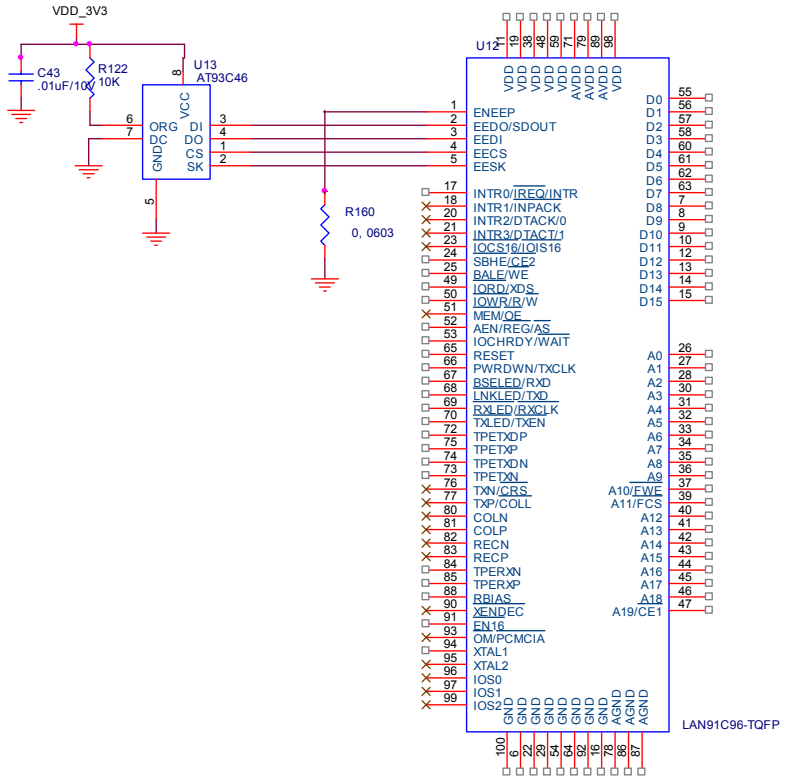


Figure 40. Ethernet EEPROM

The LAN91C96 has the ability to retrieve configuration information from a serial EEPROM on reset or power-up. The serial EPROM acts as storage of configuration and IEEE Ethernet address information.

The device used is the **AT93C46** EEPROM from Atmel. The AT93C46 provides 1024bits of serial electrically erasable programmable read only memory (EEPROM) organized as 64words of 16 bits each. The **ORG** pin is pulled high which controls the bit configuration.

Pin 1 on the LAN91C96 is the EEPROM enabled pin. It has an internal pull-up in the LAN91C96. If the EEPROM is not to be used, then **R160** must be populated. The default is that **R160** is not installed. Power for the AT93C46 is provided by the 3.3V voltage rail which is the same rail as is used by the LAN91C96.

5.11.8 Status LEDS

There are four status LEDS on the LAN91C96 device. Table 14 defines the meaning of each LED and the corresponding color for each LED and how each of the status LEDS are used by the LANC9196.

Table 14. Ethernet Status LEDs

LED	Function
TX	Activated by transmit activity.
RX	Activated by receive activity.
LINK	Reflects the link integrity status.
BSE	Board select LED. Activated when the board space is accessed, namely on accesses to the LAN91C96 register space or the ROM area decoded by the LAN91C96. The signal is stretched to 125ms.

6.0 Expansion Connectors

This section defines the type and pinout of the expansion connectors for the system. In order to insure proper operation of the system, the functions of each pin on the connector is being fixed. Not all pins on the connectors will be used by all processors.

A lot of the pins have multiple functions that they can perform. All of these expansion cards will have access to all of the functions found on each pin if needed. The default naming convention will not show any additional functions in the name; however the

additional functions are defined in the OMAP5912 datasheet. If certain signals are used by the OMAP5912 TM in something other than the default mode, this will also be indicated. Descriptions for the signals will only cover the signal as it is used on the OMAP5912 TM.

The following sections cover each of the four expansion connectors.

6.1 Connector A

Connector A contains the Flash Bus and its control signals. It also contains the SD/MMC interface for the OMAP5912. Table 15 shows the pinout of the A Connector.

Table 15. Connector A Pinout

Name	No.	Name	Name
GND	1	2	GND
GND	3	4	GND
3.3V	5	6	3.3V
3.3V	7	8	3.3V
	9	10	
MPU_BOOT	11	12	MMC.CMD
MMC.DAT2	13	14	MMC.DAT3
MMC.DAT0	15	16	MMC.DAT1
MMC.CLK	17	18	FLASH.ADV
FLASH.RDY	19	20	FLASH.CLK
FLASH.BE0	21	22	FLASH.BE1
FLASH.WE	23	24	FLASH.WP
FLASH.RP	25	26	FLASH.OE
FLASH.CS3	27	28	FLASH.CS2U
FLASH.CS2	29	30	FLASH.CS1U
FLASH.CS1	31	32	FLASH.D[15]
FLASH.D[14]	33	34	FLASH.D[13]
FLASH.D[12]	35	36	FLASH.D[11]
FLASH.D[10]	37	38	FLASH.D[9]
FLASH.D[8]	39	40	FLASH.D[7]
FLASH.D[6]	41	42	FLASH.D[5]
FLASH.D[4]	43	44	FLASH.D[3]
FLASH.D[2]	45	46	FLASH.D[1]
FLASH.D[0]	47	48	GPIO1
FLASH.A25	49	50	FLASH.A24
FLASH.A23	51	52	FLASH.A22
FLASH.A21	53	54	FLASH.A20
FLASH.A19	55	56	FLASH.A18
FLASH.A17	57	58	FLASH.A16
FLASH.A15	59	60	FLASH.A14
FLASH.A13	61	62	FLASH.A12
FLASH.A11	63	64	FLASH.A10
FLASH.A9	65	66	FLASH.A8
FLASH.A7	67	68	FLASH.A6
FLASH.A5	69	70	FLASH.A4
FLASH.A3	71	72	FLASH.A2
FLASH.A1	73	74	nEX_CS3
nEX_CS4	75	76	FLASH_DIS
GND	77	78	GND
GND	79	80	GND

6.2 Connector B

Connector CB contains the serial buses such as SPI, McBSP, MCSI, and standard serial ports. Table 16 is the pin out of the B Connector.

Table 16. Connector B Pin out

Name	No.		Name
GND	1	2	GND
GND	3	4	GND
DC	5	6	DC
DC	7	8	DC
3.3V	9	10	3.3V
3.3V	11	12	3.3V
NC	13	14	NC
RTC_WAKE_INT	15	16	MCBSP1.FSX
MCSI1.SYNC	17	18	MCSI1.CLK
MCSI1.DIN	19	20	MCSI1.DOUT
MCSI2.SYNC	21	22	MCSI2.CLK
MCSI2.DIN	23	24	MCCS2.DOUT
BCLK	25	26	MCLK_REQ
BCLK_REQ	27	28	CLK32K_OUT
MCLK	29	30	MCBSP1.DX
MCBSP1.CLKS	31	32	MCBSP1.DR
NC	33	34	NC
MCBSP1.CLKX	35	36	MCBSP2.DR
MCBSP2.FSR	37	38	MCBSP2.CLKX
MCBSP2.DX	39	40	MCBSP2.CLKR
MCBSP2.FSX	41	42	UART3.TX
UART3.RX	43	44	UART1.RTS
UART1.Tx	45	46	UART1.CTS
UART1.RX	47	48	UART2.CTS
UART2.TX	49	50	UART2.RX
UART2.RTS	51	52	UART2.BCLK
UART1.DIS	53	54	BFAIL
USB_DM	55	56	RTC_ON_OFF
USB_DP	57	58	USB_PUEN
RESET_IN	59	60	nRESET_OUT
GPIO 4	61	62	GPIO 8
MCBSP3.CLKX	63	64	GPIO 11
MPUI04	65	66	MPUI03
JTAG_DIS	67	68	GPIO62
nTRST	69	70	TMS
TDI	71	72	nEMU0
nEMU1	73	74	TCK
RTCK	75	76	TDO
GND	77	78	GND
GND	79	80	GND

6.3 Connector C

Connector C contains the camera, LCD, GPIO, I2C, and GPIO pins. **Table 17** is the pin out of the C Connector

Table 17. Connector C Pin out

Name	No.		Name
GND	1	2	GND
GND	3	4	GND
DC	5	6	DC
DC	7	8	DC
3.3V	9	10	3.3V
3.3V	11	12	3.3V
NC	13	14	NC
GPIO7	15	16	GPIO 3
GPIO2	17	18	GPIO 6
GPIO 9	19	20	GPIO 13
GPIO 12	21	22	GPIO 15
GPIO14	23	24	MPUIO2
MPUIO1	25	26	CAM.EXCLK
CAM.D0	27	28	CAM.D1
CAM.D2	29	30	CAM.D3
CAM.D4	31	32	CAM.D5
CAM.D6	33	34	CAM.D7
CAM.LCLK	35	36	CAM.HS
CAM.VS	37	38	CAM.RST
I2C.SDA	39	40	I2C.SCL
LCD.P0	41	42	LCD.P1
LCD.P2	43	44	LCD.P3
LCD.P4	45	46	LCD.P5
LCD.P6	47	48	LCD.P7
LCD.P8	49	50	LCD.P9
LCD.P10	51	52	LCD.P11
LCD.P12	53	54	LCD.P13
LCD.P14	55	56	LCD.P15
LCD.PCLK	57	58	LCD.AC
LCD.VS	59	60	LCD.HS
KB.C0	61	62	KB.C1
KB.C2	63	64	KB.C3
KB.C4	65	66	KB.C5
KB.R0	67	68	KB.R1
KB.R2	69	70	KB.R3
KB.R4	71	72	UWIRE.SDI
UWIRE.CS0	73	74	UWIRE.CS3
UWIRE.SDO	75	76	UWIRE.SCLK
GND	77	78	GND
GND	79	80	GND

6.4 Connector D

The D connector is mainly reserved for future expansion to allow other cards that meet the TM form factor, but need additional signal to be routed to Expansion cards or the ADM. **Table 18** is the pin out of the D connector.

Table 18. Connector D Pin out

Name	No.		Name
GND	1	2	GND
GND	3	4	GND
DC	5	6	DC
DC	7	8	DC
3.3V	9	10	3.3V
3.3V	11	12	3.3V
	13	14	
GND	15	16	VLYNQ.TX1
GND	17	18	VLYNQ.TX0
GND	19	20	VLYNQ.CLK
GND	21	22	VLYNQ.RX1
GND	23	24	VLYNQ.RX0
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	
	35	36	
	37	38	
	39	40	
	41	42	
	43	44	
	45	46	
	47	48	
	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	
	69	70	
	71	72	
	73	74	
	75	76	
GND	77	78	GND
GND	79	80	GND

6.5 Connector Specification

The Expansion connectors are a Hirose FX2 series 1.27mm pitch connector. This is required due to the minimum height restrictions from board to board. This connector and the mating connector will give a .484”(12.3mm) spacing between cards. **Figure 42** is a picture of the connector.

Figure 41. Expansion Connector

Each connector has 2 rows with 40 pins per row. The Hirose part number for the connector is FX2-80P-1.27SV. The TM uses the header part. The connector is a surface mount device. Surface mount connectors are required for the Expansion cards to allow for connectors to be placed on both sides of the board and still be aligned with each other.

7.0 I/O Connectors

This section defines the pin outs of each of the I/O connectors on the OMAP5912 TM.

7.1.1 Serial

Table 19 defines the pin out of the DB9 connector on the TM.

Table 19. Serial Connector Pin out

Description	Name	No.		Name	Description
		1	2	RX	Receive Input
Transmit Output	TX	3	4		
Ground	GND	5	6		
		7	8		
			9		

All other pins on the DB9 connector are not connected.

7.1.2 Ethernet

Table 20 defines the pin out of the RJ45 connector.

Table 20. Ethernet Pin out

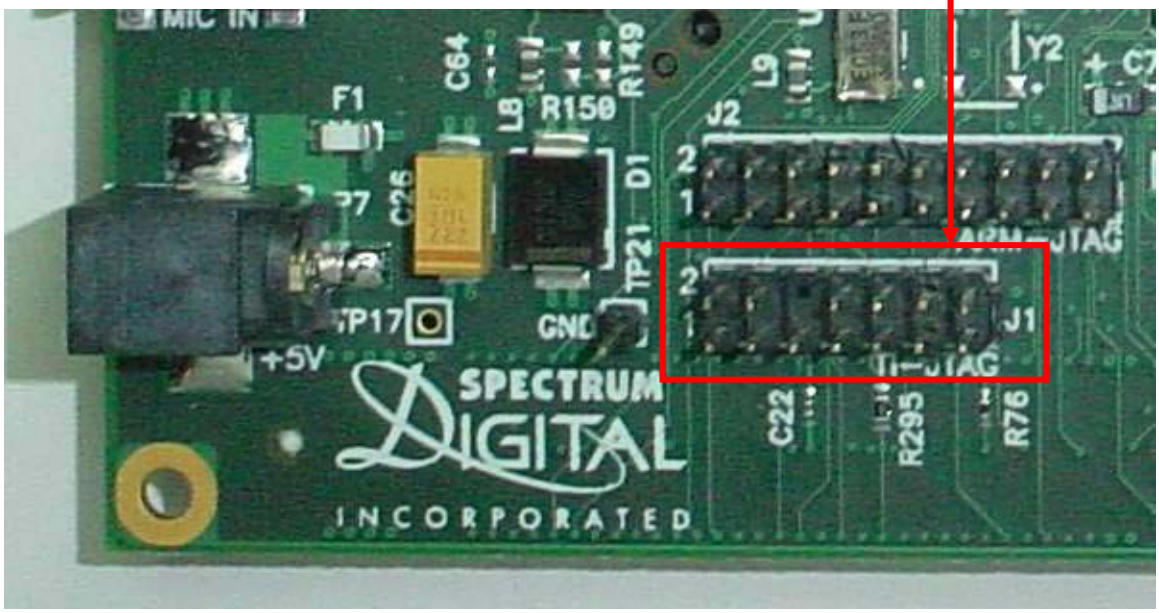
No.	Name	Description
1	TX+	Plus side of transmit pair
2	TX-	Minus side of receive pair
3	RX+	Plus side of receive pair
4		
5		
6	RX-	Minus side of receive pair.
7		
8		

7.1.3 JTAG

Table 21 defines the pin out of the JTAG connector on the TM.

Table 21. JTAG Pinout

Name	No.		Name
TMS	1	2	TRST
TDI	3	4	GND
3.3V	5	6	NC
TDO	7	8	GND
TCKR	9	10	GND
TCK	11	12	GND
EMU0	13	14	EMU1



7.1.4 MultiICE

Figure 42 is the pin out of the MultiICE connector.

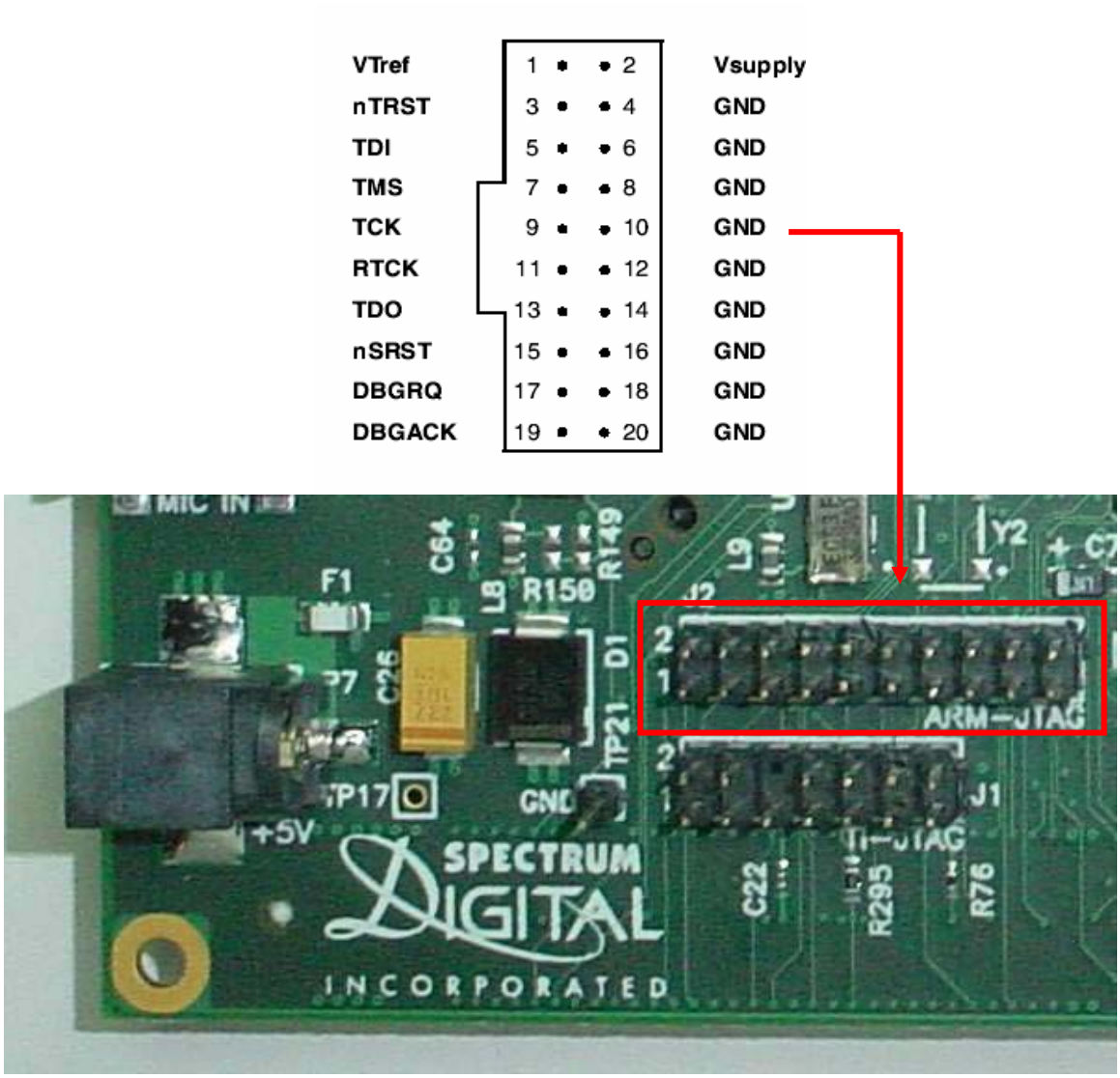


Figure 42. MultiICE Connector Pin out

7.1.5 DC Power

Figure 43 shows the pin configuration of the DC connector on the 5912 TM.

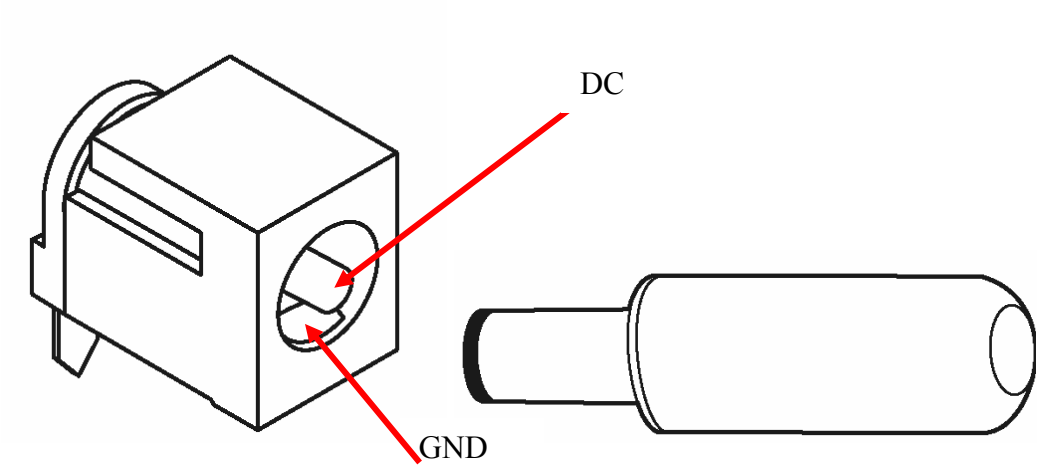


Figure 43. DC Power Jack Pin out

7.1.6 Compact Flash

Table 22 is the pin out of the Compact Flash connector.

Table 22. Compact Flash Connector Pin out

Function						Function	
Mem	I/O		Pin			Mem	I/O
GND		---	1	26	-->	nCD1	
D03		<-->	2	27	<-->	D11	
D04		<-->	3	28	<-->	D12	
D05		<-->	4	29	<-->	D13	
D06		<-->	5	30	<-->	D14	
D07		<-->	6	31	<-->	D15	
nCE1		-->	7	32	<--	nCE2	
A10		-->	8	33	-->	nVS1	
!OE		-->	9	34	<--	NU	nIORD
A09		-->	10	35	<--	NU	nIOWR
A08		-->	11	36	<--	nWE	
A07		-->	12	37	-->	RDY/BSY	IREQ
VCC		---	13	38	---	VCC	
A06		-->	14	39	<--	nCSEL	
A05		-->	15	40	-->	nVS2	
A04		-->	16	41	<--	RESET	
A03		-->	17	42	-->	nWAIT	
A02		-->	18	43	-->	NU	nINPACK
A01		-->	19	44	<--	nREG	
A00		-->	20	45	<-->	BVD2(H)	nSPKR
D00		<-->	21	46	<-->	BVD1(H)	!STSCHG
D01		<-->	22	47	<-->	D08	
D02		<-->	23	48	<-->	D09	
WP	!IOIS16	-->	24	49	<-->	D10	
nCD2		<--	25	50	---	GND	

Figure 45 is the mechanicals of the CF connector used on the TM.

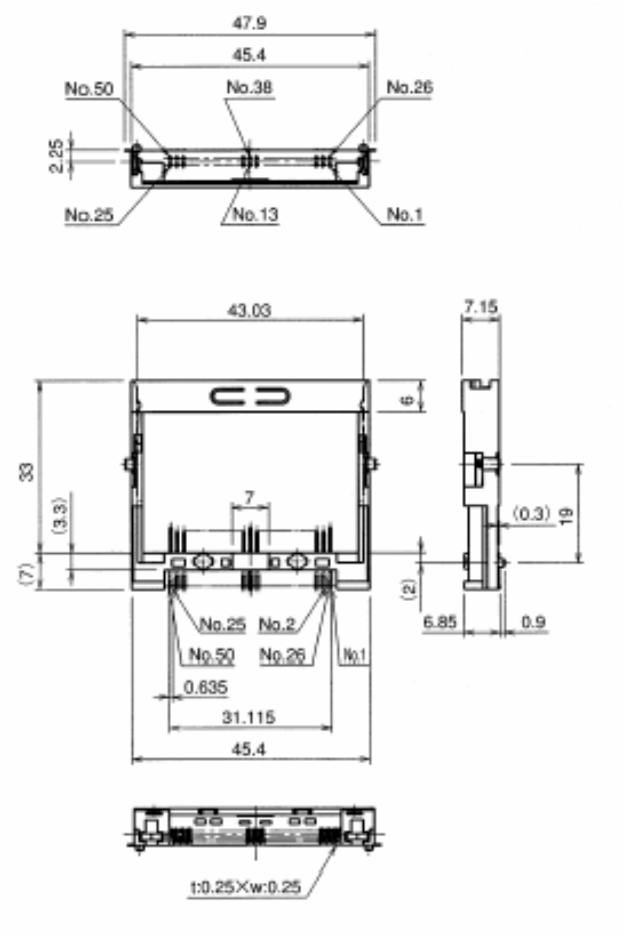


Figure 44. Compact Flash Connector

7.1.7 Headphones

Table 23 is the pin out of the headphone jack. Figure 46 gives the locations of the pin numbers.

Table 23. Headphone Pin out

Description	Name	No.
Left Channel Out	Left	1
		2
		3
Right Channel Out	Right	4
Ground	GND	5

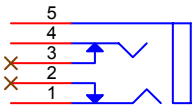


Figure 45. Headphone Pin out

7.1.8 Line In

Table 24 is the pin out of the Lin In jack on the TM. **Figure 47** gives the pin out of the connector.

Table 24. Line In Pin out

Description	Name	No.
Left Channel In	Left In	1
		2
		3
Right Channel IN	Right In	4
Ground	GND	5

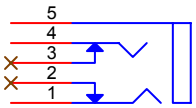


Figure 46. Line In Pin out

7.1.9 Microphone In

Table 25 is the pin assignments for the Microphone input jack. **Figure 48** gives the pin out of the connector.

Table 25. Microphone Input Pin out

Description	Name	No.
Ground	GND	1
Microphone In	MIC In	2
		3
		4
		5

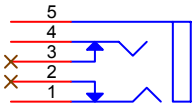


Figure 47. Microphone Jack Pin out

7.1.10 USB Host

Table 26 gives the pin out of the USB host connector.

Table 26. USB Host Pinout

Description	Name	No.
+5 volt power output.	+5V	1
Negative polarity data	-DATA	2
Positive polarity data	+DATA	3
Ground	GND	4

7.1.11 USB Client Adapter

Figure 49 is the adapter used to convert the Host interface to the Client interface.

Figure 48. USB Client Adapter

This adapter is made by Video Products Inc.

Part Number	Description	UPC Code
USBAF-USBBF	USB Adapter & Gender Changers : USB A Female to B Female Adapter	

It can be purchased at www.vpi.us

8.0 Mechanical Specifications

This section defines the physical requirements for each of the card types. At this point, these dimensions are preliminary and subject to change.

8.1.1 TM Card

This section defines the mechanical dimensions and configuration of the TM Card. The exact dimensions of the TM are subject to change based on the final layout of the PCB. **Figure 50** gives the general outline and component placement of the TM from the top side.

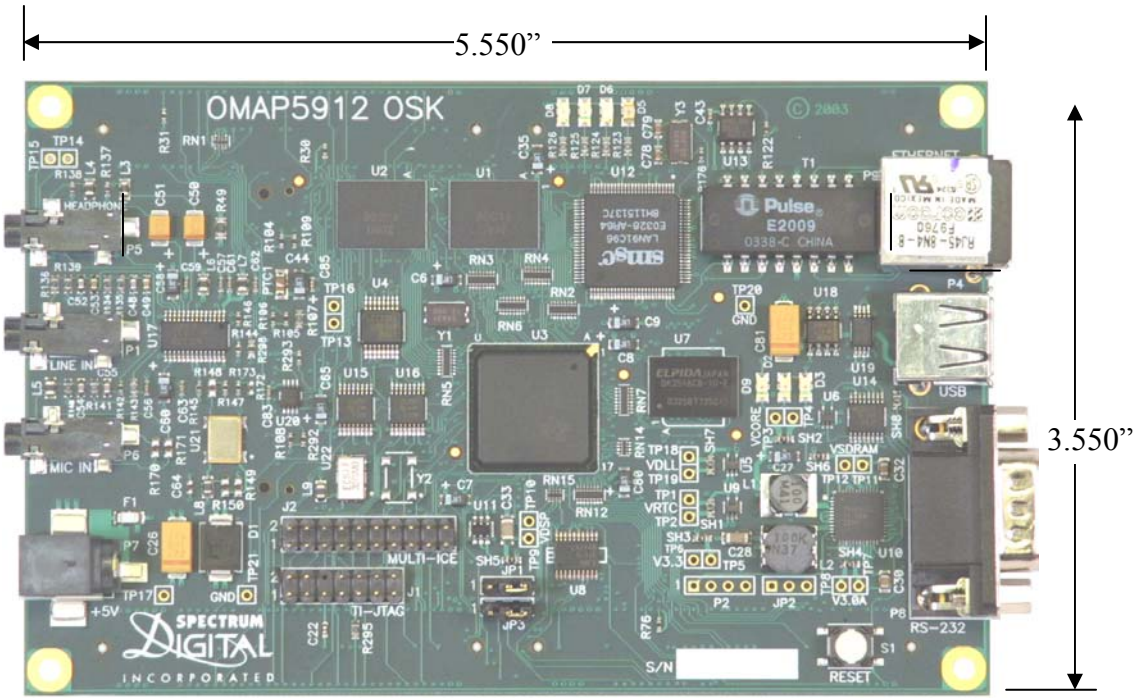


Figure 49. OMAP5912 TM Top Side

Figure 51 shows the TM form the back side.

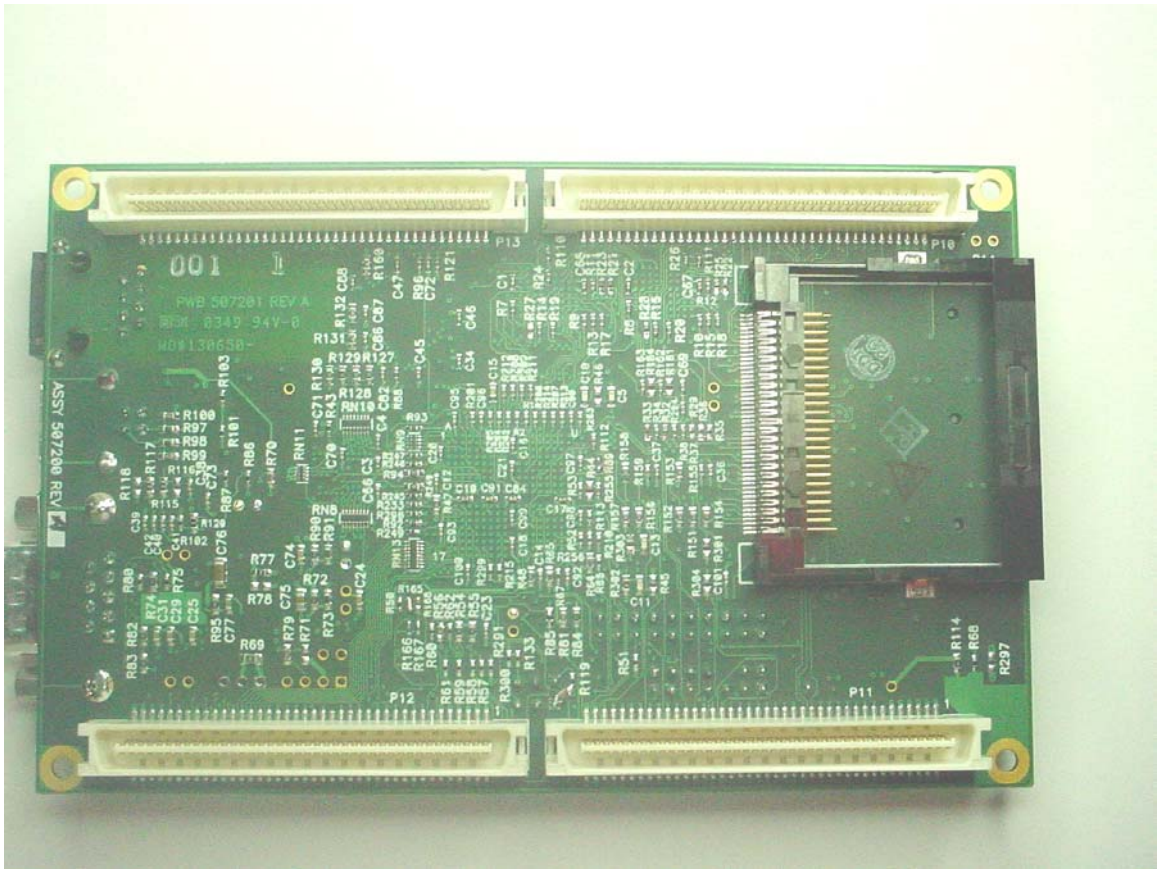


Figure 50. OMAP5912 TM Back Side

9.0 Component Locations

This section describes where on the board the different components of the board can be found.

9.1 Key Components

Figure 52 shows the key components on the top side of the OMAP5912 TM.

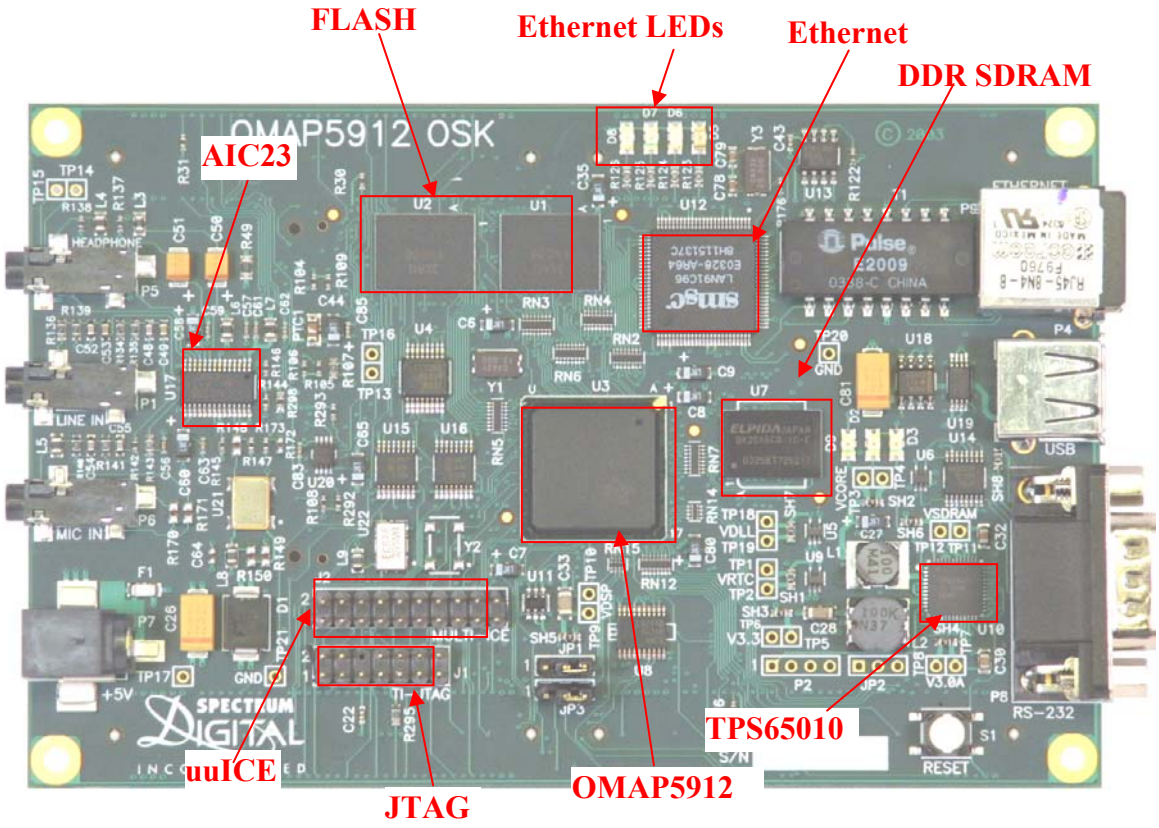


Figure 51. Key Top Side Components

9.2 Connectors and Jumpers

Figure 53 defines the connectors and jumpers for the TM.

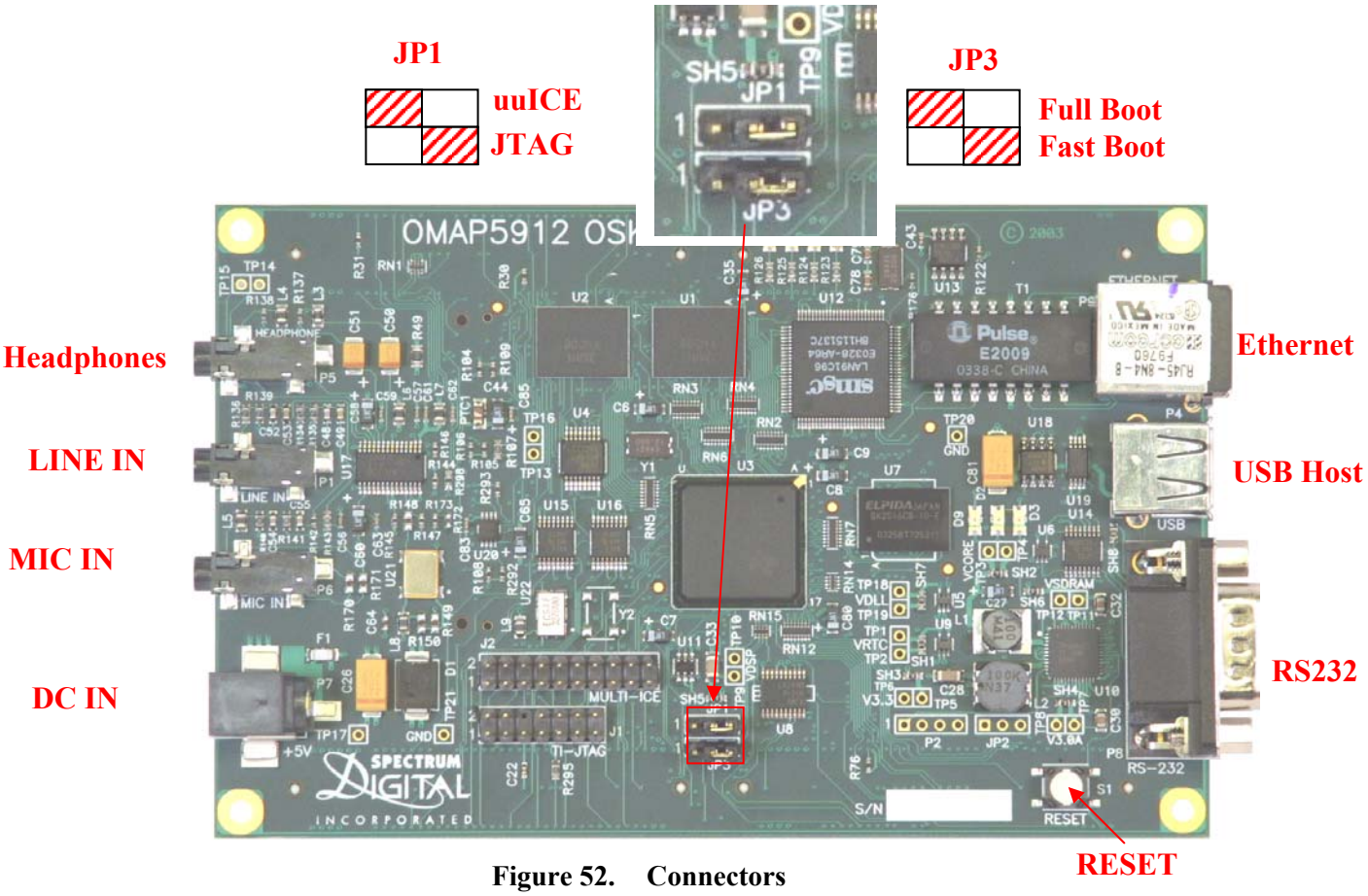


Figure 52. Connectors

9.3 Indicators

Figure 54 shows the placement of the indicators on the board.

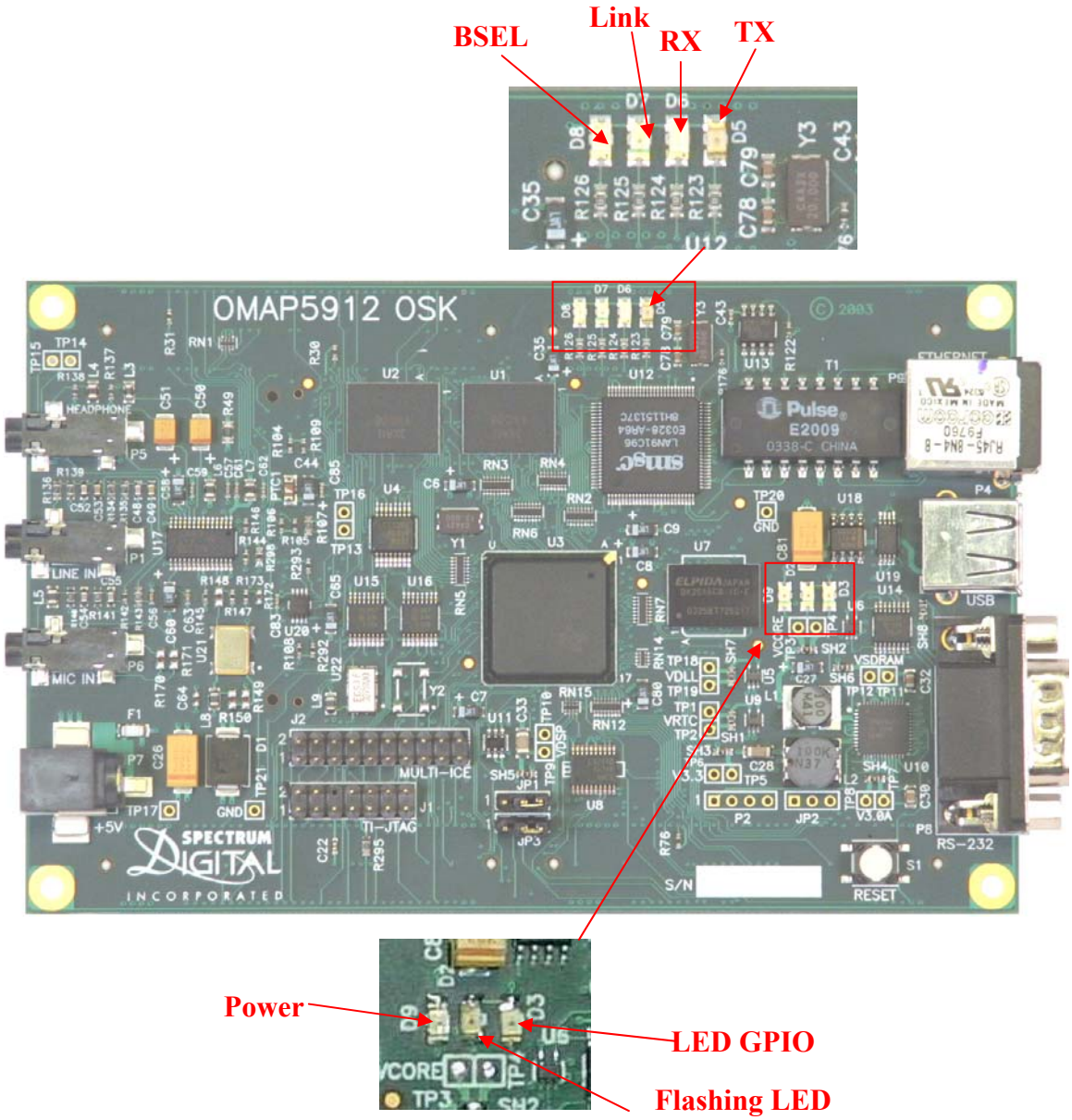
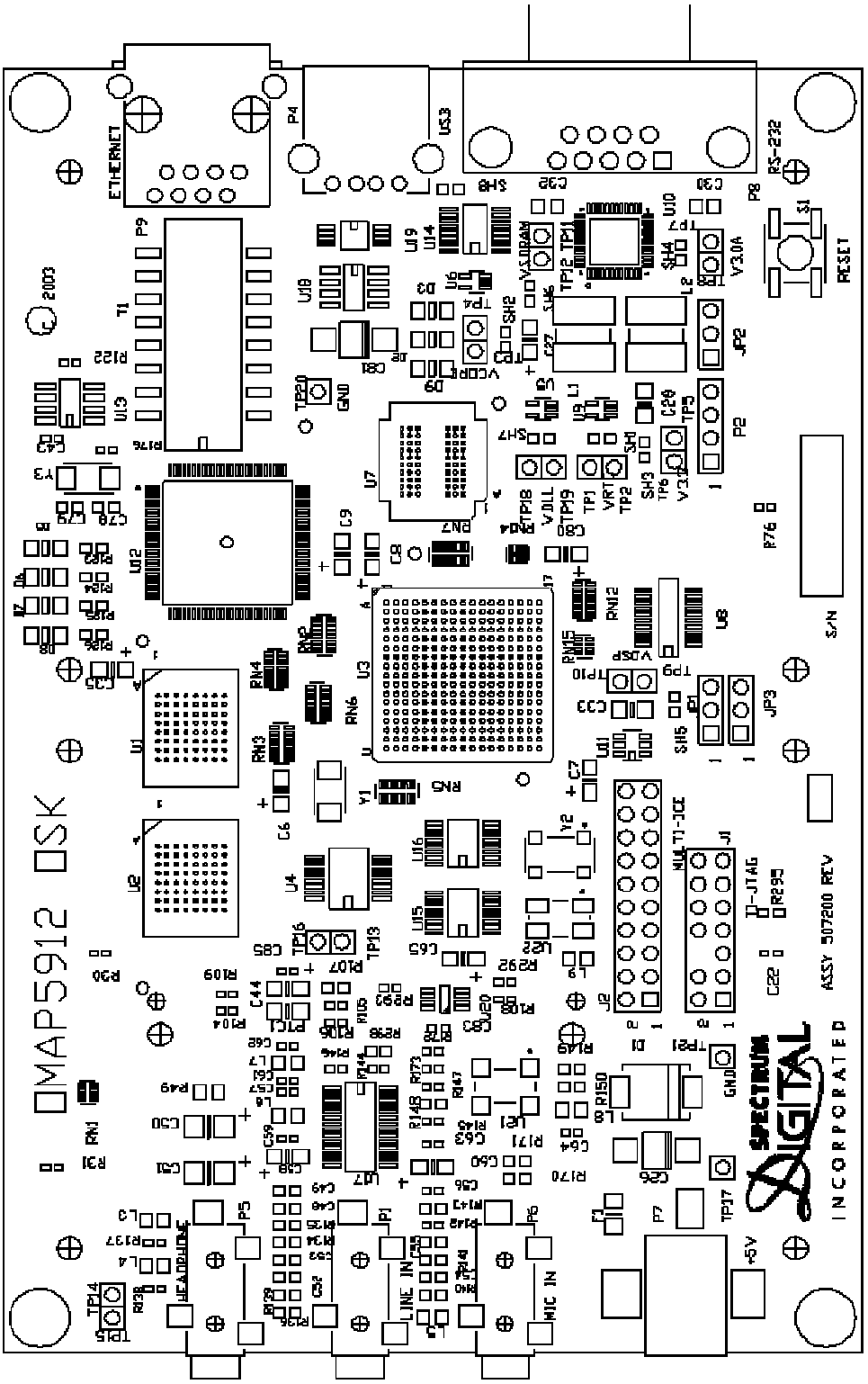
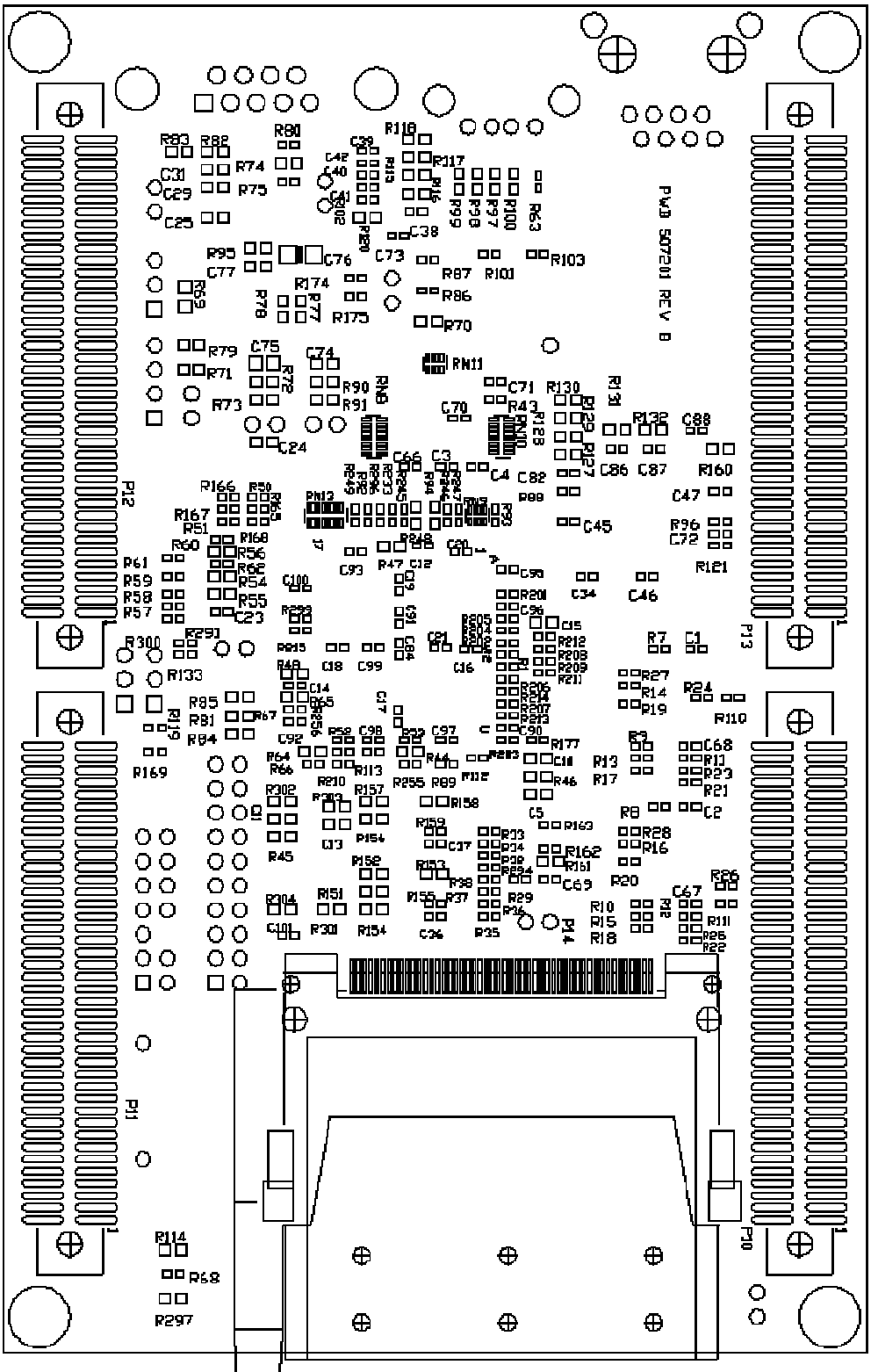


Figure 53. Indicators

Appendix A- Component Locations

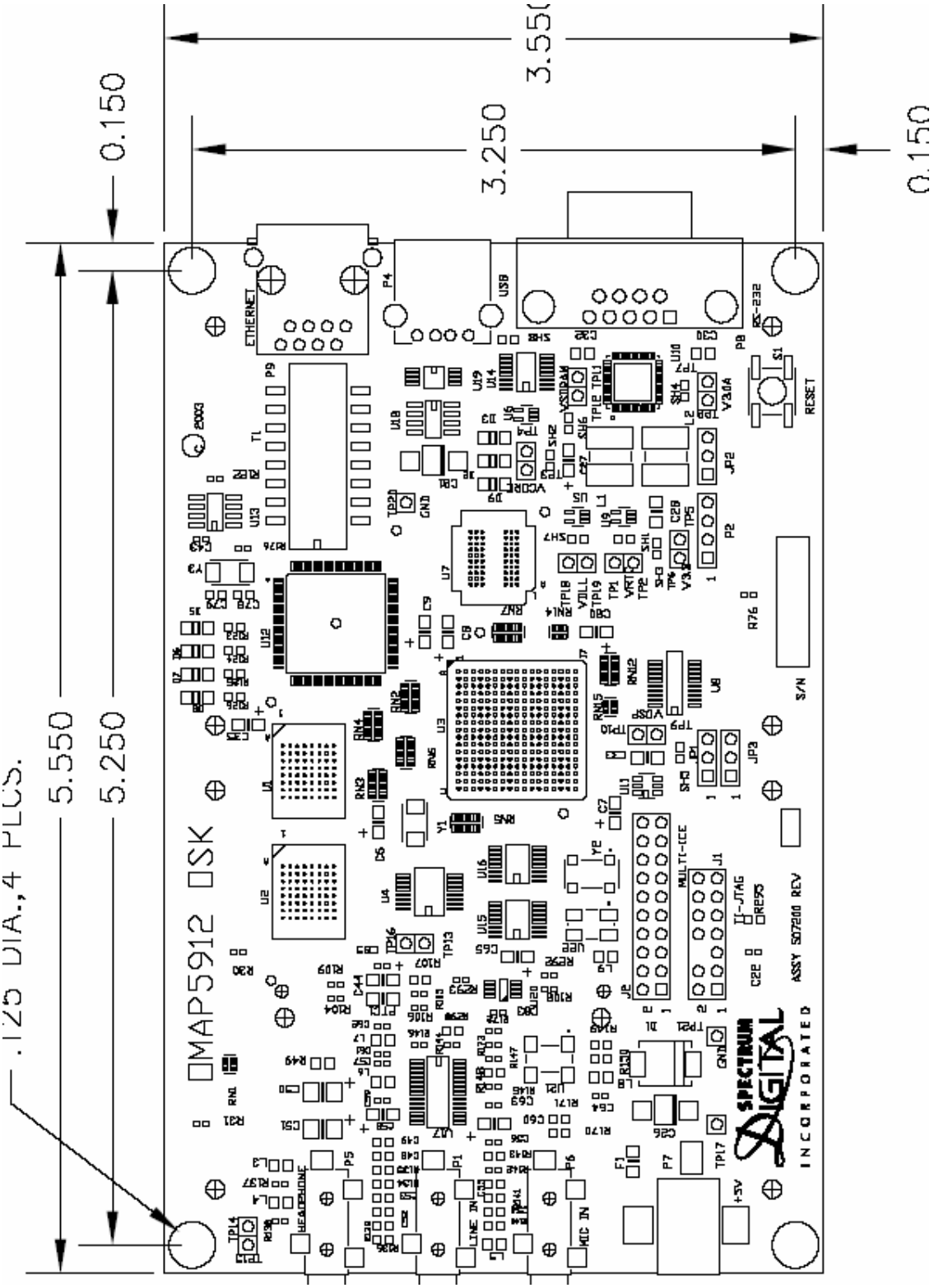


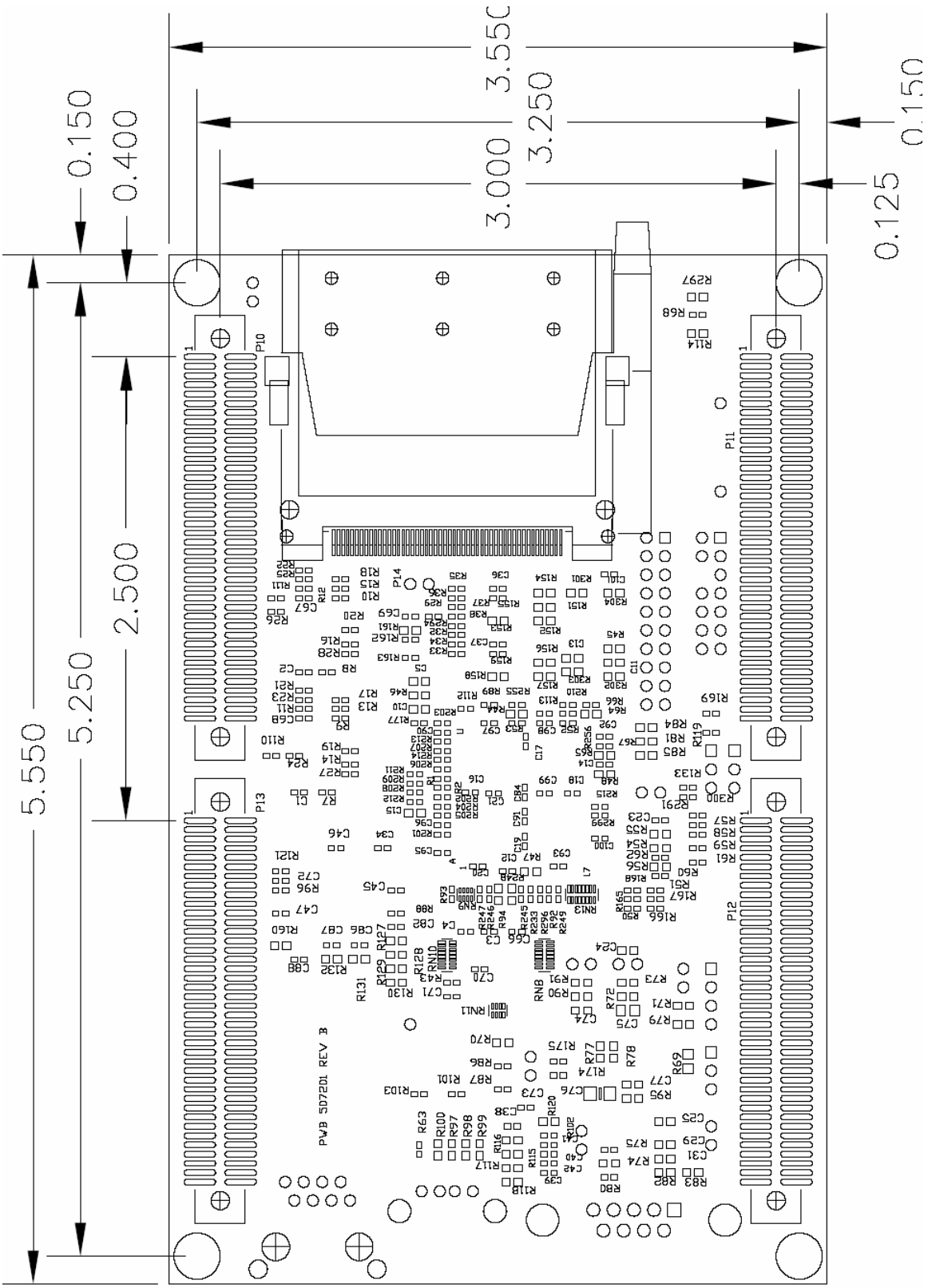
TOP SIDE COMPONENT LOCATIONS



BOTTOM SIDE COMPONENT LOCATIONS

Appendix B- Board Dimensions




0.150
0.400
2.500
5.250
5.550
3.000
3.250
3.550
0.125
0.150
PWB SD72D1 REV B

Appendix C- Schematics

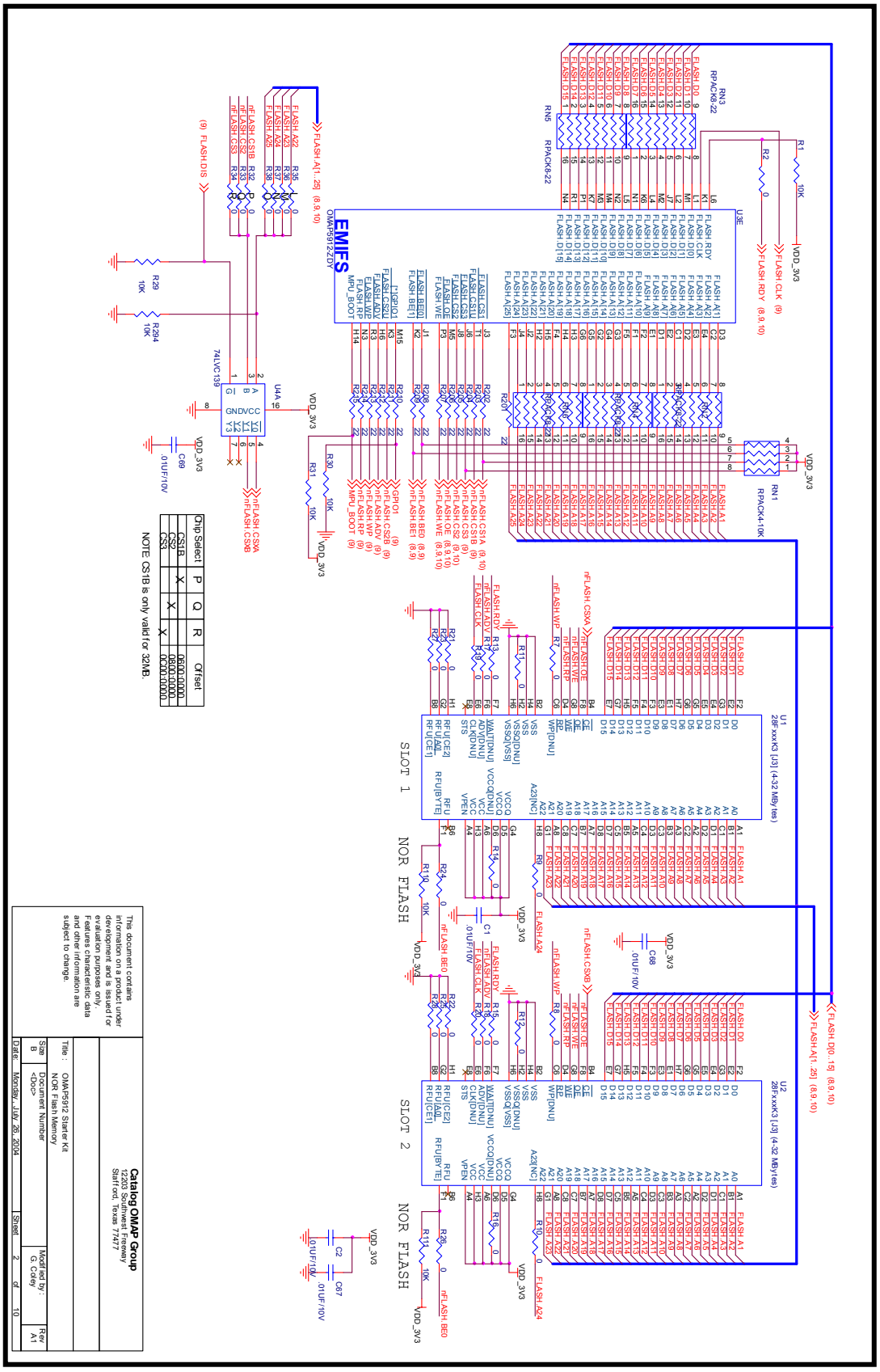
Version	Date	Author	Notes
A	5/11/04	G. Coley	Revision A release.
A1	7/26/04	G. Coley	Updated Symbol to official symbol. Make corrections for a few typos.

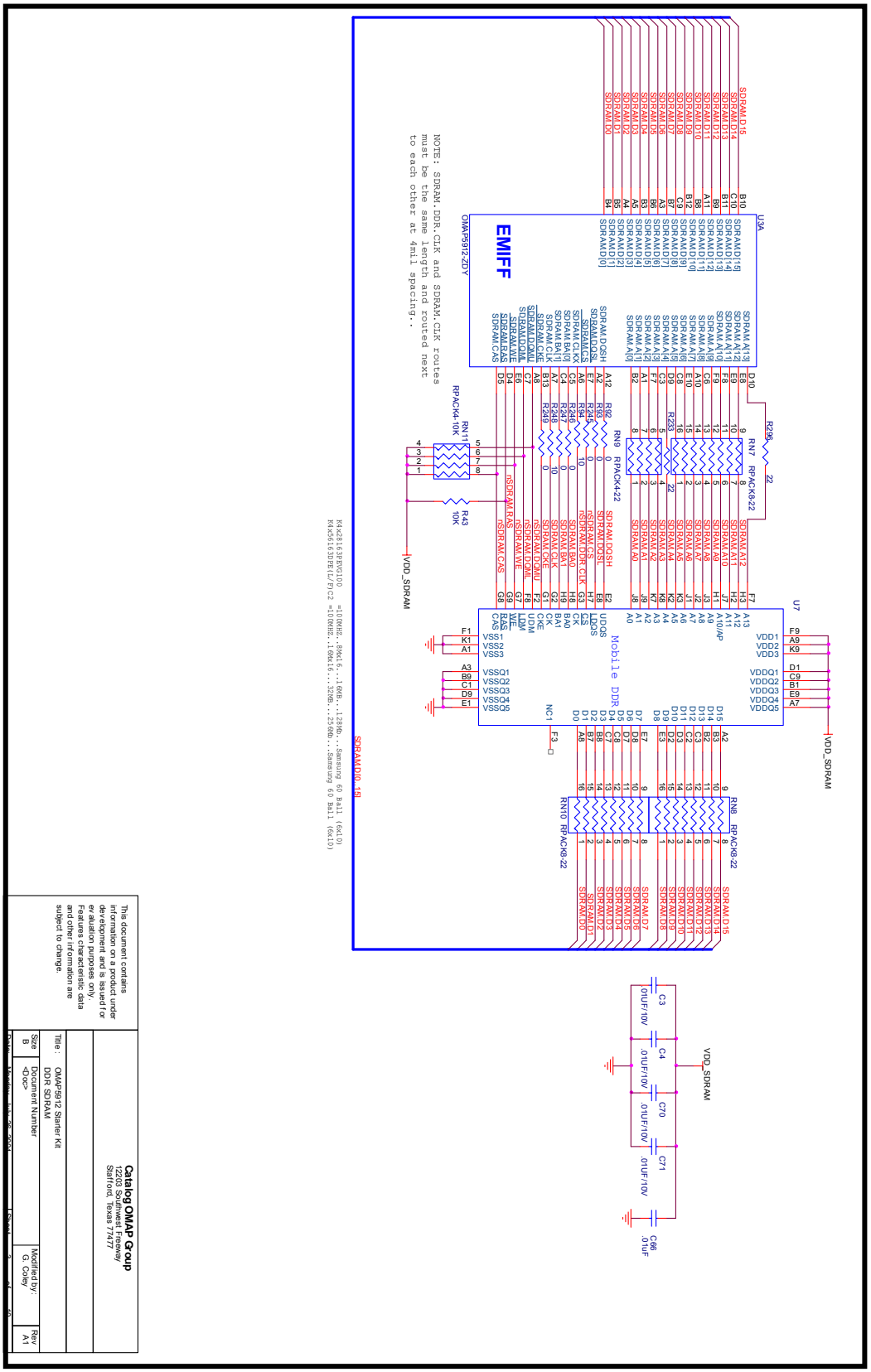
NOTES:

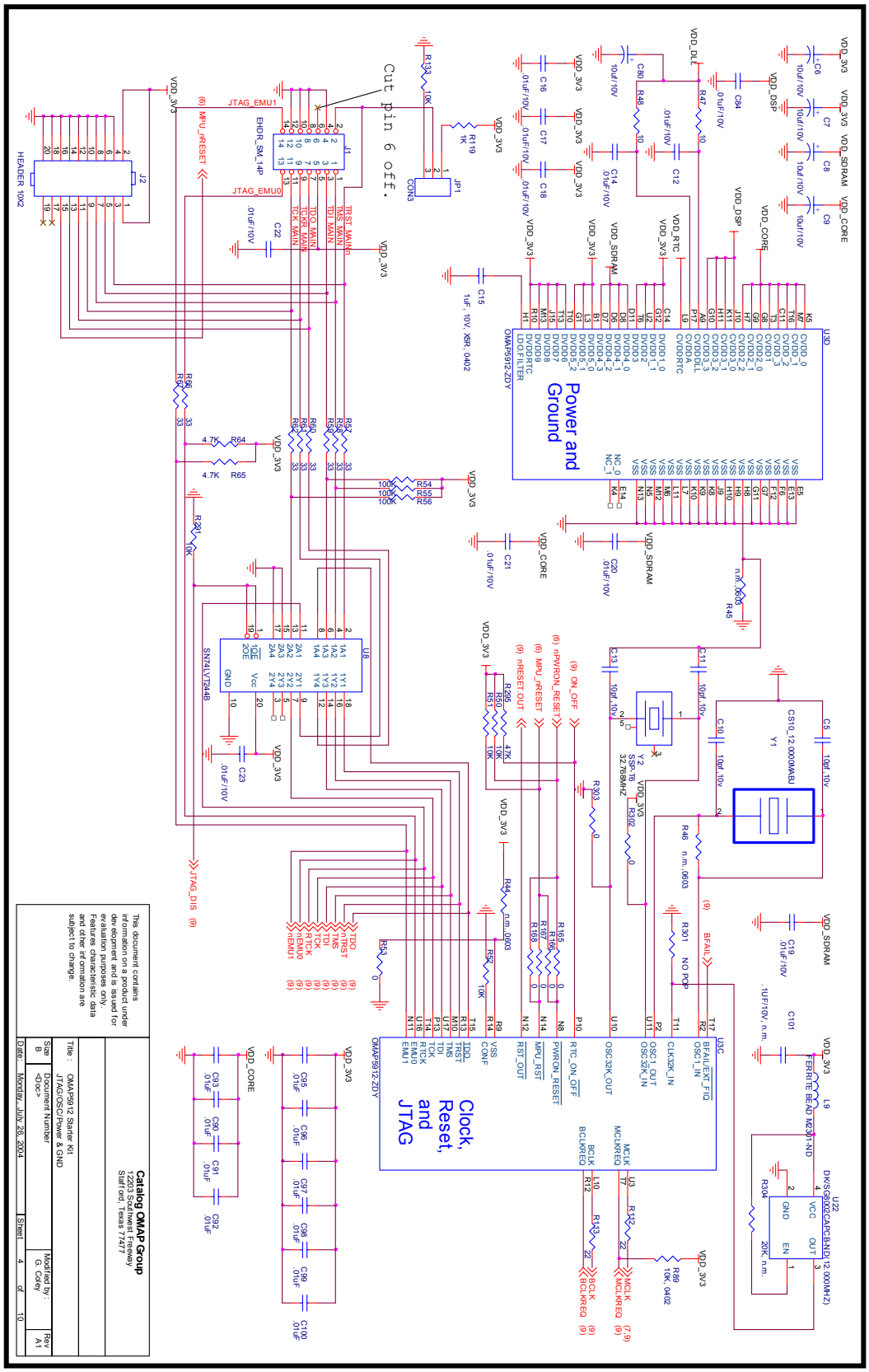
1. All resistors are in the 0402 package unless otherwise specified.
2. There is an ESD ring around the outer edges of the board on the top and bottom side.
3. The ESD ring is connected to the standoffs and extends around the edge of the board.

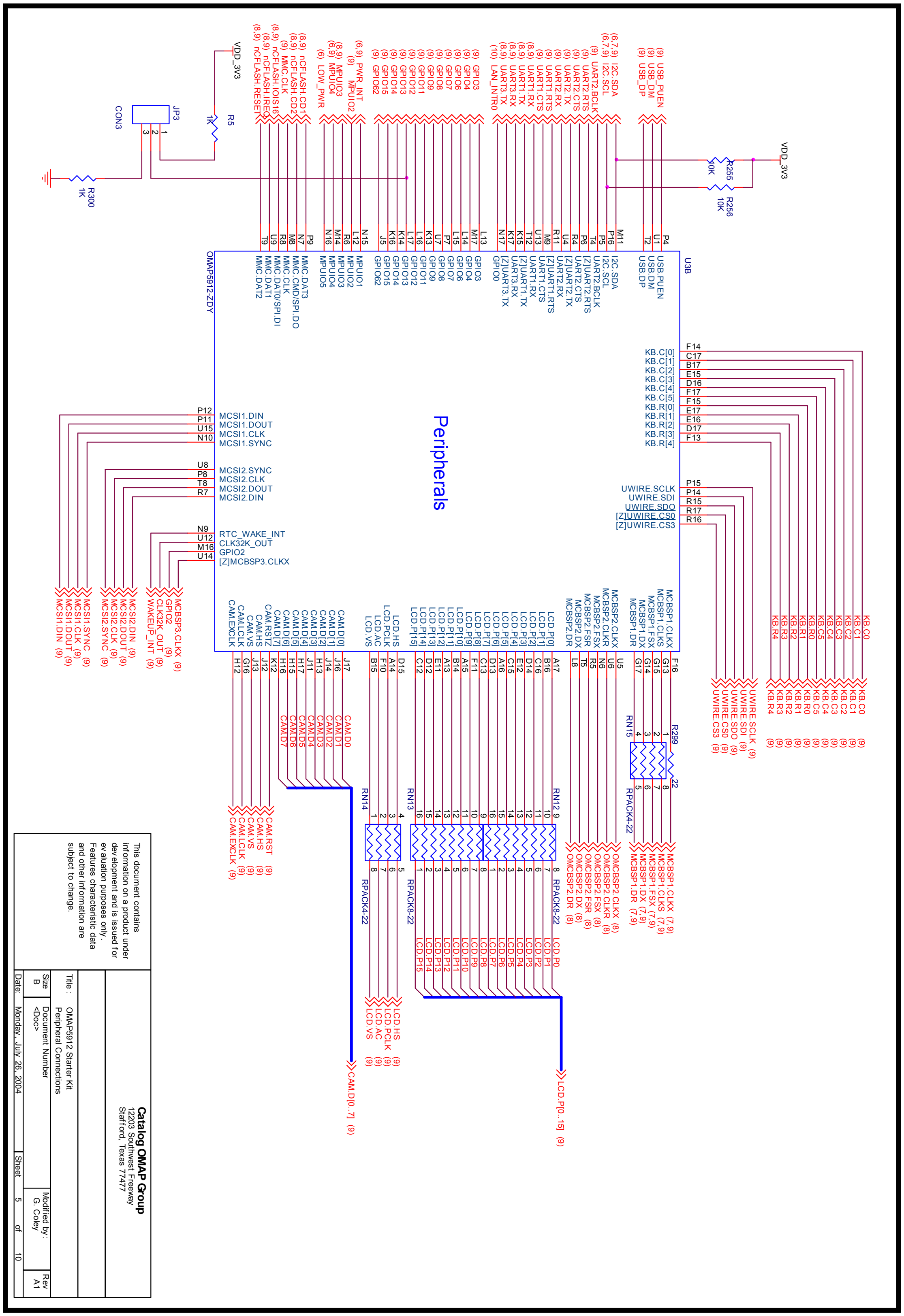
Catalog OMAP Group
12203 Southwest Freeway
Stafford, Texas 77477

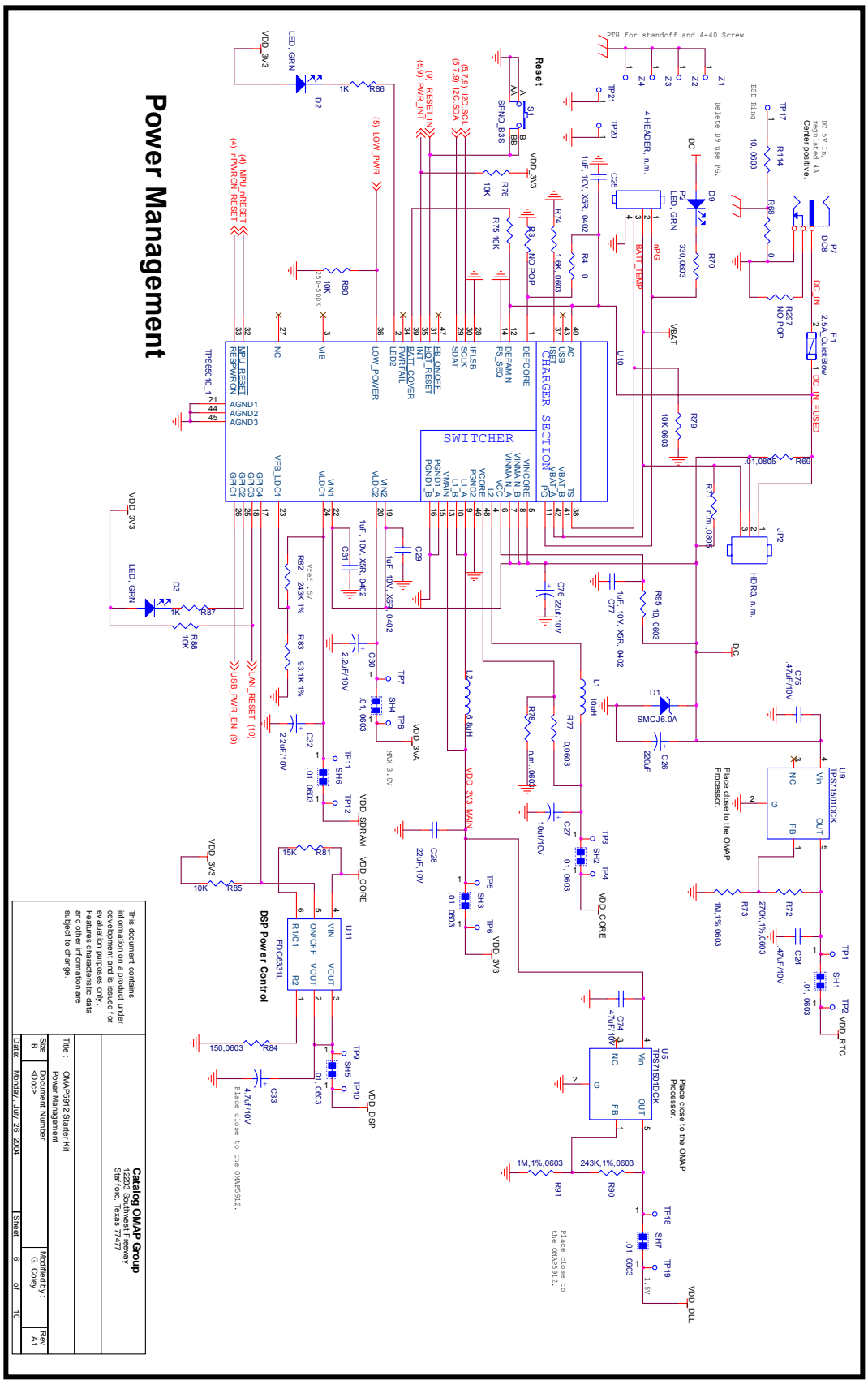
Title : OMAP5912 Starter Kit
Notes Page
Size: B | Document Number | Modified by: G. Coley | Rev: A1
Date: Monday, July 26, 2004 | Sheet 1 of 10

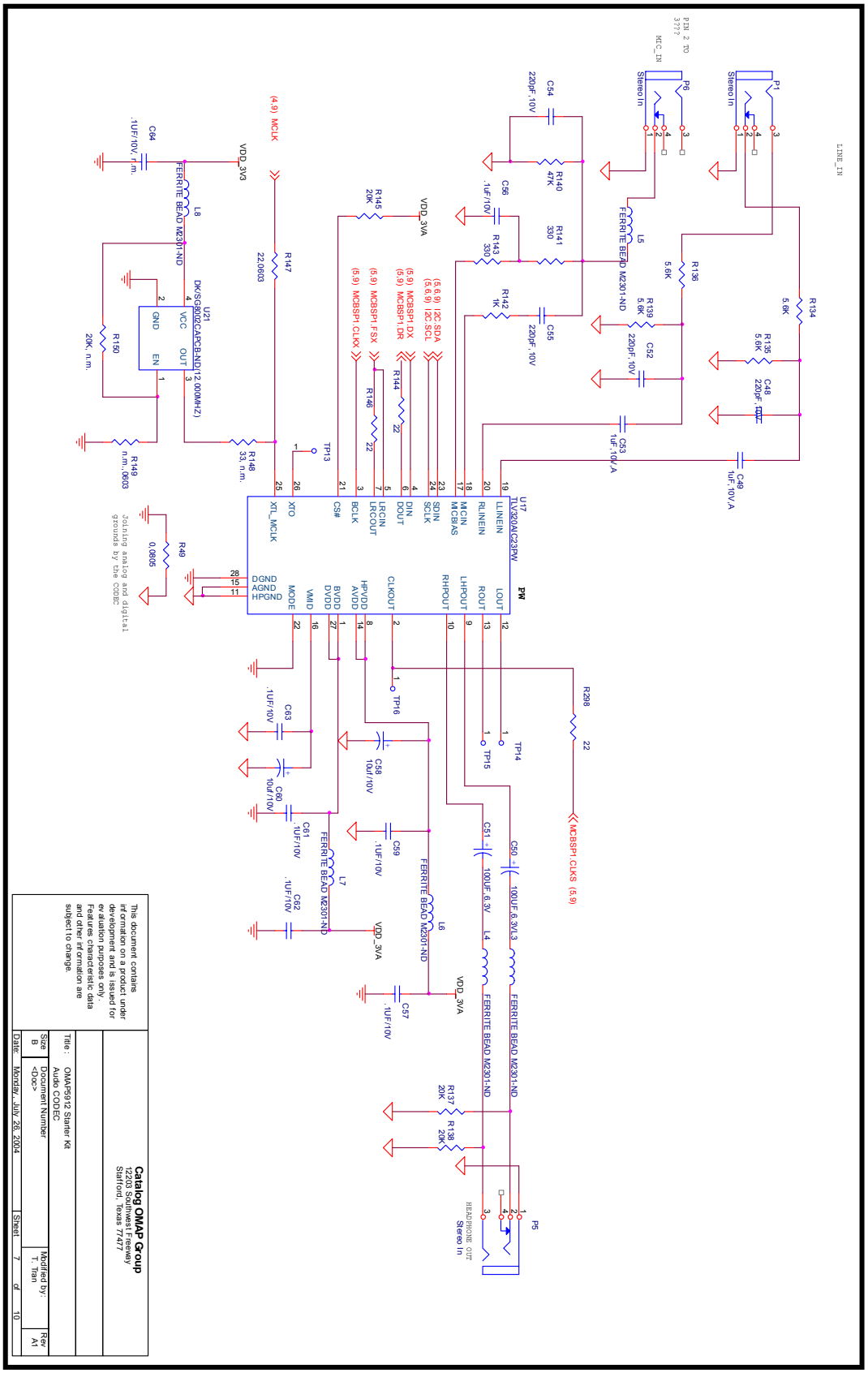

EMIFS
OMAP5912-ZDY
U3E
RN3
RPACK8-22
RN5
RPACK8-22
RN1
RPACK4-10K
U4A
74LVC139
U1
28Fxxxk3 [U3] (4-32 Mbytes)
SLOT 1
NOR FLASH
SLOT 2
NOR FLASH
Chip Select
CS1B
CS2
CS3
Offset
0800.0000
0C00.0000
1000.0000
NOTE: CS1B is only valid for 32MB.
Catalog OMAP Group
12203 Southwest Freeway
Stafford, Texas 77477
This document contains information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.
Title : OMAP5912 Starter Kit
NOR Flash Memory
Size B
Document Number <Doc>
Modified by: G.Coley
Rev A1
Date: Monday, July 26, 2004
Sheet 2 of 10

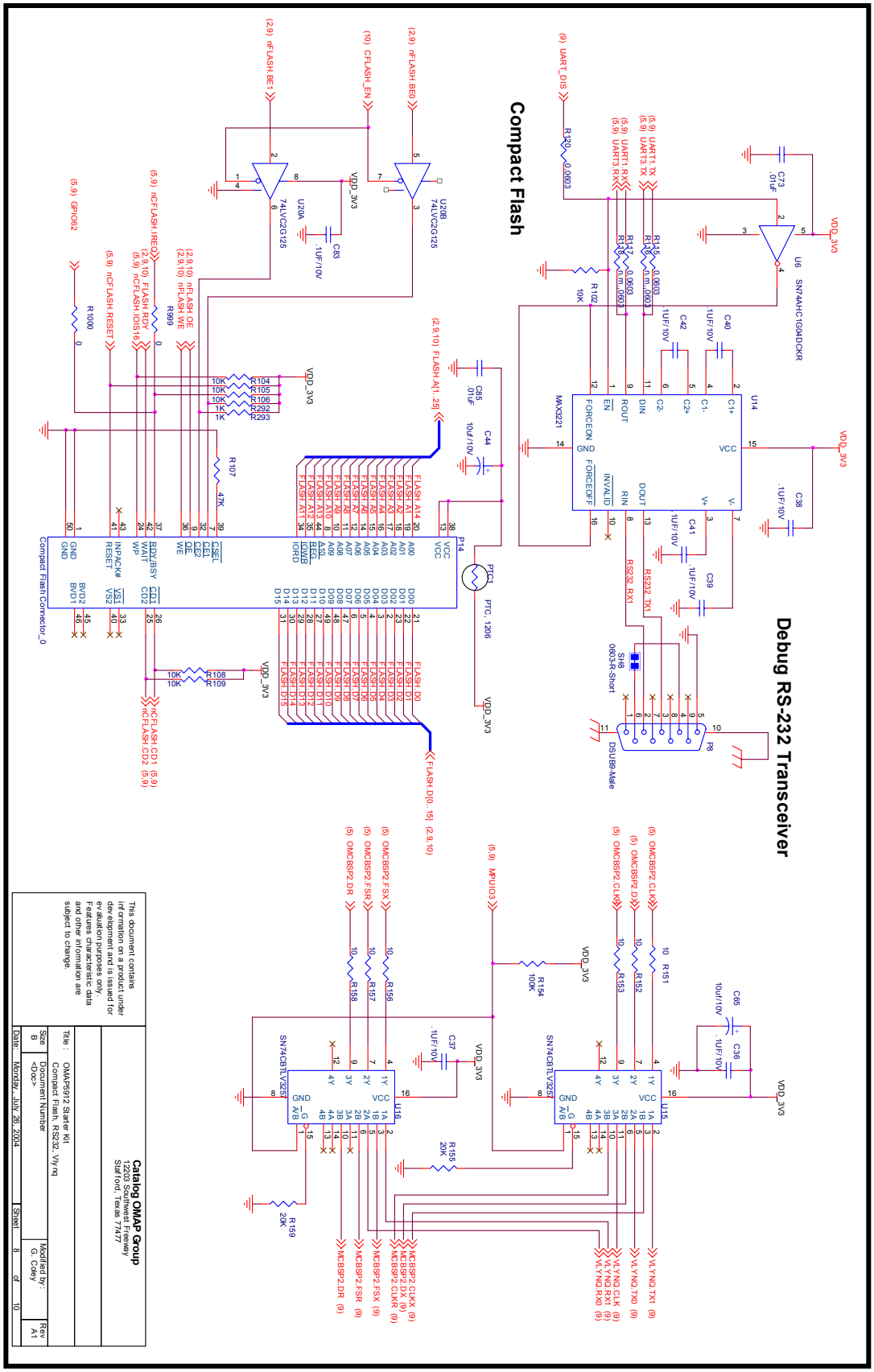

EMIFF
OMAP5912-ZDY
U3A
NOTE: SDRAM.DDR.CLK and SDRAM.CLK routes must be the same length and routed next to each other at 4mil spacing..
Mobile DDR
VDD_SDRAM
SDRAM.D[15..0]
Catalog OMAP Group
12203 Southwest Freeway
Stafford, Texas 77477
This document contains information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.
Title: OMAP5912 Starter Kit DDR SDRAM
Size: B
Document Number: <Doc>
Modified by: G. Daley
Rev: A1


Power and Ground
Clock, Reset, and JTAG
Cut pin 6 off.
Catalog OMAP Group
12203 Southwest Freeway
Stafford Texas 77477
Title : OMAP5912 Starter Kit
JTAG/OSC/ Power & GND
Document Number
<Doc>
Modified by : G. Coley
Monday, July 26, 2004
Sheet 4 of 10
Rev A1


Peripherals
U3B
OMAP5912-ZDY
This document contains information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.
Catalog OMAP Group
12203 Southwest Freeway
Stafford, Texas 77477
Title: OMAP5912 Starter Kit Peripheral Connections
Size B
Document Number <Doc>
Modified by: G. Coley
Rev A1
Date: Monday, July 26, 2004
Sheet 5 of 10


Power Management
DSP Power Control
SWITCHER
CHARGER SECTION
Catalog OMAP Group
12203 Southwest Freeway
Stafford, Texas 77477
Title : OMAP5912 Starter Kit
Power Management
Document Number: <Doc>
Rev A1
Sheet 6 of 10
Date: Monday, July 26, 2004
Modified by: G. Coley


LINE_IN
MIC_IN
Stereo In
P1
P6
P5
HEADPHONE OUT
Stereo In
R134 5.6K
R135 5.6K
R136 5.6K
R139 5.6K
C48 220pF .10V
C52 220pF .10V
C53 1uF .10V,A
C49 1uF .10V,A
C54 220pF .10V
R140 47K
R141 330
R142 1K
R143 330
C56 .1uF/10V
C55 220pF .10V
L5 FERRITE BEAD M2301-ND
R145 20K
R144 22
R146 22
R147 22.0603
R148 33, n.m.
R149 n.m. .0603
R150 20K, n.m.
C64 .1UF/10V, n.m.
L8 FERRITE BEAD M2301-ND
U21 DK(SG532CAPCB-ND(13.000MHZ)
VDD_3V3
VDD_3VA
(4.9) MCLK
(5.9) MCBSP1.FSX
(5.9) MCBSP1.CLKX
(5.9) MCBSP1.DX
(5.9) MCBSP1.DR
(5.6.9) I2C SDA
(5.6.9) I2C SCL
TP13
U17 TLV320AIC23IPW
XTO XTI_MCLK
LLINEIN RLINEIN
MICIN MICBIAS
SDIN SCLK
DIN DOUT
LRCIN LRCOUT
CS# BCLK
LOUT ROUT
LHPOUT RHPOUT
CLKOUT
HPVDD AVDD
BVDD DVDD
VMID MODE
DGND AGND HPGND
R49 0.0805
Joining analog and digital grounds by the CODEC
C63 .1UF/10V
C60 10uF/10V
C61 .1UF/10V
C62 .1UF/10V
C58 10uF/10V
C59 .1UF/10V
C57 .1UF/10V
L7 FERRITE BEAD M2301-ND
L6 FERRITE BEAD M2301-ND
TP16
TP15
TP14
R298 22
MCBSP1.CLKS (5.9)
C51 100UF 6.3V
C50 100UF 6.3V
L3 FERRITE BEAD M2301-ND
L4 FERRITE BEAD M2301-ND
R137 20K
R138 20K
This document contains information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.
Catalog OMAP Group
12203 Southwest Freeway
Stafford, Texas 77477
Title : OMAP5912 Starter Kit
Audio CODEC
Size B
Document Number <Doc>
Rev A1
Date: Monday, July 26, 2004
Sheet 7 of 10
Modified by: T. Tran


Compact Flash
Debug RS-232 Transceiver
Compact Flash Connector_0
MAX3221
SN74AHC1G04DCKR
SN74CBTLV3257
74LVC2G125
DSUB9-Male
SH6 0603-R-Short
PTC, 1206
Catalog OMAP Group
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Stafford, Texas 77477
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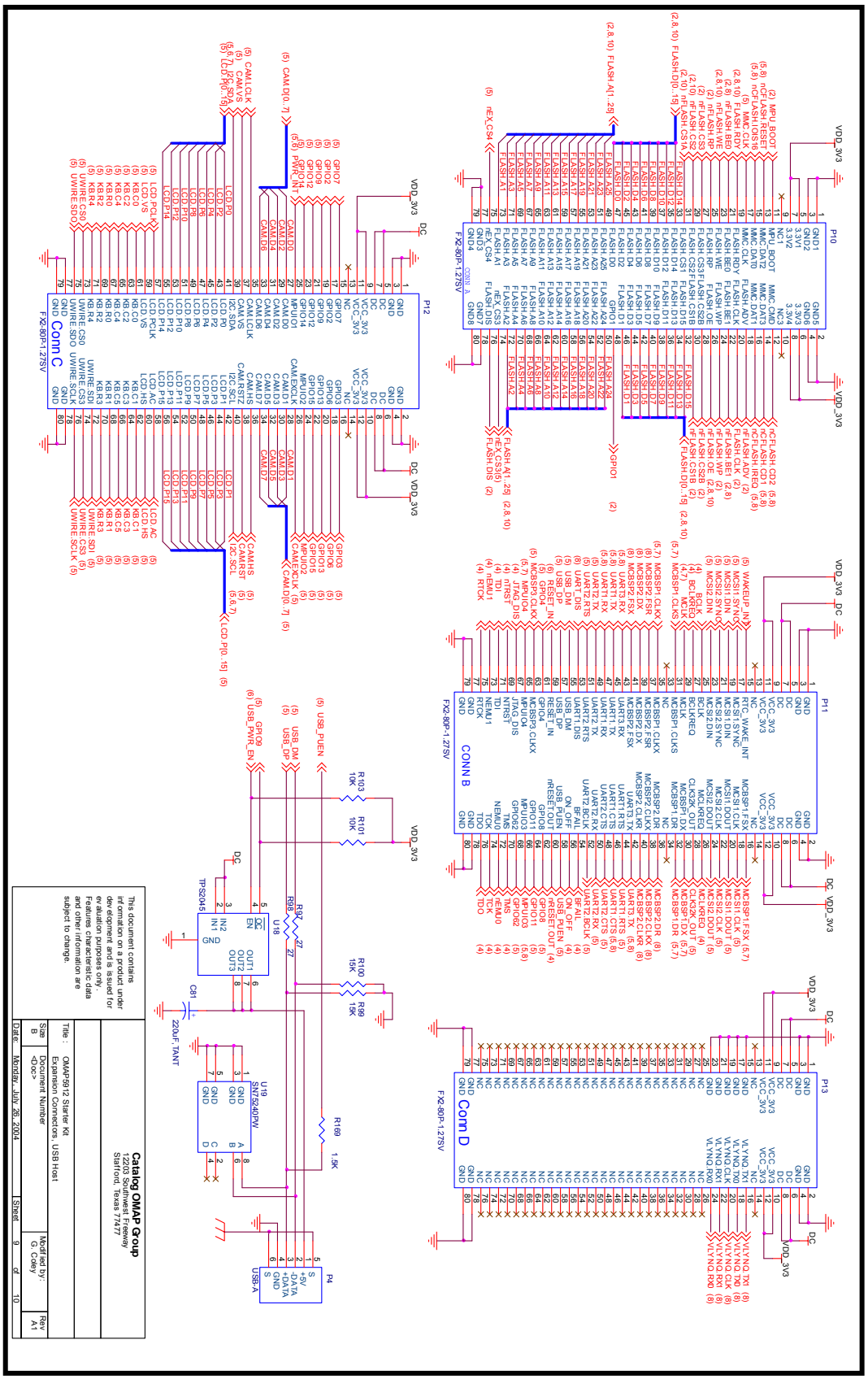
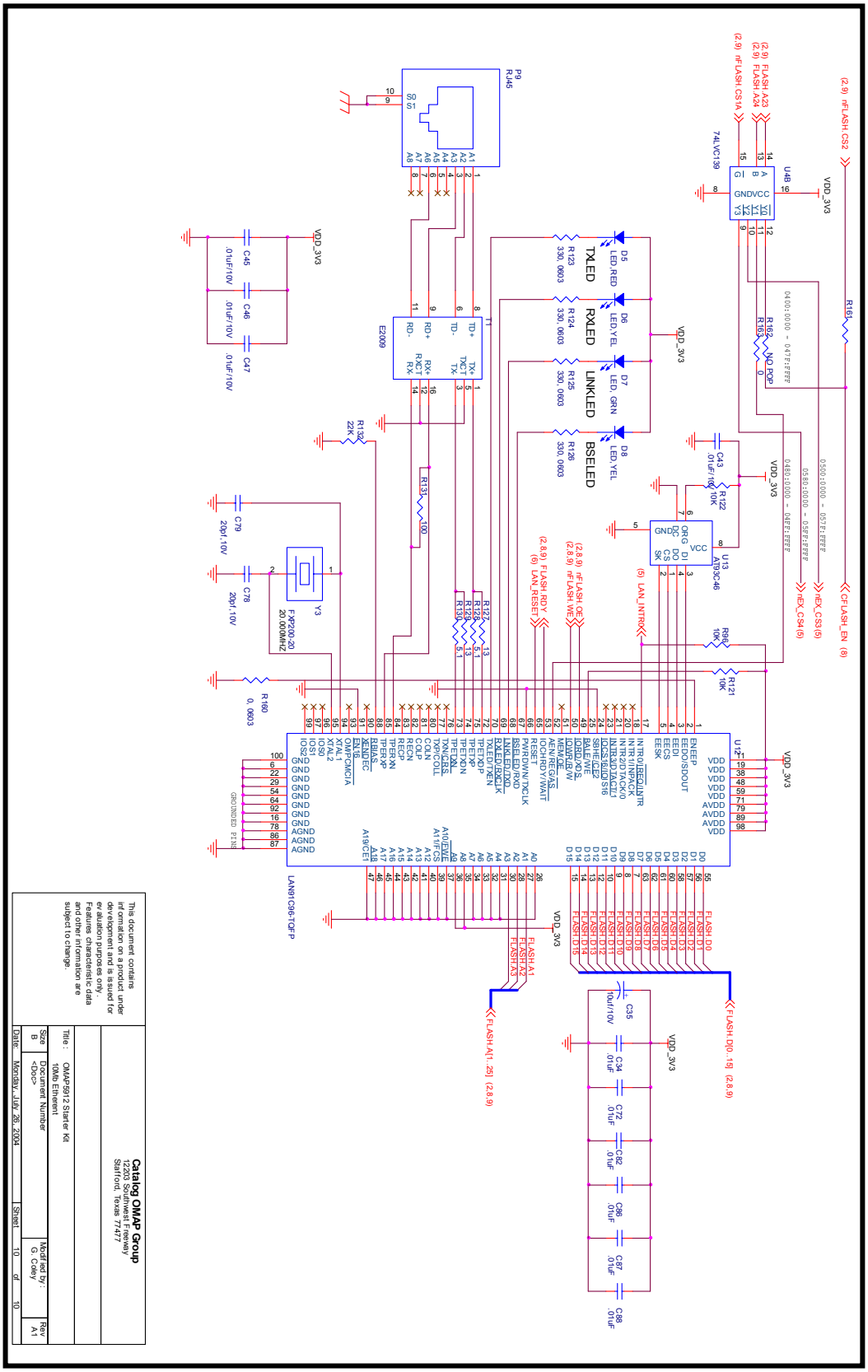
Title : OMAP5912 Starter Kit
Compact Flash, RS232, V0y.ng
Size B
Document Number <Doc>
Rev A1
Date: Monday, July 26, 2004
Sheet 8 of 10
Modified by: G. Coley


P10
P11
P12
P13
P4
Conn C
CONN B
Conn D
FX2-80P-1.27SV
TPS2045
SN75240PW
Catalog OMAP Group
1210 Southwest Freeway
Stafford, Texas 77477
This document contains information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.
Title : OMAP5912 Starter Kit
Expansion Connectors, USB Host
Size B
Document Number <Doc>
Modified by: G. Coley
Rev A1
Date: Monday, July 26, 2004
Sheet 9 of 10


LAN91C96-TQFP
74LVC139
E2009
FXP200.00
20.000MHZ
AT93C46
TXLED
RXLED
LINKLED
BSELED
Catalog OMAP Group
12203 Southwest Freeway
Stafford, Texas 77477
This document contains information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.
Title : OMAP5912 Starter Kit
10Mb Ethernet
Size B
Document Number
<Doc>
Rev A1
Date: Monday, July 26, 2004
Sheet 10 of 10
Modified by: G. Coley

Appendix D- Current Measurement Procedure

This appendix describes how to properly use the test points on the OMAP5912 OSK Target Module to take current measurements for each of the voltage rails.

Basic Principle

The basic concept is measuring the voltage drop across a .1 ohm resistor to determine the total current consumed. These technique is voltage level independent The formula used to determine the current is:

Voltage Drop /resistor = Current (ma)

The table below shows the measured voltage drop across a .1 resistor for each of the subsequent current flows:

Voltage Drop	Current(ma)
.0001	1
.001	10
.05	50
.01	100
.02	200
.05	500
.1	1000

The reason such a small value has been chosen is to:

- limit the power
- limit the size of the resistor
- limit the voltage drop to a point where it minimizes the impact on the actual voltage level

Basic Measuring Techniques

Care must be taken to minimize the impact on the operation of the circuitry on the voltage rails while taking the measurements. There are two basic ways in which the voltage drop across the resistors can be measured without impacting the operation of the circuit:

- Mill volt Voltmeter
  - Good for steady state current readings
  - Poor response to current changes

- Oscilloscope
  - Good for real-time measurement
  - Good for storage of the data
  - Good response to current changes

Following are the connection methods and setup for each of these methods.

Voltmeter-

WARNING:

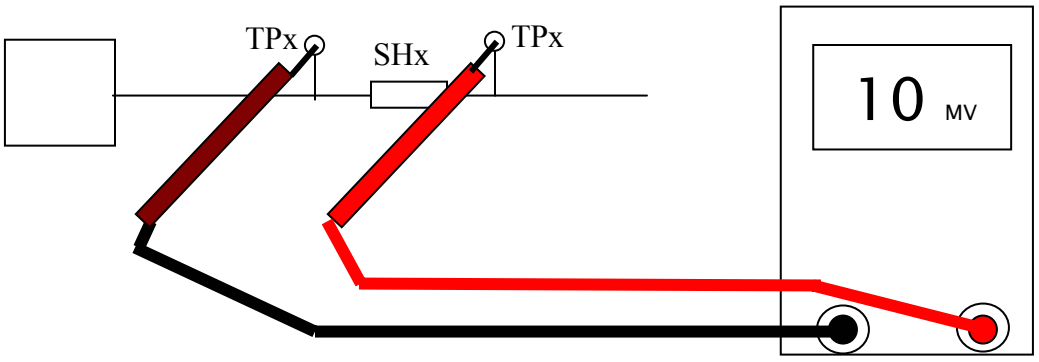
Insure that the voltmeter used is either battery powered or if AC powered, that the ground of the meter is isolated from the earth and system ground. We don't want to tie one side of the resistor to ground while attempting the test . It will result in shorting out the voltage supply.

1) Power off the system.

2) Set the meter to the Mv setting

3) Set the scale to 1000mv

4) Connect the meter as shown below:



5) Turn on the system power.

6) The voltage displayed will be in mV. A display of 10mV is equal to 100ma.

Oscilloscope-

WARNING:

Insure that the Oscilloscope used is either battery powered or if AC powered, that the ground of the scope is isolated from the earth and system ground. We don't want to tie one side of the resistor to ground while attempting the test. It will result in shorting out the voltage supply.

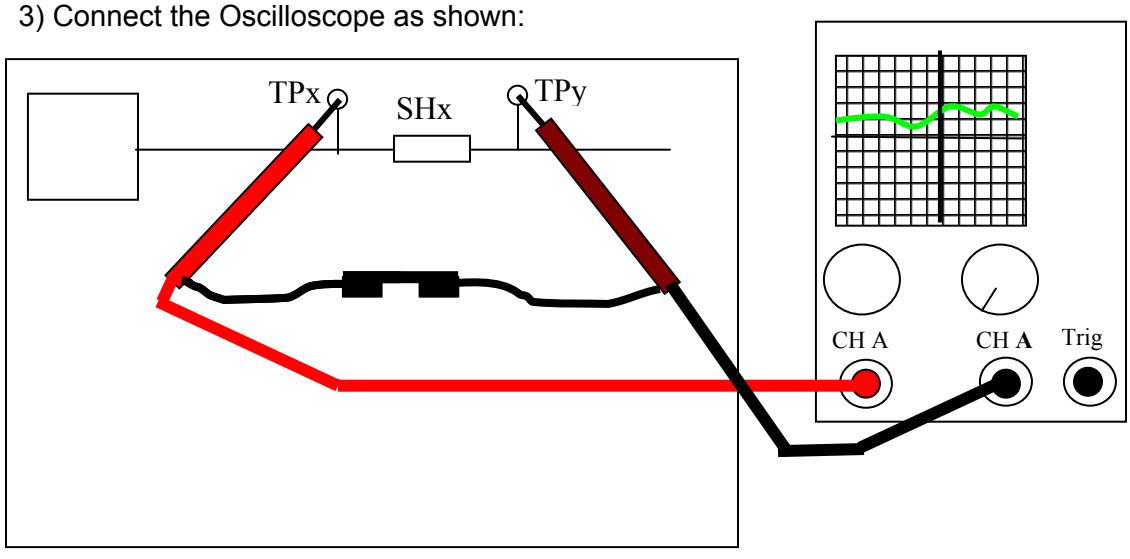
This test will take two probes for the test. It will take the voltage measured at TPx and add it to the inverted level measured at TPy, giving the differential voltage between the two points displayed on the Oscilloscope.

1) Power off the system.

2) Set the Oscilloscope as follows:

- A channel to DC
- B channel to DC
- Set trigger source as A
- Set A channel to .01 V/DIV
- Set B channel to .01 V/DIV
- Set B channel to inverted
- Set A channel + B channel (Add)
- Set to .1 Sec/Div (Various settings are OK)

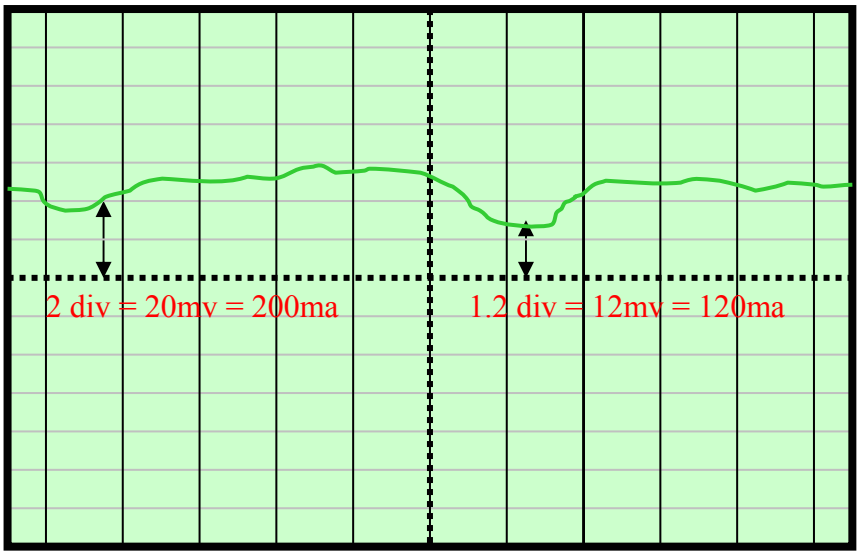
3) Connect the Oscilloscope as shown:



5) Turn on the system power.

6) The voltage displayed will be in mV. A display of 10mV is equal to 100ma.

7) Current can be measured over time by getting the value at any point across the trace. As current loads change, the voltage display will change. An example scope display is shown below.



Oscilloscope Techniques-

Another nice function of the oscilloscope is to trigger the collection of data. This can be useful when you want to measure the current based upon an event from Software or during a specific period where the SW is in a particular piece of code.

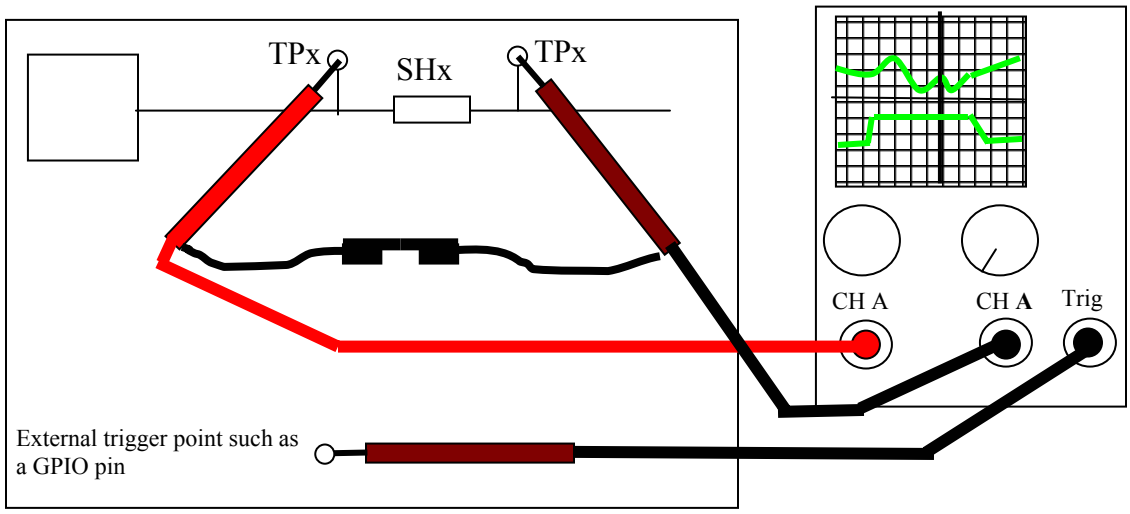
The following procedure shows how to set things up for this technique. This will require a 4 channel scope.

1) Power off the system.

2) Set the Oscilloscope as follows:

- A channel to DC
- B channel to DC
- Set trigger source as external
- Set A channel to .01 V/DIV
- Set B channel to .01 V/DIV
- B channel inverted
- Set A channel + B channel
- Set to .1 Sec/Div

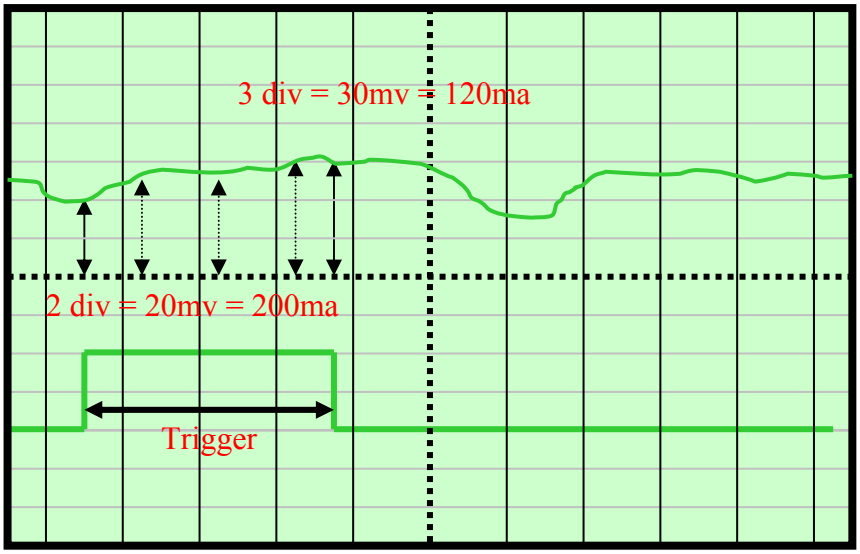
3) Connect the Oscilloscope as shown:



5) Turn on the system power.

6) The voltage displayed will be in mV. A display of .100mV is equal to 10ma.

7) Using the storage mode of the scope, current can be measured during the event or triggered by the event. As current loads change, the voltage display will change. An example scope display is shown below.



By measuring the voltage at multiple points within the trigger window, the average current can be calculated.