10W High Power SPDT Switch

■ FEATURES

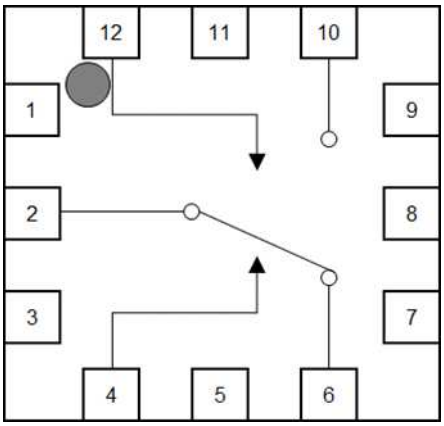
- Control voltage range 2.7 V to 5.0 V
- Low insertion loss
  - 0.35 dB typ. @ 3.85 GHz, V_{CTL} (H) = 3.3 V
  - 0.40 dB typ. @ 4.7 GHz, V_{CTL} (H) = 3.3 V
  - 0.45 dB typ. @ 6.0 GHz, V_{CTL} (H) = 3.3 V
- High isolation
  - 27dB typ. @ 3.85 GHz, V_{CTL} (H) = 3.3 V
  - 27dB typ. @ 4.7 GHz, V_{CTL} (H) = 3.3 V
  - 25dB typ. @ 6.0 GHz, V_{CTL} (H) = 3.3 V
- High linearity
  - $P_{-0.1dB}$ = +40 dBm typ. @ 6.0 GHz, V_{CTL} (H) = 3.3 V
- High switching speed 150 ns typ.
- Small & thin Package
  - EQFN12-E4 (2.0 mm x 2.0 mm x 0.397 mm typ.)
- RoHS compliant and Halogen Free, MSL1

■ APPLICATION

- 5G (Sub-6GHz) Small-cell base station
- Commercial radio application
- Transmit/receive switching, antenna switching and others switching applications

■ BLOCK DIAGRAM (EQFN12-E4)

(TOP VIEW)



■ GENERAL DESCRIPTION

The NJG1817ME4 is a high power SPDT switch GaAs MMIC suitable for 5G base station system, also is used commercial radio system requiring high power.

This switch has high power handing capability of +40dBm. Features are high linearity and low insertion loss up to 6GHz. Furthermore, high switching speed of the NJG1817ME4 is enough capable on 5G communications. Integrated ESD protection device on each RF port achieves excellent ESD robustness.

The NJG1817ME4 is packaged 2mm x 2mm EQFN12-E4 small size package despite its high power handling.

■ TRUTH TABLE

"H" = V_{CTL} (H), "L" = V_{CTL} (L)

ON PATH	VCTL1	VCTL2
PC-P1	H	L
PC-P2	L	H

■PIN CONFIGURATION

PIN NO.	SYMBOL	DESCRIPTION
1	NC(GND)	No connected terminal (Connect to ground)
2	PC	Common RF terminal
3	NC(GND)	No connected terminal (Connect to ground)
4	VCTL1	Control signal input terminal.
5	NC(GND)	No connected terminal (Connect to ground)
6	P1	RF terminal
7	GND	Ground terminal
8	GND	Ground terminal
9	GND	Ground terminal
10	P2	RF terminal
11	NC(GND)	No connected terminal (Connect to ground)
12	VCTL2	Control signal input terminal.
Exposed Pad		Ground terminal

■ PRODUCT NAME INFORMATION

NJG1817 ME4 (TE1)

Part number	Package	Taping form

■ ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs.)
NJG1817ME4	EQFN12-E4	Yes	Yes	SnBi	1817	4.7	3,000

■ ABSOLUTE MAXIMUM RATINGS

(General conditions: T_a = +25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
RF input power	P_{IN}	+40(1)	dBm
Control voltage	V_{CTL}	6.0	V
Power dissipation(2)	P_D	1200	mW
Operating temperature	T_{opr}	-40 to +105	°C
Storage temperature	T_{stg}	-55 to +150	°C

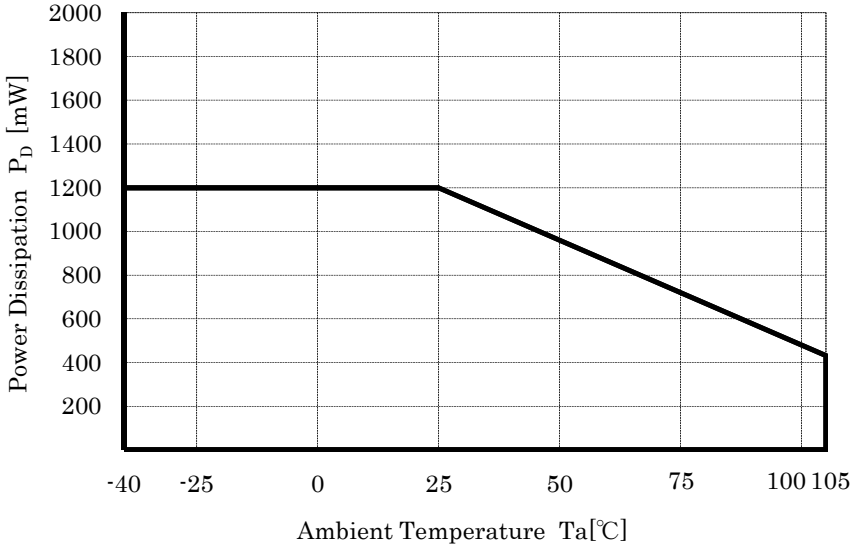
(1): V_{CTL} (H) = 3.3 V, V_{CTL} (L) = 0 V, on state port
(2): 4-layer FR4 PCB with through-hole (101.5 x 114.5 mm), Tj = 150°C

■ POWER DISSIPATION VS.AMBIENT TEMPERATURE

Please, refer to the following Power Dissipation and Ambient Temperature.
(Please note the surface mount package has a low maximum rating of Power Dissipation [P_D], a special attention should be paid in designing of thermal radiation.)

Power Dissipation—Ambient Temperature Characteristic

Mounted on PCB board



■ **ELECTRICAL CHARACTERISTICS 1 (DC CHARACTERISTICS)**

(General conditions: T_a = +25°C, Z_s = Z_l = 50 Ω, with application circuit)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Control voltage (HIGH)	V_{CTL} (H)		2.7	3.3	5.0	V
Control voltage (LOW)	V_{CTL} (L)		-0.2	0	0.2	V
Control current	I_{CTL}	V_{CTL} (H) = 3.3V, V_{CTL} (L) = 0V	-	7	15	μA

■ **ELECTRICAL CHARACTERISTICS 2 (RF CHARACTERISTICS)**

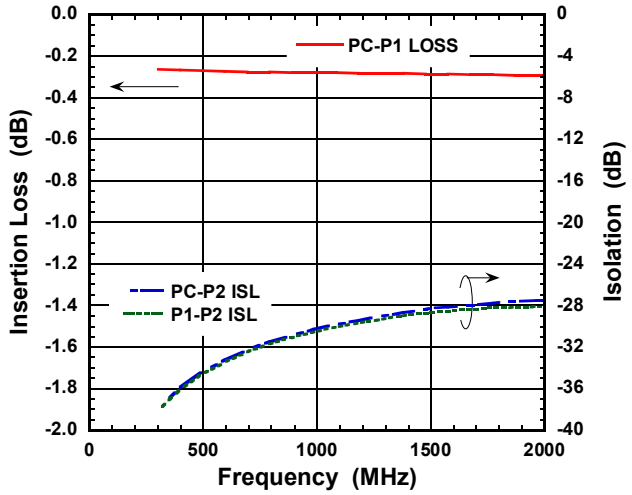
(General conditions: V_{CTL}(H) = 3.3 V, V_{CTL} (L) = 0 V, T_a = +25°C, Z_s = Z_l = 50 Ω, with application circuit)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Insertion loss	LOSS	f = 0.7GHz	-	0.30	0.45	dB
		f = 3.85 GHz	-	0.35	0.50	
		f = 4.7 GHz	-	0.40	0.60	
		f = 6.0 GHz	-	0.45	0.65	
Isolation	ISL	f = 0.7 GHz	28	30	-	dB
		f = 3.85 GHz	25	27	-	
		f = 4.7 GHz	25	27	-	
		f = 6.0 GHz	22	25	-	
Input power at 0.1dB compression point	$P_{-0.1dB}$	f = 6.0 GHz	+39	+40	-	dBm
VSWR	VSWR	f = 0.7 GHz	-	1.1	1.3	-
		f = 3.85 GHz	-	1.1	1.3	
		f = 4.7 GHz	-	1.1	1.3	
		f = 6.0 GHz	-	1.2	1.4	
Switching time	T_{SW}	50% V_{CTL} to 10%/ 90% RF	-	150	350	ns

■ **ELECTRICAL CHARACTERISTICS** (With application circuit list 1, loss of external circuit are excluded.)

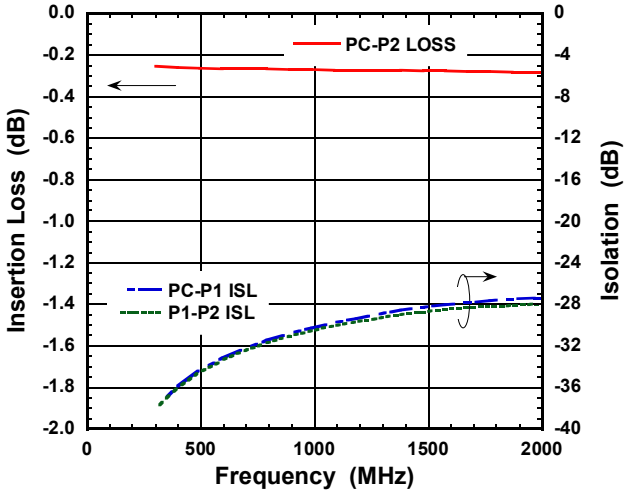
Loss, Isolation vs Frequency

(PC-P1 ON, VCTL1=3.3V, VCTL2=0V)



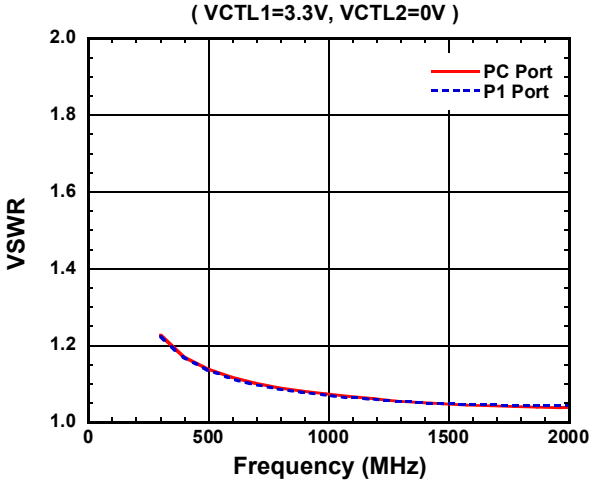
Loss, Isolation vs Frequency

(PC-P2 ON, VCTL1=0V, VCTL2=3.3V)



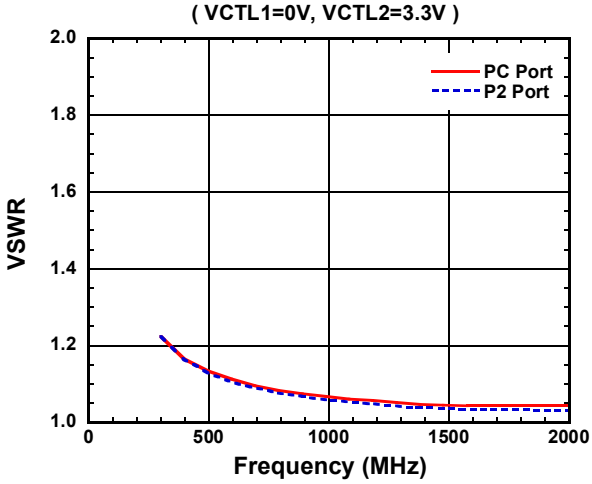
VSWR vs. Frequency

(VCTL1=3.3V, VCTL2=0V)



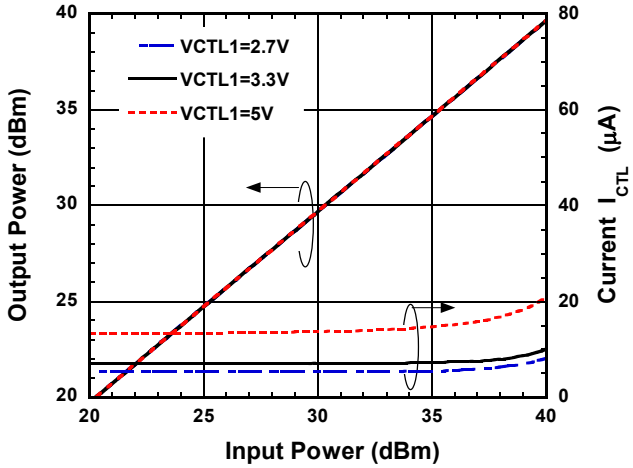
VSWR vs. Frequency

(VCTL1=0V, VCTL2=3.3V)



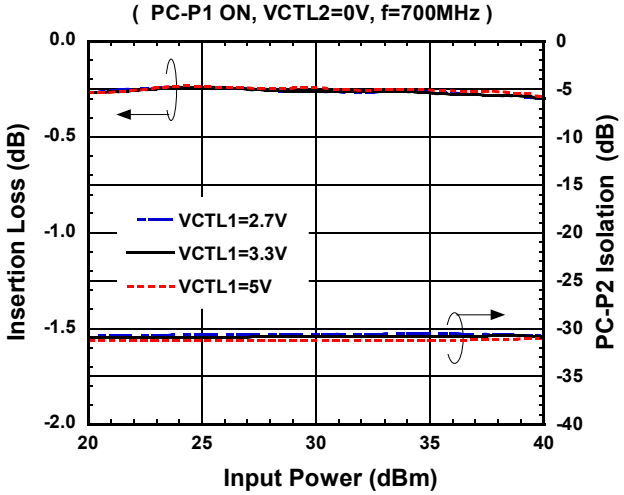
Output Power, Current vs. Input Power

(PC-P1 ON, VCTL2=0V, f=700MHz)

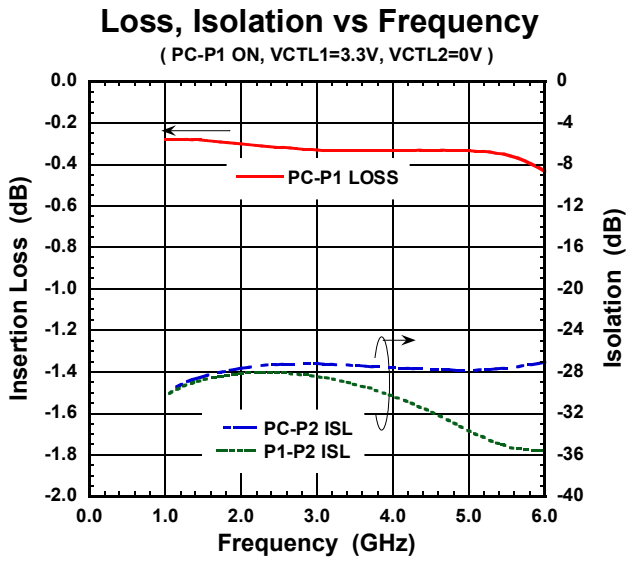


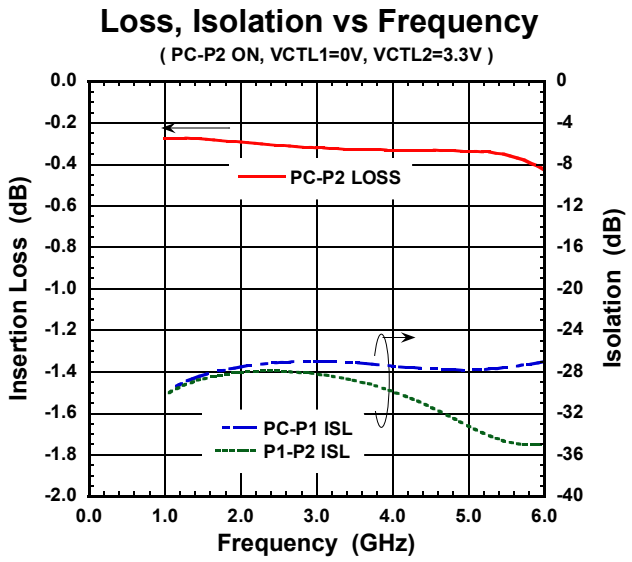
Loss, Isolation vs. Input Power

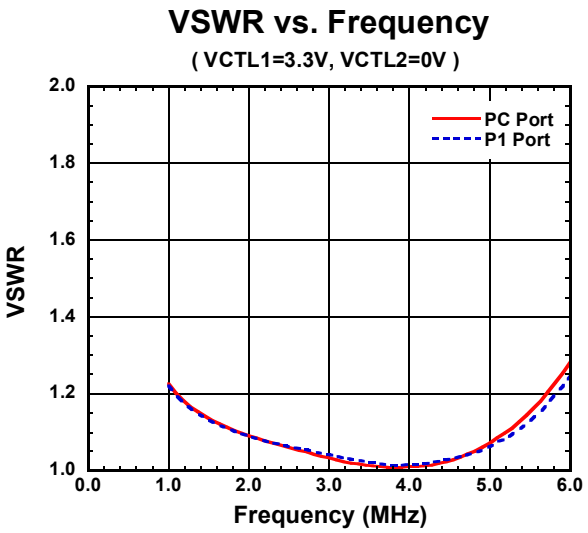
(PC-P1 ON, VCTL2=0V, f=700MHz)

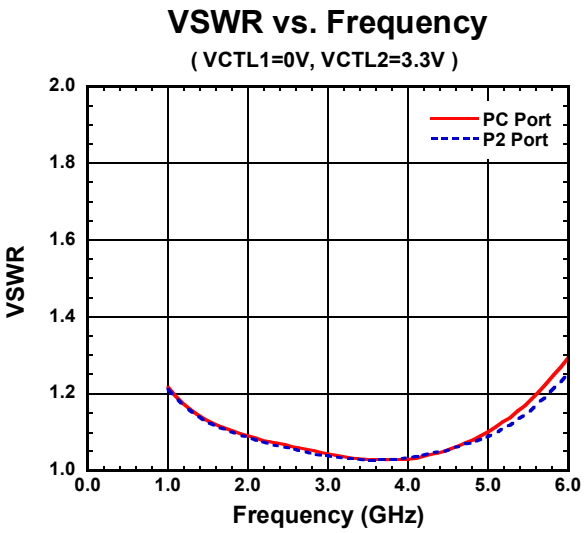


■ **ELECTRICAL CHARACTERISTICS** (With application circuit list 2, losses of external circuit are excluded.)





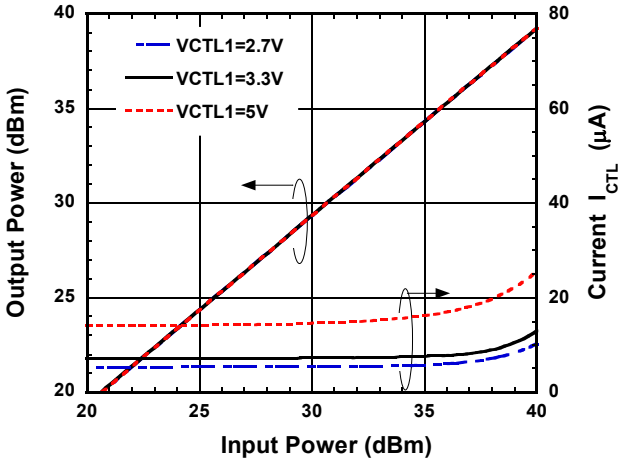




■ **ELECTRICAL CHARACTERISTICS** (With application circuit list 2, losses of external circuit are excluded.)

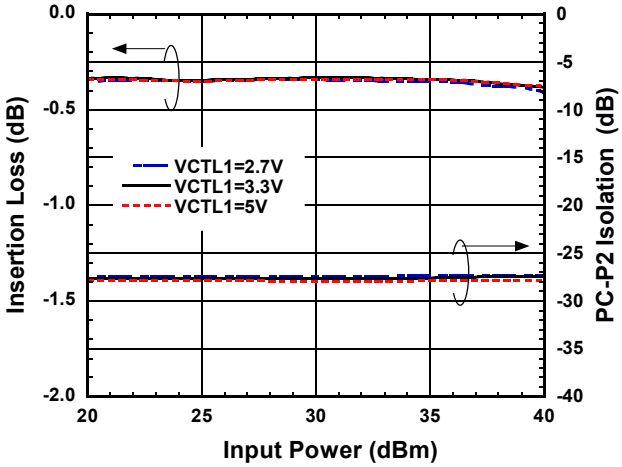
Output Power, Current vs. Input Power

(PC-P1 ON, VCTL2=0V, f=3.85GHz)



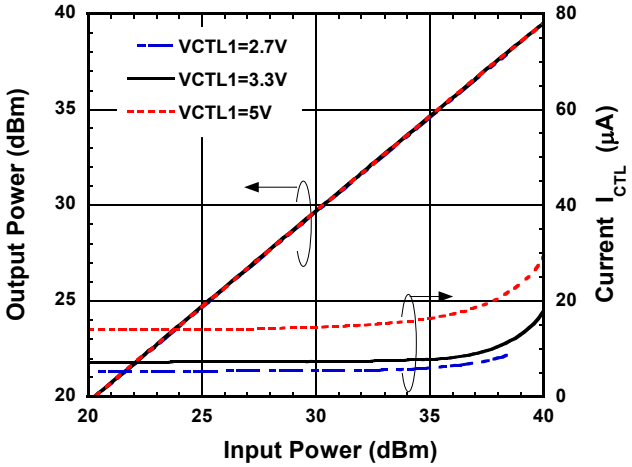
Loss, Isolation vs. Input Power

(PC-P1 ON, VCTL2=0V, f=3.85GHz)



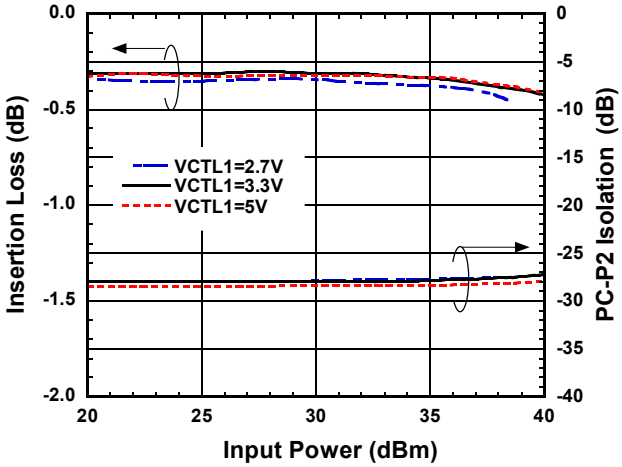
Output Power, Current vs. Input Power

(PC-P1 ON, VCTL2=0V, f=4.7GHz)



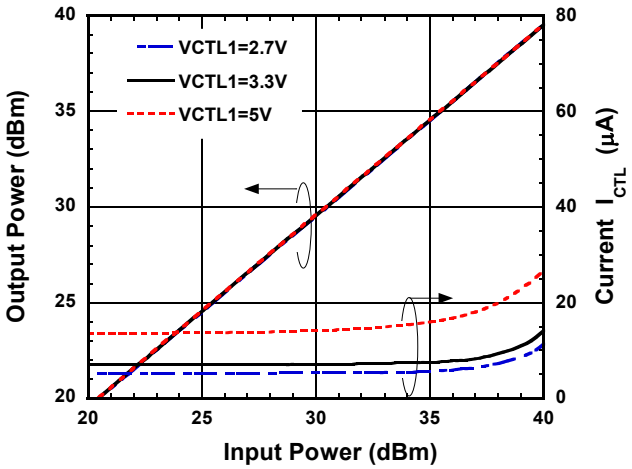
Loss, Isolation vs. Input Power

(PC-P1 ON, VCTL2=0V, f=4.7GHz)



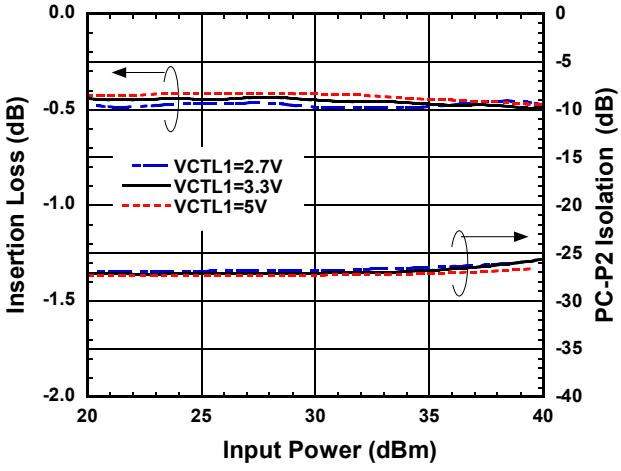
Output Power, Current vs. Input Power

(PC-P1 ON, VCTL2=0V, f=6GHz)



Loss, Isolation vs. Input Power

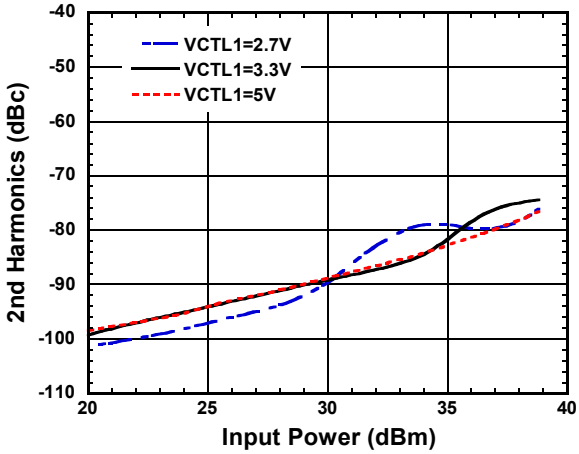
(PC-P1 ON, VCTL2=0V, f=6GHz)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit list 2, losses of external circuit are excluded.)

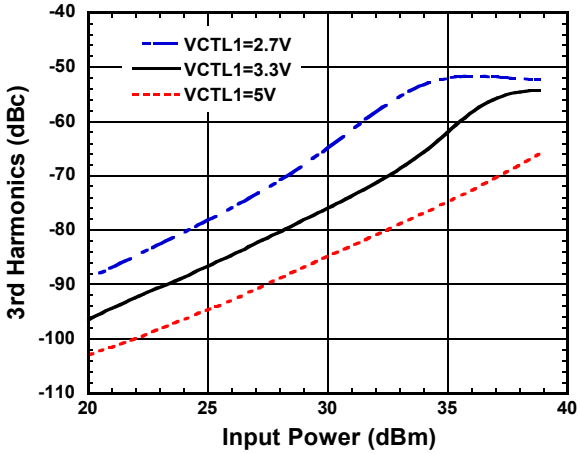
2nd Harmonics vs. Input Power

(f=3.85GHz, VCTL2=0V, PC-P1 ON)



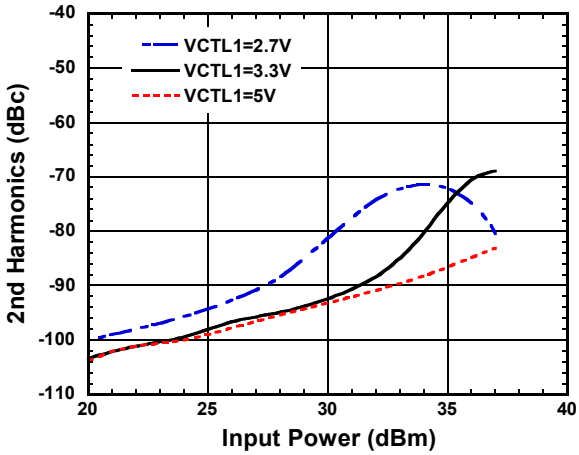
3rd Harmonics vs. Input Power

(f=3.85GHz, VCTL2=0V, PC-P1 ON)



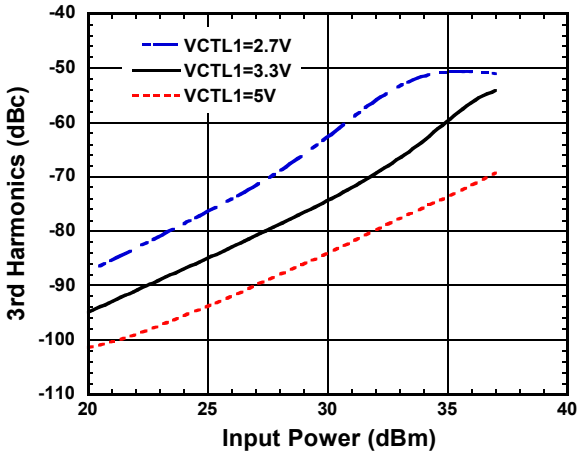
2nd Harmonics vs. Input Power

(f=4.7GHz, VCTL2=0V, PC-P1 ON)



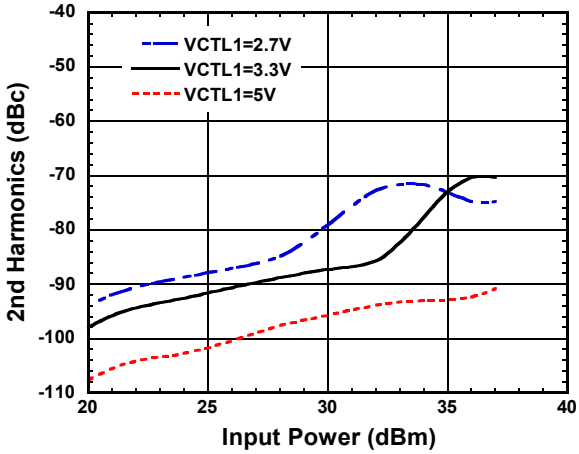
3rd Harmonics vs. Input Power

(f=4.7GHz, VCTL2=0V, PC-P1 ON)



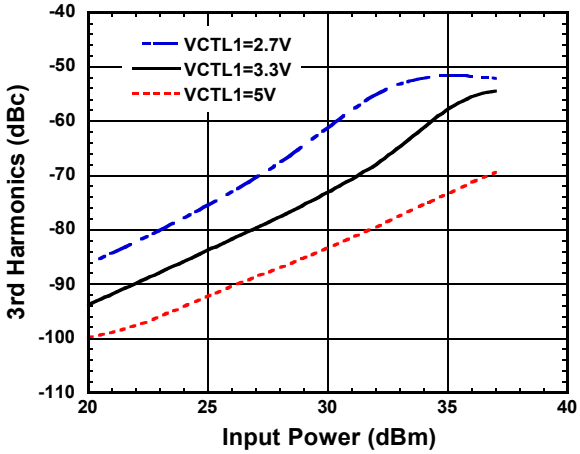
2nd Harmonics vs. Input Power

(f=6GHz, VCTL2=0V, PC-P1 ON)



3rd Harmonics vs. Input Power

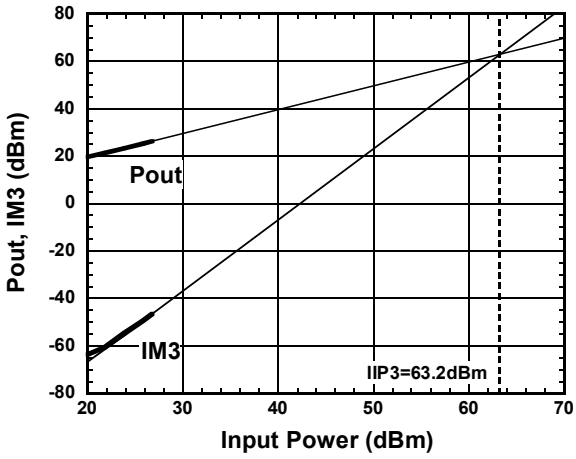
(f=6GHz, VCTL2=0V, PC-P1 ON)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit list 2, losses of external circuit are excluded.)

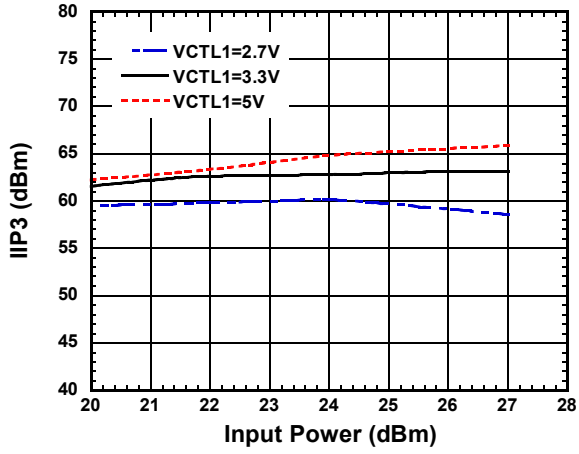
Pout, IM3 vs. Input Power

(VCTL1=3.3V, VCTL2=0V, f=3850+3851MHz)



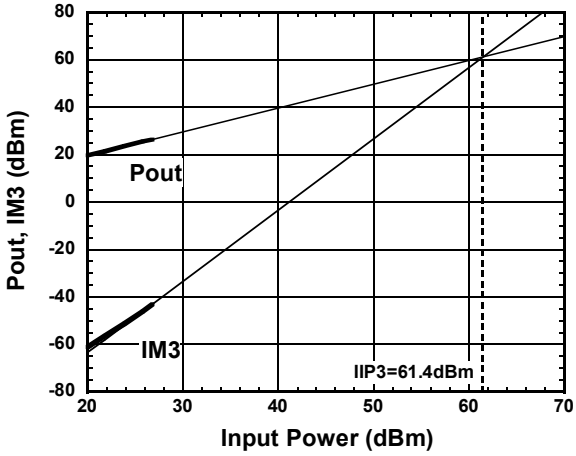
IIP3 vs. Input Power

(f=3850+3851MHz, VCTL2=0V, PC-P1 ON)



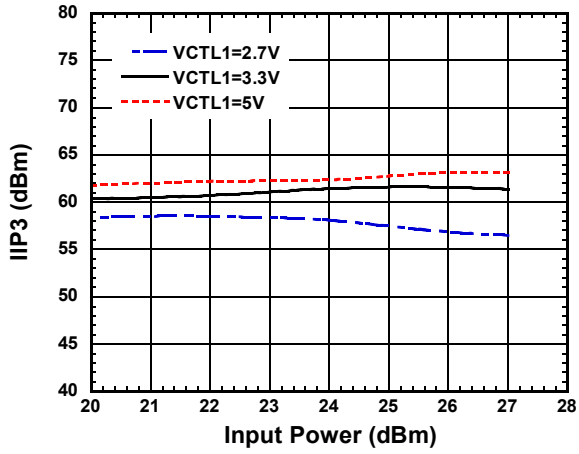
Pout, IM3 vs. Input Power

(VCTL1=3.3V, VCTL2=0V, f=4700+4701MHz)



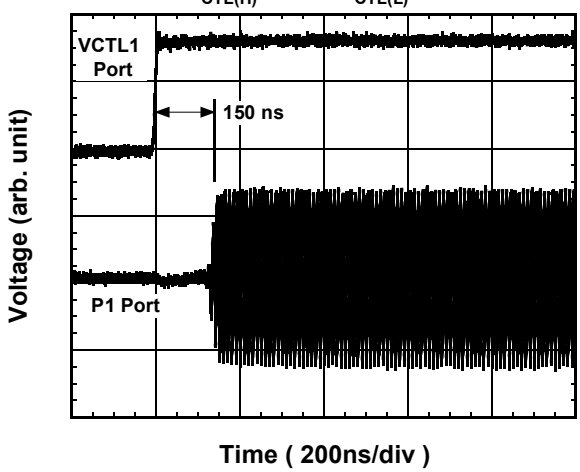
IIP3 vs. Input Power

(f=4700+4701MHz, VCTL2=0V, PC-P1 ON)



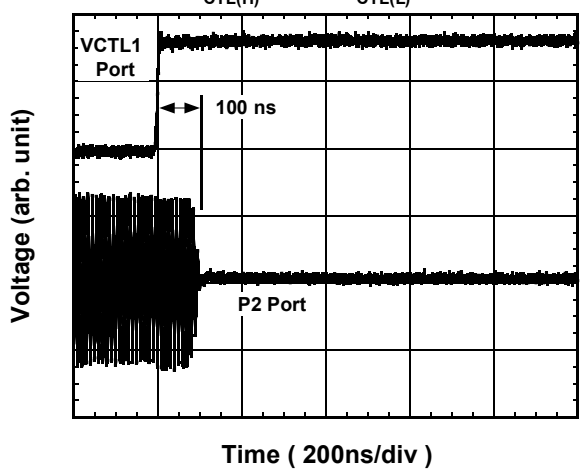
Switching Time

($V_{CTL(H)}$=3.3V, $V_{CTL(L)}$=0V)



Switching Time

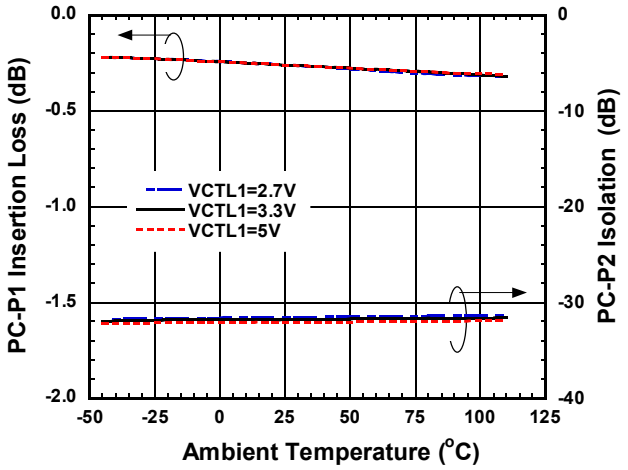
($V_{CTL(H)}$=3.3V, $V_{CTL(L)}$=0V)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit list 1, losses of external circuit are excluded.)

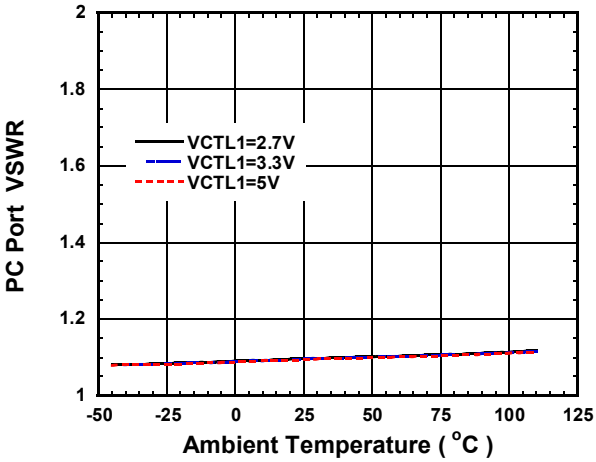
Loss, Isolation vs. Temperature

(PC-P1 ON, VCTL2=0V, f=0.7GHz)



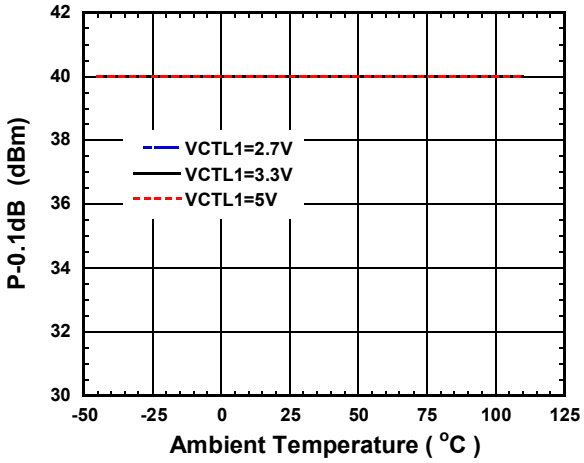
VSWR vs. Temperature

(PC-P1 ON, VCTL2=0V, f=0.7GHz)



$P_{-0.1dB}$ vs. Temperature

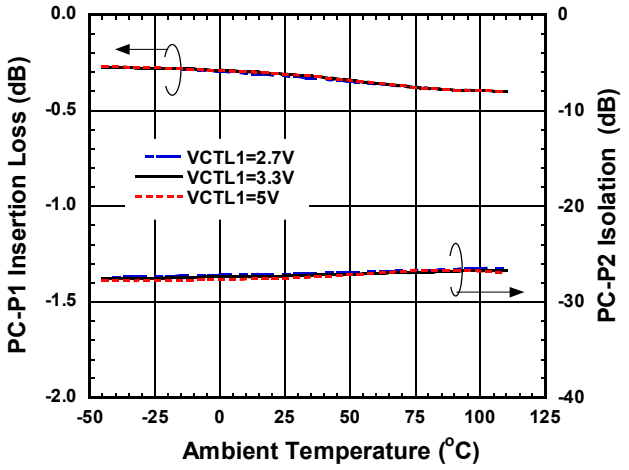
(f=700MHz, PC-P1, VCTL2=0V)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit list 2, losses of external circuit are excluded.)

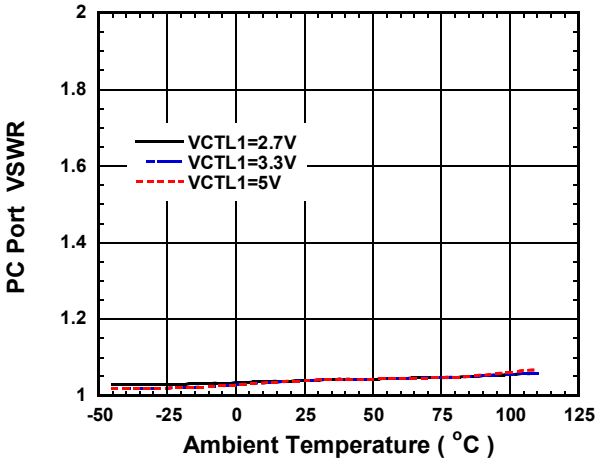
Loss, Isolation vs. Temperature

(PC-P1 ON, VCTL2=0V, f=3.85GHz)



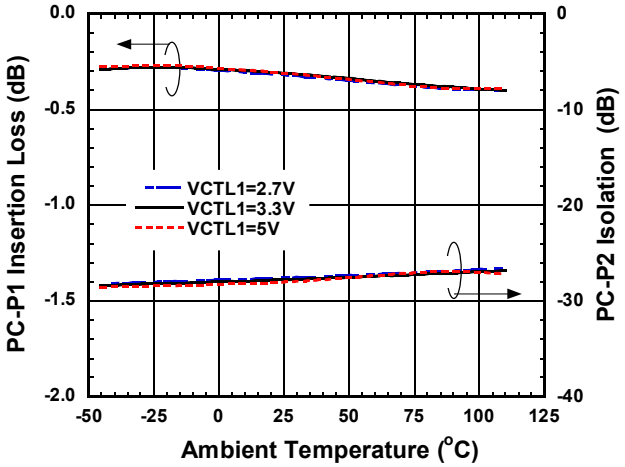
VSWR vs. Temperature

(PC-P1 ON, VCTL2=0V, f=3.85GHz)



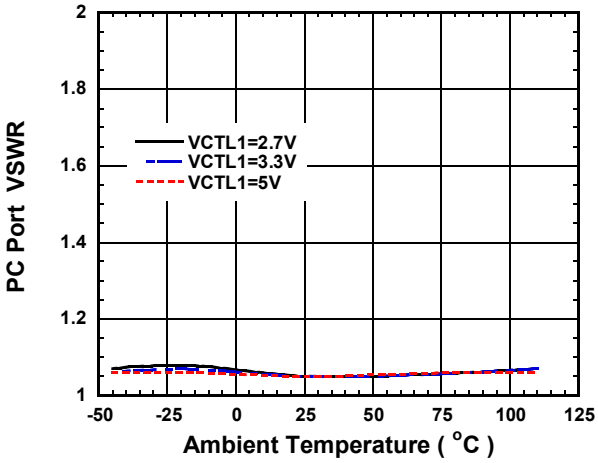
Loss, Isolation vs. Temperature

(PC-P1 ON, VCTL2=0V, f=4.7GHz)



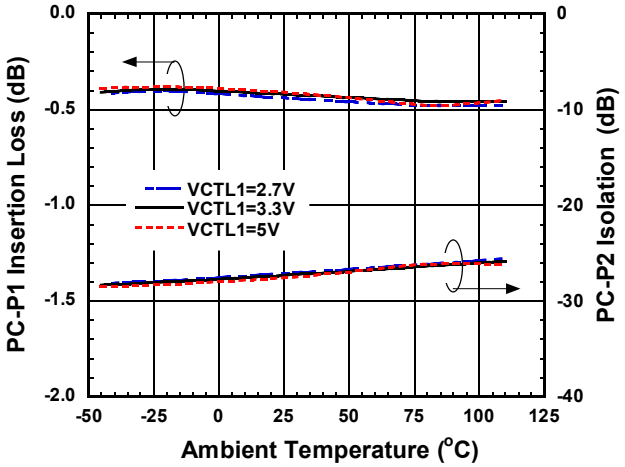
VSWR vs. Temperature

(PC-P1 ON, VCTL2=0V, f=4.7GHz)



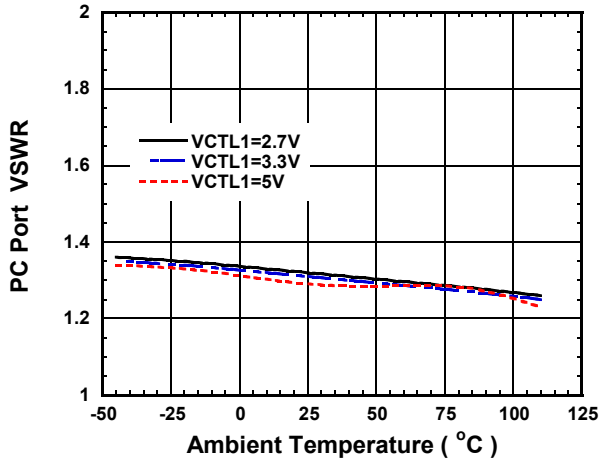
Loss, Isolation vs. Temperature

(PC-P1 ON, VCTL2=0V, f=6GHz)

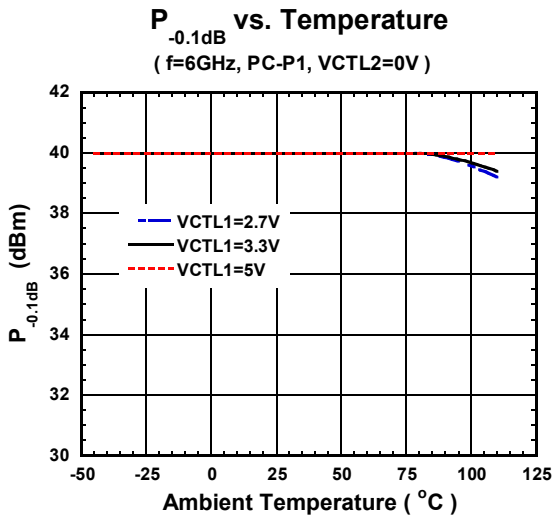


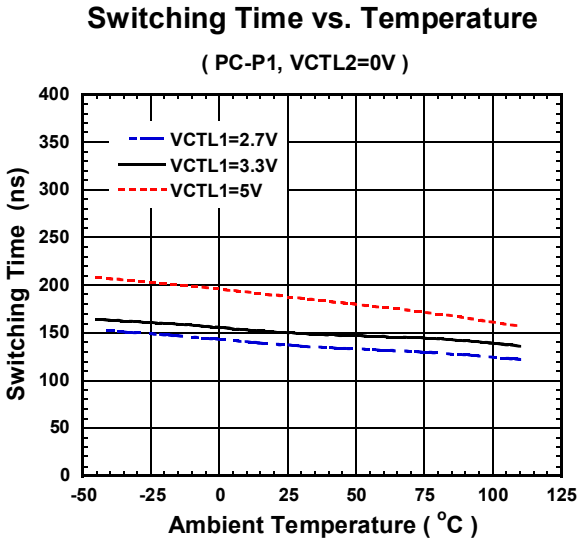
VSWR vs. Temperature

(PC-P1 ON, VCTL2=0V, f=6GHz)



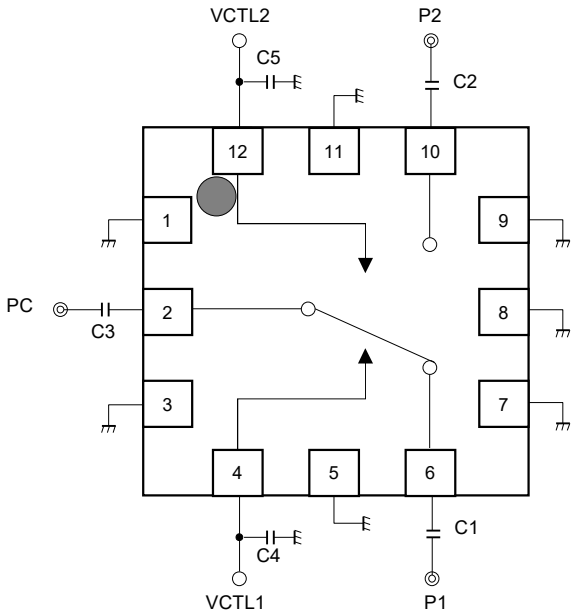
■ **ELECTRICAL CHARACTERISTICS** (With application circuit list 2, losses of external circuit are excluded.)





■ **APPLICATION CIRCUIT**

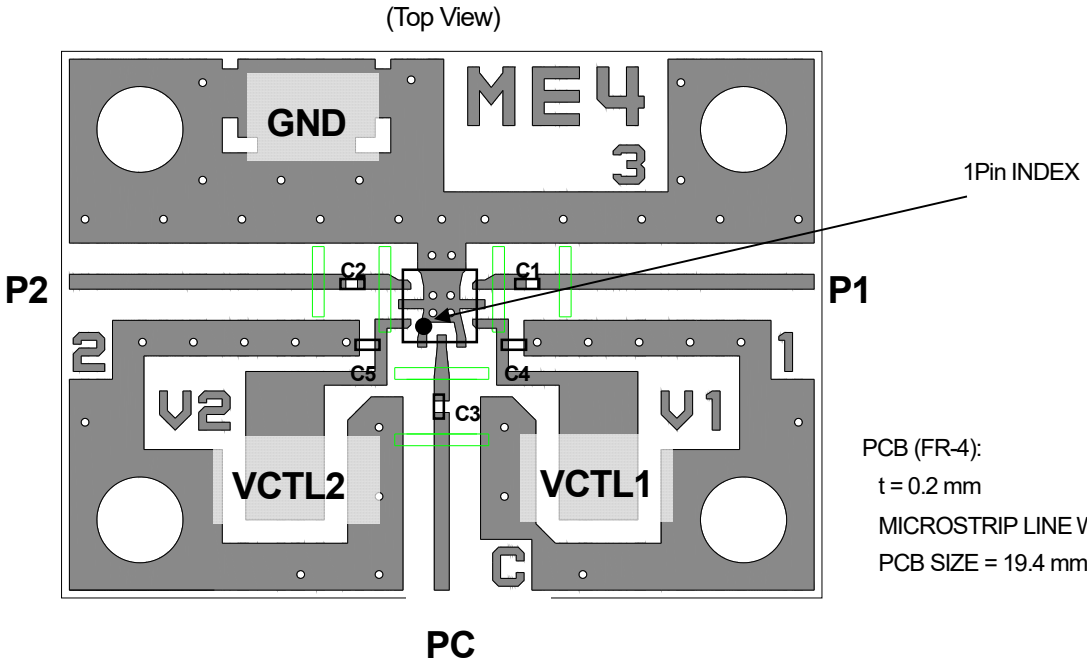
(Top View)



＜ **PARTS LIST**＞

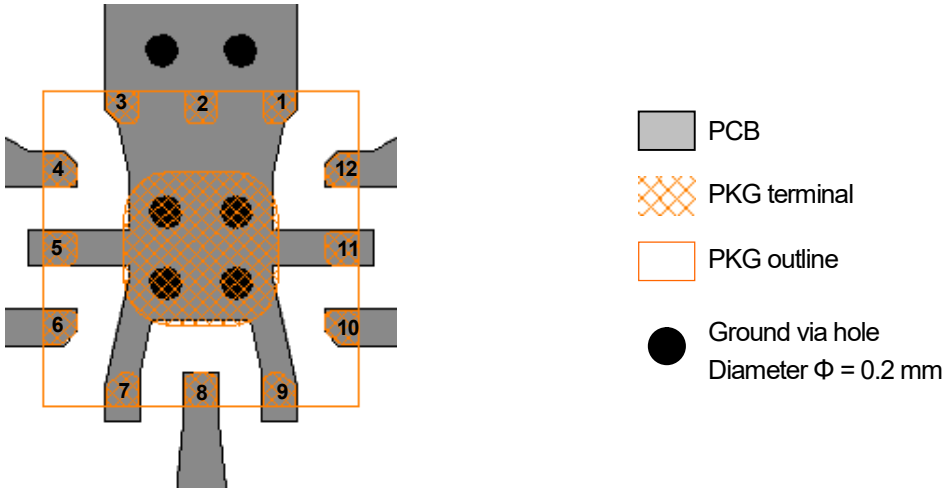
Part ID	Value		Notes
	List 1	List 2	
	f = 0.3 to 2.0 GHz	f = 2.0 to 6.0 GHz	
C1 to C3	100 pF	27 pF	MURATA (GRM03)
C4, C5	10 pF	10 pF	MURATA (GRM03)

■ EVALUATION BOARD



PCB (FR-4):
t = 0.2 mm
MICROSTRIP LINE WIDTH = 0.38 mm (Z_0 = 50 Ω)
PCB SIZE = 19.4 mm x 14.0 mm

■ PCB LAYOUT GUIDELINE (EQFN12-E4)



PRECAUTIONS

[1] The DC blocking capacitors should be placed at RF terminals. Please choose appropriate capacitance value at the application frequency.
[2] For good RF performance, all GND terminals are must be connected to PCB ground plane of the substrate, and through - holes for GND should be placed near the IC.
[3] Please connect Exposed PAD to PCB ground plane of substrate, and through - holes for ground should be placed under the IC.
[4] Please place through holes under the IC as many as possible in order to improve thermal conduction.

■ RECOMMENDED FOOTPRINT PATTERN (EQFN12-E4 PACKAGE Reference)

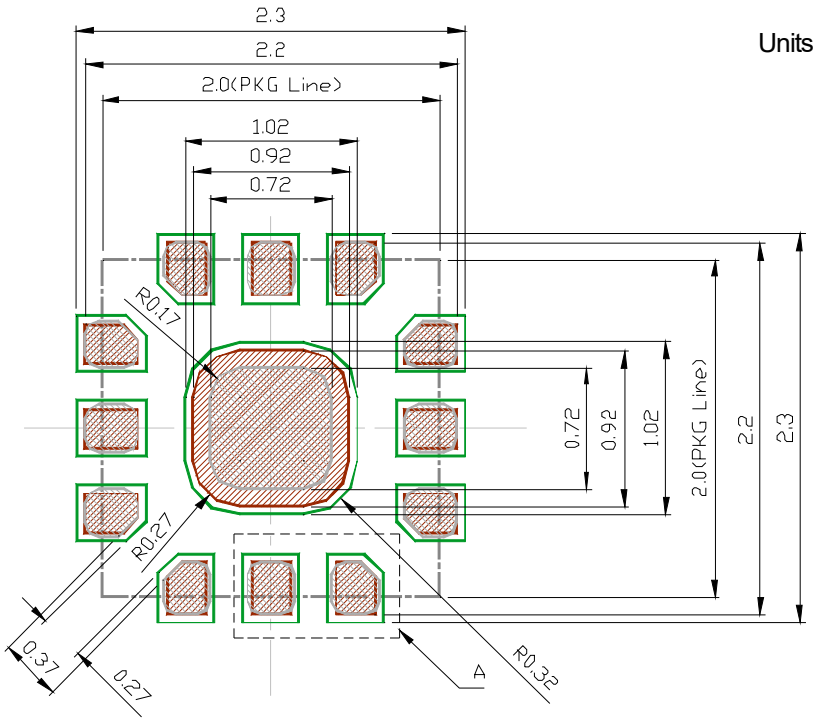
PKG: 2.0 mm x 2.0 mm
Pin pitch: 0.5 mm

: Land

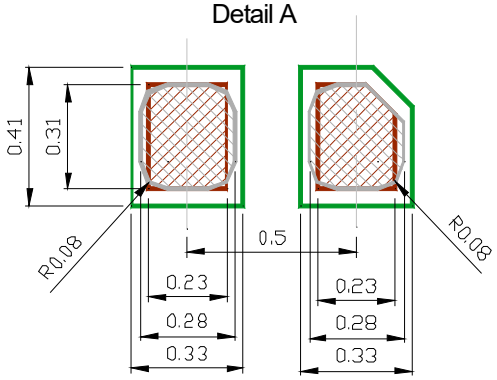
: Mask (Open area) *Metal mask thickness: 100 μm

: Resist (Open area)

Units : mm

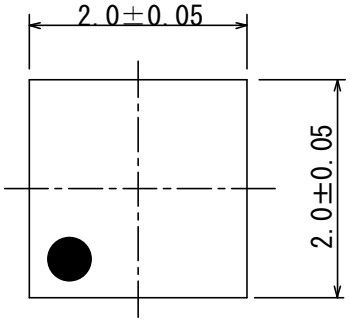


Detail A



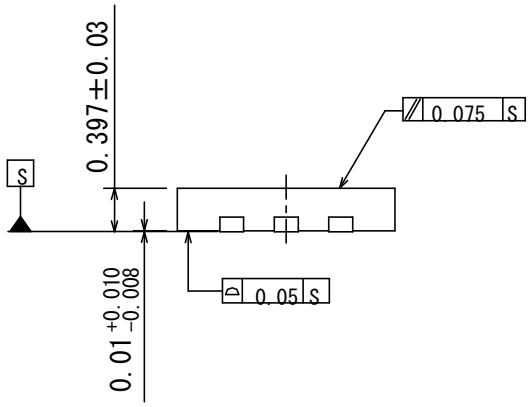
■ PACKAGE OUTLINE (EQFN12-E4)

TOP VIEW

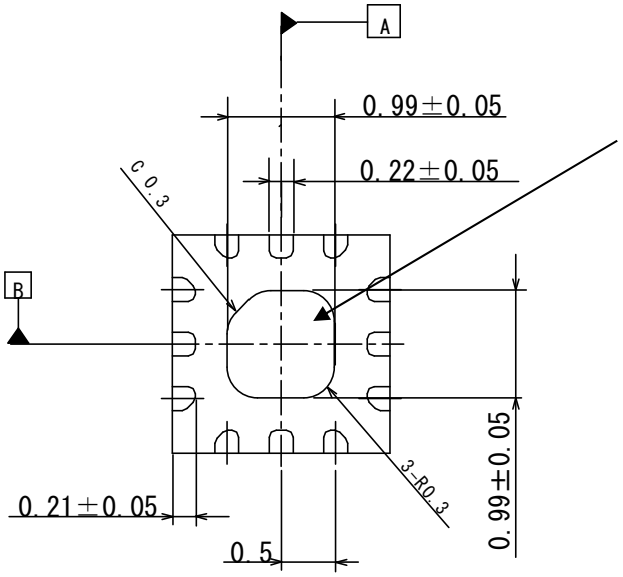


Units	: mm
Board	: Cu
Terminal treat	: SnBi
Molding material	: Epoxy resin
Weight	: 4.7mg

SIDE VIEW



BOTTOM VIEW

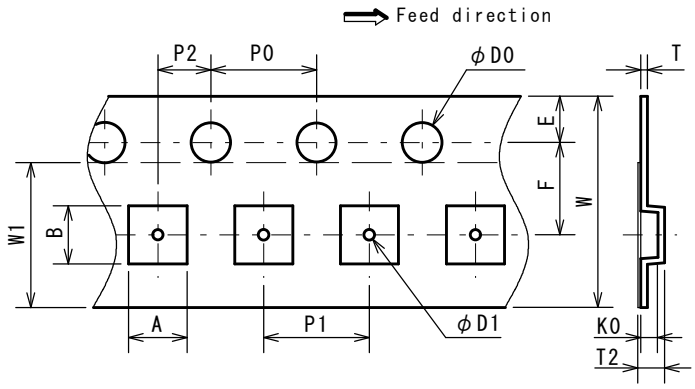


Ground connection is required.

■PACKING SPECIFICATION

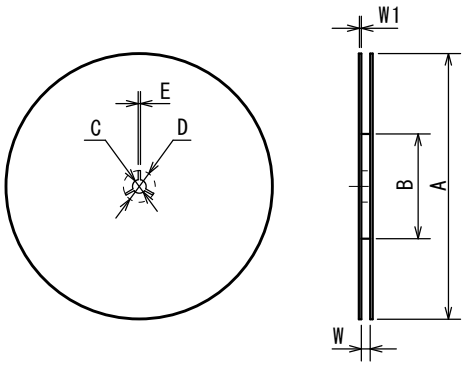
Unit: mm

TAPING DIMENSIONS



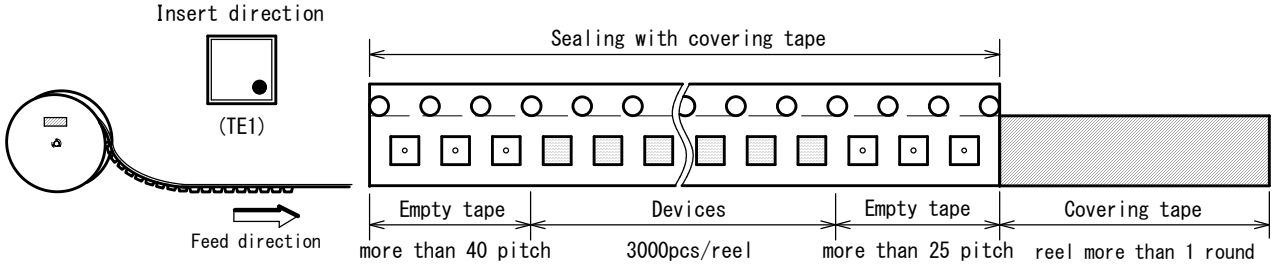
SYMBOL	DIMENSION	REMARKS
A	2.25±0.05	BOTTOM DIMENSION
B	2.25±0.05	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	0.5±0.1	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.00±0.07	
K0	0.65±0.05	
W	8.0±0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

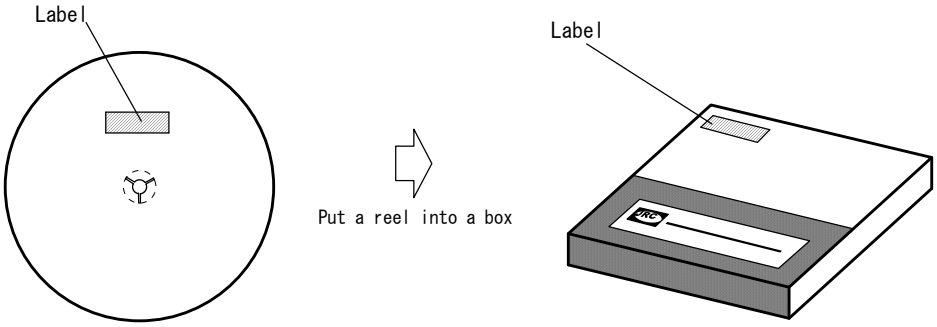


SYMBOL	DIMENSION
A	$\phi 180^{0}_{-1.5}$
B	$\phi\ 60^{+1}_{0}$
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9^{+1}_{0}
W1	1.2

TAPING STATE



PACKING STATE



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