






VL-FS-MDLS161612D-02 REV. A  
(MDLS161612D-LV-G-LED04G-IC-NT3881DH-01A)

JULY/2002

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DOCUMENT NUMBER AND REVISION  
**VL-FS-MDLS161612D-02 REV. A**  
**(MDLS161612D-LV-G-LED04G-IC-NT3881DH-01A)**

DOCUMENT TITLE:  
**SPECIFICATION**  
**OF**  
**LCD MODULE TYPE**  
**ITEM NO.: MDLS161612D-02**

DEPARTMENT	NAME	SIGNATURE	DATE
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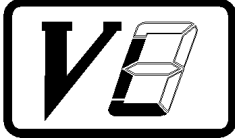
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## VARITRONIX LIMITED

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### Specification of LCD Module Type Item No.: MDLS161612D-02

#### 1. General Description

- 16 characters (5 x 8 dots) x 1 line STN Positive Yellow Transflective Dot Matrix LCD module.
- Viewing Angle: 6 O'clock direction.
- Driving duty: 1/16 Duty, 1/5 bias.
- 'NOVATEK' NT3881DH-01/AI (die form) LCD Controller and Driver or equivalent
- Yellow-green LED04 backlight.

#### 2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	154.4(W) x 43.5(H) x 14.0 MAX.(D)	mm
Effective viewing area	119.4(W) x 18.7(H)	mm
Display format	16 characters x 1 line	-
Character size	5.90(W) x 12.70(H) (5 x 8 dots)	mm
Character spacing	1.00(W)	mm
Character pitch	6.90(W)	mm
Dot size	1.10(W) x 1.50(H)	mm
Dot spacing	0.10(W) x 0.10(H)	mm
Dot pitch	1.20(W) x 1.60(H)	mm
Weight	TBD	grams

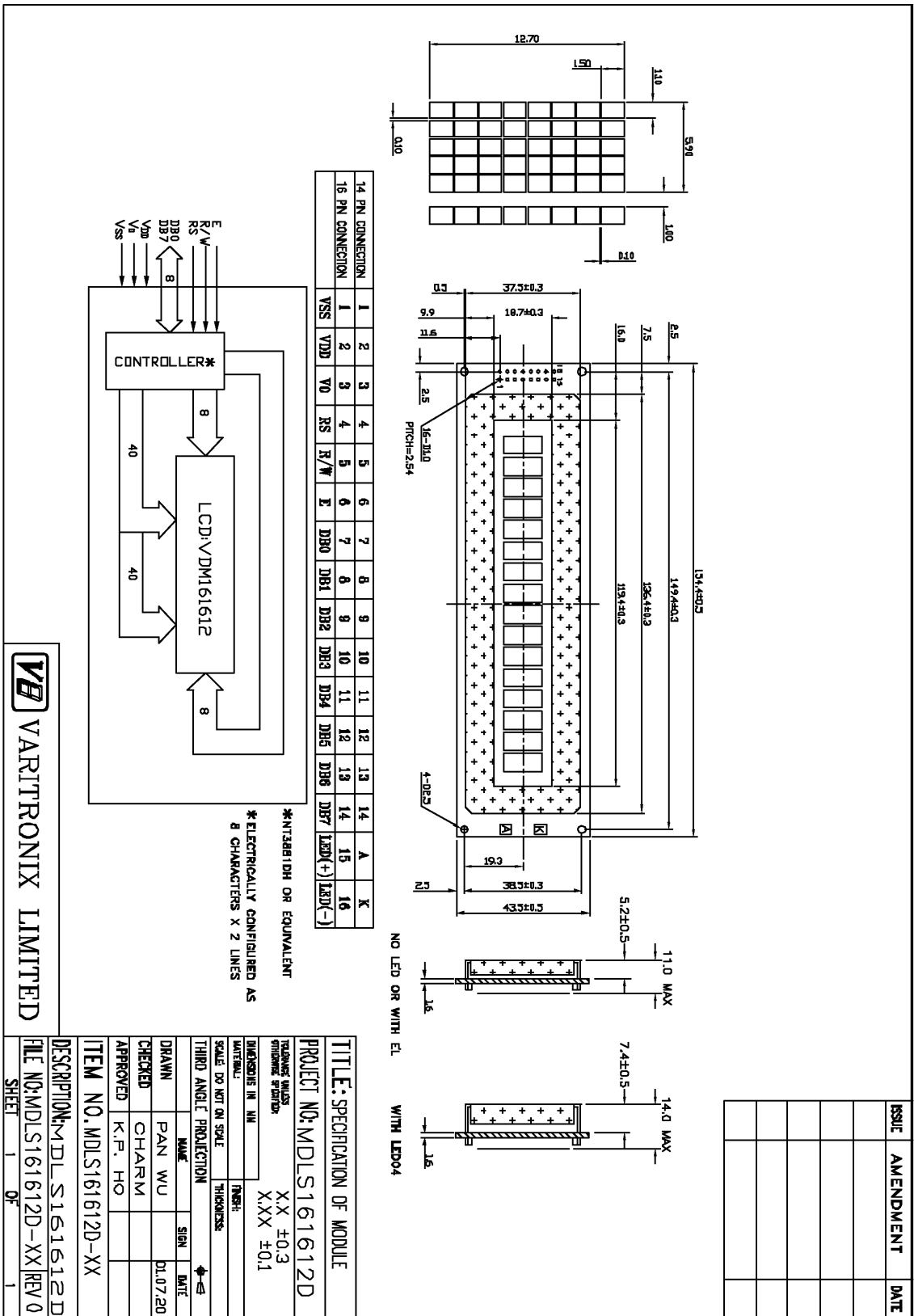


Figure 1: Outline Drawing

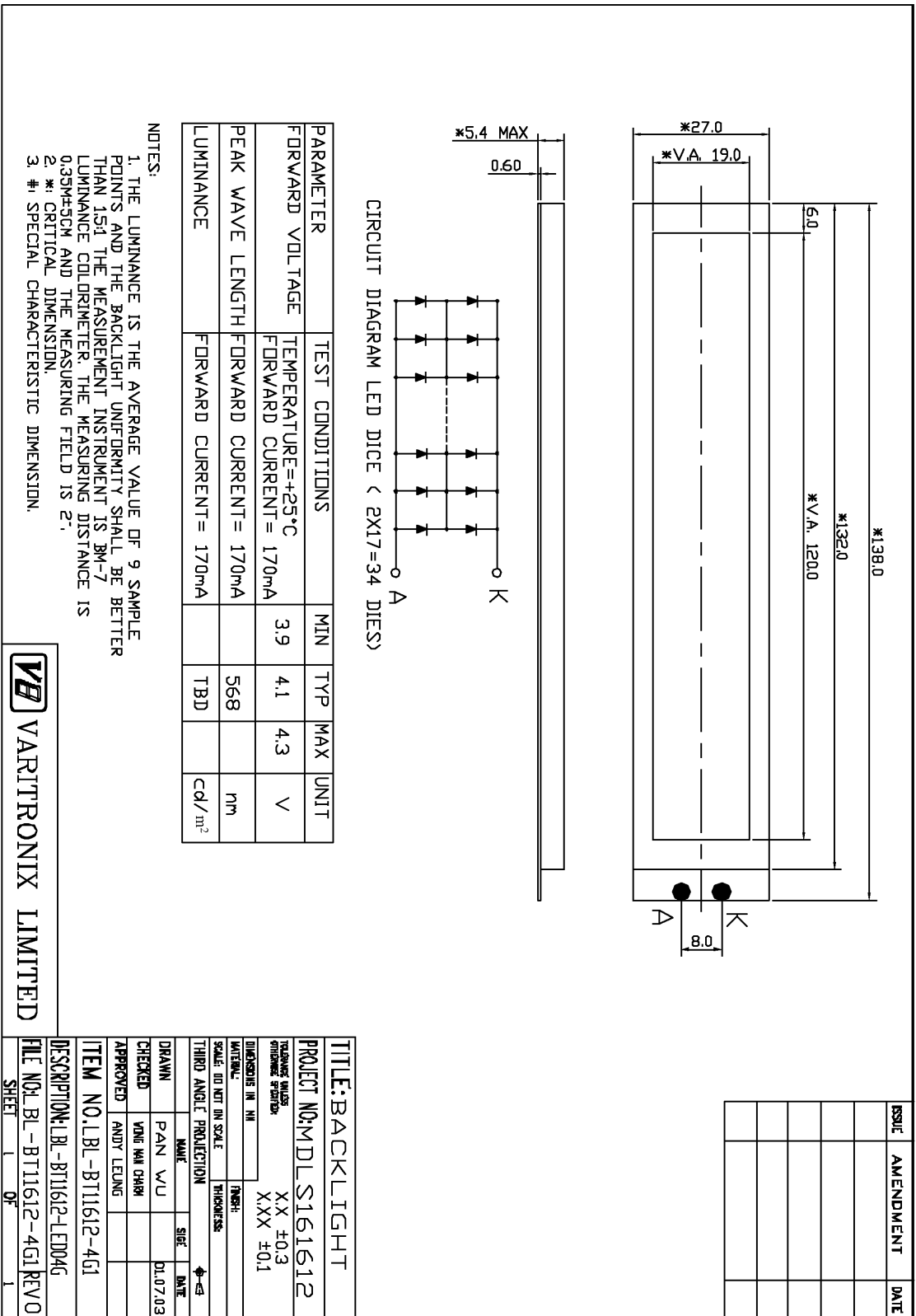


Figure 2: Backlight Drawing



### 3. Interface signals

Table 2

Pin No.	Symbol	Description
1	VSS	Ground(0V).
2	VDD	Power supply for logic (+5V).
3	V0	Power supply for LCD driver.
4	RS	Register Select Input: "High" for Data register (for read and write) "Low" for Instruction register (for write), Busy flag, address counter (for read).
5	R/W	Read/Write signal: "High" for Read mode. "Low" for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Data input/output (LSB).
8	DB1	Data input/output.
9	DB2	Data input/output.
10	DB3	Data input/output.
11	DB4	Data input/output.
12	DB5	Data input/output.
13	DB6	Data input/output.
14	DB7	Data input/output (MSB).
15 or A	LED(+)	Anode of LED backlight.
16 or K	LED(-)	Cathode of LED backlight.



#### 4. Absolute Maximum Ratings

##### 4.1 Electrical Maximum Ratings(Ta = 25 °C)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD – VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD=VDD – V0	-0.3	+13.5	V
Input voltage	Vin	-0.3	VDD +0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

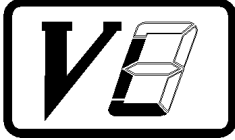
All voltage values are referenced to VSS = 0V.

##### 4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s <sup>2</sup> = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions





## 5. Electrical Specifications

### 5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 5V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.00	5.25	V
Supply voltage (LCD)	VLCD =VDD-V0	VDD =5.0V, Note1.	4.1	4.5	4.9	V
Input signal voltage for E,DB0-DB7,R/W,RS.	V <sub>IH</sub>	"H" level	2.2	-	VDD	V
	V <sub>IL</sub>	"L" level	-0.3	-	0.8	V
Supply Current (Logic & LCD)	IDD	Character mode, Note 1	-	1.4	2.1	mA
Supply Current (LCD)	I0	Character mode, Note 1	-	1.0	1.5	mA
Supply Voltage of yellow-green LED04 backlight	VLED04	Forward current =170 mA  No. of LED chips =2x17 =34	3.9	4.1	4.3	V

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.



## 5.2 Timing Specifications

At  $T_a = 0\text{ }^{\circ}\text{C}$  To  $+50\text{ }^{\circ}\text{C}$  ,  $V_{DD} = +5V \pm 5\%$  ,  $V_{SS} = 0V$ .

Refer to Fig. 3, the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit	Remarks
Enable cycle time	$t_{CYCE}$	500	-	ns	
Enable "High" level pulse width	$t_{WHE}$	300	-	ns	
Enable rise time	$t_{RE}$	-	25	ns	
Enable fall time	$t_{FE}$	-	25	ns	
RS, R/W set-up time	$t_{AS}$	60	-	ns	8-bit operation mode
		100			4-bit operation mode
RS, R/W address hold time	$t_{AH}$	10	-	ns	
Data output delay	$t_{DS}$	100	-	ns	
Data hold time	$t_{DHR}$	10	-	ns	

Refer to Fig. 4, the bus timing diagram for read mode .

Table 7

Parameter	Symbol	Min.	Max.	Unit	Remarks
Enable cycle time	$t_{CYCE}$	500	-	ns	
Enable "High" level pulse width	$t_{WHE}$	300	-	ns	
Enable rise time	$t_{RE}$	-	25	ns	
Enable fall time	$t_{FE}$	-	25	ns	
RS, R/W set-up time	$t_{AS}$	60	-	ns	8-bit operation mode
		100			4-bit operation mode
RS, R/W address hold time	$t_{AH}$	10	-	ns	
Read data output delay	$t_{RD}$	-	190	ns	
Read data hold time	$t_{DHR}$	20	-	ns	

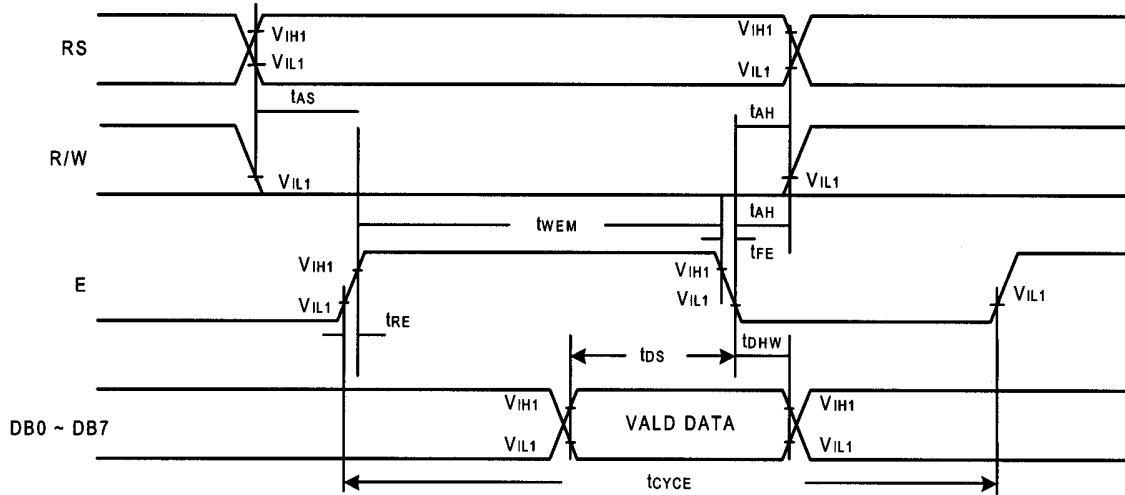


Figure 3: Bus write operation sequence (Writing data from MPU to NT3881).

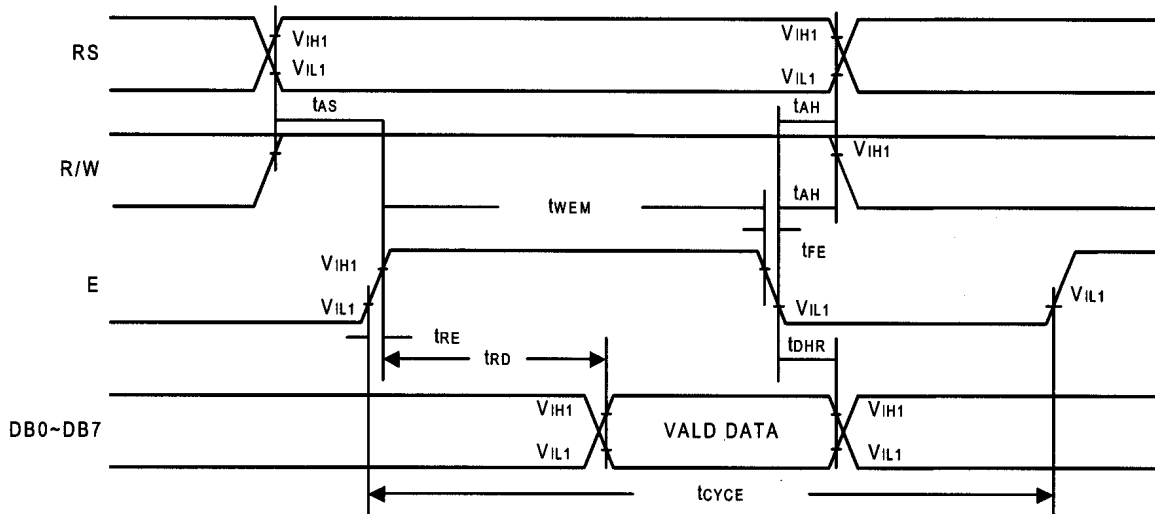


Figure 4: Bus read operation sequence (Reading out data from NT3881 to MPU).



### 5.3 Timing Diagram of VDD against V0.

Power on sequence shall meet the requirement of Figure 5, the timing diagram of VDD against V0.

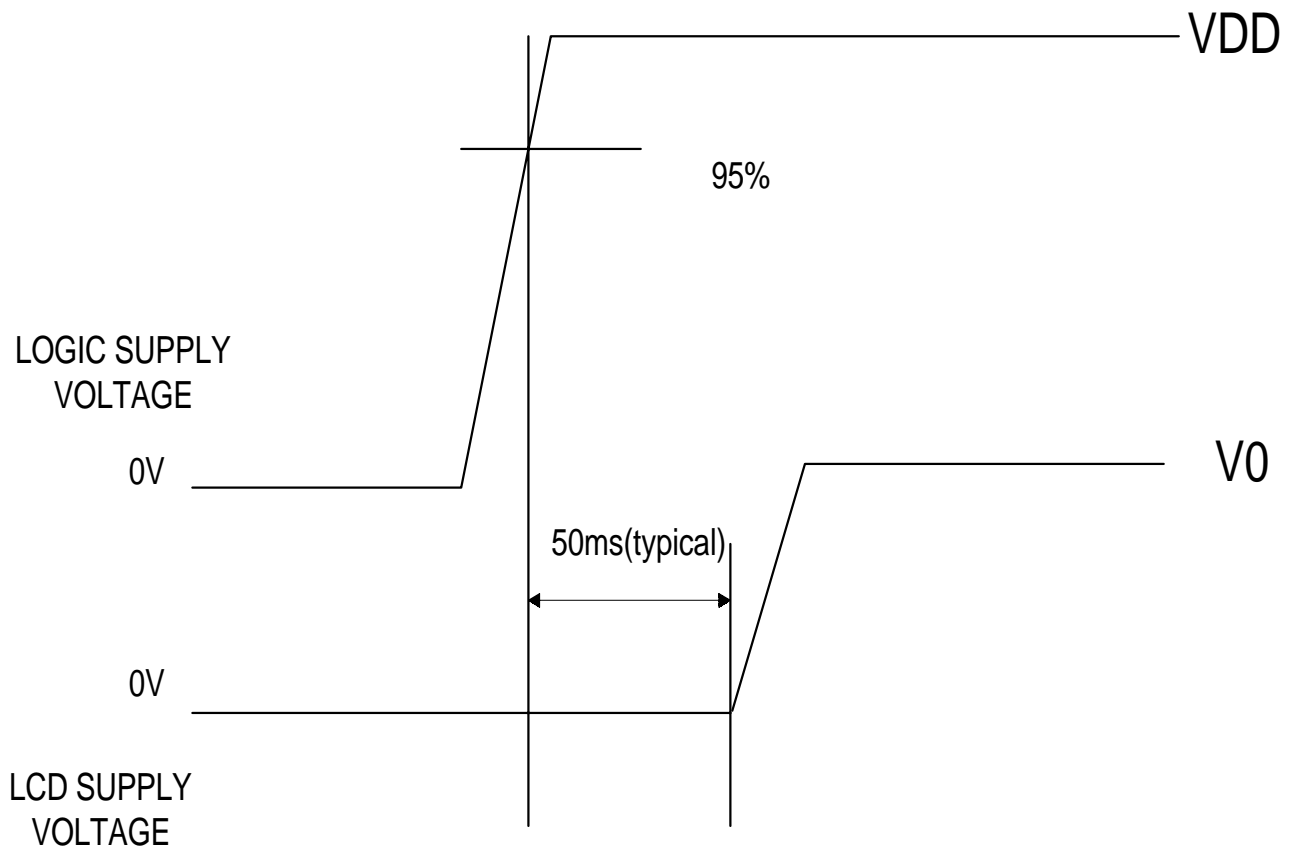


Figure 5: Timing diagram of VDD against V0.



**5.4 Correspondence between Character Codes and Character Patterns  
 (NOVATEK Standard NT3881D-01)**

		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	0	CG RAM (1)			0	@	P	`	P					一	夕	ミ	α	ρ
	1	CG RAM (2)		!	1	A	Q	a	q				。	ア	チ	△	Δ	q
	2	CG RAM (3)		"	2	B	R	b	r				「	イ	ツ	×	β	θ
	3	CG RAM (4)		#	3	C	S	c	s				」	ウ	テ	モ	ε	ω
	4	CG RAM (5)		\$	4	D	T	d	t				、	エ	ト	ト	μ	Ω
	5	CG RAM (6)		%	5	E	U	e	u				、	オ	ナ	1	ε	ü
	6	CG RAM (7)		&	6	F	V	f	v				ヲ	カ	ニ	ヨ	ρ	Σ
	7	CG RAM (8)		'	7	G	W	g	w				ア	キ	ヌ	ラ	g	π
	8	CG RAM (1)		(	8	H	X	h	x				イ	ク	ネ	リ	γ	⊗
	9	CG RAM (2)		)	9	I	Y	i	y				ウ	ケ	ル	ル	γ	γ
	A	CG RAM (3)		*	:	J	Z	j	z				エ	コ	ル	レ	j	〒
	B	CG RAM (4)		+	;	K	[	k	[				オ	サ	ヒ	ロ	*	〒
	C	CG RAM (5)		,	<	L	¥	l	l				カ	シ	フ	ワ	φ	〒
	D	CG RAM (6)		-	=	M	]	m	]				ユ	ズ	ン	ト	ト	÷
	E	CG RAM (7)		.	>	N	^	n	→				ヨ	セ	ホ	ン	ん	
	F	CG RAM (8)		/	?	0	_	o	+				ッ	ッ	マ	マ	ö	

“Varitronix Limited reserves the right to change this specification.”

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