

am^u OSRAM Preliminary PCN

AO-PCN-2022-013-N

Introduction of 2nd source for classic InGaAlP chip for TOPLED

Customer information package

OS Q CQM AM ITR
15.04.2022

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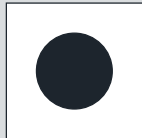
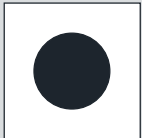
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Reason for change

Item	Description
1.	Secure continuous supply
2.	Introduction of additional supplier chips
3.	Introduction of additional production location of released plater



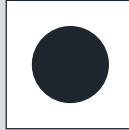
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Description of change for standard chips

Item	Current status	2 nd source chip A	2 nd source chip B	2 nd source chip C
Wafer size [mm]	100	100	100	100
Wafer substrate	GaAs	GaAs	GaAs	GaAs
Height [μm]	220	175	180	180
Chip dicing process	Sawing	Sawing	Sawing	Sawing
Picture (schematic)				
Chip size [μm]	200 x 200	200 x 200	180 x 180	180 x 180
Front metal type	Al	Au	Au	Au
Front metal thickness [μm]	1.50	2.50	2.90	2.25
Back metal type	Au	Au	Au	Au
Back metal thickness [μm]	0.25	0.05	0.50	0.35
Bond pad size [μm]	100	100	100	100
Wafer Fab location	Regensburg/Germany	Supplier	Supplier	Supplier

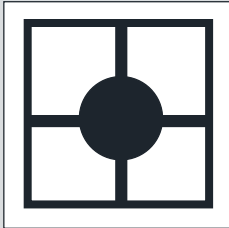
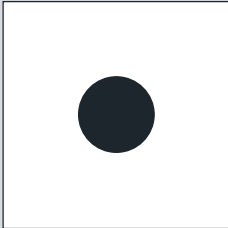
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Description of change for low current chips

Item	Current status	2 nd source chip D	2 nd source chip E
Wafer size [mm]	100	100	100
Wafer substrate	GaAs	GaAs	GaAs
Height [μm]	190	180	180
Chip dicing process	Sawing	Sawing	Sawing
Picture (schematic)			
Chip size [μm]	170 x 170	160 x 160	170 x 170
Front metal type	Al	Au	Au
Front metal thickness [μm]	1.50	2.90	2.25
Back metal type	Au	Au	Au
Back metal thickness [μm]	0.25	0.50	0.35
Bond pad size [μm]	100	90	100
Wafer Fab location	Regensburg/Germany	Supplier	Supplier

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Description of change for HOP Chip

Item	Current status	2 nd source chip F
Wafer size [mm]	100	100
Wafer substrate	GaAs	GaAs
Height [μm]	220	220
Chip dicing process	Sawing	Sawing
Picture (schematic)		
Chip size [μm]	300 x 300	300 x 300
Front metal type	Al	Au
Front metal thickness [μm]	1.50	2.25
Back metal type	Au	Au
Back metal thickness [μm]	0.25	0.35
Bond pad size [μm]	110	100
Wafer fab location	Regensburg/Germany	Supplier

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Description of change for all devices

Current status	New status
Plater location: Wuxi/China	Plater location: Wuxi & Shanghai/China

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List of affected products

Standard				
Brand	Device	Chip A	Chip B	Chip C
TOPLED	LS T676		X	X
	LA T676	X		X
	LO T676		X	X
	LY T676	X	X	
	LG T676	X		X
	LP T676		X	X
Low current				
Brand	Device	Chip D	Chip E	
TOPLED	LS T67K	X	X	
	LO T67K		X	
	LY T67K	X	X	
	LG T67K	X	X	
HOP				
Brand	Device	Chip F		
TOPLED	LP T675	X		

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PCN Samples (planned availability at Final PCN publication)

Standard	Low current	HOP
LS T676	LS T67K	LP T675
LA T676	LO T67K	
LO T676	LY T67K	
LY T676	LG T67K	
LG T676		
LP T676		

Color code: available on request

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Qualification Plan

Test item	Test condition	Test duration
Wet High Temperature Operating Life WHTOL1	$T_A = 85^\circ\text{C}$; r.H. = 85%; $I_F = \text{max. acc. to datasheet}$; $T_{\text{on/off}} = 30 \text{ min}$	1000 h
Wet High Temperature Operating Life WHTOL2	$T_A = 85^\circ\text{C}$; r.H. = 85%; $I_F = \text{min. acc. to datasheet}$	1000 h
Powered Temperature Cycle PTC	$T_A = -40/+85^\circ\text{C}$; $I_F = \text{max acc. to derating curve}$	1000 c
Temperature Cycling TC	$T_A = -40/+100^\circ\text{C}$; 15 min each extrem	1000 c
High Temperature Operating Life HTOL1	$T_s = \text{max acc. to datasheet}$; $I_F = \text{corresponding max. acc. to derating curve}$	1000 h
High Temperature Operating Life HTOL2	$I_F = \text{max acc. to datasheet}$; $T_s = \text{corresponding max. acc. to derating curve}$	1000 h
Pulsed Operating Life PLT	$T_A = 25^\circ\text{C}$; $I_F = \text{max acc. to datasheet}$; $t_p = 0,1 \text{ ms}$; $D = 3\%$	1000 h

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Qualification Plan

Test item	Test condition	Test duration
DEW	$T_{A,min} = 10^{\circ}\text{C}$; $T_{A,max} = 80^{\circ}\text{C}$; r.H. = 53-100%	10 c
H ₂ S	$T_A = 40^{\circ}\text{C}$; r.H. = 90%; 15 ppm H ₂ S	336 h
Flowing Mixed Gas FMG	$T_A = 25^{\circ}\text{C}$, r.H. = 75%; Test method 4	500 h
Board Flex BF	2 mm	1 x
Electrostatic Discharge HBM	Human Body Model	2000 V
Electrostatic Discharge CDM	Charged Device Model	750 V

Note:

- Planned devices for qualification tests: LS T676, LA T676, LO T676, LY T676, LG T676, LP T676, LS T67K, LY T67K, LG T67K, LP T675 (please refer to next slide)

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Test vehicle overview

Standard				
Brand	Device	Chip A	Chip B	Chip C
TOPLED	LS T676		1 lot	1 lot
	LA T676	1 lot		
	LO T676			1 lot
	LY T676	1 lot	1 lot	
	LG T676	1 lot		
	LP T676			1 lot
Low current				
Brand	Device	Chip D	Chip E	
TOPLED	LS T67K	1 lot	1 lot	
	LO T67K			
	LY T67K	1 lot	1 lot	
	LG T67K	1 lot	1 lot	
HOP				
Brand	Device	Chip F		
TOPLED	LP T675	3 lot		

Note:

- Qualification results expected for: 07/2022

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Time schedule

for publication final PCN:	01.07.2022	
for PCN material (<u>after</u> implementation of change):		
Final qualification report	01.07.2022	
Samples available	01.07.2022	
Intended Start of delivery	01.12.2022 *)	*) or earlier if released by customer and upon mutual agreement
Customer Review Finalization:	01.07.2023 **)	***) Expected final feedback of customer. Released order volume is related to deliveries of material from both previous and additional source(s).

Note:
Pre-PCN material: Products of current status, means before implementation of the changes as described in the PCN.
PCN material: Products with implementation of the changes as described in the PCN.

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