

50 V moisture resistant DMOS transistor for ISM applications

Datasheet - production data

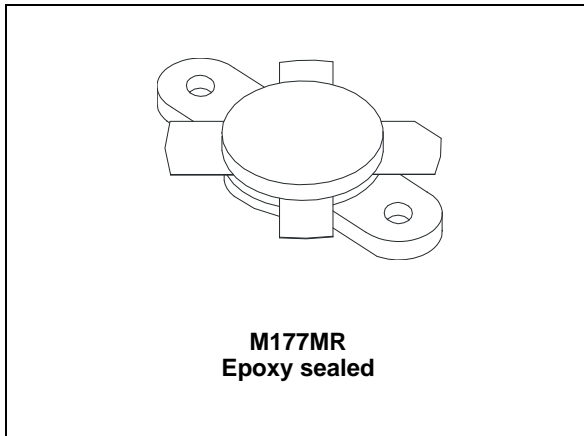
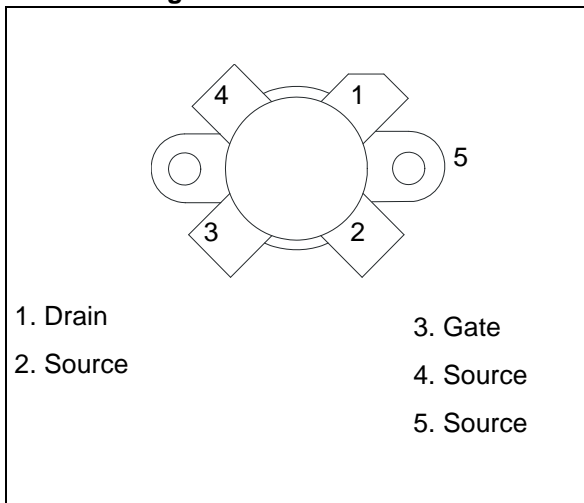


Figure 1. Pin connection



Features

- Improved ruggedness $V_{(BR)DSS} > 200\text{ V}$
- Excellent thermal stability
- 20:1 all phases load mismatch capability
- $P_{OUT} = 300\text{ W}$ min. with 24 dB gain @ 30 MHz
- In compliance with the 2002/95/EEC European directive
- Moisture resistant package specifically designed to operate under extreme environments

Description

The SD4933MR is an N-channel MOS field-effect RF power transistor. It is intended for use in 50 V ISM applications up to 100 MHz.

The SD4933MR benefits from the latest generation of environmentally designed packaging, ruggedized against cyclic high moisture operating and severe storage conditions.

Table 1. Device summary

Order code	Marking	Base qty.	Package	Packaging
SD4933MR	SD4933MR ⁽¹⁾	25 pcs	M177MR	Plastic tray

1. For more details please refer to [Chapter 8: Marking, packing and shipping specifications](#).

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1 Electrical data

1.1 Maximum ratings

($T_{CASE} = 25\text{ °C}$)

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain source voltage	200	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 1\text{ M}\Omega$)	200	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current	40	A
P_{DISS}	Power dissipation	648	W
E_{AS}	Avalanche energy Single pulse ($I_D = 56\text{ A} - 800\text{ }\mu\text{H}$ coil)	1200	mJ
T_J	Max. operating junction temperature	200	$^{\circ}\text{C}$
T_{STG}	Storage temperature	-65 to +150	$^{\circ}\text{C}$

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.27	$^{\circ}\text{C/W}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$)

2.1 Static

Table 4. Static

Symbol	Test conditions		Min	Typ	Max	Unit
$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$	$I_{DS} = 100\text{ mA}$	200	240		V
I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 100\text{ V}$			2	mA
I_{GSS}	$V_{GS} = 20\text{ V}$	$V_{DS} = 0\text{ V}$			1	μA
V_{TH}	$I_D = 250\text{ mA}$		2.5		3.75	V
$V_{DS(ON)}$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$		3.5	4.0	V
G_{FS}	$V_{DS} = 10\text{ V}$	$I_D = 5\text{ A}$	8		14	S
C_{ISS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 50\text{ V}$		1000		pF
C_{OSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 50\text{ V}$		400		pF
C_{RSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 50\text{ V}$		16		pF

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions		Min	Typ	Max	Unit
P_{OUT}	$V_{DD} = 50\text{ V}$	$I_{DQ} = 250\text{ mA}$ $f = 30\text{ MHz}$	300		-	W
G_{PS}	$V_{DD} = 50\text{ V}$	$I_{DQ} = 250\text{ mA}$ $P_{OUT} = 300\text{ W}$ $f = 30\text{ MHz}$	20	24	-	dB
h_D	$V_{DD} = 50\text{ V}$	$I_{DQ} = 250\text{ mA}$ $P_{OUT} = 300\text{ W}$ $f = 30\text{ MHz}$	50	58	-	%
Load mismatch	$V_{DD} = 50\text{ V}$	$I_{DQ} = 250\text{ mA}$ $P_{OUT} = 300\text{ W}$ $f = 30\text{ MHz}$ All phase angles	10:1	20:1	-	VSWR

3 Impedance data

Figure 2. Impedance data

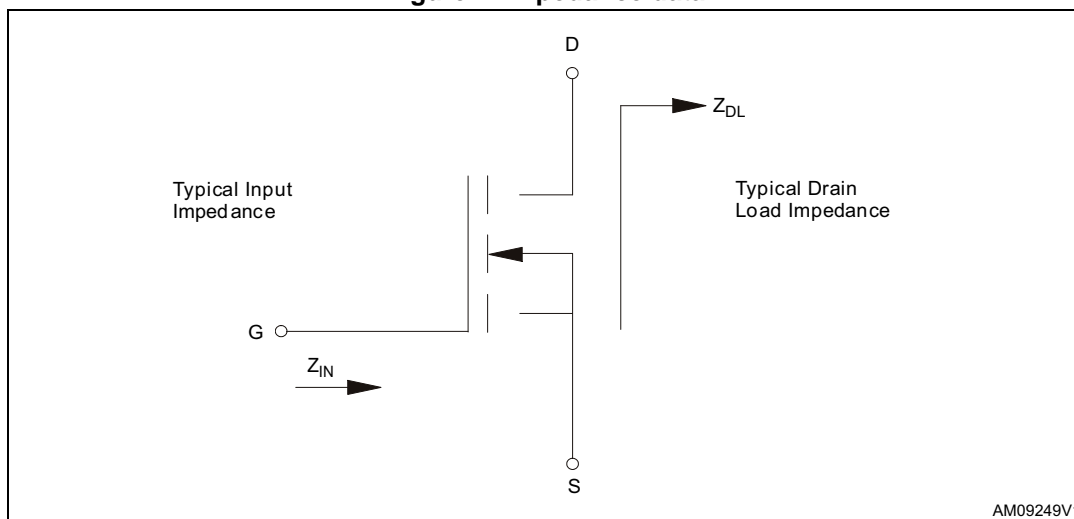


Table 6. Impedance values

Z_{in}	Z_{dl}
1.6 - j 5.0	3.3 + j 1.0

4 Typical performance

Figure 3. Capacitance vs. drain voltage

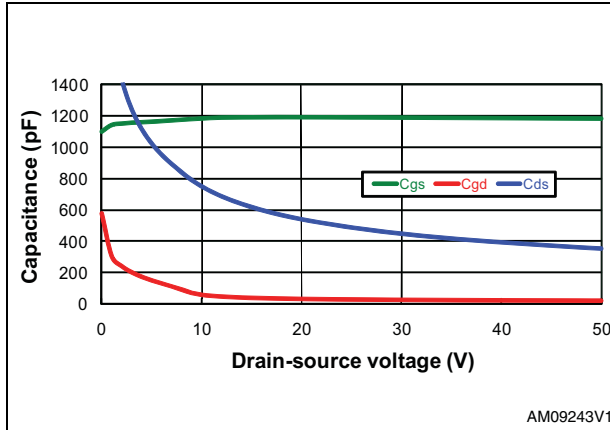


Figure 4. Drain current vs. drain-source voltage

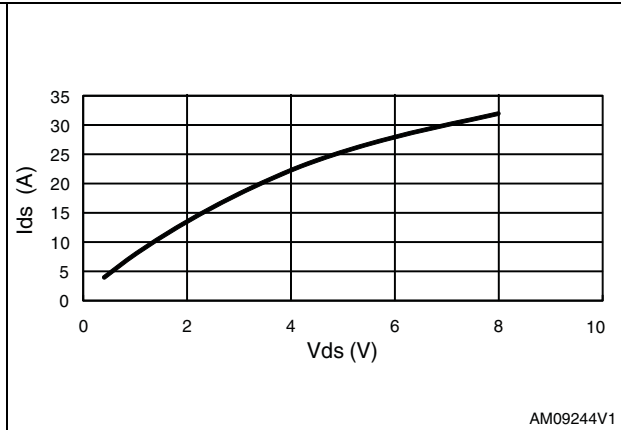


Figure 5. Drain current vs. drain-source voltage at different temperatures

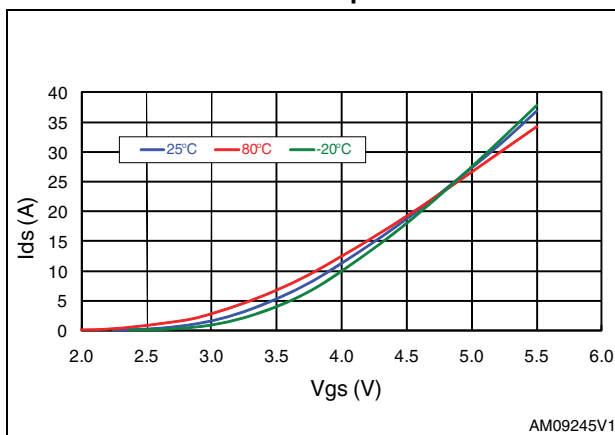


Figure 6. Transient thermal impedance

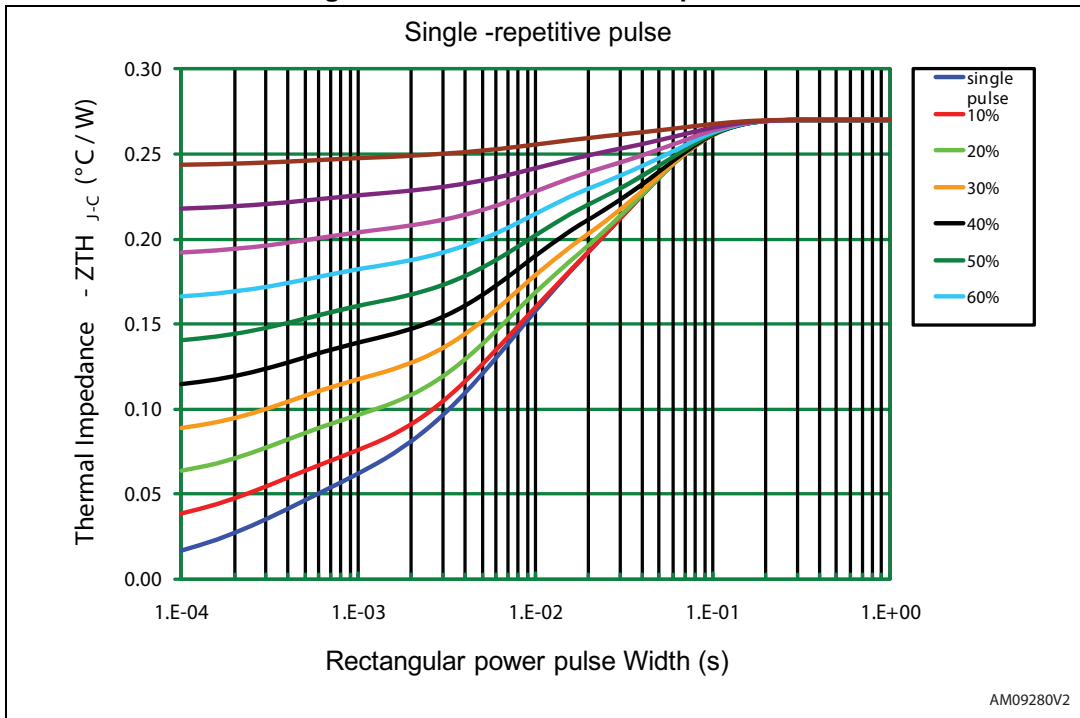
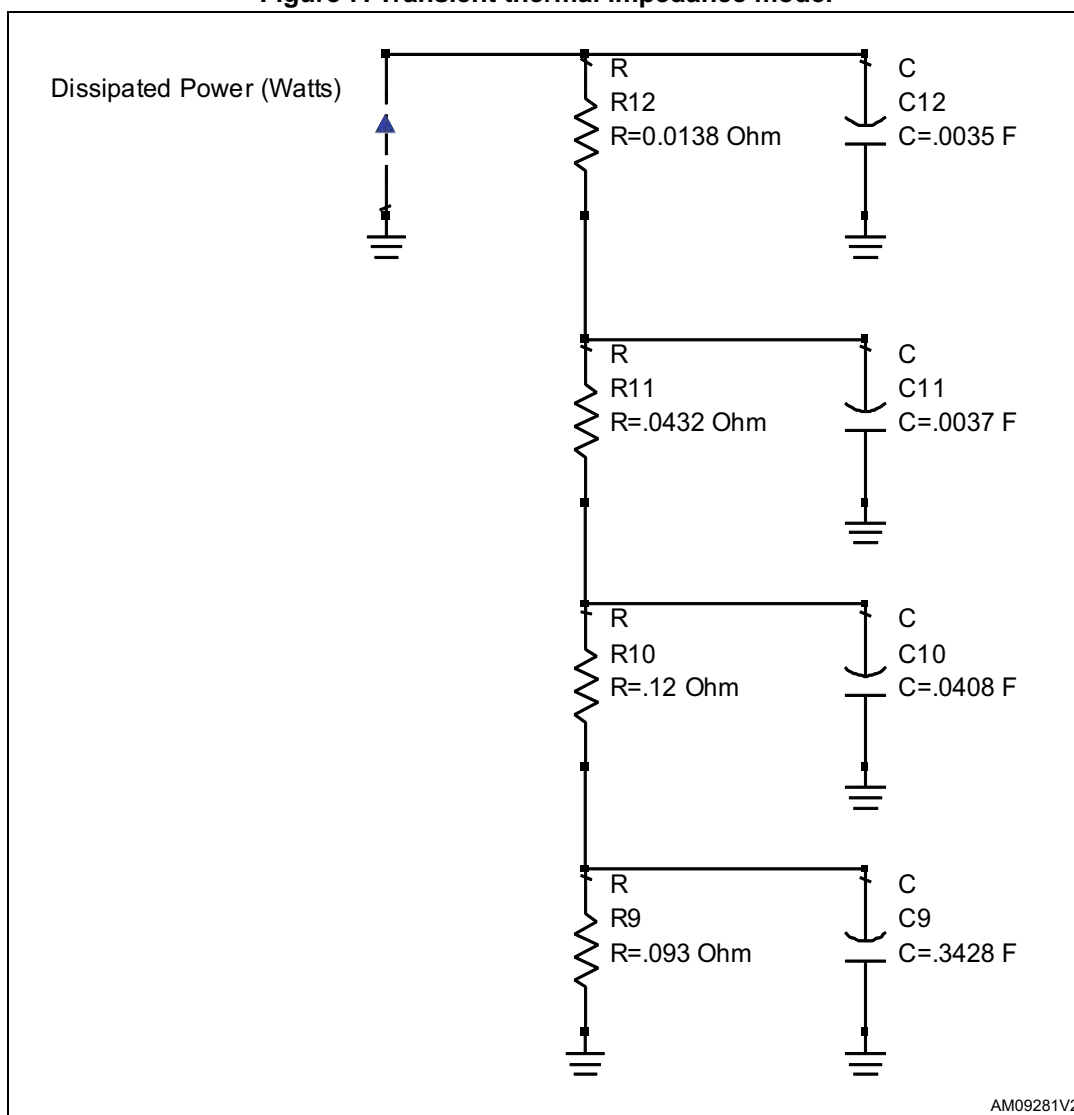


Figure 7. Transient thermal impedance model



5 Typical performance (30 MHz)

Figure 8. Gain and efficiency vs. output power at $V_{dd} = 50\text{ V}$, $I_{dq} = 250\text{ mA}$, $f_{req} = 30\text{ MHz}$

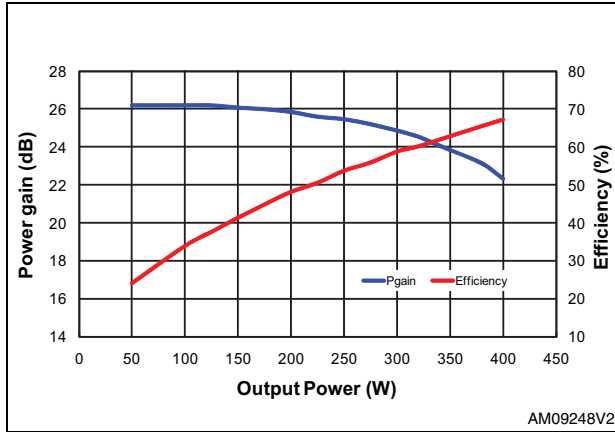


Figure 9. Output power vs. input power

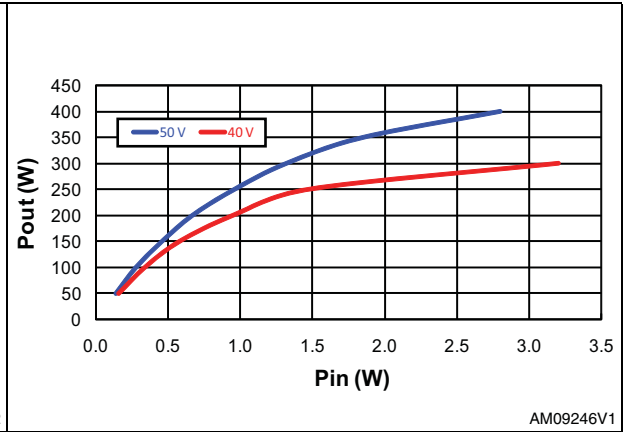


Figure 10. Output power vs. supply voltage

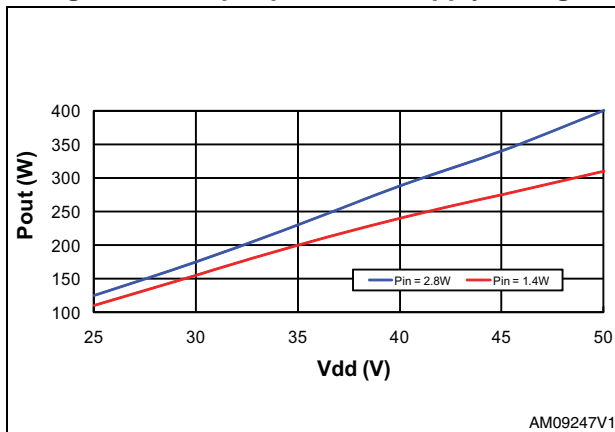
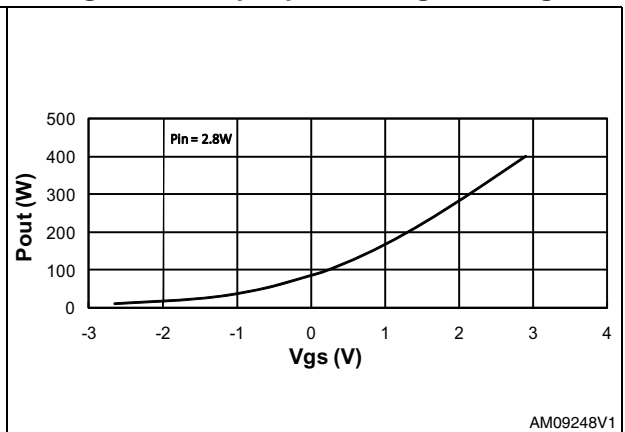


Figure 11. Output power vs. gate voltage



5.1 Test circuit (30 MHz)

Figure 12. 30 MHz test circuit schematic

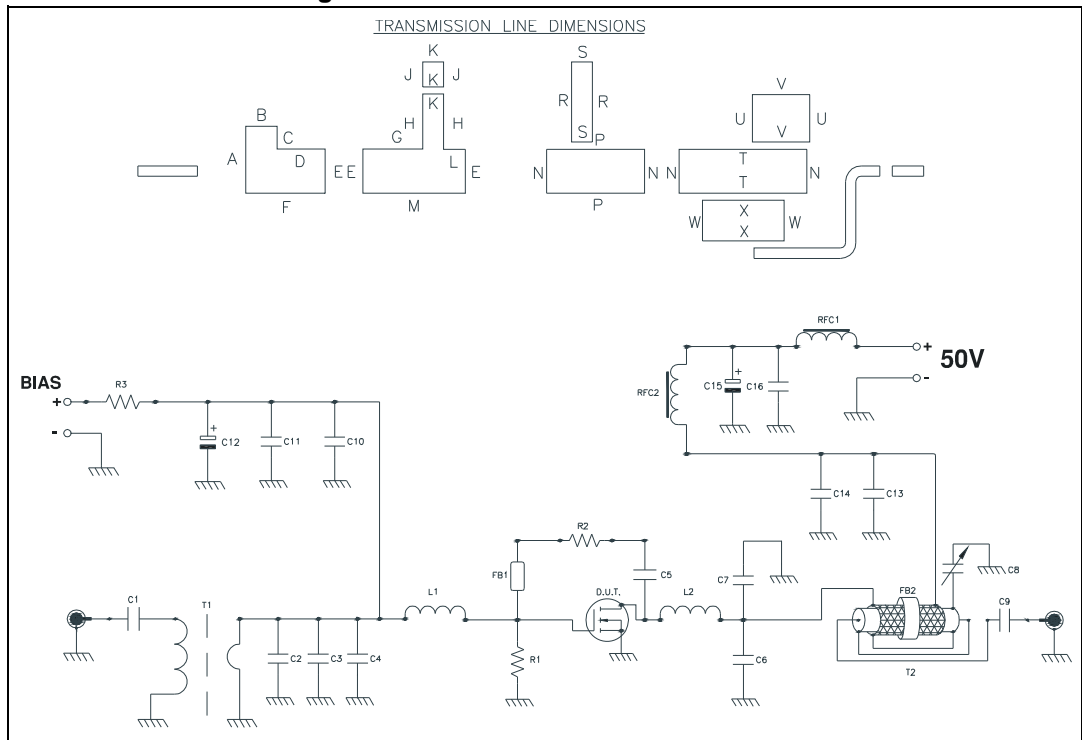


Table 7. Transmission line dimensions

Dim.	Inch	mm
A	0.532	13.51
B	0.250	6.35
C	0.181	4.59
D	0.383	9.37
E	0.351	8.91
F	0.633	16.08
G	0.477	12.12
H	0.438	11.12
J	0.200	5.08
K	0.164	4.16
L	0.174	4.42
M	0.817	20.75
N	0.350	8.89
P	0.779	19.79
R	0.639	16.23

Table 7. Transmission line dimensions (continued)

Dim.	Inch	mm
S	0.165	4.19
T	1.017	25.84
U	0.375	9.52
V	0.456	11.58
W	0.325	8.24
X	0.650	16.50

Table 8. 30 MHz test circuit component list

Component	Description
C1,C9	0.01 μ F / 500 V surface mount ceramic chip capacitor
C2, C3	750 pF ATC 700B surface mount ceramic chip capacitor
C4	300 pF ATC 700B surface mount ceramic chip capacitor
C5,C10,C11,C14,C16	10000 pF ATC 200B surface mount ceramic chip capacitor
C6	510 pF ATC 700B surface mount ceramic chip capacitor
C7	300 pF ATC 700B surface mount ceramic chip capacitor
C8	175-680 pF type 46 standard trimmer capacitor
C12	47 μ F / 63 V aluminum electrolytic radial lead capacitor
C13	1200 pF ATC 700B surface mount ceramic chip capacitor
C15	100 μ F / 63 V aluminum electrolytic radial lead capacitor
R1,R3	1 K OHM 1 W surface mount chip resistor
R2	560 OHM 2 W wire-wound axils lead resistor
T1	HF 2-30 MHz surface mount 9:1 transformer
T2	RG - 142B/U 50 OHM coaxial cable OD = 0.165[4.18] L 15"[381.00] covered with 15"[381.00] tinned copper tubular brand 13/65" [5.1] width
L1	1 3/4 turn air-wound 16 AWG ID = 0.219 [5.56] poly-coated magnet wire
L2	1 3/4 turn air-wound 12 AWG ID = 0.250 [6.34] bus bar wire
RFC1,RFC2	3 turns 14 AWG wire through ferrite toroid
FB1	Surface mount EMI shield bead
FB2	Toroid
PCB	ULTRALAM 2000. 0.030" THK, $\epsilon_r = 2.55$, 2 Oz ED CU both sides

6 Circuit layout

Figure 13. Test fixture component layout

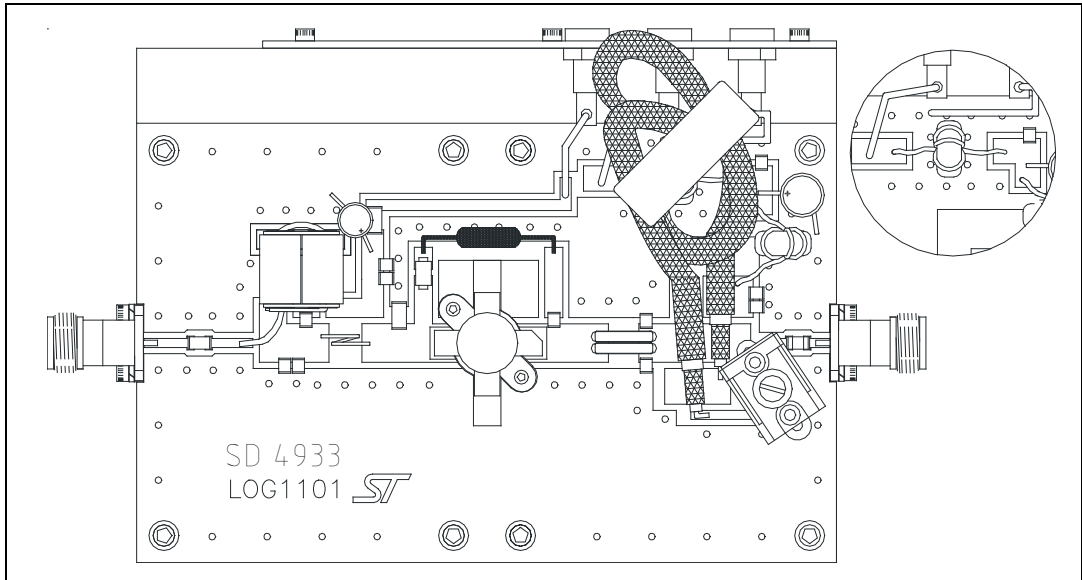
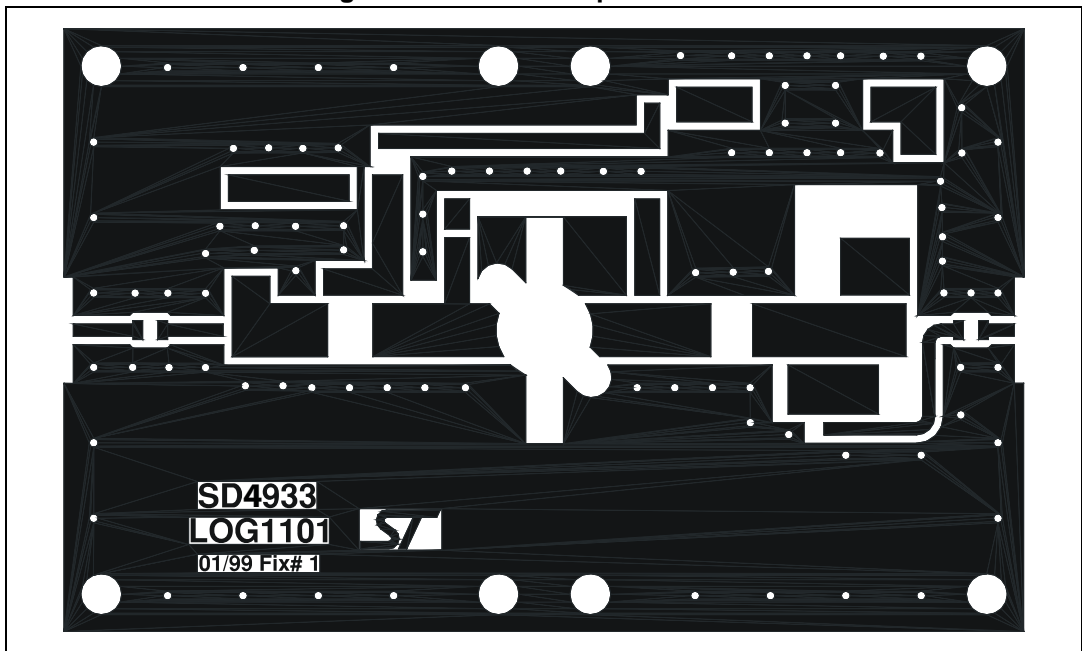


Figure 14. Test circuit photomasters



7 V_{GS}/G_{FS} sorts

Table 9. V_{GS}/G_{FS} sorts

Marking	V _{GS} (min)	V _{GS} (max)	G _{FS} (min)	G _{FS} (max)
E4	2.50	2.75	8	9
E5	2.50	2.75	9	10
E6	2.50	2.75	10	11
E7	2.50	2.75	11	12
E8	2.50	2.75	12	13
E9	2.50	2.75	13	14
F4	2.75	3.00	8	9
F5	2.75	3.00	9	10
F6	2.75	3.00	10	11
F7	2.75	3.00	11	12
F8	2.75	3.00	12	13
F9	2.75	3.00	13	14
G4	3.00	3.25	8	9
G5	3.00	3.25	9	10
G6	3.00	3.25	10	11
G7	3.00	3.25	11	12
G8	3.00	3.25	12	13
G9	3.00	3.25	13	14
H4	3.25	3.50	8	9
H5	3.25	3.50	9	10
H6	3.25	3.50	10	11
H7	3.25	3.50	11	12
H8	3.25	3.50	12	13
H9	3.25	3.50	13	14
I4	3.50	3.75	8	9
I5	3.50	3.75	9	10
I6	3.50	3.75	10	11
I7	3.50	3.75	11	12
I8	3.50	3.75	12	13
I9	3.50	3.75	13	14

8 Marking, packing and shipping specifications

Table 10. Packing and shipping specifications

Order code	Packaging	Pcs per tray	Dry pack humidity	Vgs and Gfs code	Lot code
SD4933MR	Plastic tray	25	< 10%	Not mixed	Not mixed

Figure 15. Marking layout

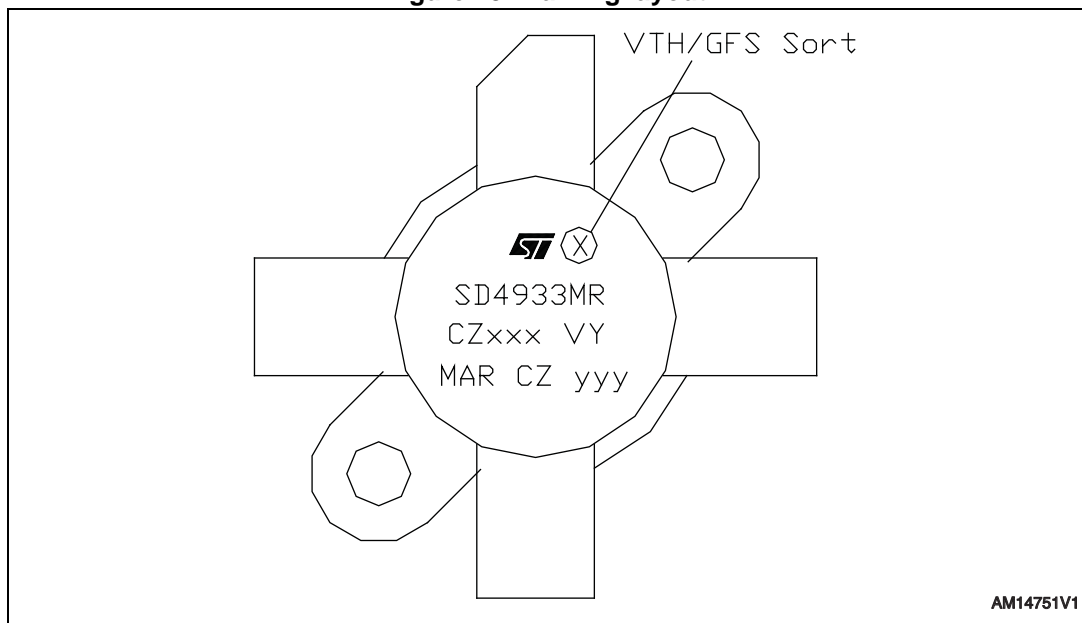


Table 11. Marking specifications

Symbol	Description
X	V _{GS} and G _{FS} sort
CZ	Assembly plant
xxx	Last 3 digits of diffusion lot
VY	Diffusion plant
MAR	Country of origin
CZ	Test and finishing plant
y	Assembly year
yy	Assembly week

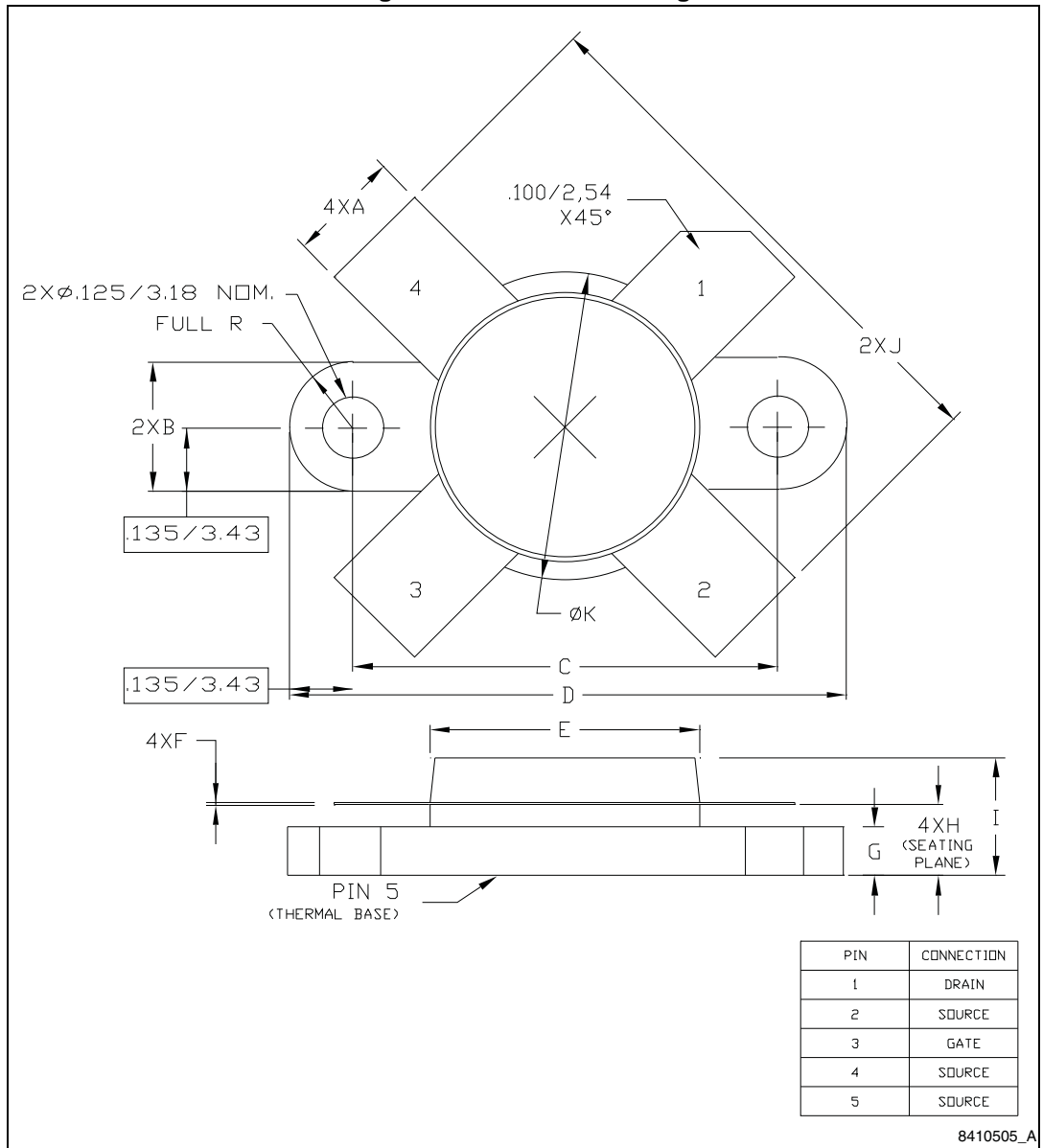
9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 12. M177MR mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.72		5.97
B	6.73		6.99
C	21.84		22.10
D	28.70		28.96
E	13.34		14.10
F	0.08		0.18
G	2.49		2.74
H	3.81		4.32
I			7.87
J	27.43		28.45
K	15.88		16.13

Figure 16. M177MR drawing



10 Revision history

Table 13. Document revision history

Date	Revision	Changes
13-Sep-2012	1	Initial release.
22-May-2013	2	Modified: I _{GSS} value in <i>Table 4: Static</i>
09-May-2017	3	Document status promoted from preliminary to production data. Updated <i>Table 4: Static</i> and <i>Table 9: V_{GS}/G_{FS} sorts</i> . Minor text changes.

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