AVR128DB28/32/48/64

AVR128DB28/32/48/64 Silicon Errata and Data Sheet Clarifications

The AVR128DB28/32/48/64 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002247), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the AVR128DB28/32/48/64 devices.

Notes:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002247) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1.   Silicon Issue Summary

Legend

-   Erratum is not applicable.

X   Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision	
		Rev. A4[1]	Rev. A5
Device	2.2.1 Some Reserved Fuse Bits are '1'	X	-
	2.2.2 Increased Current Consumption May Occur When VDD Drops	X	X
ADC	2.3.1 Increased Offset in Single-Ended Mode	X	-
CCL	2.4.1 The CCL Must be Disabled to Change the Configuration of a Single LUT	X	X
	2.4.2 The LINK Input Source Selection for LUT3 is Not Functional on 28- and 32-Pin Devices	X	-
CLKCTRL	2.5.1 External Clock/Crystal Status Bit is Not Set When the External Clock Source is Ready	X	-
	2.5.2 RUNSTDBY is Not Functional When Using External Clock Sources	X	-
	2.5.3 The PLL Will Not Run when Using XOSCHF with an External Crystal	X	X
OPAMP	2.6.1 OPAMP Consume More Power Than Expected	X	-
	2.6.2 The Input Range Select is Read-Only	X	-
PORT	2.7.1 PD0 Input Buffer is Floating	X	X
RSTCTRL	2.8.1 BOD Registers Not Reset When UPDI is Enabled	X	-
TCB	2.9.1 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X	X
TCD	2.10.1 Asynchronous Input Events Not Working When TCD Counter Prescaler is Used	X	X
	2.10.2 CMPAEN Controls All WOx For Alternative Pin Functions	X	X
TWI	2.11.1 The Output Pin Override Does Not Function as Expected	X	X
USART	2.12.1 Open-Drain Mode Does Not Work When TXD is Configured as Output	X	X
	2.12.2 Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'	X	X
ZCD	2.13.1 All ZCD Output Selection Bits are Tied to the ZCD0 Bit	X	-

Note:
1.   This revision is the initial release of the silicon.

2. Silicon Errata Issues

2.1 Errata Details

- Erratum is not applicable.

X Erratum is applicable.

2.2 Device

2.2.1 Some Reserved Fuse Bits are '1'

For material with date code 2021 (manufactured in year 2020, week 21) or older, the default fuse values are not compliant with the data sheet. The fuse values will read out as listed below:

- BODCFG = `0x10`
- OSCCFG = `0x78` (Device will use the OSCHF clock source)
- SYSCFG0 = `0xF6`
- SYSCFG1 = `0xE8`

Work Around
None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.2.2 Increased Current Consumption May Occur When V_{DD} Drops

The device may experience increased current consumption of approximately 1.5 mA if V_{DD} drops below 2.1V and is held in the range 1.9-2.1V. This will only occur if V_{DD} is originally at a higher level and then drops down to the mentioned voltage range.

Work Around
Ensure V_{DD} is always kept above 2.1V by setting the BOR trigger level to 2.2V to keep the device from executing if V_{DD} drops towards the affected voltage range. If operation in voltage range 1.9-2.1V is required, make sure V_{DD} does not rise above 2.1V and then drops down again. Note that the voltage levels given are not absolute values but typical values.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.3 ADC - Analog-to-Digital Converter

2.3.1 Increased Offset in Single-Ended Mode

The ADC result has a typical offset of -3 mV (V_{DD} = 3.0V, Temp = 25°C) when the ADC is operating in single-ended mode. The typical offset drift vs. V_{DD} is -0.3 mV/V, and the typical offset drift vs. temperature is -0.02 mV/°C.

Work Around

To reduce the offset, use the ADC in differential mode and connect the negative ADC input pin externally to GND.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.4 CCL - Configurable Custom Logic

2.4.1 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure a LUT, the CCL peripheral must be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

Work Around
None

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.4.2 The LINK Input Source Selection for LUT3 is Not Functional on 28- and 32-Pin Devices

The LINK option (INSELn in LUT3CTRLB or LUT3CTRLC is '0x2') does not work; the output from LUT0 will not get connected as an input to LUT3. This occurs only on 28-pin and 32-pin devices.

Work Around
Connect LUT0 output to LUT3 input using the event system.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.5 CLKCTRL - Clock Controller

2.5.1 External Clock/Crystal Status Bit is Not Set When the External Clock Source is Ready

If an external clock source is selected (SELHF in XOSCHFCTRLA is '1') and the Run Standby (RUNSTDBY) bit in XOSCHFCTRLA is '1' without the clock source being requested, the External Clock/Crystal Status (EXTS) bit will not be set to '1' when the external clock source is ready.

Work Around
Request the clock from RTC or TCD before checking the EXTS bit.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.5.2 RUNSTDBY is Not Functional When Using External Clock Sources

When using any of the External Clock Sources, the related Run Standby (RUNSTDBY) bit, found in the XOSC32KCTRLA register, will not force the oscillator source to stay on during sleep modes.

Work Around

Enable a peripheral, with the external oscillator as the clock source, to keep the clock source active during sleep modes.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.5.3 The PLL Will Not Run when Using XOSCHF with an External Crystal

When the PLL is configured to run from an external source (SOURCE in CLKCTRL.PLLCTRLA is '1'), the PLL will only run if XOSCHF is configured to use an external clock (SELHF in CLKCTRL.XOSCHFCTRLA is '1'). It will not work with an external crystal.

Work Around

None

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.6 OPAMP - Analog Signal Conditioning

2.6.1 OPAMP Consume More Power Than Expected

The OPAMP peripheral consumes up to three times more current than specified when the output is driven closer to either the upper or lower rails.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.6.2 The Input Range Select is Read-Only

The Input Range Select (IRSEL) bit is read-only. When the Analog Signal Conditioning (OPAMP) peripheral is active, the input voltage range will be rail-to-rail.

Work Around

None.

Affected Silicon Revisions

Rev. A4	Rev. A5

X	-

2.7 PORT - I/O Configuration

2.7.1 PD0 Input Buffer is Floating

On 28- and 32-pin package parts, the PD0 input buffer is floating. Because the default direction setting for PD0 is as an input pin, this may cause unexpected current consumption.

Work Around

Disable the PD0 input (ISC in PORTD.PIN0CTRL) or configure the pin as an output (bit 0 in PORTD.DIR).

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.8 RSTCTRL - Reset Controller

2.8.1 BOD Registers Not Reset When UPDI is Enabled

The VLMCTRL, INTCTRL and INTFLAGS registers in BOD will not be reset by other reset sources than POR if the UPDI is enabled.

Work Around

None

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

2.9 TCB - 12-Bit Timer/Counter Type B

2.9.1 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.10 TCD - 12-Bit Timer/Counter Type D

2.10.1 Asynchronous Input Events Not Working When TCD Counter Prescaler is Used

When the TCD is configured to use asynchronous input events (CFG in TCDn.EVCTRLx is '$0x2$') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '$0x0$' events can be missed.

Work Around

Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '$0x2$') if the input events are longer than one CLK_TCD_CNT cycle.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.10.2 CMPAEN Controls All WOx For Alternative Pin Functions

When TCD alternative pins are enabled (TCD0 in PORTMUX.TCDROUTEA is not '$0x0$'), all waveform outputs (WOx) are controlled by Compare A Enable (CMPAEN in TCDn.FAULTCTRL).

Work Around
None.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.11 TWI - Two-Wire Interface

2.11.1 The Output Pin Override Does Not Function as Expected

When TWI is enabled, it overrides the output pin driver, but not the output value. So when the value in the PORTx.OUT register is '1', for the pins corresponding to the SDA or SCL, the output on the line will always be high.

Work Around
Ensure that the value in the PORTx.OUT register corresponding to the SCL and SDA pins are '0' before enabling the TWI.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.12 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.12.1 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '`0`' when using Open-Drain mode.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.12.2 Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'

The Start-of-Frame Detector can unintentionally be enabled when the device is in Active mode and when the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is '`0`'. If the Receive Data (RXDATA) registers are read while receiving new data, RXCIF is cleared, and the Start-of-Frame Detector will be enabled and falsely detects the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '`0`' when in Active mode, so no interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '`0`' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register, when the device is in Active mode. Enable it again by writing the bit to '`1`' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.13 ZCD - Zero-Cross Detector

2.13.1 All ZCD Output Selection Bits are Tied to the ZCD0 Bit

The Zero Cross Detector n Output (ZCDn) bits in the Pin Position (PORTMUX.ZCDROUTEA) register are tied to ZCD0. Any write to ZCD0 will be reflected in the ZCD1 and ZCD2 as well. Writing to ZCD1 and/or ZCD2 has no effect.

Work Around

The event system or CCL can be used to make the output of ZCD1 or ZCD2 available on a pin.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	-

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40002247).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 Typical Characteristics

3.1.1 OPAMP

Some additional plots are added to the OPAMP section of the Typical Characteristics:

- I_{DD} over V_{DD} and temperature with IRSEL = 0
- I_{DD} over V_{DD} and temperature with IRSEL = 1
- Output sinking short-circuit current over V_{DD} and temperature
- Output sourcing short-circuit current over V_{DD} and temperature
- Output impedance over frequency at 3V and 25°C
- Small-signal non-inverting pulse response at 3V V_{DD}
- Large-signal non-inverting pulse response at 3V V_{DD}

Unless otherwise noted, the typical graphs are valid for the following conditions:

- Output load: 50 pF||3 kΩ
- Input common-mode voltage at V_{DD}/2
- Internal voltage follower mode
- IRSEL = 0

Figure 3-1. I_{DD} Over V_{DD} and Temperature With IRSEL = 0
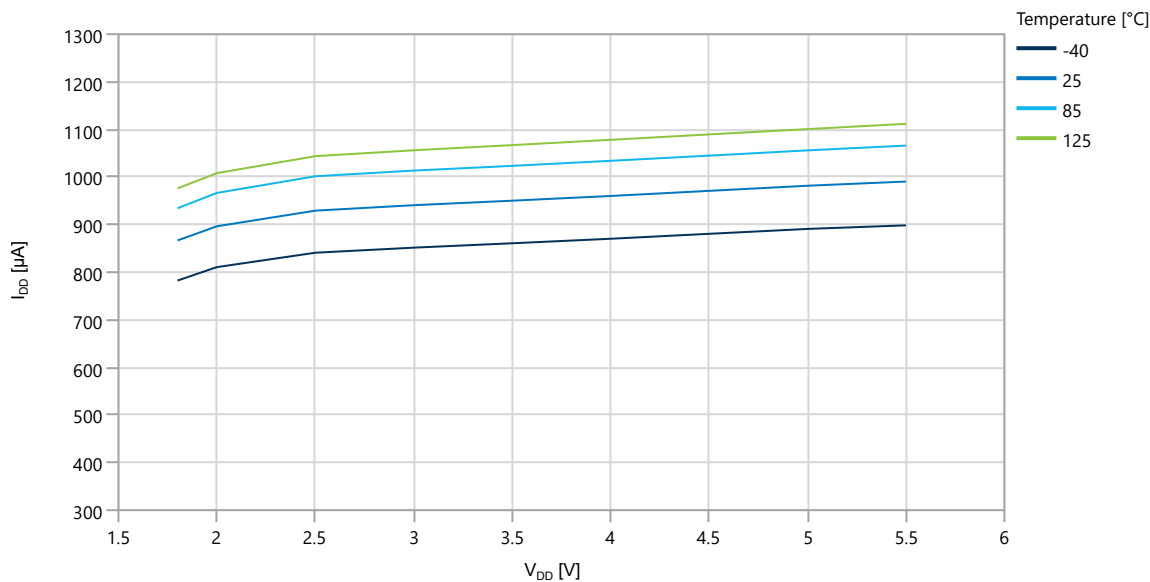
Note: This plot is only valid for revision A5 and later.

Figure 3-2. I$_{DD}$ Over V$_{DD}$ and Temperature With IRSEL = 1
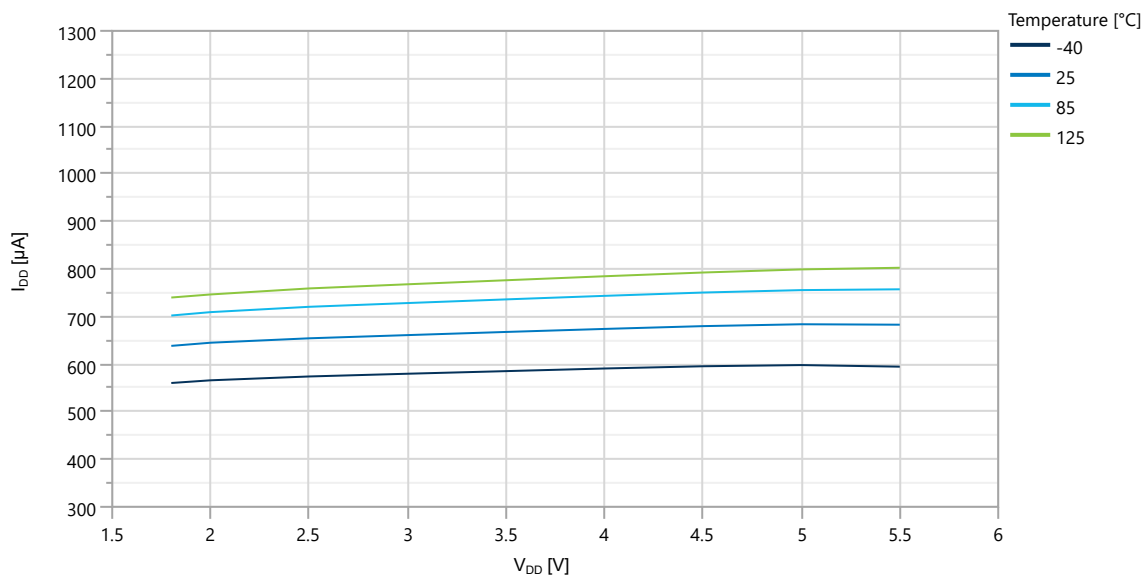
Note: This plot is only valid for revision A5 and later.

Figure 3-3. Output Sinking Short Circuit Current Over V$_{DD}$ and Temperature
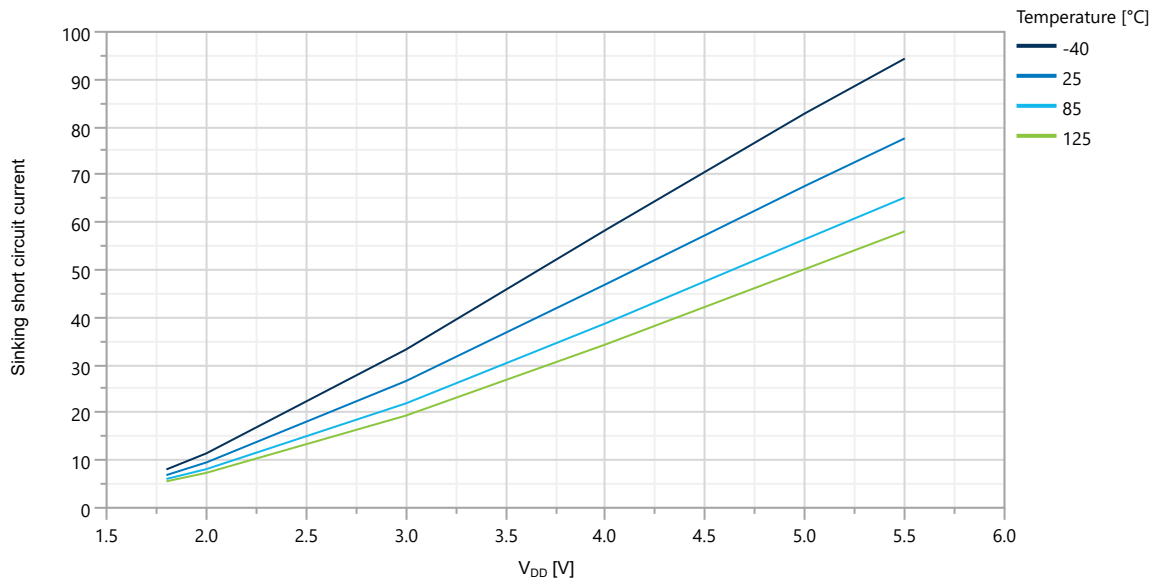
Figure 3-4. Output Sourcing Short Circuit Current Over V$_{DD}$ and Temperature
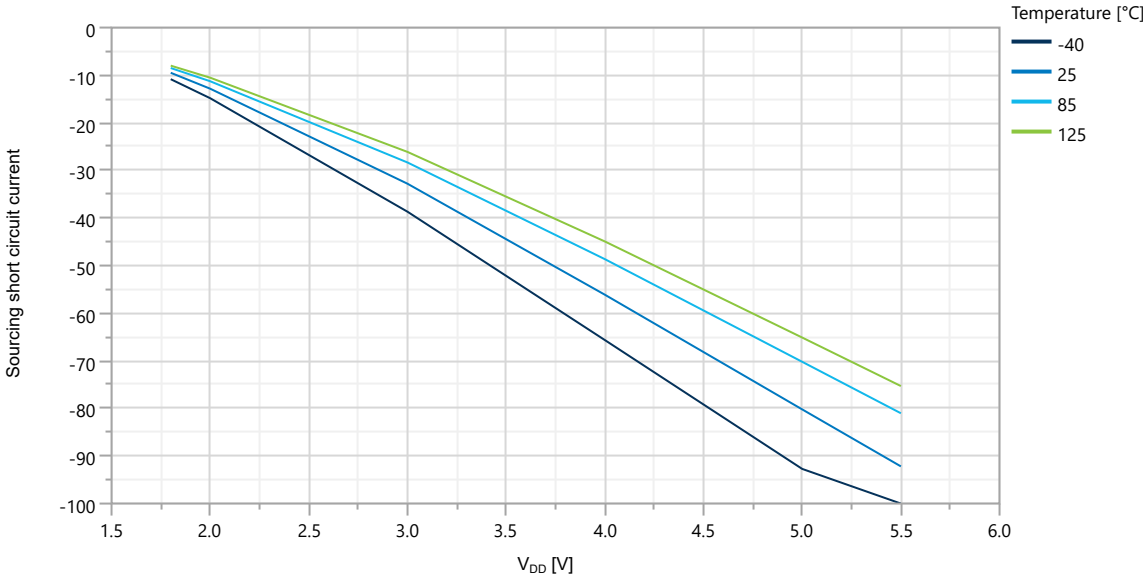
Figure 3-5. Output Impedance Over Frequency at 3V and 25°C
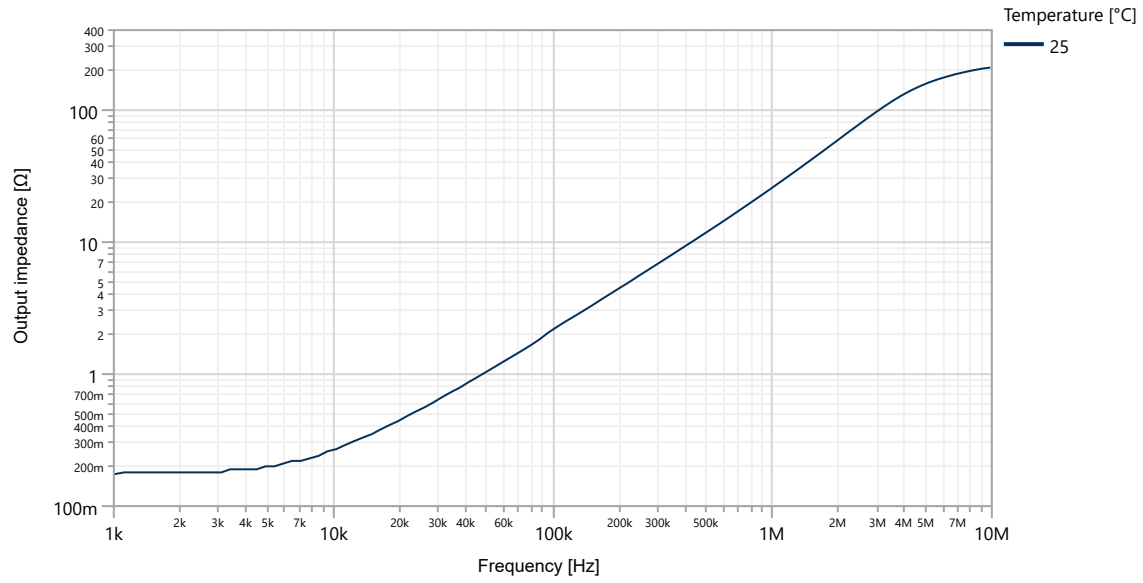
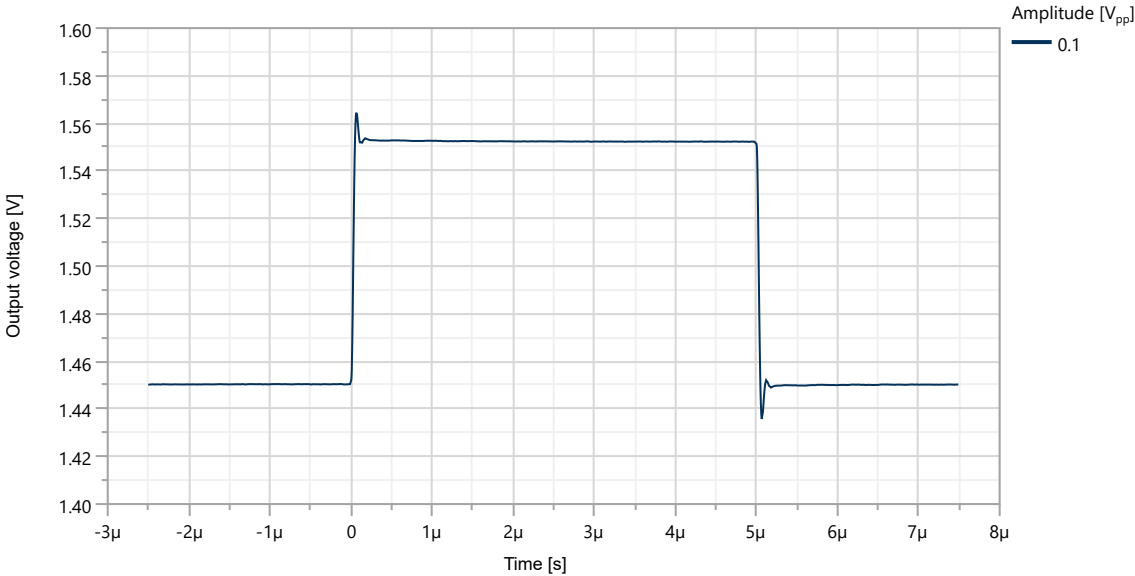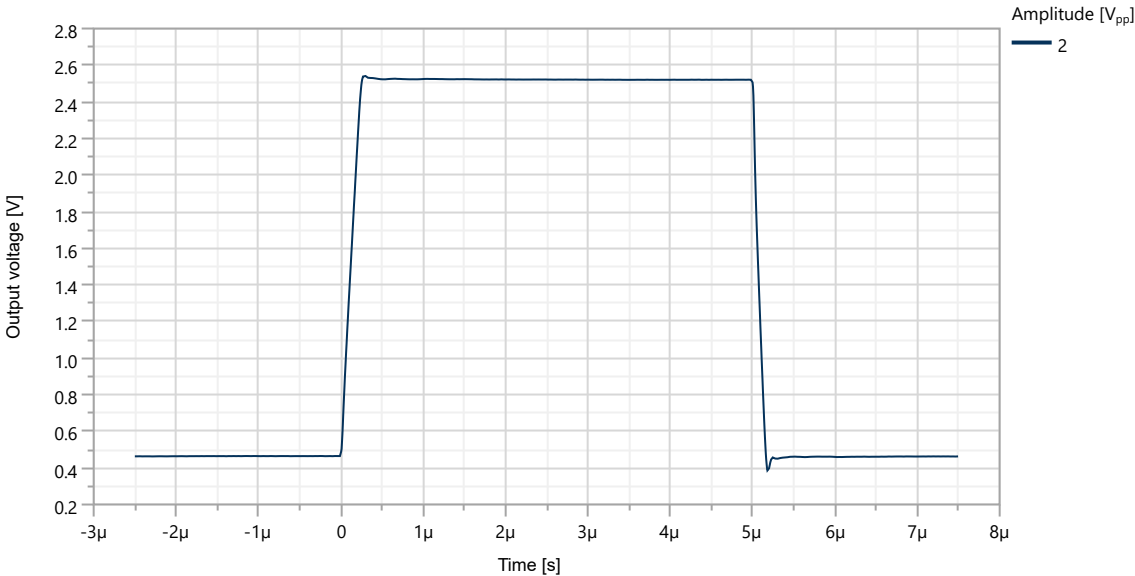**Figure 3-6. Small-signal Non-Inverting Pulse Response at 3V V$_{DD}$ Using 10 kΩ Load**

Figure 3-7. Large-Signal Non-Inverting Pulse Response at 3V V$_{DD}$ Using 10 kΩ Load

4. Document Revision History

Note: The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

Doc. Rev.	Date	Comments

B	10/2020	Added errata:
		• Device: *Increased Current Consumption May Occur When VDD Drops*
		• CLKCTRL: *The PLL Will Not Run When Using XOSCHF With an External Crystal*
		• TCB: *CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode*
		• TCD:
		  – *Asynchronous Input Events Not Working When TCD Counter Prescaler is Used*
		  – *CMPAEN Controls All WOx For Alternative Pin Functions*
		
		Updated errata:
		• CCL:
		  – *The CCL Must be Disabled to Change the Configuration of a Single LUT*
		  – *The LINK Input Source Selection for LUT3 is Not Functional on 28- and 32- pin Devices*
		• ZCD: *All ZCD Output Selection Bits are Tied to the ZCD0 Bit*
		
		Added data sheet clarification:
		Added Typical Characteristics section with additional plots for OPAMP peripheral.

A	08/2020	Initial document release

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