transphorm

TPH3206LSGB

650V Cascode GaN FET PQFN88 Series

Description

The TPH3206LSGB 650V, 150mΩ gallium nitride (GaN) FET is a normally-off device. Transphorm GaN FETs offer better efficiency through lower gate charge, faster switching speeds, and smaller reverse recovery charge, delivering significant advantages over traditional silicon (Si) devices.

Transphorm is a leading-edge wide band gap supplier with world-class innovation and a portfolio of fully-qualified GaN transistors that enables increased performance and reduced overall system size and cost.

Related Literature

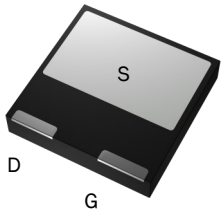
- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing

Product Series and Ordering Information

Part Number*	Package	Package Configuration
TPH3206LSGB	8 x 8mm PQFN	Source

* Add "-TR" suffix for tape and reel
** LDGB package offers larger gate pad

TPH3206LSGB
8x8 PQFN
(bottom view)



Features

- JEDEC qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - Intrinsic lifetime tests
  - Wide gate safety margin
  - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

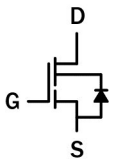
- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers

Applications

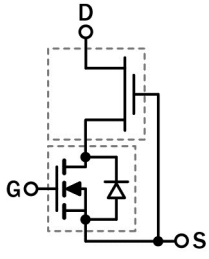
- Datacom
- Broad industrial
- PV inverter
- Servo motor

Key Specifications	
V_{DS} (V) min	650
V_{TDS} (V) max	800
$R_{DS(on)}$ (mΩ) max*	180
Q_{rr} (nC) typ	52
Qg (nC) typ	6.2

* Includes dynamic $R_{(on)}$



Cascode Schematic Symbol



Cascode Device Structure

Absolute Maximum Ratings (T_C=25°C unless otherwise stated.)

Symbol	Parameter		Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
$V_{(TR)DSS}$	Transient drain to source voltage [a]		800	
V_{GSS}	Gate to source voltage		±18	
P_D	Maximum power dissipation @T_C=25°C		81	W
I_D	Continuous drain current @T_C=25°C [b]		16	A
	Continuous drain current @T_C=100°C [b]		10	A
I_{DM}	Pulsed drain current (pulse width: 10µs)		60	A
$(di/dt)_{RDMC}$	Reverse diode di/dt, repetitive [c]		1200	A/µs
$(di/dt)_{RDMT}$	Reverse diode di/dt, transient [d]		2400	A/µs
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{SOLD}	Soldering peak temperature [e]		260	°C

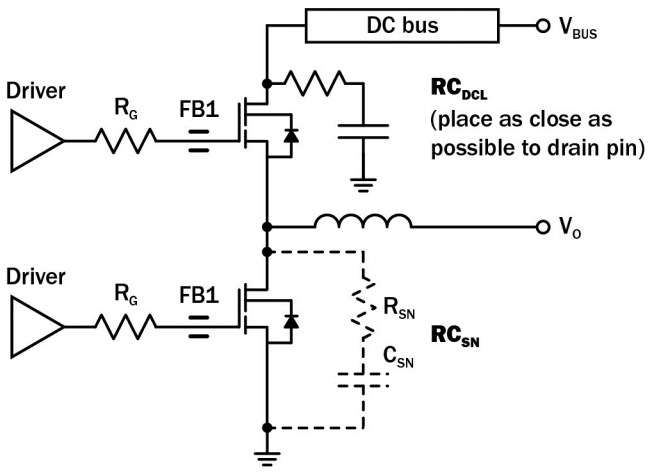
Notes:
a. In off-state, spike duty cycle D<0.01, spike duration <1µs
b. For increased stability at high current operation, see Circuit Implementation on page 3
c. Continuous switching operation
d. ≤300 pulses per second for a total duration ≤20 minutes
e. For 10 sec., 1.6mm from the case

Thermal Resistance

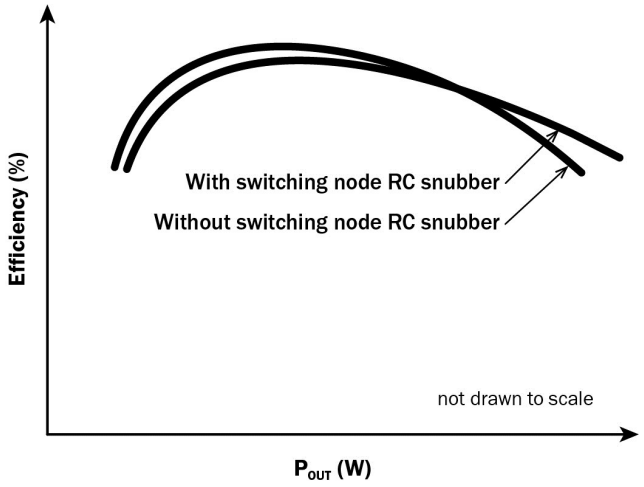
Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	1.55	°C/W
$R_{\Theta JA}$	Junction-to-ambient [a]	45	°C/W

Notes:
a. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70µm thickness)

Circuit Implementation



Simplified Half-bridge Schematic



Efficiency vs Output Power

Recommended gate drive: (0V, 8-10V) with $R_{G(tot)}$ = 25Ω, where $R_{G(tot)} = R_G + R_{DRIVER}$

Gate Ferrite Bead (FB1)	Required DC Link RC Snubber (RC_{DCL}) [a]	Recommended Switching Node RC Snubber (RC_{SN}) [b, c]
MMZ1608Q121BTA00	10nF + 8Ω	22pF + 15Ω

Notes:
a. RC_{DCL} should be placed as close as possible to the drain pin
b. A switching node RC snubber (C, R) is recommended for high switching currents (>70% of I_{RDMC1} or I_{RDMC2}; see page 5 for I_{RDMC1} and I_{RDMC2})
c. I_{RDM} values can be increased by increasing R_G and C_{SN}

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	1.65	2.1	2.6	V	V_{DS}=V_{GS}, I_D=500µA
$R_{DS(on)eff}$	Drain-source on-resistance [a]	—	150	180	mΩ	V_{GS}=8V, I_D=10A
		—	308	—		V_{GS}=8V, I_D=10A, T_J=150°C
I_{DSS}	Drain-to-source leakage current	—	2.5	30	µA	V_{DS}=650V, V_{GS}=0V
		—	8	—		V_{DS}=650V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=18V
	Gate-to-source reverse leakage current	—	—	-100		V_{GS}=-18V
C_{ISS}	Input capacitance	—	720	—	pF	V_{GS}=0V, V_{DS}=480V, *f*=1MHz
C_{OSS}	Output capacitance	—	46	—		
C_{RSS}	Reverse transfer capacitance	—	5.5	—		
$C_{O(er)}$	Output capacitance, energy related [b]	—	65	—	pF	V_{GS}=0V, V_{DS}=0V to 480V
$C_{O(tr)}$	Output capacitance, time related [c]	—	106	—		
Q_G	Total gate charge	—	6.2	—	nC	V_{DS}=100V, V_{GS}=0V to 4.5V, I_D=10A
Q_{GS}	Gate-source charge	—	2.1	—		
Q_{GD}	Gate-drain charge	—	2.2	—		
Q_{OSS}	Output charge	—	44.4	—	nC	V_{GS}=0V, V_{DS}=0V to 400V
$t_{D(on)}$	Turn-on delay	—	6	—	ns	V_{DS}=480V, V_{GS}=0V to 10V, I_D=10A, R_G=22Ω
t_R	Rise time	—	4.5	—		
$t_{D(off)}$	Turn-off delay	—	9.7	—		
t_F	Fall time	—	4	—		

Notes:
a. Dynamic on-resistance; see Figures 19 and 20 for test circuit and conditions
b. Equivalent capacitance to give same stored energy as V_{DS} rises from 0V to 400V
c. Equivalent capacitance to give same charging time as V_{DS} rises from 0V to 400V

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	10	A	V_{GS}=0V, T_C=100°C, ≤25% duty cycle
V_{SD}	Reverse voltage [a]	—	2.4	—	V	V_{GS}=0V, I_S=10A
		—	3.7	—		V_{GS}=0V, I_S=10A, T_J=150°C
		—	1.7	—		V_{GS}=0V, I_S=5A
t_{RR}	Reverse recovery time	—	17	—	ns	I_S=11A, V_{DD}=400V, di/dt=2000A/µs
Q_{RR}	Reverse recovery charge	—	52	—	nC	
$(di/dt)_{RDMC}$	Reverse diode di/dt, repetitive [b]	—	—	1200	A/µs	
I_{RDMC1}	Reverse diode switching current, repetitive (dc) [c, e]	—	—	11	A	Circuit implementation and parameters on page 3
I_{RDMC2}	Reverse diode switching current, repetitive (ac) [c, e]	—	—	14	A	Circuit implementation and parameters on page 3
$(di/dt)_{RDMT}$	Reverse diode di/dt, transient [d]	—	—	2400	A/µs	
I_{RDMT}	Reverse diode switching current, transient [d,e]	—	—	18	A	Circuit implementation and parameters on page 3

Notes:
a. Includes dynamic $R_{DS(on)}$ effect
b. Continuous switching operation
c. Definitions: dc = dc-to-dc converter topologies; ac = inverter and PFC topologies, 50-60Hz line frequency
d. ≤300 pulses per second for a total duration ≤20 minutes
e. I_{RDM} values can be increased by increasing R_G and C_{SN} on page 3

Typical Characteristics (25 °C unless otherwise stated)

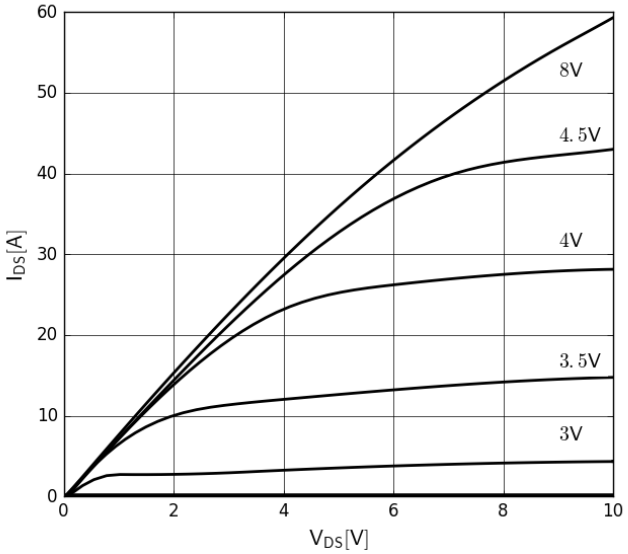


Figure 1. Typical Output Characteristics T_J=25 °C
Parameter: V_{GS}

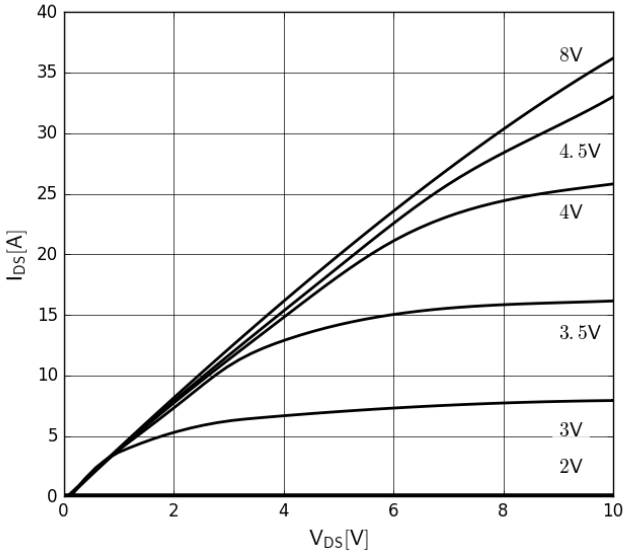


Figure 2. Typical Output Characteristics T_J=150 °C
Parameter: V_{GS}

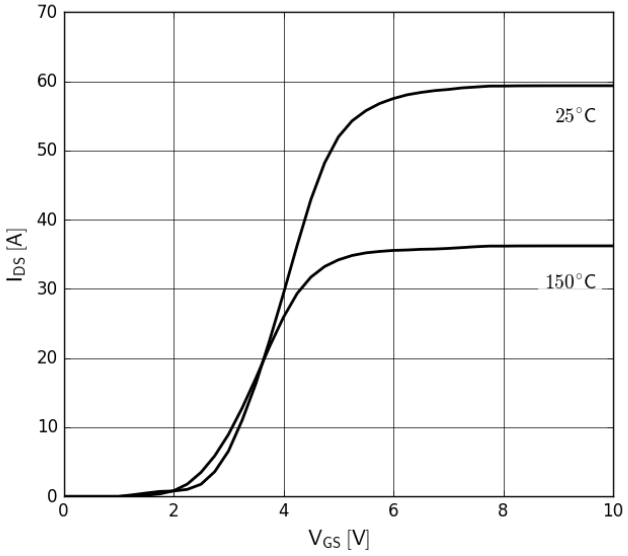


Figure 3. Typical Transfer Characteristics
V_{DS}=10V, parameter: T_J

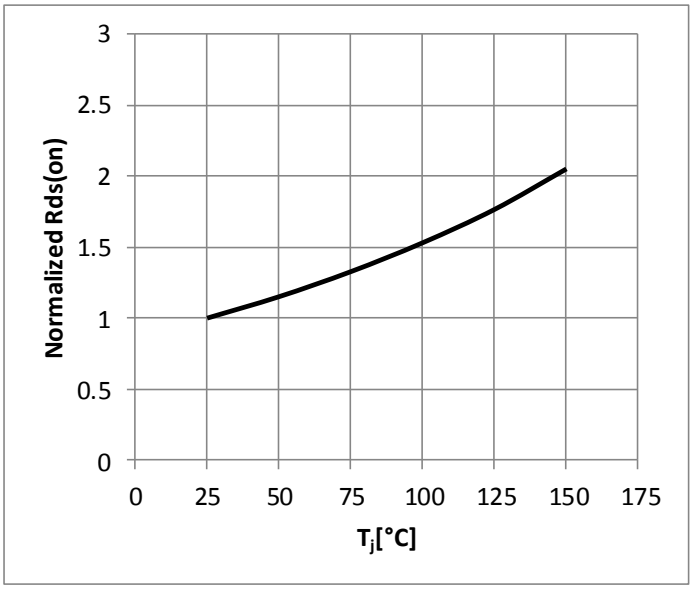


Figure 4. Normalized On-Resistance
I_D=12A, V_{GS}=8V

Typical Characteristics (T_C=25 °C unless otherwise stated)

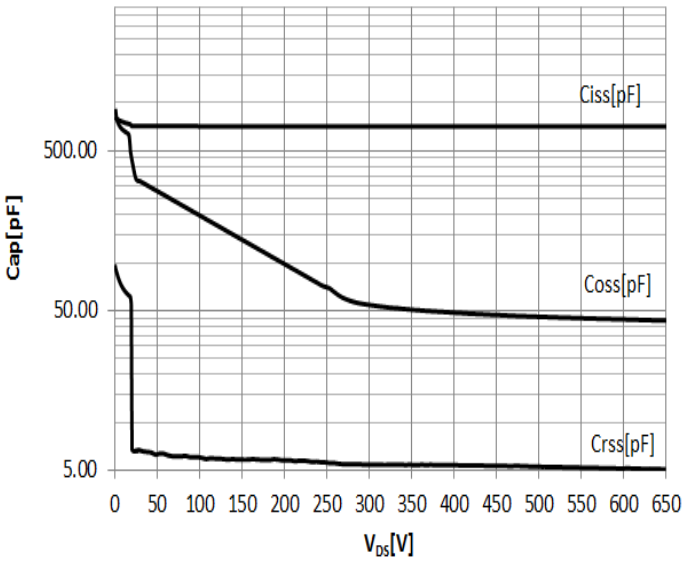


Figure 5. Typical Capacitance
V_{GS}=0V, f=1MHz

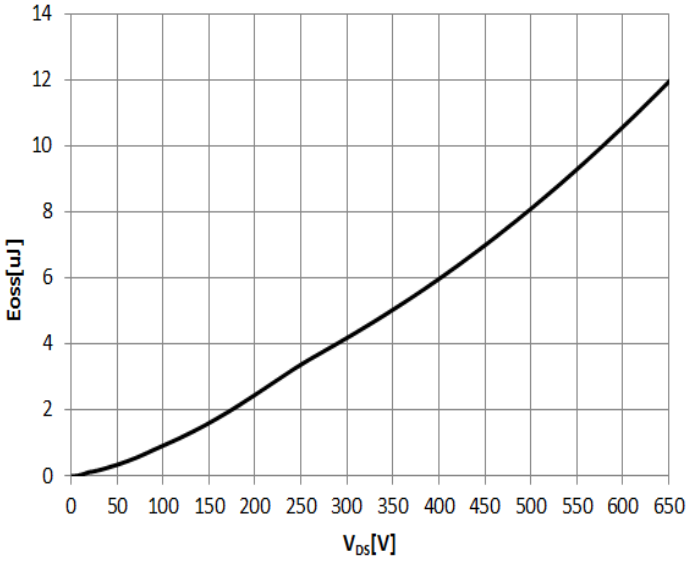


Figure 6. Typical C_{oss} Stored Energy

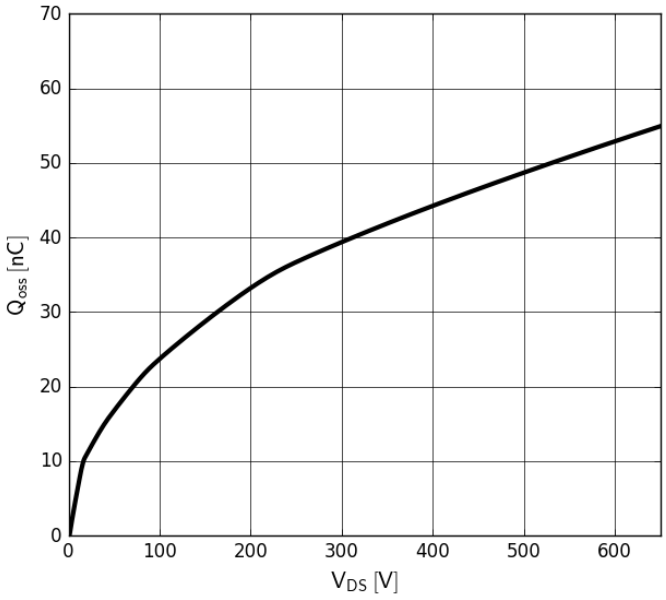


Figure 7. Typical Q_{oss}

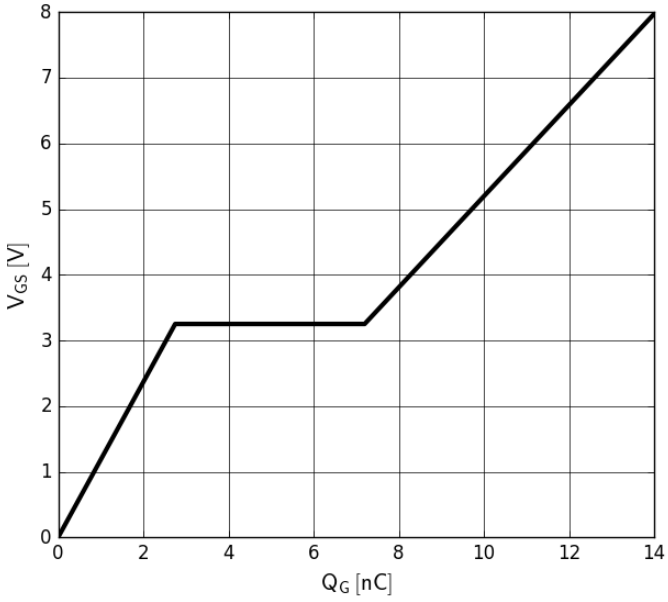


Figure 8. Typical Gate Charge
I_{DS}=10A, V_{DS}=400V

Typical Characteristics (T_C=25°C unless otherwise stated)

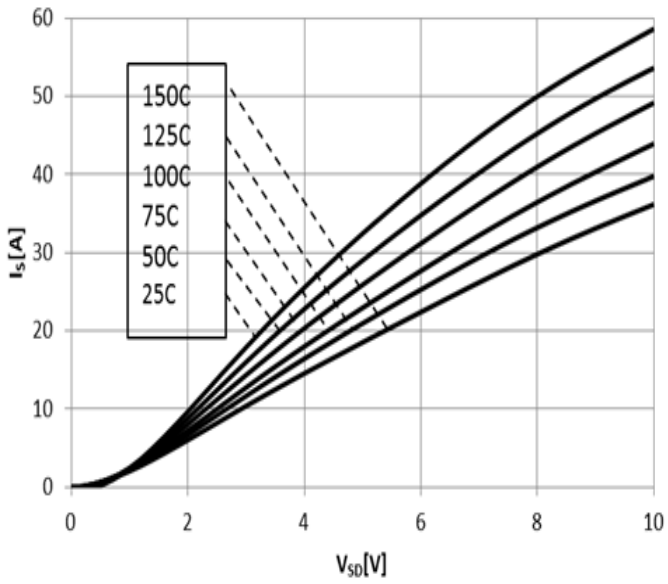


Figure 9. Forward Characteristics of Rev. Diode
$I_S=f(V_{SD})$, Parameter T_J

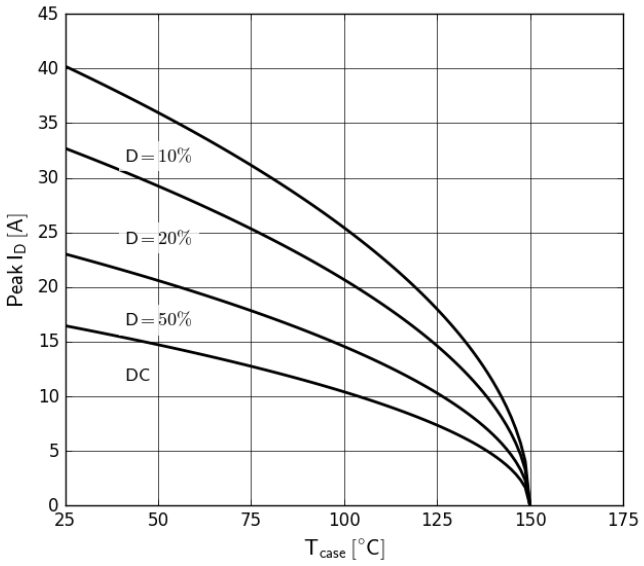


Figure 10. Current Derating
Pulse width = 100µs

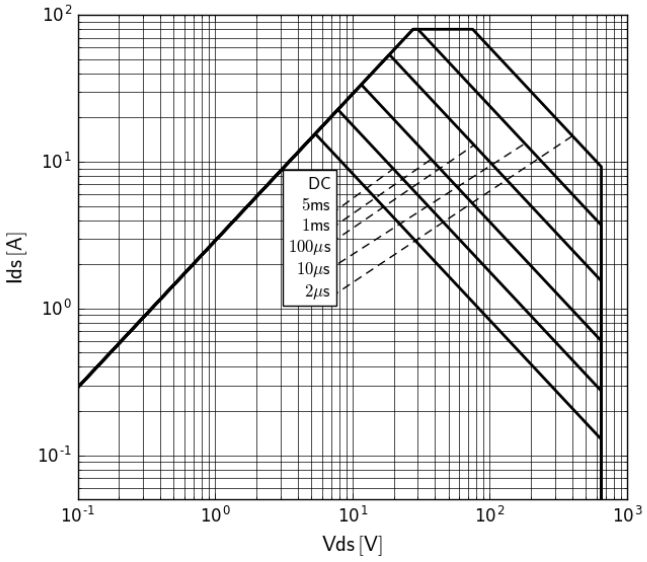


Figure 11. Safe Operating Area T_C=25°C
(calculated based on thermal limit)

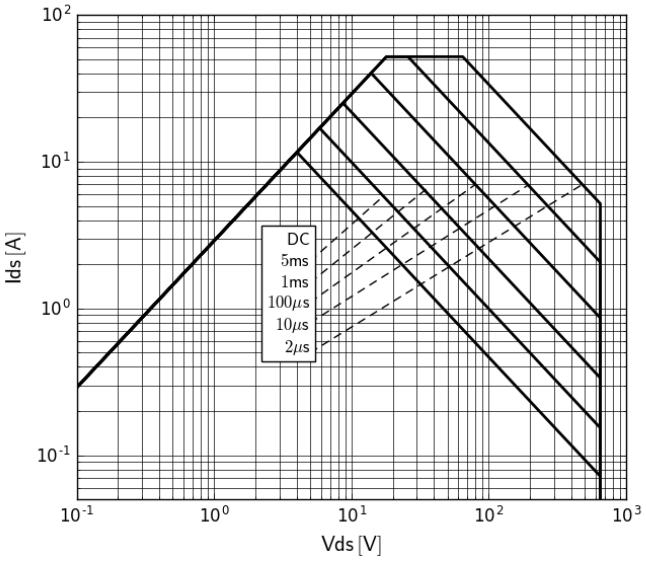


Figure 12. Safe Operating Area T_C=80°C
(calculated based on thermal limit)

Typical Characteristics (T_C=25 °C unless otherwise stated)

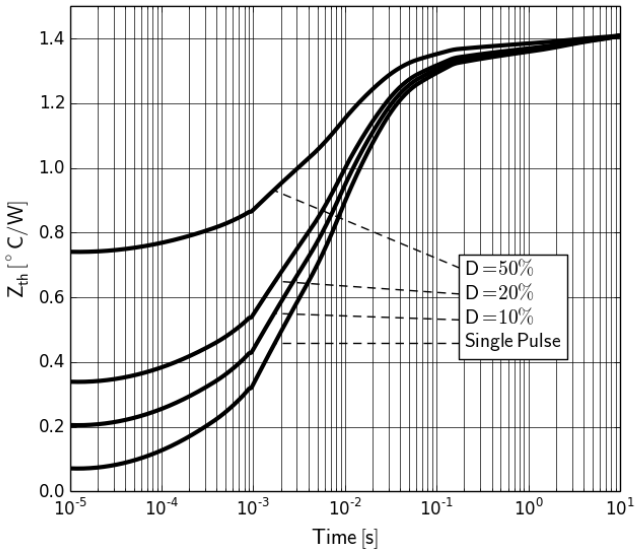


Figure 13. Transient Thermal Resistance

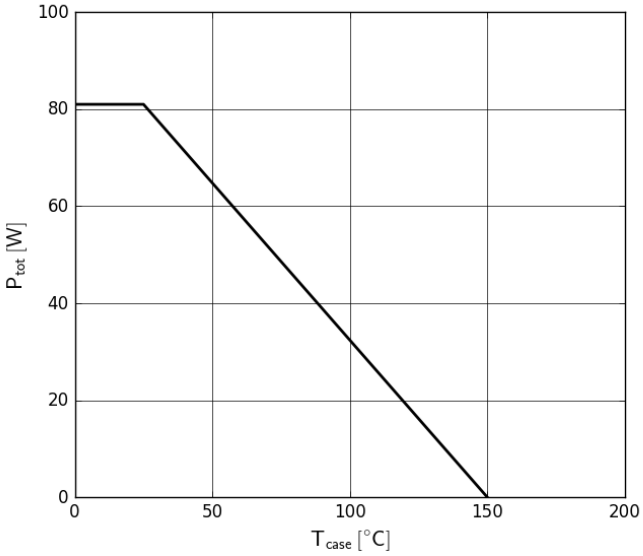


Figure 14. Power Dissipation

Test Circuits and Waveforms

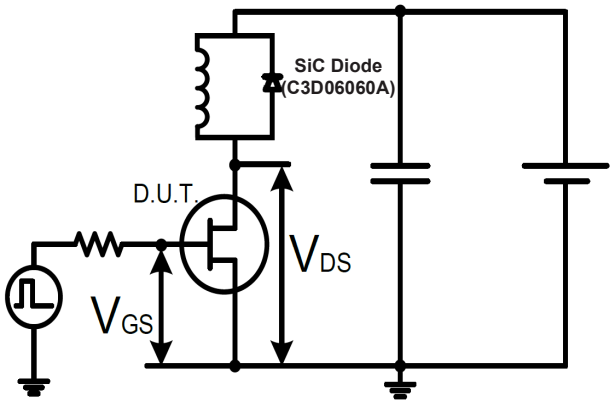


Figure 15. Switching Time Test Circuit
(see circuit implementation on page 3
for methods to ensure clean switching)

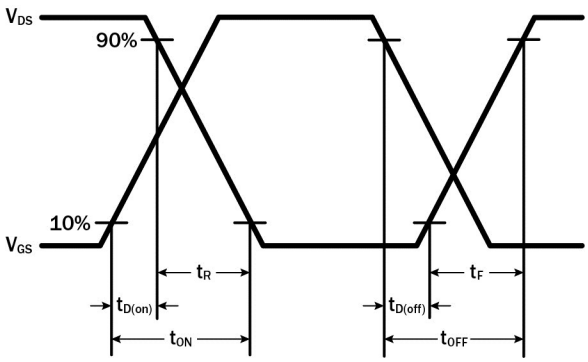


Figure 16. Switching Time Waveform

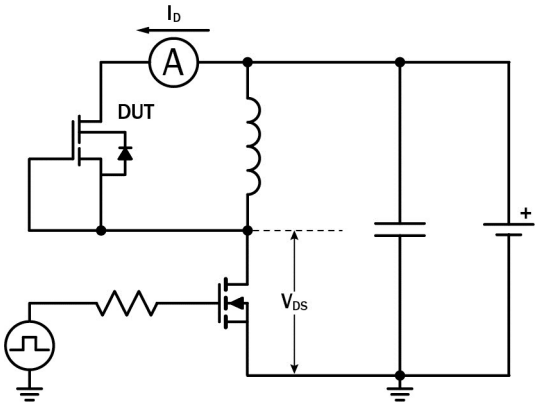


Figure 17. Diode Characteristics Test Circuit

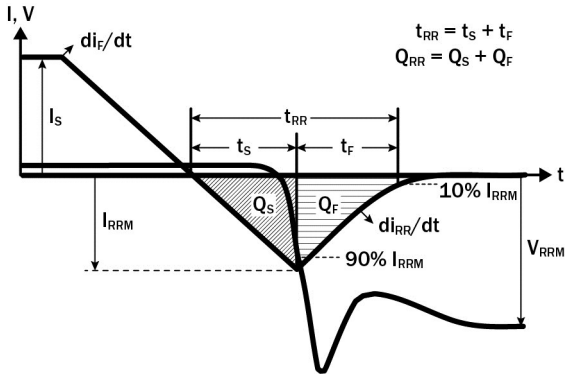


Figure 18. Diode Recovery Waveform

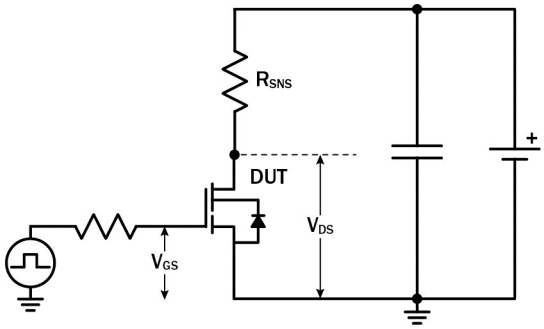


Figure 19. Dynamic $R_{DS(on)eff}$ Test Circuit

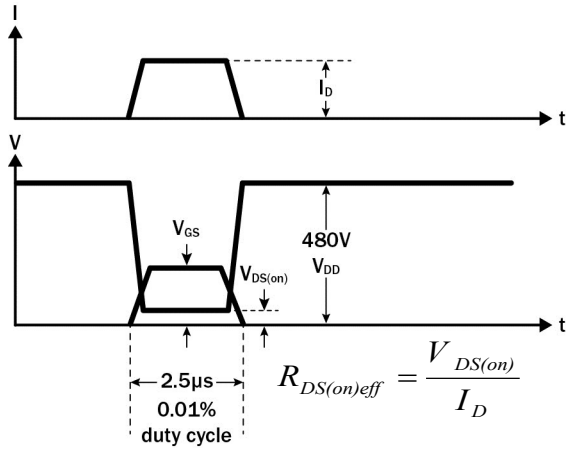
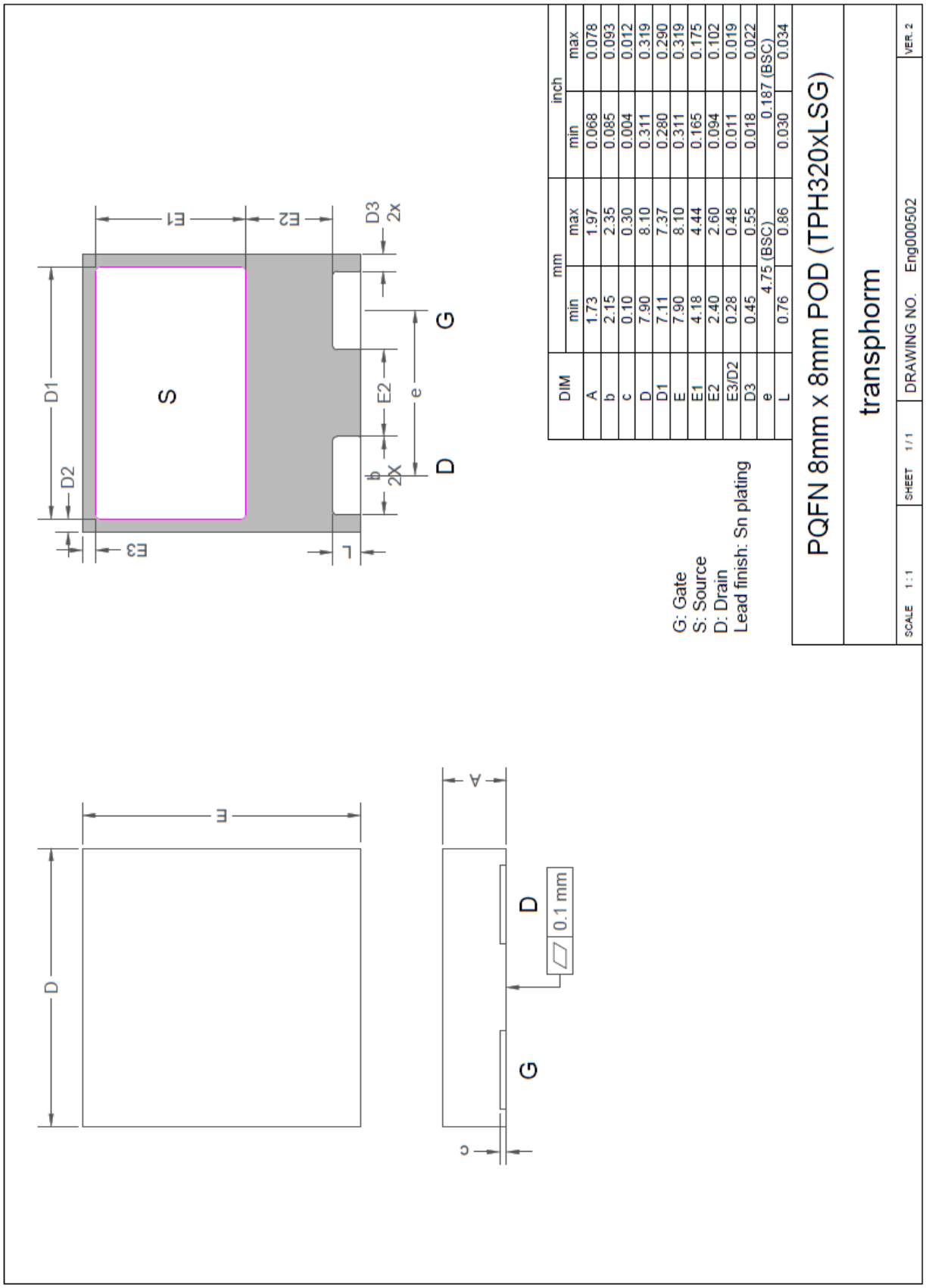


Figure 20. Dynamic $R_{DS(on)eff}$ Waveform

8x8 PQFN (LSGB) Package

Mechanical



Design Considerations

The fast switching of GaN devices reduces current-voltage cross-over losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003: Printed Circuit Board Layout and Probing	

Application Notes

- AN0002: Characteristics of Transphorm GaN Power Switches
- AN0003: Printed Circuit Board Layout and Probing
- AN0004: Designing Hard-switched Bridges with GaN
- AN0008: Drain Voltage and Avalanche Ratings for GaN FETs
- AN0009: Recommended External Circuitry for GaN FETs

Revision History

Version	Date	Change(s)
0	1/11/2019	New datasheet