IRPS5401 PMIC

Flexible Power Management Unit

Features

- Full power system including 5 integrated outputs
- 4A, 4A, 2A and 2A Switching Regulators
- 500mA Source/Sink Linear regulator
- Single rail operation 5.5V to 12V
- Output Range from 0.25V to 5.1V for outputs A-D and 0.5V to 3.6V for LDO
- Allows combining outputs and/or the use of an external IR MOSFET™ Power Stage to increase output current to as high as 50A
- Emulated current mode control without external compensation
- Differential voltage sensing on Switcher A for higher accuracy
- I2C / PMBus with integrated level shifter
- Advanced Sequencing control
- Extensive PMBus command set of 74 commands
- Integrated current sensing and full telemetry including voltage, current, temperature and faults
- Rated for -40°C to +125°C T_J operation
- Pb-Free, RoHS6, 7x7mm, 56-pin, 0.4mm pitch QFN

Potential applications

- High density ASIC, FPGA & CPU multi-rail systems
- Embedded Computing systems
- Communications and Storage systems

Description

The IRPS5401 is a complete power management unit delivering up to 5 output voltages to processors, FPGA's and other multi-rail power systems. Four high efficiency configurable switching regulators and a Source/Sink Linear regulator provide the typical rails required such as core voltage, memory voltage and I/O voltages.

Integrated, accurate current, voltage and temperature sensing allows telemetry and fault reporting through the I2C/PMBus.

The IRPS5401 switching regulators utilize fixed frequency emulated current mode control, and thus no external compensation is required.

The IRPS5401 is highly flexible. Switchers A and B deliver 2A each. Switchers C and D, deliver 4A each and can also be combined to deliver 8A. Further, Switcher A can be configured to use an external IR MOSFET™ Power Stage to deliver up to 50A or more.

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1 Ordering Information

Table 1 Ordering Information

Base part number	Package type	Standard pack	Orderable part number	Description
IRPS5401M	QFN 7 mm x 7 mm	Tape and Reel	IRPS5401MTRPBF	Unprogrammed
IRPS5401M	QFN 7 mm x 7 mm	Tape and Reel	IRPS5401MXI03TRP	Pre-programmed per Table 2
IRPS5401M	QFN 7 mm x 7 mm	Tape and Reel	IRPS5401MXI04TRPXUMA1	Pre-programmed per Table 3

Table 2 IRPS5401MXI03TRP Loop Configurations

Config	R_MTP R_ADDR	A (bold = external PS)	B	C	D	LDO (supplied from)
1	8.87kΩ	1.8V/0.5A	1.8V/1.4A	0.85V/0.6A	0.85V/3.7A	1.2V (B)
2	10kΩ	1.2V/1.2A	0.85V/0.6A	3.3V/1.5A	0.85V/4A	1.8V (C)
3	11kΩ	1.8V/0.5A	5V/1.5A	3.3V/3.3A	0.85V/2A	1.8V (C)
4	2.32kΩ	**0.85V/16A**	1.2V/1.5A	1.8V/1A	1.8V/4A	1.2V (D or external)
5	2.87kΩ	**0.85V/25A**	1.2V/1.5A	1.8V/1A	1.8V/4A	1.2V (D or external)
6	3.48kΩ	3.3V/1.4A	1.8V/1A	0.9V/3A	1.2V/3A	0.85V (A)
7	4.12kΩ	**0.72V/9A**	3.3V/2A	0.85V/7A		1.2V (B)
8	4.75kΩ	**0.72V/15A**	3.3V/2A	0.85V/7A		1.2V (B)
9	5.49kΩ	1.8V/1A	1.2V/1.5A	1.8V/4A	2.5V/1.5A	1.8V (D)
10	6.19kΩ	0.9V/2A	1.2V/1.5A	1.8V/2.5A	1.2V/2A	0.85V (C)
11	6.98kΩ	**0.72V/9A**	1.2V/1.5A	0.85V/4A	1.8V/2A	1.2V (D or external)
12	7.87kΩ	**0.72V/20A**	1.2V/1.2A	0.85V/4A	1.8V/2A	1.2V (D or external)

Table 3 IRPS5401MXI04TRPAUMA1 Loop Configurations

Config	R_MTP R_ADDR	A (bold = external PS)	B	C	D	LDO (supplied from)
1	Not used					
2	Not used					
3	Not used					
4	2.32kΩ	**0.85V/ 15A**	1.8V/2A	1.2V/5A		0.9V/0.5A (external 2.5V)
5	2.87kΩ	**3.3V/10A**	1.13V/1A	5V/2.1A	1.8V/3A	0.85V/0.5A (external 2.5V)
6	3.48kΩ	**0.85V/15A**	1.8V/2A	0.85V/7A		3.3V/0.5A (optional)
7	4.12kΩ	**3.3V/10A**	2.5V/2A	1.2V/6A		0.85V/0.5A (external 2.5V)
8	4.75kΩ	**1.2V/6A**	2.5V/0.5A	1.8V/5A		1.8V/0.5A (external 2.5V)

2 Application Circuit

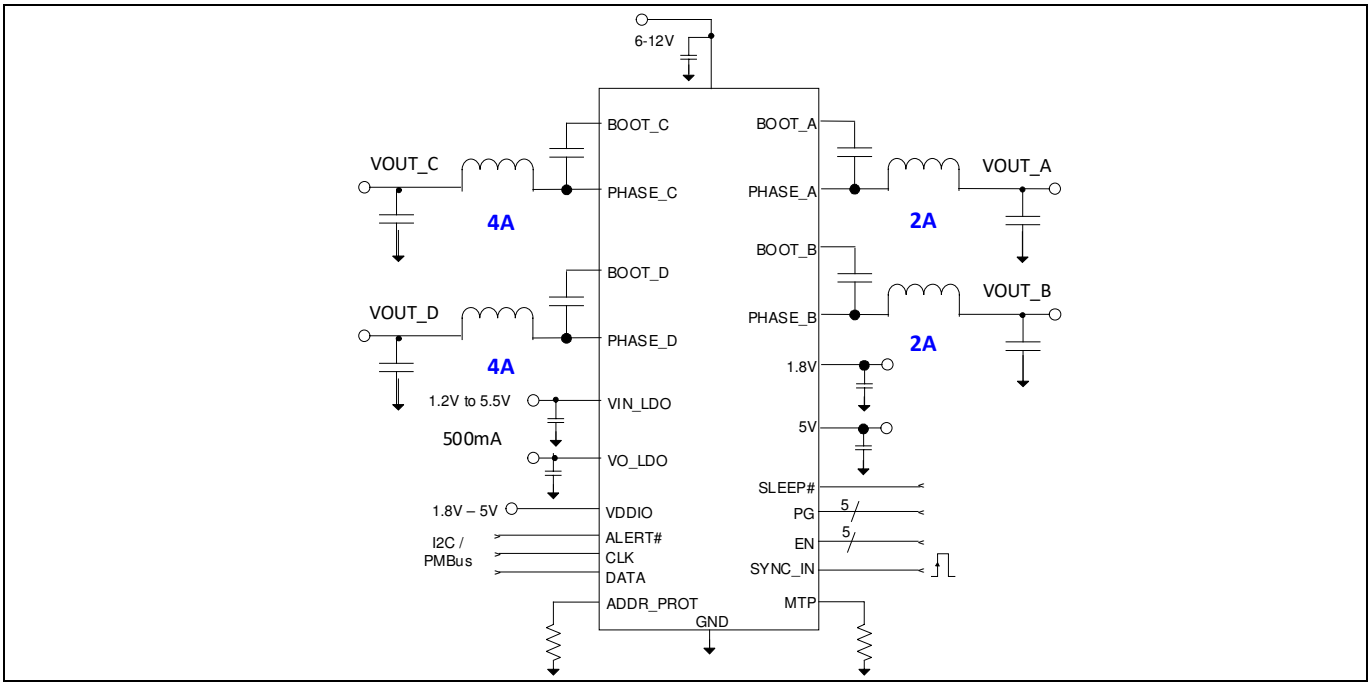


Figure 1 IRPS5401 Basic application circuit

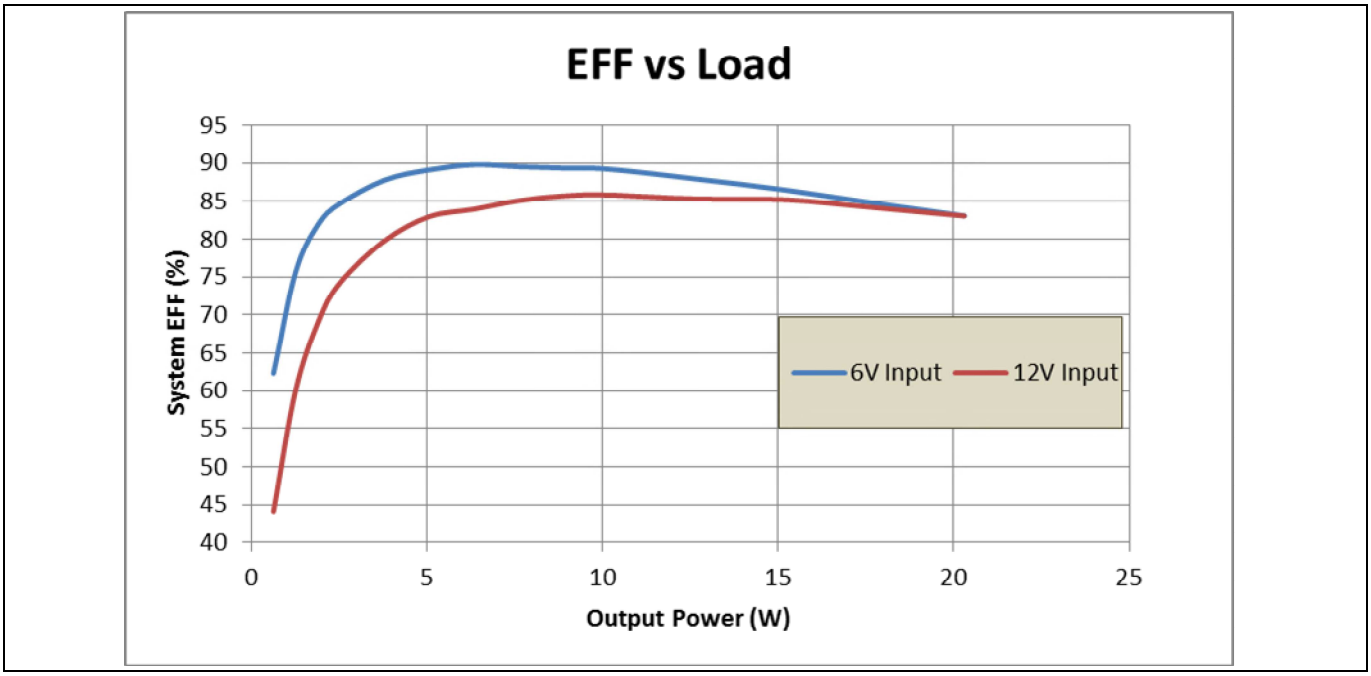


Figure 2 System efficiency with VO= 2.5V, FSW=800kHz, Tj=45°C

3 Pinout Diagram

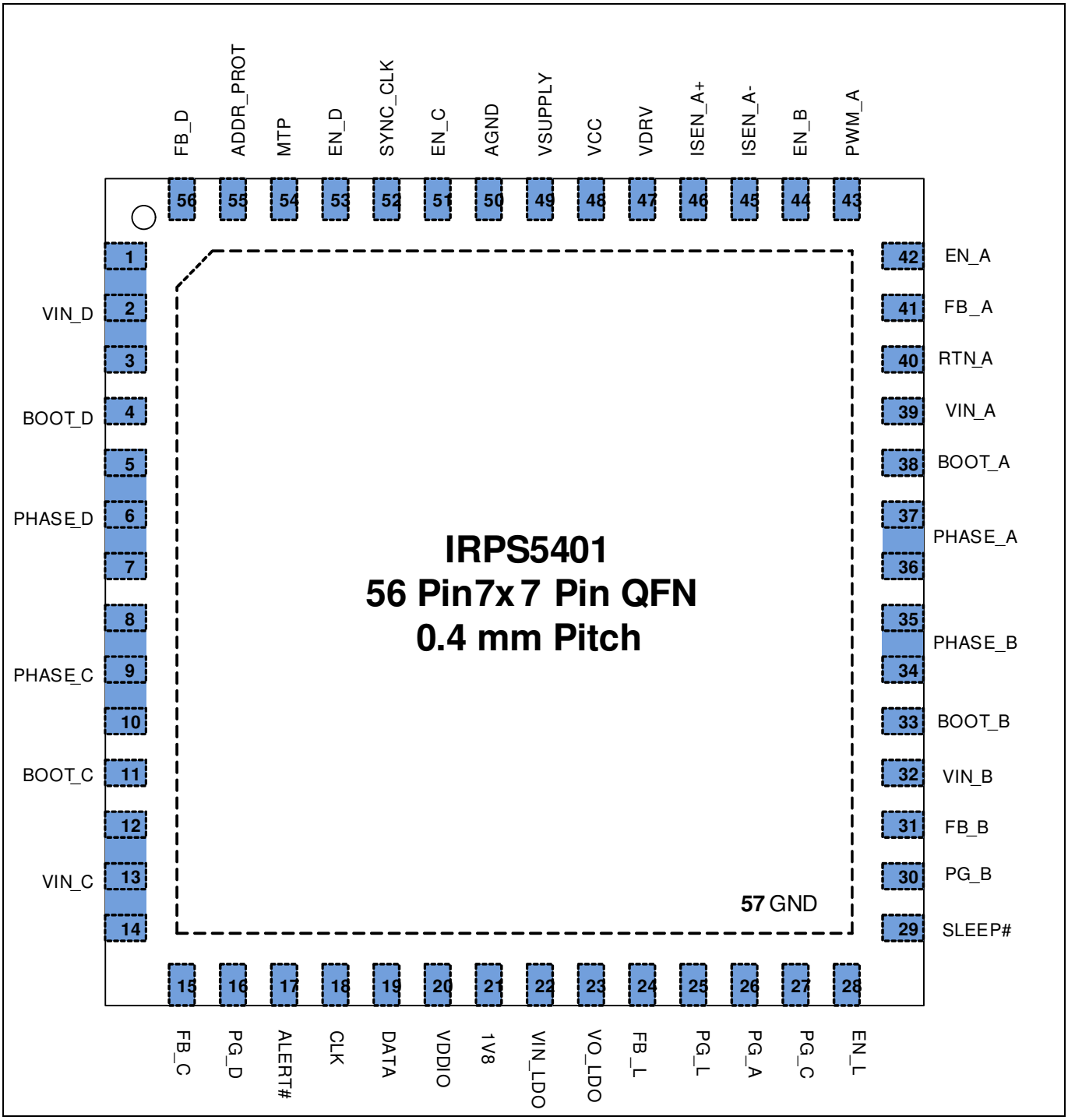


Figure 3 Pinout diagram 7mm x 7mm QFN (Top View)

4 Pin Function

Table 4 PIN Function

PIN			Description	If not used
#	Name	TYP		
1,2,3	VIN_D	P [I]	Input supply voltage pins for Switcher D. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
4	BOOT_D	A [B]	Supply input for Switcher D high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_ D pins. An internal diode is connected between VDRV and this pin	Open
5,6,7	PHASE_D	P [O]	Switch node of Switcher D. Connect directly to the output inductor.	Open
8,9, 10	PHASE_C	P [O]	Switch node of Switcher C. Connect directly to the output inductor.	Open
11	BOOT_C	A [B]	Supply input for Switcher C high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_C pins. An internal diode is connected between VDRV and this pin	Open
12, 13,14	VIN_C	P [I]	Input supply voltage pins for Switcher C. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
15	FB_C	A [I]	Switcher C feedback input. Connect directly to VOUT_C for output voltages less than 2.55V. Connect to VOUT_C with a 2:1 resistor divider for output voltages greater than 2.55V.	Open
16	PG_D	D [O]	Open drain power good output indicating Switcher D is powered up	Open
17	ALERT#	D [O]	I2C/PMBus Alert line. This alert signal can indicate one or more faults, allowing the system bus manager to poll the device and identify the root cause. All faults or customer selected faults such as overcurrent or over-temperature may be specifically masked to this pin.	Open
18	CLK	D [B]	I2C/PMBus Clock Line. Pull up to VDDIO with 10K	n/a
19	DATA	D [B]	I2C/PMBus Data Line. Pull up to VDDIO with 10K	n/a
20	VDDIO	P [I]	Pull-up signal voltage for I2C communications. Connect to the same I/O rail used by the I2C master.	n/a
21	1V8	A [O]	1.8V reference used by the device for internal analog and digital control. Decouple using a 1.0uF X7R type ceramic capacitor	n/a
22	VIN_LDO	P [I]	Input to the linear regulator. See linear regulator section for specific requirements. This voltage can range from 1.2V to 5.5V, with restrictions on overall power dissipation	Short To GND
23	VO_LDO	A[O]	LDO output	Open
24	FB_L	A [I]	LDO feedback input	Open
25	PG_L	D[I]	Open drain power good output indicating LDO is powered up. Pull up to 5V with 10K	Open
26	PG_A	D[I]	Open drain power good output indicating switcher A is powered up. Pull up to 5V with 10K	Open

Pin Function

PIN			Description	If not used
#	Name	TYP		
27	PG_C	D[I]	Open drain power good output indicating switcher C is powered up. Pull up to 5V with 10K	Open
28	EN_L	D[I]	LDO enable input control. Active High, external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	Short To GND
29	SLEEP#	D[I]	Active low signal to place the device in a low power mode LVTTL threshold levels. 'SLEEP ENABLED' threshold is 0.8V maximum	Short to VCC
30	PG_B	D[I]	Open drain power good output indicating switcher B is powered up. Pull up to 5V with 10K	Open
31	FB_B	A [I]	Switcher B feedback input. Connect directly to VOUT_B for output voltages less than 2.55V. Connect to VOUT_B with a 2:1 resistor divider for output voltages greater than 2.55V.	Open
32	VIN_B	P [I]	Input supply voltage pin for Switcher B. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
33	BOOT_B	A [B]	Supply input for Switcher B high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_ B pins. An internal diode is connected between VDRV and this pin	Open
34,35	PHASE_B	P [O]	Switch node of Switcher B. Connect directly to the output inductor.	Open
36,37	PHASE_A	P [O]	Switch node of Switcher A. Connect directly to the output inductor.	Open
38	BOOT_A	A [B]	Supply input for Switcher A high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_A pins. An internal diode is connected between VDRV and this pin	Open
39	VIN_A	P [I]	Input supply voltage pin for Switcher A. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
40	RTN_A	A [I]	Differential feedback return signal for Switcher A. This can be connected remotely to the return location of VOUT_A.	Short together
41	FB_A	A [I]	Differential feedback positive signal for Switcher A. Connect directly to VOUT_A for output voltages less than 2.55V. Connect to VOUT_A with a 2:1 resistor divider for output voltages greater than 2.55V.	Short together
42	EN_A	D [I]	Switcher A enable input control; external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	Short To GND
43	PWM_A	A [O]	PWM signal for Switcher A to be used when Switcher A is configured for use with an external IR MOSFET™ Power Stage. This PWM pin is a 5V PWM. This pin is used to drive a 5V capable external power stage such as an IR355x power stage and is a tri-state or tri-level signal. A resistor and zener clamp must be used when paired with a 3.3V only power stage (see figure 11). Leave floating if this pin is not used	Open
44	EN_B	D [I]	Switcher B enable input control; external termination required, do not leave floating. LVTTL threshold levels. 'ON'	Short To GND

PIN			Description	If not used
#	Name	TYP		
			threshold is 2.1V minimum	
45	ISEN_A-	A[I]	Negative (return) sense point for Switcher A external IOUT sense.	Short together
46	ISEN_A+	A[I]	Positive sense point for Switcher A external IOUT sense.	Short together
47	VDRV	A [O]	5V drive voltage used to power the internal MOSFET drivers. Use a 2.2Ω, 2.2uF filter from VCC to insure noise from this switching node is not injected into the VCC pin. See the application section. Terminate decoupling cap to GND (pin 57)	n/a
48	VCC	A [O]	5V source used by the device to power internal analog and digital control. When VCC is self-generated by the device (from VSUPPLY), do not load this pin with any load other than VDRV. Decouple using a 2.2uF X7R type ceramic capacitor. Terminate decoupling cap to AGND (pin 50)	n/a
49	VSUPPLY	A [I]	Input voltage for internal LDO for internally generated VCC	Short to VCC
50	AGND		Ground reference for the analog and digital control.	n/a
51	EN_C	D[I]	Switcher C enable input control; external termination required, do not leave floating. LVTTL threshold levels. ‘ON’ threshold is 2.1V minimum	Short To GND
52	SYNC_CLK	D[I]	External Synchronization pin. LVTTL threshold levels. ‘HIGH’ threshold is 2.1V minimum, ‘LOW’ is 0.8V maximum	Short to GND
53	EN_D	D [I]	Switcher D enable input control; external termination required, do not leave floating. LVTTL threshold levels. ‘ON’ threshold is 2.1V minimum	Short to GND
54	MTP	A [I]	A resistor placed to ground on this pin selects which of 15 MTP banks of memory are used. By allowing up to 15 MTP memory banks, a user can use up to 15 identical IRPS5401 devices on a single board using just one customer-configuration file. If this pin is above 2V when POR occurs, the device will not load OTP and the I2C address will be 0Ah. Decouple with 0.01uF cap.	n/a
55	ADDR_PROT		Use a resistor on this pin to set the I2C and/or PMBus Address offset for the device If the I2C register R/W protect security function is used and ‘PIN’ protect is enabled, this pin must be asserted high to disable the R/W protection. Decouple with 0.01uF cap.	n/a
56	FB_D	A [I]	Switcher D feedback input. Connect directly to VOUT_D for output voltages less than 2.55V. Connect to VOUT_D with a 2:1 resistor divider for output voltages greater than 2.55V.	Open
57	GND		Ground. The large metal pad on the bottom must be connected to Ground.	n/a

5 Block Diagram

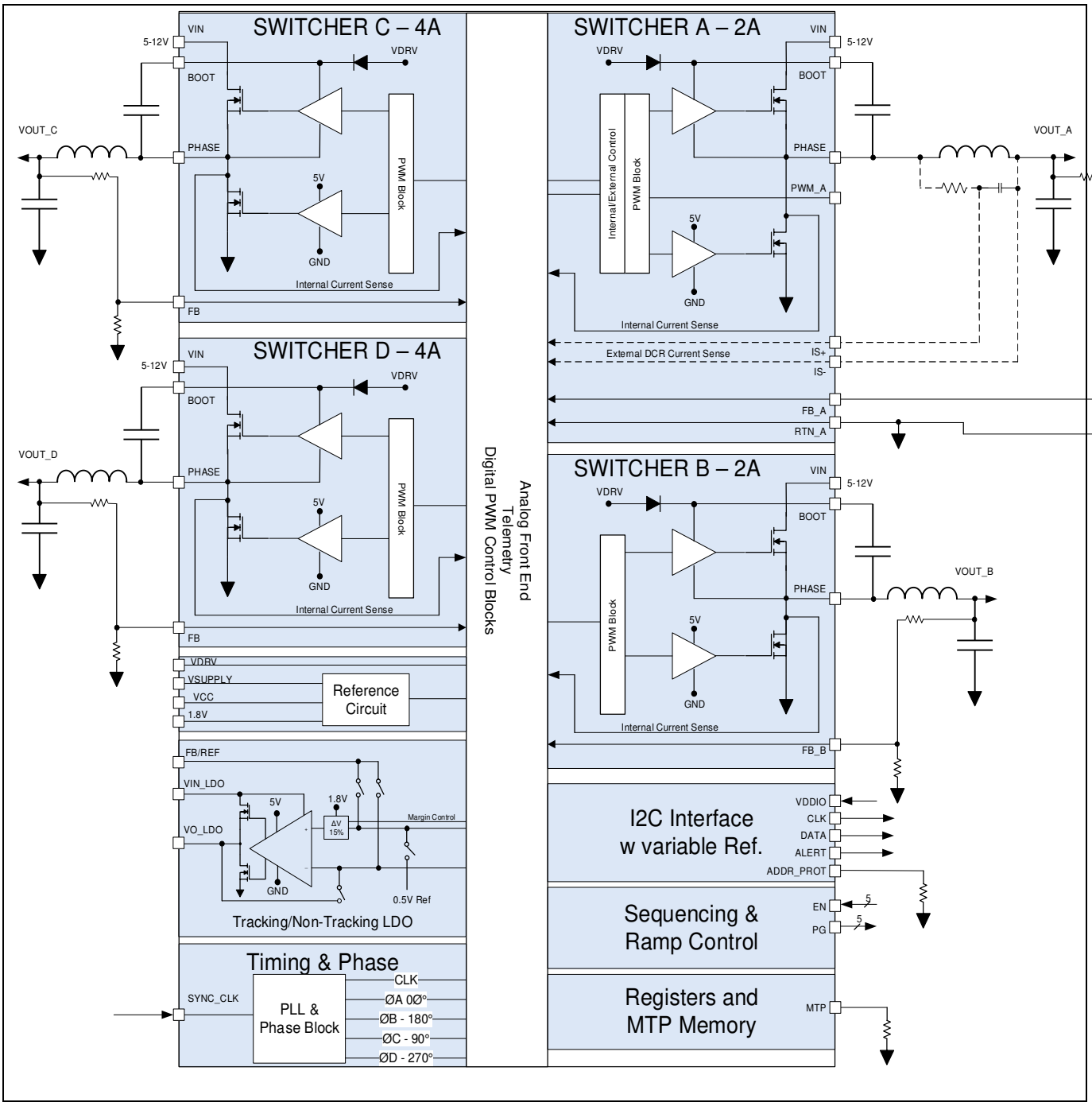


Figure 4 IRPS5401 Block Diagram

6 Absolute Maximum Ratings

Stresses beyond these listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Table 5 Voltage Ratings

Vin [A_B_C_D], VSUPPLY	-0.3V to 16V
VCC, VDRIVE	-0.3V to 6V
VDDIO	-0.3 to 5.5V
1V8	-0.3V to 2V
BOOT [A_B_C_D]	-0.3V to 22V
BOOT [A_B_C_D] <10ns transient	-0.3V to 24V
SW [A_B_C_D]	-0.3V to 16V
SW [A_B_C_D] <10ns transient	-4V to 18V
BOOT to SW [A_B_C_D]	-0.3V to VCC +0.3V (Note2)
Input / Output Pins	-0.3V to VCC +0.3V (Note1)
GND to AGND	-0.3V to +0.3V

Table 6 Thermal Information

Junction to Ambient Thermal Resistance Θ_{JA}	13.5°C/W
Junction to PCB Thermal Resistance $\Theta_{J\text{-}PCB}$	3°C/W
Maximum Storage Temperature Range	-55°C To 150°C
Maximum Junction Operating Temperature Range	-40°C To 125°C (Note 3)
Maximum Lead Temperature (Soldering 10s)	300°C

Note:

1. *Voltages referenced to GND unless otherwise specified*
2. *Must not exceed 6V*
3. *Cold temperature performance is verified via correlation using statistical quality control. Not tested in production.*

7 Electrical Specifications

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

Table 7

Recommended Operating Ambient Temperature Range*	-40°C to 85°C
VIN [A to D]	1.2V to 14V (with external VCC)
VSUPPLY (for Internal VCC)	6V to 14V
External VCC and VDRIVE Voltage Range	4.5V to 5.5V
VDDIO	3.3V
SWA and SWB Output Load	0A to 2A
SWC and SWD Output Load	0A to 4A
Combined SWC+SWD Output Load	0A to 8A

Note: *The electrical characteristics table lists the spread of values verified within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.*

Note: **For operation below 0°C, a delay of 60ms between applying power and output ramp up is required. See more details in 9.3*

Table 8 Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
UVLO Turn-on Threshold				4.2	4.5	V
UVLO Turn-off Threshold			3.6	3.9		V
Supply Current	I_{VCC}	All outputs disabled (low power disabled)		40	45	mA
Supply Current	I_{VCC}	All outputs disabled (low power enabled)		25	30	mA
Supply Current	I_{VCC}	SLEEP# = low (Sleep Mode Enabled)		10	25	uA
VDRV						
UVLO Turn-on Threshold				4.2	4.5	V
UVLO Turn-off Threshold			3.6	3.9		V
Supply Current	I_{vdrv}	All outputs Enabled, fsw =800kHz		15		mA
Internal Supply VCC LDO						
Input Voltage			6	-	14	V
Output Voltage (on Vcc pin)	V_{cc}	Ta=25°C, 6.0V<VSUPPLY<14V, 0mA<Iout<50mA	4.6	4.85	5.1	V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Current	I_{outmax}			-	75	mA
VDDIO						
Input Voltage[1]		I2C termination voltage	1.62	-	5.5	V
Input High Voltage		% of VDDIO	60	-	-	%
Input Low Voltage		% of VDDIO	-	-	30	%
Input Leakage		Vpad = 0 to 5.5V	-1	-	1	µA
Reference Voltage (DAC) [A to D]						
Range			0.25		2.55	V
Resolution				5		mV
Accuracy (0°C to 85°C junction temperature)		VID = 1.0 to 2.55V	-0.8	-	0.8	%
		VID = 0.5V to 0.995V	-8	-	8	mV
		VID = 0.25V to 0.495V	-10	-	10	mV
Accuracy[1] (-40°C to 125°C junction temperature)		VID = 1.0 to 2.55V	-1.5	-	1.5	%
		VID = 0.5V to 0.995V	-15	-	15	mV
		VID = 0.25V to 0.495V	-20	-	20	mV
Oscillator & PWM Generator						
Internal Oscillator[1]			-	48	-	MHz
Frequency Accuracy		0°C to 85°C junction temperature	-3	-	3	%
Frequency Accuracy		-40°C to 125°C	-6.25		+6.25	%
PWM Frequency Range[1]			200	-	2000	kHz
PWM Resolution[1]			-	2.6	-	ns
Digital Inputs – TTL	**ADDR_PROT, EN_x**					
Input High Voltage			2.1	-	-	V
Input Low Voltage			-	-	0.8	V
Input Leakage		Vpad = 0 to 5.5V	-1	-	1	µA
Digital Inputs – TTL	**SLEEP#**					
Input High Voltage			2.1	-	-	V
Input Low Voltage			-	-	0.8	V
Input Leakage		Vpad = 0 to 5.5V	-10	-	10	µA
External Sync	**SYNC**					
Frequency range			200		1000	kHz
Voltage Range			0		5	Vdc
Input High voltage			2.1			V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Low Voltage					0.8	V
Input Leakage current		Vpad = 0 to 5.5V			±5	µA
Sync pin capacitance		Vpad = 0 to 5.5V			10	pF
Synchronization Range (From OTP setting)		0°C to 85°C	-6.25		+6.25	%
Synchronization Range (From OTP setting)		-40°C to 125°C	-3		+3	%
Sync signal Duty Cycle			45	50	55	%
Remote Voltage Sense Inputs	**FB [A to D], RTN_A**					
FB_x Input Current		VOUT = 0.25V to 2.55V	-35	-	90	µA
RTN_A Input Current			-	-50	-	µA
Differential Input Voltage Range[1]		RTN_A = ±100mV	0		2.55	V
RTN_A Input CM Voltage[1]			-100	-	100	mV
Remote Current Sense Inputs	**ISEN_A+/ISEN_A-**					
Common Mode Voltage Range[1]			-0.1	-	Vcc-1	V
Differential Voltage Range[1]			-10	-	60	mV
Analog Address/Level Inputs	**ADDR_PROT, MTP**					
Output Current[1]		Vpad = 0 to 1.2V	96	100	104	µA
Open-Drain Outputs	**PG_x, DATA, ALERT#**					
Output Low Voltage		4mA	-	-	0.3	V
Output Leakage		Vpad = 0 to 5.5V	-	-	±5	µA
PWM I/O	**PWM_A**					
Output Low Voltage		I = -4mA	-	-	0.4	V
Output High Voltage		I = +4mA	VCC-0.45V	-	-	V
Tri-State Leakage		Vpad = 0 to Vcc	-	-	±1	µA
I2C/PMBus						
Bus Speed[1]		Normal	-	100	-	kHz
		Fast	-	400	-	kHz
		Maximum	-	1000	-	kHz

Telemetry Reporting - Switching Outputs [A to D]						
Iout, Iin, Vin and Temperature Filter Rate[1]		Selectable (Selected Frequency applies to all parameters for all loops)	-	0.97, 1.9, 3.8, 7.7, 15.5, 31, 63, 126	-	Hz
Iout, Iin, Vin, Temperature Update Rate[1]			-	25	-	kHz
Vin Reporting Range[1]			0	-	17.5	V
Vin Reporting Accuracy (-2 to 2%)		VIN = 12V	-2	-	2	%
Vin Reporting Accuracy		VIN = 5V	-5	-	5	%
Vin Reporting Resolution[1]			-	31.25	-	mV
Vout Reporting Range[1]		With 2:1 scaling	-	-	5.1	V
Vout Reporting Accuracy[1]		READ_VOUT reports DAC setting		0.5		%
Vout Reporting Resolution[1]	User Selectable per output through VOUT_MODE command. Actual resolution is 5mV/10mV depending on VOUT_SCALING	-	0.244 1.953 3.906	-	mV	
Iout Reporting Gain Accuracy[1]	gain_error	Iread=Iout(1±gain_error)±I_os*full scale	-5		5	%
Iout Reporting Offset Accuracy[1]	I_os	full Scale = 2A for A/B and 4A for C/D	-2.5		2.5	%
Iout Reporting Resolution[1]			-	15.625	-	mA
Iin Reporting Resolution[1]			-	7.8125	-	mA
P_in Reporting Resolution[1]			-	31.25	-	mW
P_out Reporting Resolution[1]			-	31.25	-	mW
Temperature Reporting Resolution[1]				0.25		°C
Temperature Reporting			-2		2	%

Accuracy[1]						
Telemetry Reporting - Switching Output A with External IR MOSFET™ Power Stage						
Iout Reporting Resolution[1]			-	125	-	mA
Iout Reporting Accuracy[1]		At 100% full load. Assumes ± 5% accurate external source	-6		6	%
Iin Reporting Resolution[1]			-	62.5	-	mA
P_in Reporting Resolution[1]			-	250	-	mW
P_out Reporting Resolution[1]			-	250	-	mW
Telemetry Reporting - LDO						
Vin Reporting Range[1]			0	-	8	V
Vin Reporting Resolution[1]			-	7.812	-	mV
Vin Reporting Accuracy			-2	-	2	%
Vout Reporting Range[1]		Vout is measured	0	-	4	V
Vout Reporting Resolution[1]		User Selectable through VOUT_MODE command.	-	0.244 1.953 3.906	-	mV
Vout Reporting Accuracy			-2	-	2	%
Iout Reporting Range[1]			0	-	0.72	A
Iout Reporting Resolution[1]			-	0.976	-	mA
Iout Reporting Accuracy[1]		At 500mA	-10		10	%
P_in Reporting Resolution[1]			-	15.625	-	mW
P_out Reporting Resolution[1]			-	15.625	-	mW

Fault Protection - Switchers [A to D]						
OVP Threshold During Start-up (until output reaches 1V)			1.2	1.35	1.5	V
OVP Threshold During Start-up (until output reaches 1V)			2.4	2.75	3.0	V
OVP and UVP Operating Threshold[1] Range:		Relative to VID, 1:1 scaling	50	-	400	mV
Resolution:			-	50	-	mV
OVP and UVP Operating Threshold[1] Range:		Relative to VID, 2:1 scaling	100		800	mV
Resolution:			-	100	-	mV
OVP and UVP delay[1]		After exceeding threshold	-	-	150	ns
OVP and UVP threshold Tolerance[1]		For thresholds > 200mV	-20		20	%
OC WARN and FAULT Range[2]		Switcher A and B	0	-	4	A
OC WARN and FAULT Range[2]		Switcher C and D	0	-	8	A
OC WARN and FAULT Range[2]		Switcher C in C+D mode	0	-	15.97	A
OC WARN and FAULT Resolution			-	31.25	-	mA
OC FAULT Threshold Tolerance (0°C to 85°C junction temperature)		At 3A for A and B, 6A for C and D, at 12A for C+D	-10		+10	%
OC FAULT Threshold Tolerance[1] (-40°C to 125°C junction temperature)		At 3A for A and B, 6A for C and D, at 12A for C+D	-20		+20	%
OT WARN and FAULT Range[1]			0		255	°C
OT WARN and FAULT Resolution[1]			-	1	-	°C
Fault Protection - Switcher A with External IR MOSFET™ Power Stage						
OC WARN and FAULT Range[2]			0	-	255	A
OC WARN and FAULT Resolution			-	0.25	-	A
External ISENSE Filter Bandwidth			-	62	-	kHz

Fault Protection - LDO						
OV FAULT		Read Only, % of VOUT as set in ldo_target_register - Non tracking OR measured VIN/2 - Tracking	-	125	-	%
OV WARN			-	112.5	-	%
UV FAULT			-	75	-	%
UV WARN			-	87.5	-	%
OC FAULT		Read Only	-	0.72	-	A
OC WARN Range			0	-	0.72	A
OC WARN Resolution			-	3.9	-	mA
MOSFET - Switcher A and B						
High Side Switch Resistance		Tj = 20°C, BOOT-PHASE = 5V	-	150	-	mΩ
Low Side Switch Resistance		Tj = 20°C, VDRV = 5V	-	45	-	mΩ
MOSFET – Switcher C and D						
High Side Switch Resistance		Tj = 20°C, BOOT-PHASE = 5V	-	85	-	mΩ
Low Side Switch Resistance		Tj = 20°C, VDRV = 5V	-	25	-	mΩ
LDO						
Input Voltage	V_{in_ldo}		1.2	-	5.5	V
Output Voltage	V_{out_ldo}		0.5	-	3.6	V
Dropout Voltage	$V_{dropout\_ldo}$	Iout=0.5A, Tj=125°C	-	-	0.5	V
Output Current	I_{out_ldo}		-	-	0.5	A
Reference Voltage	V_{ref_ldo}	Ta = 25°C	490	500	510	mV
		-40°C<Tj < 85°C	485	500	515	mV
Timing Information						
Automatic Configuration from MTP[1]		Time from POR to end of configuration loaded from NVM to working registers	-	1	-	ms
Isense AMP Automatic Trim Time[1]			-	1	-	ms
Delay from Enable high to ramp start[1]		Low power mode disabled	-	3	-	µs
Delay from Enable high to ramp start[1]		Low power mode enabled	-	600	-	µs

1. *Verified by design*
2. *Actual OC limit (MAX sustained load the VR can handle) is a function of inductor ISAT and system thermal solution. SW A and B limited to 2A max DC load. SW C and D limited to 4A max DC load*

8 Typical Application Diagrams

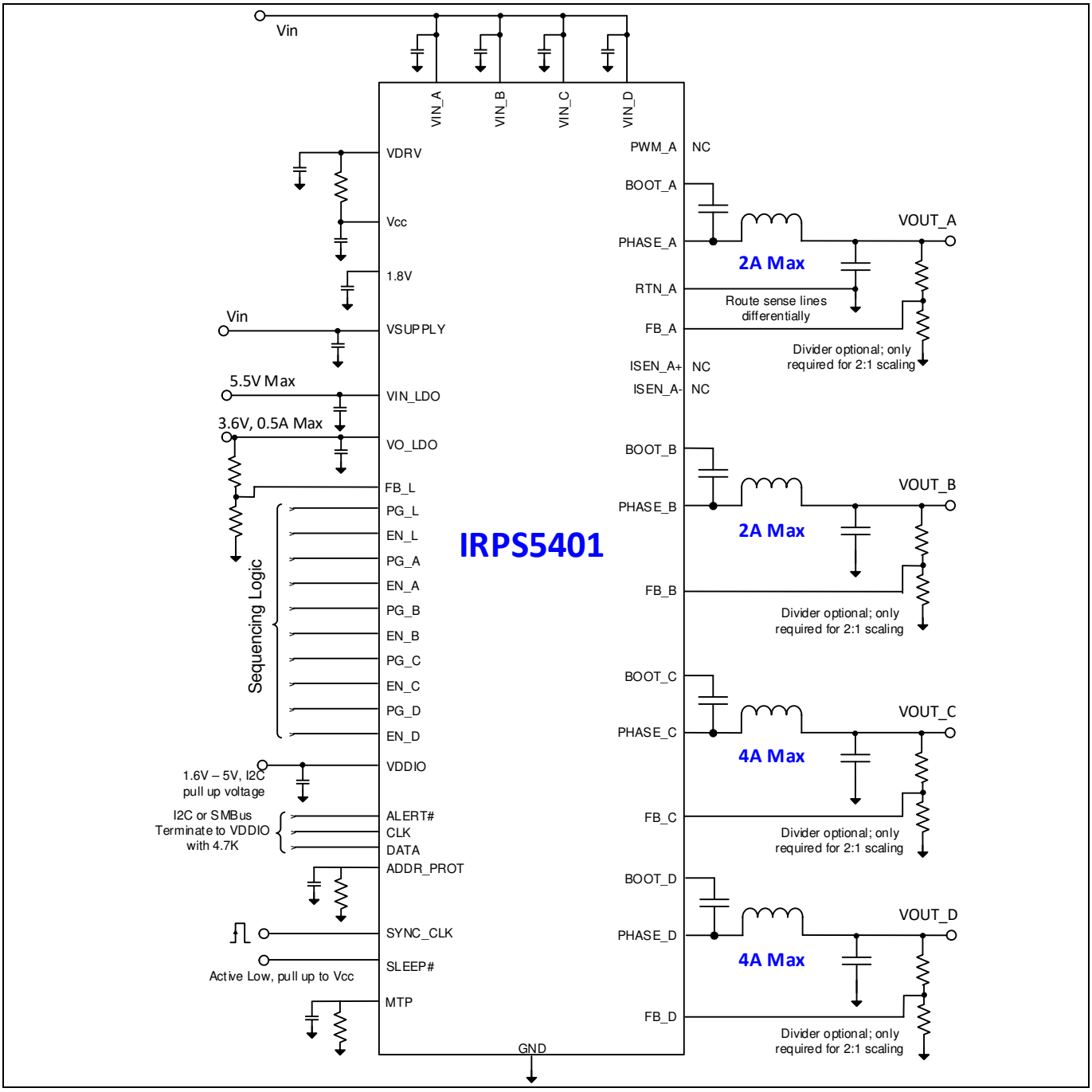


Figure 5 IRPS5401 in 5 output configuration with Vcc from internal LDO

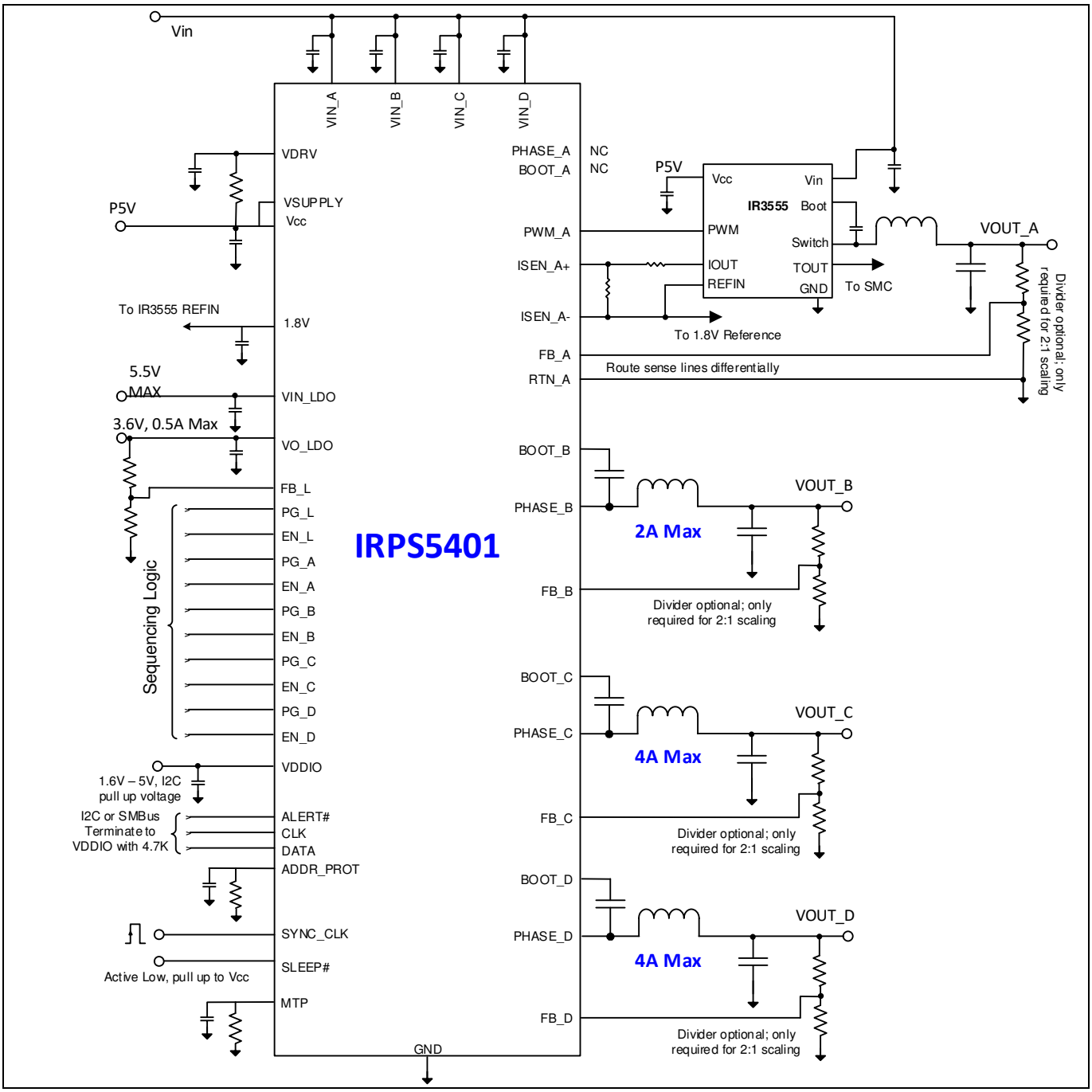


Figure 6 IRPS5401 using external IR MOSFET™ Power Stage for high Current Output

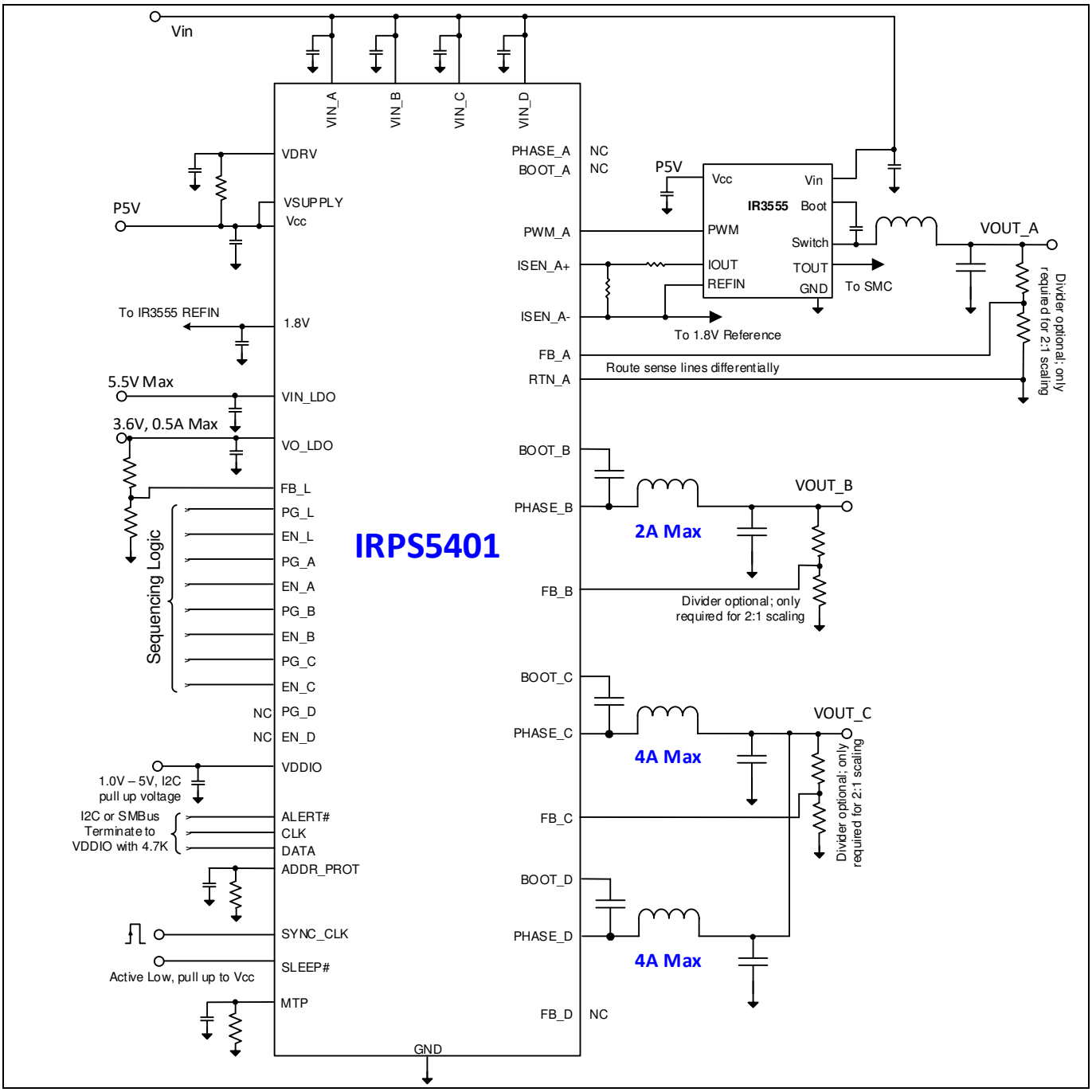
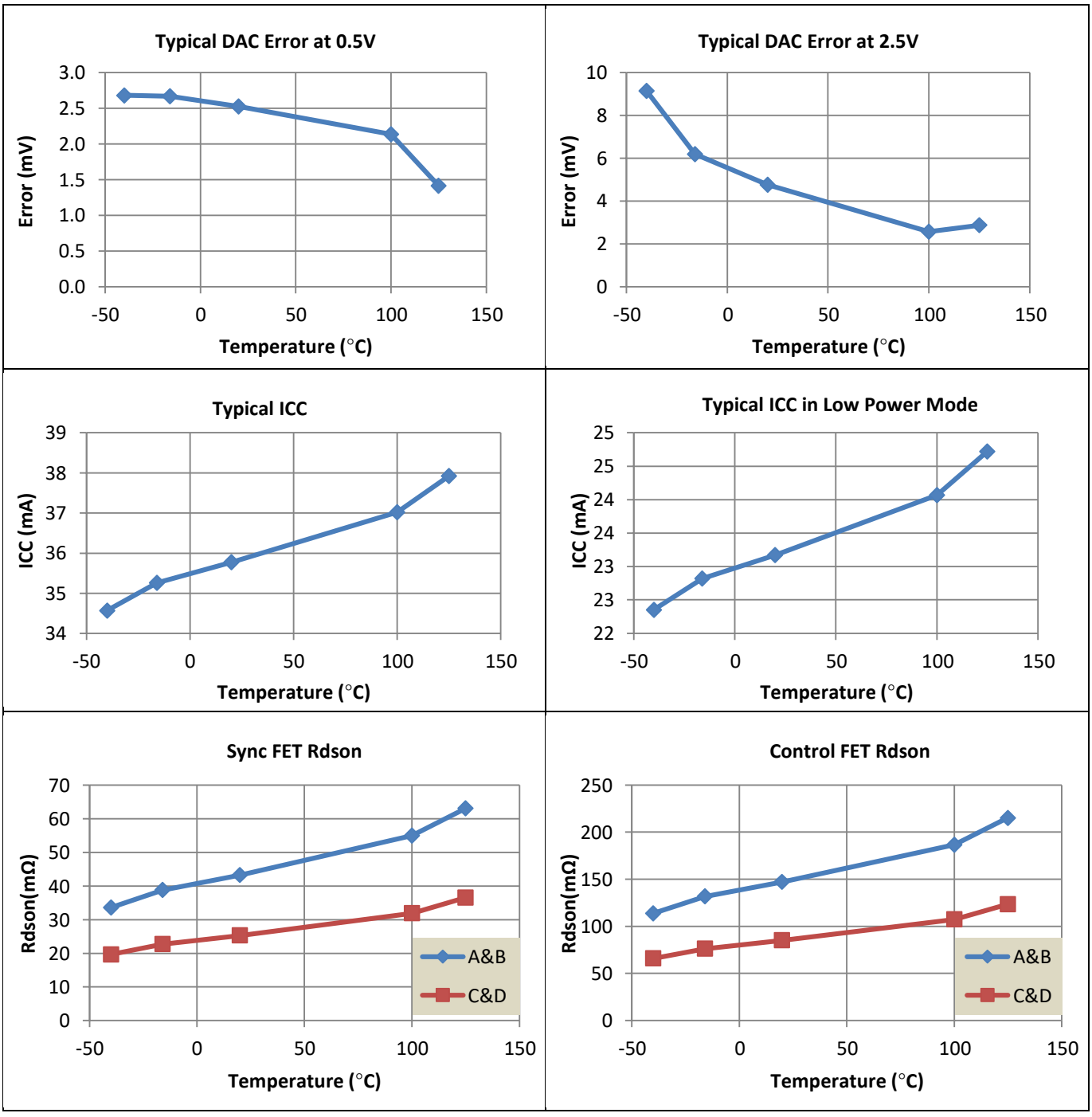


Figure 7 IRPS5401 using Switcher C and Switcher D in parallel for higher current applications

TYPICAL OPERATING CHARACTERISTICS

VCC=5V, -40°C to 125°C



9 Description

The IRPS5401 is a digitally configurable flexible power management unit, with an I2C/PMBus interface. It can support up to 5 rails, with 4 independent switching regulators and one linear regulator.

The switching frequency is programmable from 200 kHz to 2MHz and provides the capability of optimizing the design in terms of size and performance.

The IRPS5401 switchers provide precisely regulated output voltages programmable from 0.25V to 2.55V without a resistor divider and up to 5.1V with a resistor divider.

The IRPS5401 can operate with an internal bias supply (LDO), typically 5.0V. This allows operation with a single supply by connecting the input of the LDO (VSUPPLY) to the bus voltage (Vin_x). A 1uF capacitor should be used at the VSUPPLY pin for decoupling purposes. The output of this LDO is brought out at the Vcc pin and must be bypassed to the analog ground (pin 50) with a 1.0uF decoupling capacitor. An additional voltage, VDRV, required by the internal driver circuitry is derived by using a 2 ohm-1uF filter from the Vcc pin to the VDRV pin. Note that the 1uF at the VDRV pin must be bypassed to the system power ground (pin 57). The Vcc pin may also be connected to the VSUPPLY pin, and an external Vcc supply between 4.5V and 5.5V may be used, allowing for an extended operating bus voltage (Vin_x) range from 1.2V to 14V.

The device utilizes the on-resistance of the low side MOSFET (synchronous MOSFET) as the current sense element. This method enhances the converter’s efficiency and reduces cost by eliminating the need for external current sense resistors.

9.1 One-time Programmable (OTP) Memory

The IRPS5401 has 64K of OTP non-volatile memory. The OTP design is based on a patented split-channel non-volatile anti-fuse memory cell. The OTP memory has a data retention rating of 20 years and an operating temperature range of -40°C to 150°C (-55°C to 150°C storage rating)

This memory space is divided up into 26 OTP segments that can be programmed 1 time. The memory space is therefore referred to as Multiple-times Programmable (MTP). This allows the user to; a) change the configuration registers and re-program the MTP up to 26 times or b) save up to 15 configuration files during initial programing and use the MTP pin to choose which file to load at start up. If option b is used, the remaining unused MTP segments are available for the user to make additional changes to the configuration file and save to MTP using the PowIRCenter GUI device programmer utility.

9.2 MTP pin (pin 54)

The table below shows the MTP segment that will be selected with a given resistor value connected to the MTP pin. The resistor must be connected to the AGND pin and bypassed with a 10nF X7R type multi-layer ceramic capacitor.

Table 9

MTP pin Resistor	MTP Segment selected
*0.845kΩ	+0
*1.30kΩ	+1
*1.78kΩ	+2
2.32kΩ	+3
2.87kΩ	+4
3.48kΩ	+5
4.12kΩ	+6
4.75kΩ	+7
5.49kΩ	+8
6.19kΩ	+9
6.98kΩ	+10
7.87kΩ	+11
8.87kΩ	+12
10.00kΩ	+13
11.00kΩ	+14

Note: *Do not use these values for applications with ambient temperatures <0°C*

Note: *The number of segments that the user chooses to program with multiple configuration files is set by a configuration register called max_prog. The max_prog register value needs to be set to the number of configuration files that will be programmed. For example, if the user programs segments +0, +1, and +2, then the* max_prog *register needs to have a value of 3. For applications with junction temperatures below 0°C, segments +0, +1, and +2 are not available.*

9.3 Device Power-up and Initialization

During the power-up sequence, when VIN is brought up, the internal LDO converts it to a regulated 5.0V at VCC. There is another LDO which further converts this down to 1.8V to supply the internal digital circuitry. An under-voltage lockout circuit monitors the voltage of the VCC pin and the P1V8 pin, and holds the POR low until these voltages exceed their thresholds and the internal 48 MHz oscillator is stable. When the device comes out of reset, it initializes an MTP load cycle, where the contents of the MTP are loaded into the working registers. Once the registers are loaded from MTP, the designer can use I2C/PMBus to re-configure the registers to suit the specific VR design requirements if desired, irrespective of the status of the enable pins.

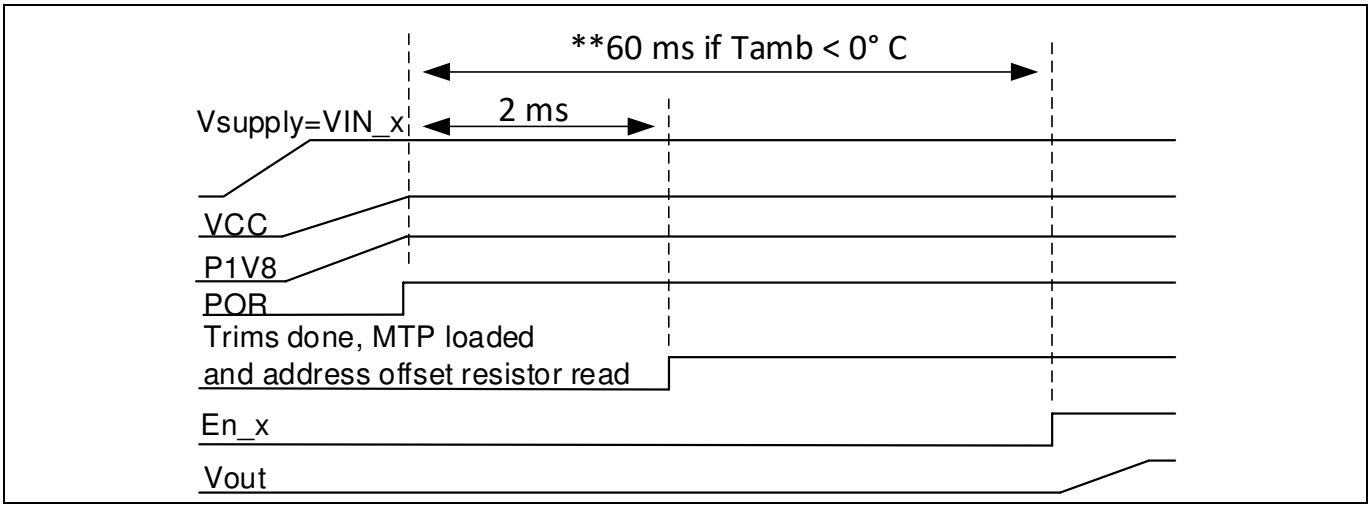


Figure 8 Power up sequence

In the default configuration, power conversion for a given loop is enabled only when the corresponding En_x pin voltage is asserted high, the Vin_x bus voltage exceeds its under voltage threshold (as stored in the MTP registers and commanded by the PMBus commands VIN_ON and VIN_OFF), the contents of the MTP have been fully loaded into the working registers and the device address has been read. IRPS5401 provides additional options to enable the device power conversion through software and these options may be configured to override the default by using the I2C interface or PMBus.

Note: The VDDIO pin voltage must remain stable after device POR. Cycling the VDDIO voltage after a device POR will cause a timing violation of the I2C bus protocol and may result in I2C and PMBus communication issues

*Note: **For Internal Switchers only (Switcher A, B, C, and D), a 60ms delay is required for applications that operate with an ambient temperature less than 0°C. The delay can also be accomplished by delaying the EN pin, using the PMBus TON_DELAY command, or a combination of both. This delay does not apply to the LDO output or Switcher A if Switcher A is configured in External Switcher mode*

9.4 Addressing the IRPS5401

The IRPS5401 has two 7-bit registers that are used to set the base I2C address and base PMBus address of the device, as follows.

Table 10

Register	Description	Default
i2c_device_address	The chip I2C address. An address of 0 will disable I2C communication	10h
pmb_device_address	The chip PMBus address. An address of 0 will disable PMBus communication.	40h

Setting another bit, i2c_take_addr_from_ext, to 1, will allow the user to offset the base address of the device using a resistor from ADDR_PROT to AGND. In such a case, the table below provides the resistor values needed to realize up to 15 offsets from the base address. For applications with junction temperatures below 0°C, address offsets of +0, +1, and +2 are not available.

Table 11

ADDR_PROT Resistor	I2C Address Offset
*0.845kΩ	+0
*1.30kΩ	+1
*1.78kΩ	+2
2.32kΩ	+3
2.87kΩ	+4
3.48kΩ	+5
4.12kΩ	+6
4.75kΩ	+7
5.49kΩ	+8
6.19kΩ	+9
6.98kΩ	+10
7.87kΩ	+11
8.87kΩ	+12
10.00kΩ	+13
11.00kΩ	+14
12.10kΩ	+15

Note: Do not use these values for applications with ambient temperatures <0°C

Another bit **i2c_pmb_addr_lock,** if set, allows the user to lock the I2C and PMBus addresses.

9.5 Switching Frequency

The switching frequency (fsw) setting of the IRPS5401 is stored in MTP and can be configured by using the PMBus command FREQUENCY_SWITCH.

The IRPS5401 with will ACK any FREQUENCY_SWITCH command from 200 kHz to 2MHz in increments of 1kHz (increments of 2kHz with commands above 1MHz). Internally the command is decoded and the actual FSW is set to the nearest value that can be supported with a 48MHz internal clock. For example, 500 kHz can be supported with ninety-six (96) 48 MHz clocks. So if you ask for 500 kHz, you get exactly 500 kHz. But if you wanted 450 kHz, the number of clocks required is 106.6667 (48/0.45). In this case, the frequency would be set to one hundred and seven (107) 48MHz clocks or 448.6 kHz. Fractional values of 0.5 and above are rounded up to the next whole number.

Because of the enforced phase relationship between the four switching regulators, the switching frequency for all four switching regulators is determined by the FREQUENCY_SWITCH command sent to Switcher C. FREQUENCY_SWITCH commands sent to Switchers A, B, and D will be ACK'd and ignored. A FREQUENCY_SWITCH read command sent to Switchers A, B, or D will respond with the value that the user wrote into the device but the actual switching frequency for Switcher B and D will be the switching frequency of Switcher C. The switching frequency of Switcher A will be the switching of Switcher C if the FREQUENCY_SWITCH value for Switcher A is the same as or greater than Switcher C. The switching frequency of Switcher A will be one half of the switching frequency of Switcher C if the FREQUENCY_SWITCH value for Switcher A is less than Switcher C. The switching frequency of Switcher A will be ½ of Switcher C even when synced to an external CLK. This frequency relationship between Switcher A and Switcher C is the same with

Switcher A using internal mode or external power stage mode. Switcher A will have the same switching frequency as Switcher C if Switcher C frequency is less than 400 kHz.

Even when running off an internal clock, all four switchers exhibit fixed phase relationships with one another, with Switcher A leading Switcher C by 90^0
which in turn leads loop B by 90^o. Finally loop D lags loop B by 90^0. Thus loops A and B are out of phase by 180^0 as are loops C and D.

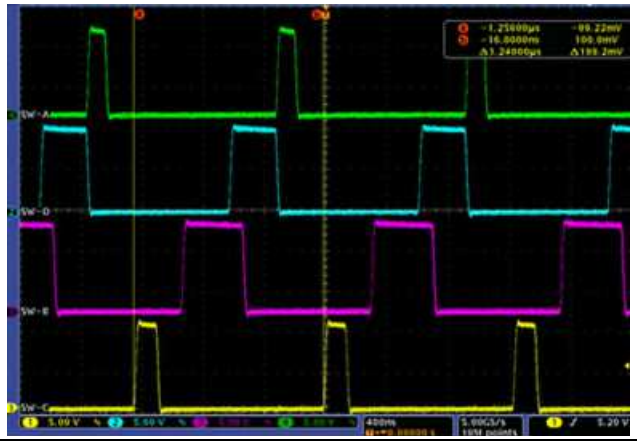


Figure 9 Switcher phase relationship

9.6 Synchronizing to an External Clock

IRPS5401 implements a frequency lock loop which forces all four switcher loops to operate at the same frequency as an external synchronization clock. The four switchers still maintain the same phase relationships with each other as they do when running from an internal clock. Switcher A shows a small phase offset (~80ns) from the sync clock.

- If the sync clock is within ± 6.25% of the programmed frequency, the device will phase and frequency lock to the incoming sync clock.
- If the sync clock is more than ± 12.5% away from the programmed frequency, the device will lose sync and will relax gradually to the programmed frequency.
- Once the device is in sync, it will have a ± 10 ns uncertainty or jitter with respect to the sync clock.
- It takes about 110us for the circuit to lock to the Sync clock.

9.7 Switcher A in External Powerstage Mode

Switchers B, C and D can only be operated in internal power stage mode, and their PWM signals are not brought out to a pin. However, using an MTP register bit, sw_a_use_internal_driver, Switcher A can be configured to operate in either internal power stage mode (sw_a_use_internal_driver=1) or in external power stage mode (sw_a_use_internal_driver = 0). In the external power stage mode, the PWM output of Switcher A is brought out to the PWM_A pin and can be connected to the PWM input pin of industry standard tri-state type drivers or Infineon power stage devices. The logic of operation for the tri-state drivers is depicted in the figure below.

Note that the PWM_A output is tri-stated whenever the Switcher A is disabled, the shut-down ramp has completed or before the soft-start ramp is initiated.

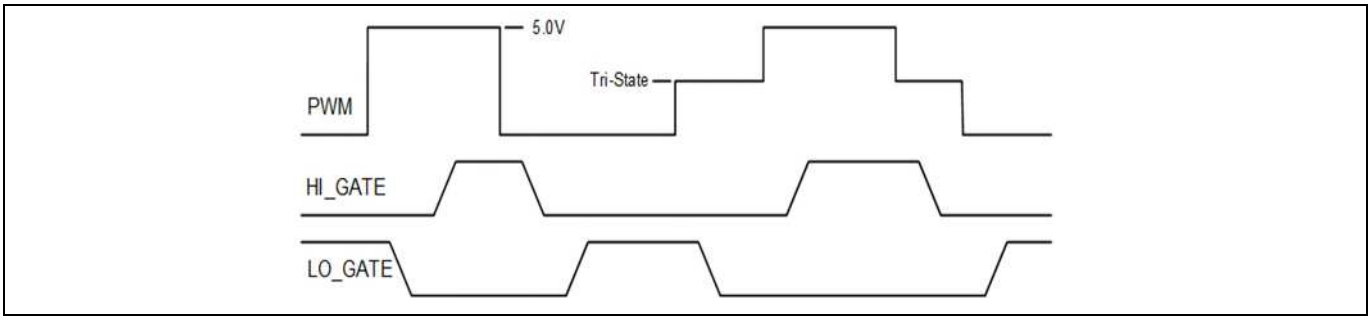


Figure 10 PWM_A tri-state details

PWM_A is a 5V PWM signal. A 3V zener clamp must be used to limit the power stage PWM pin voltage when the IRPS5401 is paired with an external power stage that does not support 5V PWM input. A series resistance of 402 Ω must used to limit the zener current.

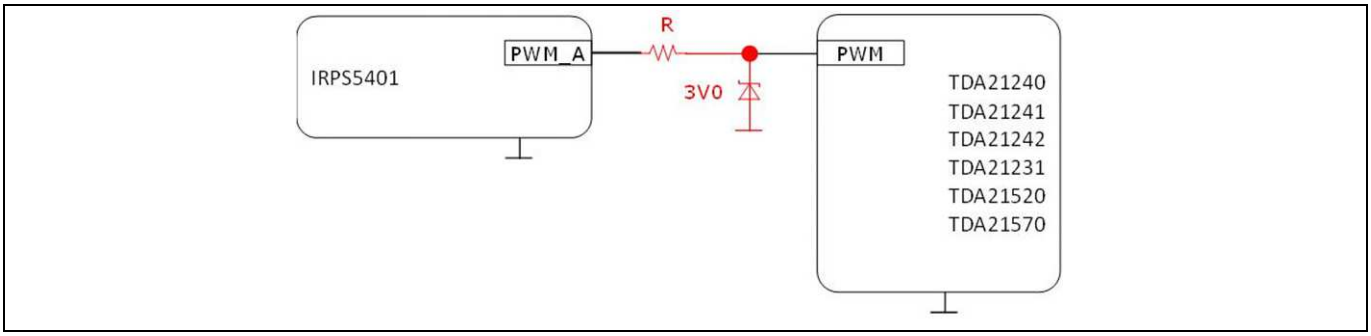


Figure 11 Zener clamp details when using power stages that only support 3.3V PWM input

9.8 Digital Controller & PWM

For the switcher loops A, B, C and D, the IRPS5401 uses a proprietary emulated current mode control scheme, which makes it possible to use PI control to stabilize the loop for all types of inductors and capacitors, including MLCC. The digitized error voltage from the high-speed voltage error ADC is processed by a digital compensator, the proportional (K_p) and Integral (K_i) coefficients, which are programmable. The output of the compensator is then compared with an emulated current signal to generate the PWM signal, with a resolution of 2.6ns to avoid limit cycling. As a close realization to a Type II analog compensator, the control engine also implements a low pass, programmable single pole (K_{pole}) filter. This defaults to 1.1MHz and in general, it should not be necessary to change the location of this pole over a wide range of applications.

Ordinarily, a power stage using low ESR capacitors such as MLCCs requires the use of Type III compensation or PID control, but, in the IRPS5401, the emulated current mode modulator provides another pole-zero pair, unburdening the compensator and allowing a simple PI compensator to stabilize even such demanding applications.

The compensator transfer function is defined as

$$(Kp + \frac{Ki}{s}) \bullet \left(\frac{1}{1 + \frac{s}{\omega p_1}} \right)$$

- Where, ωp_1 is the pole typically positioned to filter noise and ripple, and programmable through the register K_{pole1}[3:0]
- K_p is the proportional coefficient, programmable through the register k_p[5:0]

- And K_i is the integral coefficient programmable through the register k_i[5:0].

9.9 Diode Emulation / Discontinuous Mode Operation/AOT

Under very light loads, efficiency can become dominated by MOSFET switching losses. Using the manufacturer specific PMBus command MFR_FCCM, it is possible to enhance the light load efficiency by allowing the controller to work in an adaptive on time (AOT) or diode emulation mode.

Table 12

MTP Register	Function	Default
diode_emu_thresh	Sets the error voltage at which an on-time pulse is started in 2mV steps	0h
diode_emu_pw	Sets the duration of the on-time pulse	4h
de_off_time_adjust	Reduces the calculated low-side FET on-time in 62.5ns steps. Useful for compensating for DrMOS or other drivers' tri-state delay for a better prediction of the zero-crossing	0h
le_th	Error threshold to go from discontinuous conduction mode to continuous conduction mode; 4 mV resolution. If Vout drops by this amount, the control will be handed to PWM and diode-emulation is ended.	1h
Inductor_ni_thresh	Total current threshold below which it is assumed that the inductor current has a negative component.	00h

When the current reading drops below ni_thresh, the controller determines that the inductor current has a negative component, and if MFR_FCCM=0, will allow AOT mode operation. Internal circuitry determines, using diode_emu_pw and the read values of Vinx and Voutx, when the inductor current declines to zero on a cycle by cycle basis and shuts off the low-side MOSFET at the appropriate time in each cycle. This reduces conduction losses and also lowers the switching frequency resulting in improved efficiency because the inductor and low-side MOSFET are not sinking power from the output capacitors at light loads.

In AOT mode, if Vout drops below a certain threshold (le_th) due to applying a fast transient load, the operation is switched to continuous current mode (CCM) instantly.

Industry standard tri-state drivers typically have slow tri-state entry times, which allows negative current to build up reducing efficiency and causing ringing.
The *off_time_adjust* variable allows the designer to compensate for the tri-state delay by reducing the low-side FET on-time by an equivalent amount.

9.10 Output Voltage Sensing, Telemetry and Faults

The IRPS5401 provides true differential remote sensing for the Switcher A output. The FB_A and RTN_A pins are connected to the load sense pins of the Switcher A output voltage to provide true differential remote voltage sensing with high common-mode rejection. This allows Switcher A (in external power stage mode) to provide excellent regulation even in high current applications. Switcher loops B, C and D have single ended feedback connections for sensing and regulation. Each loop has a high bandwidth error amplifier that generates the error voltage between this remote sense voltage and the target voltage. The error voltage is digitized by a fast, high-precision ADC. This digitized error is used for Vout under voltage fault and warning detection as well as for Vout overvoltage fault warning detection. Vout is reported using the READ_VOUT PMBus command. The reported Vout is the DAC reference value and not the actual measure output voltage.

As shown in the figure below, the Vsen and Vrtn inputs have a 20kΩ pull-up to an internal 1V rail. This causes some current flow in the Vsen and Vrtn lines so external impedance should be kept to a minimum to avoid creating an offset in the sensed output voltage.

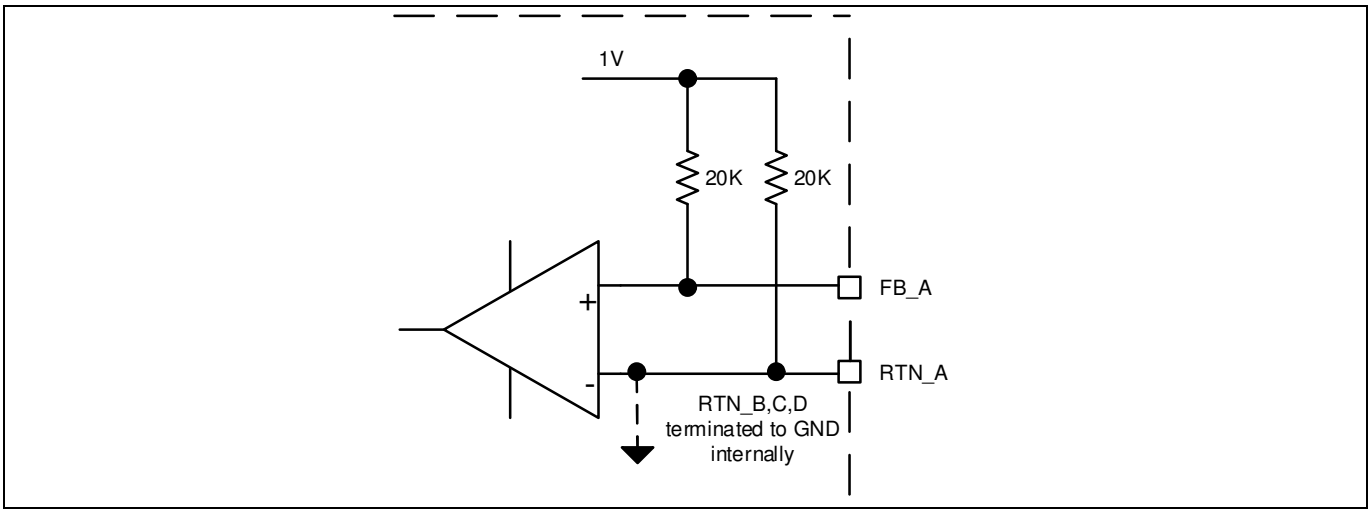


Figure 12 Output Voltage Sensing impedance

9.11 Output Over Voltage Protection (OVP)

If the output voltage exceeds a user-programmable (through PMBUS) threshold, the IRPS5401 detects an output over-voltage fault and latches on the low-side MOSFET to limit the output voltage rise

It should be noted, however, that although the overvoltage threshold is programmable to any value using the PMBus command, VOUT_OV_FAULT_LIMIT, internally it is translated into an offset from the commanded or reference voltage, with a resolution of 50 mV (100 mV if a 2:1 divider is used) and with a minimum value of 50 mV (100 mV if a 2:1 divider is used) and maximum value of 400 mV (800 mV if a 2:1 divider is used).

Under OVP conditions, depending on the setting of the VOUT_OV_FAULT_RESPONSE, the converter can be configured to keep regulating or to go into a latched shutdown, where the high side FET or Control FET is turned off and low side FET or Sync FET is turned on. Note however that there is an MTP register, vpu_high_release_en, that allows the low side FET operation to be configured in one of two ways: a) remain latched on indefinitely or b) remain latched on until the output voltage falls below 200mV at which time the low-side FET is released. This release mode can reduce or prevent undershoot of the output voltage.

During soft-start, OVP is triggered at the fixed soft-start level. This level can be chosen, using an MTP register, from two different values of 1.35V or 2.75V respectively. If a 2:1 divider is used, these values automatically scale to 2.7V and 5.5V respectively. In fact, it is this value which limits the maximum output voltage the IRPS5401 can support to 5.5V.

Note that in the FET release mode, if the output voltage rises above the fixed OVP level, the low side MOSFET's will again be turned on until Vout drops below the release threshold level.

The user can cycle out of a latched over voltage fault by cycling En_x, VCC or the PMBus Operation command.

The other output are unaffected by the OVP event unless global_fault_en=1

Note: An OCP event may cause the VOUT_OV_WARN bit in the STATUS_VOUT register to falsely assert

Figure 13 OVP with vpu_high_release_en=1

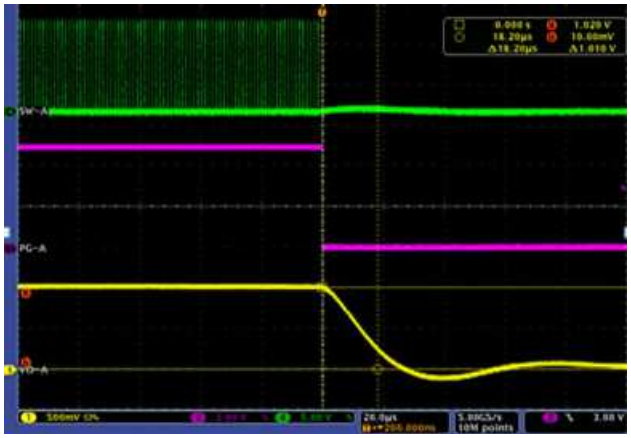


Figure 14 OVP with vpu_high_release_en=0

9.12 Output Under Voltage Protection (UVP)

The IRPS5401 detects an output under-voltage condition if the sensed voltage is below the user-programmable (through PMBus) UVP threshold. Upon detecting of an output under-voltage condition, the IRPS5401 can be configured using the PMBus command, VOUT_UV_FAULT_RESPONSE to keep regulating or to go into a latched shutdown.

It should be noted, however, that although the undervoltage threshold is programmable to any value using the PMBus command, VOUT_UV_FAULT_LIMIT, internally the UV threshold depends upon the setting of a register bit, vout_uv_by_adc, which can be set to either 0 (Vout undervoltage mechanism is through an analog comparator) or to 1 (Vout undervoltage mechanism is through the hign speed error ADC saturation).

If the Vout undervoltage mechanism by comparator is selected, the VOUT_UV_FAULT_LIMIT is translated into an offset from the commanded or reference voltage, with a resolution of 50 mV (100 mV if a 2:1 divider is used) and with a minimum value of 50 mV (100 mV if a 2:1 divider is used) and maximum value of 400 mV (800 mV if a 2:1 divider is used).

On the other hand, if the ADC saturation mechanism is selected, the undervoltage threshold is implicitly 250 mV (500 mV if a 2:1 divider is used) below the commanded or reference value.

The user can cycle out of a latched under voltage fault by cycling Enable, VCC or the PMBus Operation command.

9.13 Current Sensing, Telemetry and Faults

The IRPS5401 has two different current sense mechanisms; a) Sync FET Rdson current sensing in internal powerstage mode and b) DCR, shunt current sensing, or Rdson sense in external powerstage mode.

Current sensing for Switchers B, C and D is always across the Rdson of the Sync FET. Current sensing for Switcher A is also across the Sync FET Rdson if in internal powerstage mode. A proprietary patented scheme allows reconstruction of the average inductor current from the voltage sensed across the Sync FET Rdson. It should be noted here that in internal powerstage mode it is this reconstructed average inductor current that is digitized by the monitor ADC and used for output current reporting. However, in this mode, the overcurrent protection mechanism relies on an analog comparator and does not depend on the ADC or on the output current reporting.

If Switcher A is operated in external powerstage mode, the current is sensed through the drop across a precision current shunt, the drop across the inductor DCR, or the IOUT signal of an Infineon Rdson power stage like the IR3555 and is fed to a differential current sense amplifer at the ISEN_A+ and ISEN_A- pins of the IRPS5401.

For DCR sensing, a suitable resistor-capacitor network of R_{sen} and C_{sen} is connected across the inductor as shown in the figure below. The time constant of this RC network is set to be equal to the inductor time constant (L/DCR) such that the voltage across the capacitor C_{sen} is equal to the voltage across the inductor DCR. A 100K NTC thermistor is also recommended across C_{sen} to compensate for the positive temperature coefficient of inductor DCR

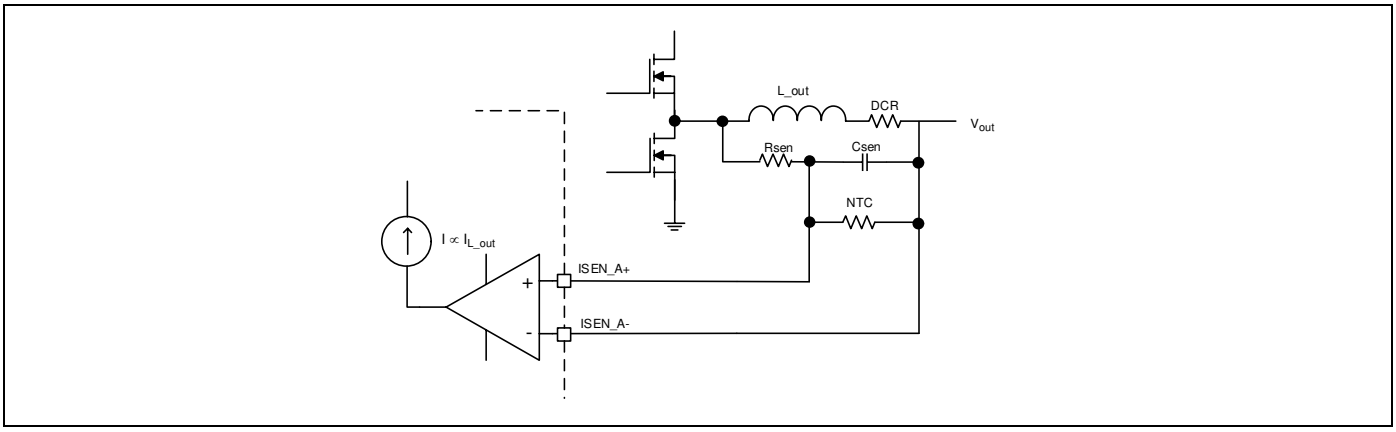


Figure 15 DCR Current Sensing

The recommended value for C_{sen} is a 220nF NPO type capacitor.

$$Rsen = \ (L\_out) \ / \ (DCR * Csen)$$

For example, if L_out is a 1uH, 2mΩ inductor, then Rsen would be set to 5kΩ (with Csen = 0.1uF)

These components must be placed close to the IRPS5401 pins.

For Rdson current sense, the signal from the power stage IOUT pin is reporting IOUT with a gain of 5mV/A. This signal should be attenuated with a 5:1 divider so that the input to the ISENSE amp is 1mV/A. For noise immunity reasons, the differential ISENSE signal is offset above GND by connecting the ISEN_A- pin to a reference voltage. This is usually the 1.8V reference provided by the internal 1.8V LDO

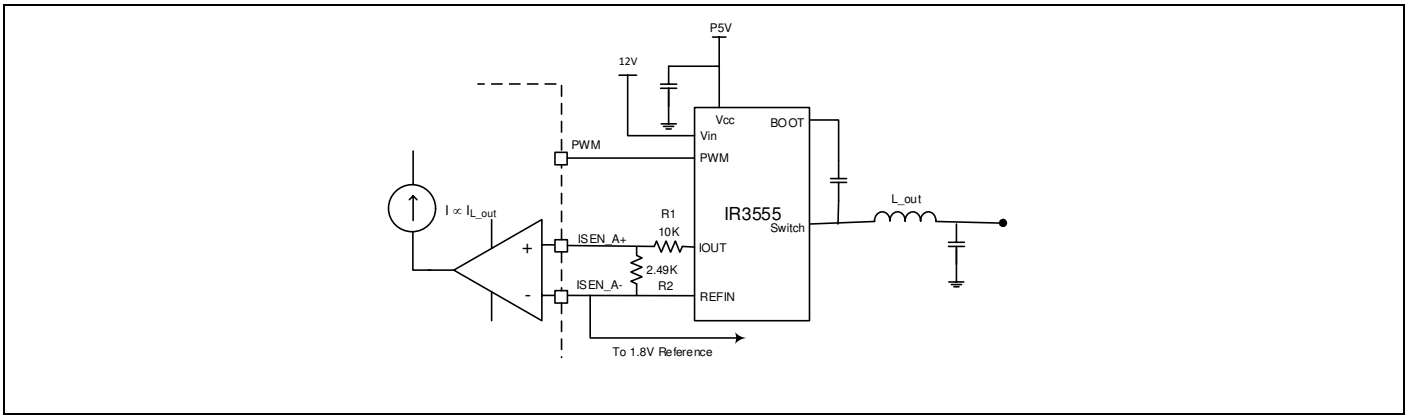


Figure 16 Rdson Current Sensing

The output of this differential current sense amplifier, the gain of which is programmable through an MTP register d2a_ecs_gain [2:0], is digitized by the monitor ADC. The output code of the ADC is then converted using the MTP register ecs_scale [7:0] into output current (in Amps), which is reported on the bus and also used for overcurrent fault detection.

Current is reported using the READ_IOUT PMBus command.

Note: Switcher outputs that are in the 'OFF' state will falsely report an output current if the user sends a READ_IOUT command to an output that is 'OFF'. This false output current will cause the IOUT_OC_WARN bit to assert in the STATUS_IOUT register. The user will need to send the CLEAR_FAULTS command after the output has been enabled.

9.14 Over-current Protection (OCP)

In internal powerstage mode, the over current (OC) protection is implemented by sensing current through the $R_{DS(on)}$ of the Synchronous MOSFET (Sync FET). This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and eliminates any layout related noise issues. The current limit scheme in the IRPS5401 uses an internal temperature compensated current source that has the same temperature coefficient as the $R_{DS(on)}$ of the Sync FET. As a result, the over-current trip threshold remains almost constant over temperature. Moreover, the IRPS5401 also incorporates Vgs compensation that limits the OCP variation with changes in VCC voltage.

The OCP circuit samples the current at the center point of the Sync FET conduction time, and trips the analog overcurrent comparator if it is more than the overcurrent protection setting as dictated by the PMBus command IOUT_OC_FAULT_LIMIT. Although the PMBus comand will allow setting the OC threshold up to a maximum of 15.97A (for internal driver), the internal circuitry saturates the current limit at 4A for Switchers A and B with the 2A internal power stages and to 8A for Switchers C and D with the 4A power stages. Moreover, the threshold set by the PMBus command is rounded to the closest higher 250 mA for the 2A power stages and to the closest higher 500 mA for the 4A power stages.

In external power stage mode, an over current fault is flagged when the digital reading of the output current exceeds IOUT_OC_FAULT_LIMIT.

Additionally, through the PMBus command IOUT_OC_FAULT_RESPONSE, the user can choose between 3 types of responses to an overcurrent fault.

Table 13

OCP Response Mode
Immediate shutdown and then latch off
Immediate shutdown and retry 6 times before latching off, 22ms period
Immediate shutdown and retry indefinitely, 22ms period

The user can cycle out of a latched over current fault by cycling En_x, VCC, VINx, or the PMBus OPERATION command (with correct ON_OFF_CONFIG setting).

Additionally, in both the internal and external power stage modes, an over current warning is flagged if the digital reading of the output current exceeds IOUT_OC_WARN_LIMIT.

9.15 Input Voltage Sensing, Telemetry and Faults

For the switchers, the input voltage is fed through a 14:1 divider to a monitor ADC. The digitized voltage is reported over the PMBus using the READ_VIN command. It is also used to implement an input under voltage lockout threshold, an input voltage warning threshold and an input voltage over voltage threshold through the following PMBus commands.

Table 14

Function	PMBus Command	Default
UVLO	VIN_ON	F001h
UVLO	VIN_OFF	F000h
Under voltage warning	VIN_UV_WARN_LIMIT	E000h
Overvoltage fault	VIN_OV_FAULT_LIMIT	E200h

Additionally, through the PMBus command VIN_OV_FAULT_RESPONSE, the user can choose between 2 types of responses.

Table 15

VIN OV Response Mode
Ignore
Immediate shutdown and then latch off

The user can cycle out of a latched VIN Overvoltage fault by cycling En_x, VCC, or the PMBus Operation command.

9.16 Die Temperature Sensing, Telemetry and Faults

The IRPS5401 uses on-die temperature sensing for accurate temperature reporting and over temperature detection. Also, to account for temperature gradients across the die, temperature sensing is actually done by two separate sense circuits at different locations on the die. So, Switchers A and B share one temperature sensor, while Switchers C and D as well as the LDO share another temperature sensor. Therefore, the READ_TEMPERATURE PMBus command reports the same temperature on Switchers A and B. Also, Switchers C and D as well as the LDO report the same temperature. The reporting resolution is 0.250°C.

PMBus commands OT_FAULT_LIMIT and OT_WARN_LIMIT allow the user to set the over temperature fault and warning thresholds respectively.

Additionally, through the PMBus command OT_ _FAULT_RESPONSE, the user can choose between 3 types of responses to an over temperature fault, i.e., when the digital reading of the temperature exceeds OT_FAULT_LIMIT.

Table 16

OT Response Mode
Ignore
Immediate shutdown and then latch off
Auto restart if fault condition disappears

The user can cycle out of a latched over temperature fault by cycling En_x, VCC or the PMBus Operation command.

9.17 Power Sequencing and Global Faults

The IRPS5401 provides flexibility in sequencing the startup and shutdown of the five outputs via the following PMBus commands:

Table 17

Output	Sequencing Function	PMBus command	Default
Switchers A,B,C and D	Startup	TON_DELAY	F800h
		TON_RISE	F004h
	Shutdown	TOFF_DELAY	F800h
		TOFF_FALL	F004h
LDO	Startup	TON_DELAY	F800h

The figure below shows the four outputs starting up and shutting down with each output delayed 0.5ms from the previous.

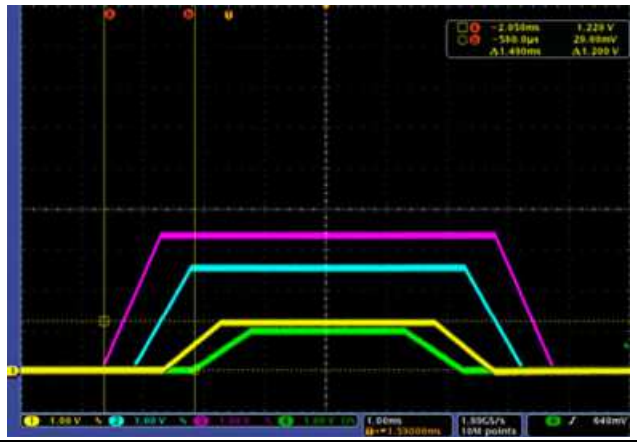


Figure 17 VO sequencing

An extra level of flexibility in sequencing the different outputs is provided by the Global Faults feature in IRPS5401. This is a useful feature that forces all 5 rails to shut down in response to a fault that shuts down any one of the rails. This is enabled by setting an MTP register bit global_fault_en. The figure below shows the response of all the IRPS5401 outputs in response to a shutdown of Switcher A by an output over voltage fault when global_fault_en=1, enabling global fault shutdown and global_fault_en=0, disabling global fault shutdown.

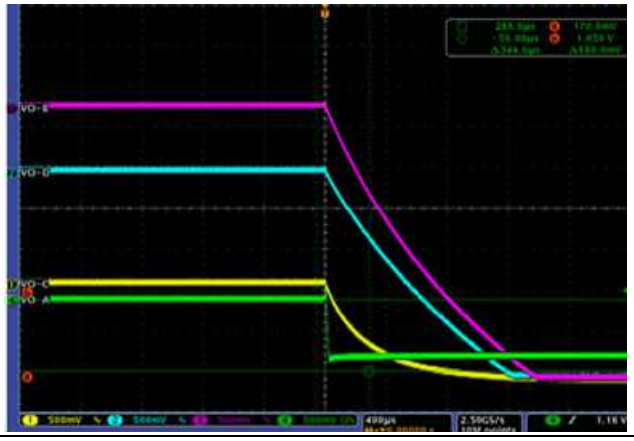


Figure 18 Global_fault_en=1

Figure 19 Global_fault_en=0

9.18 Sleep

The IRPS5401 has an input pin, SLEEP#, which can be pulled low to act as a master disable for all the rails if MTP register bit, por_sleep_mode_en, is set. In fact, pulling this pin low will put the device into an ultra-low power state with <10 uA quiescent current. It will cause the 1.8V to go low, disable all communication and force a power-on reset, so that the contents of all the volatile registers are lost and restored to their reset values. If this pin is pulled high again, the device has to go through a POR cycle again requiring a full MTP load.

9.19 Combined Switcher C and D Operation

Switchers C and D may be combined into a single output and operated in parallel to support load currents up to 8A. In order to do this an MTP register bit, *combine_outputs_c_d*, must be set to 1. In this mode Switcher C and D SW pin output are 180° out of phase. Switcher C takes over the error voltage sensing and the control loop and the internal PWM_C signal is used for the internal power stages of both loops C and D. The table below summarizes the modification to the reporting, fault and warning thresholds as a result of combining Switchers C and D. Any PMBus command to Switcher D will be NACK'd

Table 18

PMBus Command to Switcher C	Response
READ_IOUT	Will report the total Switcher C+D output current
READ_VIN	Will report the Switcher C input voltage (VIN_D and VIN_C must be connected to the same input)
READ_IIN	Will report the total input current for Switcher C+D
IOUT_OC_FAULT_LIMIT	Will set the Switcher C and D FAULT value to ½ this value
IOUT_OC_WARN_LIMIT	Will set the Switcher C and D WARN value to ½ this value
VIN_ON VIN_OFF	Will be applied to Switcher C (VIN_D and VIN_C must be connected to the same input)
IOUT_CAL_OFFSET	Will be applied to the total Switcher C+D output current

9.20 Linear Regulator

The IRPS5401 also has a linear regulator (LDO) in addition to the four switchers. This regulator can accept a wide input voltage range from 1.2V to 5.5V and provide output voltages from 0.5V to 3.3V, delivering up to 0.5A of continuous current with a low dropout voltage of 0.6V. Moreover, the regulator can be configured using an MTP register bit ldo_track_config. To operate in source-only mode, set ldo_track_config to 0. To operate in tracking mode, set ldo_track_config to 1. The tracking mode of operation makes it ideal for use in memory termination tracking applications (Vtt). The LDO also supports a manufacturer specific PMBus command, MFR_LDO_MARGIN, to allow margining the output voltage ±15%.

The reference voltage for the LDO is nominally 0.5V and hence a resistor divider is needed from Vo_LDO to FB_L to generate output voltages higher than 0.5V. In tracking mode, the reference is an internal 2:1 divider to Vin_LDO. It should be noted here that for the LDO, the VOUT_OV_FAULT_LIMIT, VOUT_UV_FAULT_LIMIT, OUT_OV_WARN_LIMIT and VOUT_UV_WARN_LIMIT PMBus commands are Read-Only, and they report the corresponding thresholds calculated internally based on either 1/2Vin_LDO (tracking mode) or on the contents of an MTP register ldo_target_vout [7:0] (non-tracking mode).

9.21 LDO Monitoring and Faults

Unlike the switcher loops, fault detection for all LDO faults except overcurrent fault relies on digital monitoring and digital comparison.

9.22 Output Voltage Reporting, Output Overvoltage Protection and Undervoltage Protection

The output voltage is fed through an internal 3.2:1 divider to a 10-bit monitor ADC. The digitized voltaged is then reported on the PMBus using the READ_VOUT command. It is this MTP register that is used to “tell” the device what the target output voltage is based on the 0.5V reference and the feedback divider. This register has a resolution of 1/64V.

The various output voltage fault and warning thresholds are shown in the table below:

Table 19

	Non-Tracking	Tracking
OV Fault limit	125% target voltage	125% (Vin_LDO/2)
UV Fault limit	75% target voltage	75% (Vin_LDO/2)
OV Warn limit	112.5% target voltage	112.5% (Vin_LDO/2)
UV Warn limit	87.5% target voltage	87.5% (Vin_LDO/2)

The responses to both the overvoltage and undervoltage faults can be programmed to either ignore or to shutdown, similar to the switchers.

9.23 Input Voltage Reporting, Input UVLO and Input Overvoltage Protection

The input voltage is fed through an internal 6.4:1 divider to a 10-bit monitor ADC. The digitized voltaged is then reported on the PMBus using the READ_VIN command. It is also used to implement an input under voltage lockout threshold, an input under voltage warning threshold and an input over voltage threshold through the following PMBus commands

Table 20

Function	PMBus Command	Default
UVLO	VIN_ON	D808h
	VIN_OFF	D800h
Under voltage Warning	VIN_UV_WARN_LIMIT	C800h
Overvoltage fault	VIN_OV_FAULT_LIMIT	CAC0h

Additionally, through the PMBus command VIN_OV_FAULT_RESPONSE, the user can choose to ignore a VIN over voltage fault or to shut down in response to it.

The user can cycle out of a latched VIN over voltage fault by cycling Enable, VCC or the PMBus Operation command.

9.24 Over Current Protection

The PMBus command IOUT_OC_FAULT_LIMIT is implemented as Read_Only for the LDO, and it reads 0.72A. Thus, the LDO has a fixed overcurrent limit of 0.72A. An internal analog control loop limits the current to this threshold and hence causes the output voltage to drop. When the output voltage drops below the UV fault limit

of the LDO, it flags a UV fault (rather than an over current fault), but still responds based on the setting of IOUT_OC_FAULT_RESPONSE (constant current limiting or shutdown).

Further, if IOUT_OC_FAULT_RESPONSE is configured for a constant current response; an additional MTP bit, ldo_foldback_enable, can be configured to allow for a current limit foldback response when the UV fault limit is exceeded. The ldo_foldback_enable configuration with constant current response will further reduce the overcurrent limit of 0.72A to ~1/4 of this value, or ~0.18A, after the UV fault limit is exceeded.

The output current can be read on the PMBus using the READ_IOUT command.

9.25 I2C Security

The IRPS5401 provides robust and flexible security options to meet a wide variety of customer applications. A combination of hardware pin and software password prevents accidental overwrites, discourages hackers, and secures custom configurations and operating data.

The following MTP registers can be used to set the Read and Write Security Zones.

Table 21

Register	Description	Default
Write_protect_section	Choose among 3 options 1) No protection or Open zone 2) Protect only configuration registers or No Configuration zone 3) Protect all registers or Secure zone	No protection or Open zone
Read_protect_section	Choose among 4 options 1) No protection or Open zone 2) Protect only configuration registers or No Configuration zone 3) Telemetry zone 4) Protect all registers or Secure zone	No protection or Open zone

The tables below describe the access levels in each of these security zones.

Table 22 Read Security Zones

Zone	Locked	Unlocked
Open	All	All
No Configuration	Debug & Telemetry	All
Telemetry	Telemetry	All
Secure	None	All

Table 23 Write security zones

Zone	Locked	Unlocked
Open	All	All
No Configuration	Debug & Telemetry	All
Secure	None	All

Further, the following protection modes or methods are available.

Table 24 Read or Write Unlock Options

Password Only
Pin Only
Pin & Password
Lock Forever

9.26 Password Protection

The system designer can set any 16-bit password (other than 00h) and this is stored in MTP in the register usr_password[15:0]. To unlock, a user must write the correct password into a “Password Try” register called usr_try_password[15:0] which is a volatile read/write register. To lock, write an incorrect password into the “Password Try” register. After a certain number of incorrect tries, the IC will lock up to prevent unauthorized access.

The following pseudo-code illustrates how to change a password:

```
#first unlock the IC
Write old password to R/W Try register
#now write new password into MTP
Write new password to the MTP Password register
# password change complete, status is locked
#Need to write new password to Try register to unlock
```

9.27 Pin Protection

The ADDR_PROT pin is a dual function pin. When the IC is enabled, the resistor value is latched and stored for use in the I2C address offset function. Thereafter, the pin acts entirely as a PROTECT pin. If enabled, the PROTECT pin must be driven high to unlock and low to lock. Note, if the resistor address offset function is being used, care must be taken to allow the IC to read the resistor value before driving the pin high or low to set the security state otherwise an erroneous address offset value may be latched in.

Recommended Circuit and Operating Parameters for Internal Switchers

Table 25

Input Voltage	Output Voltage	Switching Frequency	Min L_out for 1Ap-p inductor ripple [1]	Min C_out for ±3% AC regulation [2]	Kp [3]	Ki [3]
V	V	kHz	uH	uF	Decimal	Decimal
12	0.5 to 1	800	1.1	7 x 22uF	35	42
	1 to 1.5		1.6	6 x 22uF	36	43
	1.5 to 2		2	5 x 22uF	38	43
	2 to 2.5		2.5	4 x 22uF	40	44
	2.5 to 3.3		3	4 x 22uF	42	46
	3.3 to 5		3.6	3 x 22uF	42	50
9	0.5 to 1		1.1	7 x 22uF	36	43
	1 to 1.5		1.5	6 x 22uF	37	43
	1.5 to 2		2	5 x 22uF	38	43
	2 to 2.5		2.2	4 x 22uF	40	44
	2.5 to 3.3		2.7	4 x 22uF	42	46
	3.3 to 5		2.7	3 x 22uF	42	50
5	0.5 to 1		1	7 x 22uF	38	44
	1 to 1.5		1.3	6 x 22uF	38	45
	1.5 to 2		1.5	5 x 22uF	40	48
	2 to 2.5		1.5	4 x 22uF	41	50
	2.5 to 3.3		1.5	4 x 22uF	42	53

Note:

1. *1A p-p = 25% of IMAX on the 4A rail, 50% of IMAX on the 2A rails*
2. *With 1A load step, 5A/us slew rate*
3. *Fco ~ 50kHz MIN, PWM jitter ~ 20% of pulse width MAX*

10 Layout Guidelines

1. The IRPS5401 can supply relatively large amounts of output current from four separate outputs. The ability of the part to dissipate the heat generated in the part is a concern and as such as much copper as possible should be dedicated on the top layer to GND, VIN, and SW to maximize cooling
2. Place output inductors as close as possible to the SW nodes to minimize the length of the copper area of the SW node. This will help to minimize the parasitic capacitance and radiated emissions
3. The PGND thermal pad (pin 57) must be connected to a dedicated GND plane with VIAS as shown. Additional internal GND layers should also be connected to the VIAS as well
4. Make PCB patterns for VIN, SW, VOUT, and GND as broad as possible
5. Decouple VIN with a minimum 1uF X7R type MLCC as close as possible to the VIN pin
6. Decouple VCC to AGND pin with 1uF X7R MLCC
7. Connect VCC to VDRV with 2Ω resistor and decouple VDRV to PGND with 1uF X7R MLCC
8. Connect MTP and ADDR_PROT resistors to AGND
9. Decouple MTP and ADDR_PROT pins with 10nF X7R MLCC to AGND
10. There must be a single point contact from AGND to PGND
11. Route sensitive nets away from SW nodes
12. Place a GND plane on the layer 2, the layer directly underneath the top side components
13. Do not allow switching current, including pulsing input currents, to be routed under the device
14. Keep the switching current loops as small as possible
15. If a scaling resistors divider is used, the lower resistor must be terminated to PGND
16. If a 2:1 scaling resistor divider is used, the recommended value is 249Ω, 1%

10.1 Sample layout

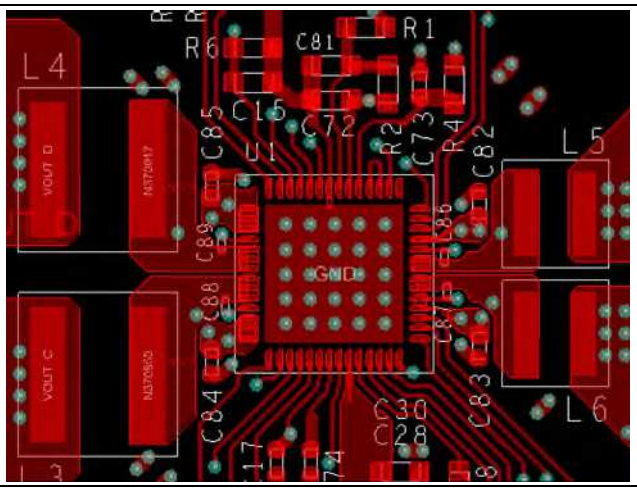


Figure 20 LAYER 1-TOP SIDE COMPONENTS PLUS POWER PLANE

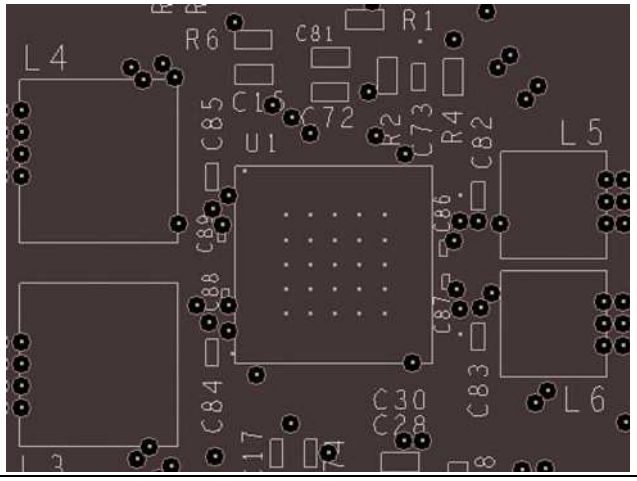


Figure 21 LAYER 2 – GROUND PLANE

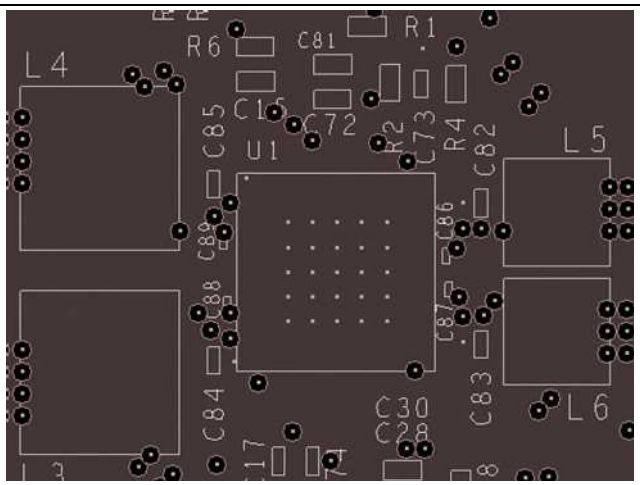


Figure 22 LAYER 3 – Signal Layer

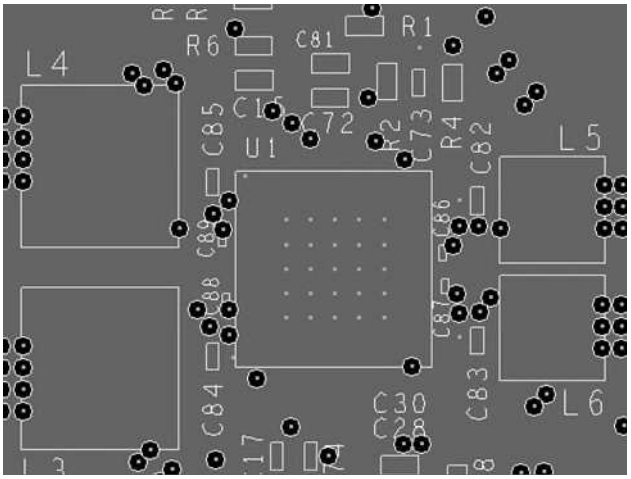


Figure 23 LAYER 4 – GrouND Plane

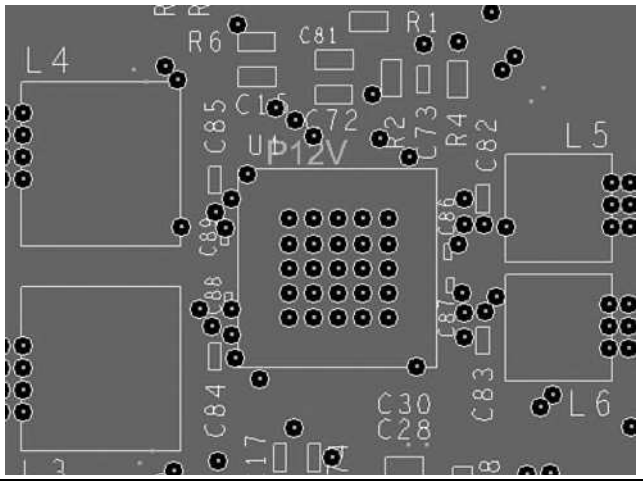


Figure 24 LAYER 5 – Power PLANE

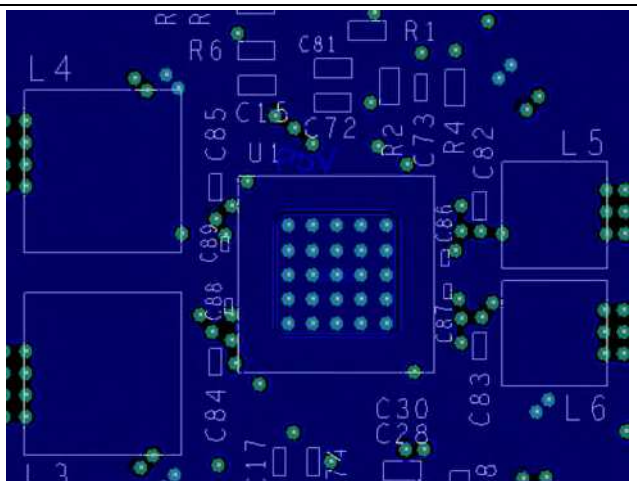


Figure 25 LAYER 6 – Power PLANE

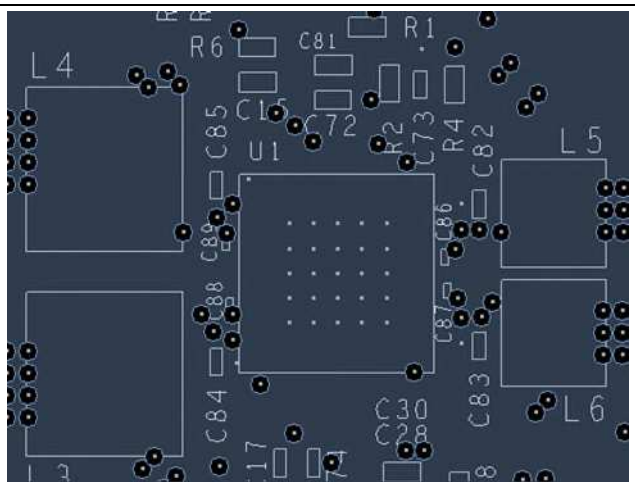


Figure 26 LAYER 7 – GROUND PLANE

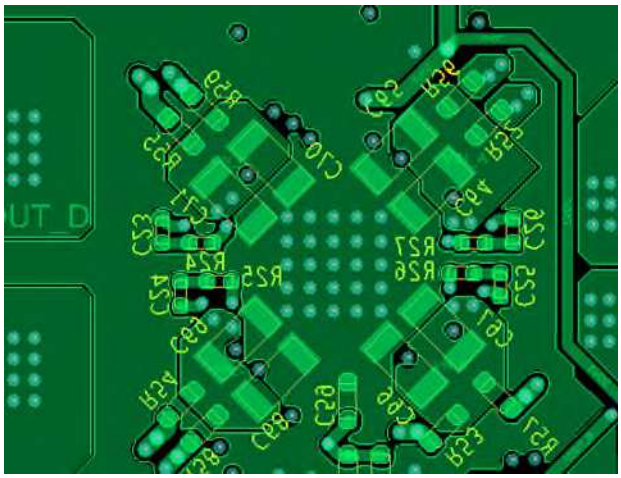


Figure 27 LAYER 8 – Botton side comp plus POWER and GROUND PLANES

11 Typical Performance

VIN=12V, VOUT=2.5V, IOUT=4A, TAMB=25°C

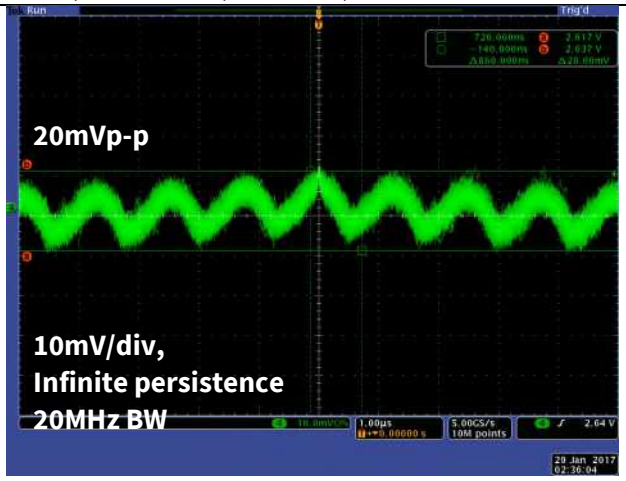


Figure 28 Output ripple

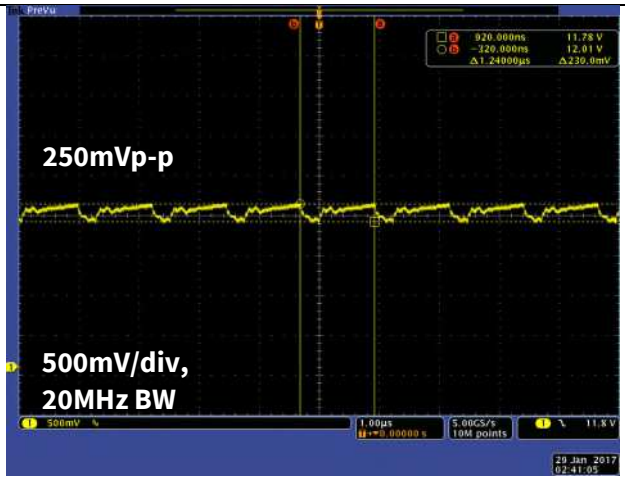


Figure 29 Input ripple

Figure 30 Transient response

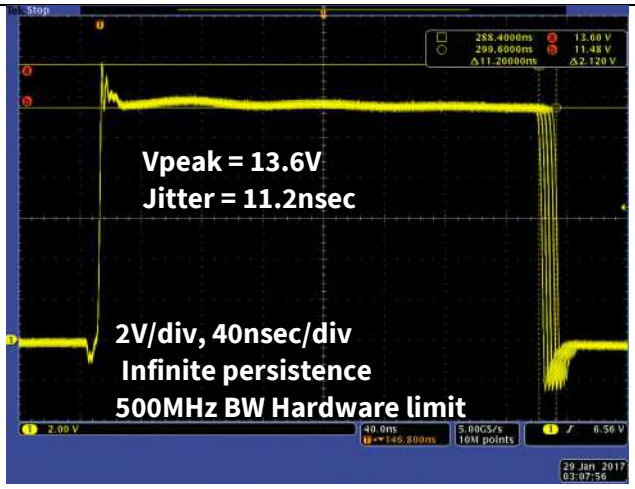


Figure 31 Switch node peak and jitter

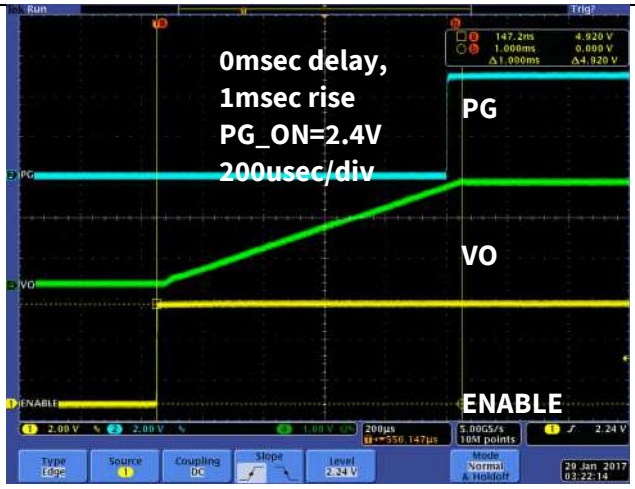


Figure 32 Enable start

Figure 33 Enable shut down

11.1 Typical thermal performance at max output power

VIN=12V, VOUT A, B, C, D=5V, IOUT A, B, C, D = 2A, 2A, 4A, and 4A, POUT = 60W, TAMB=25°C

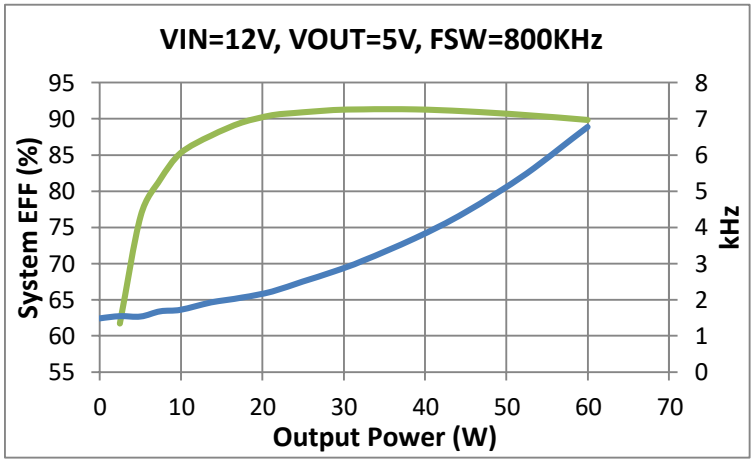


Figure 34 Total System Efficiency and power dissipation from 0W to 60W out

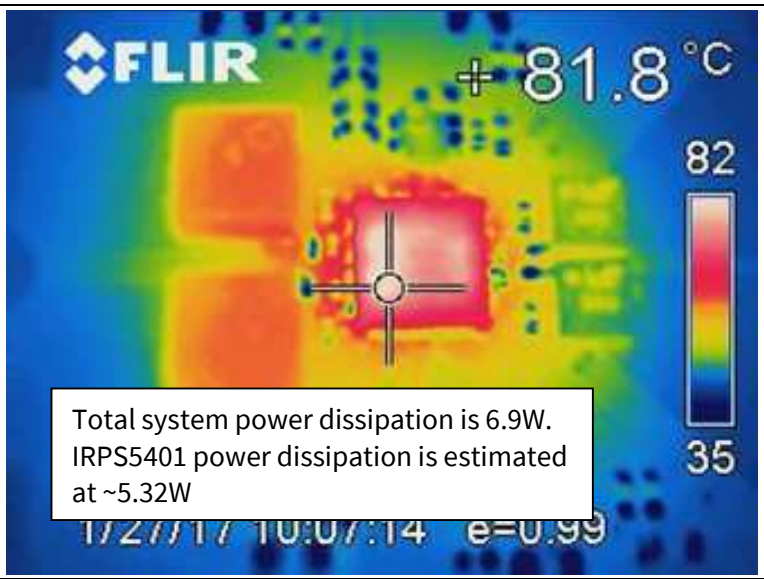


Figure 35 Temperature rise at room temp, natural convection cooling, 60W out

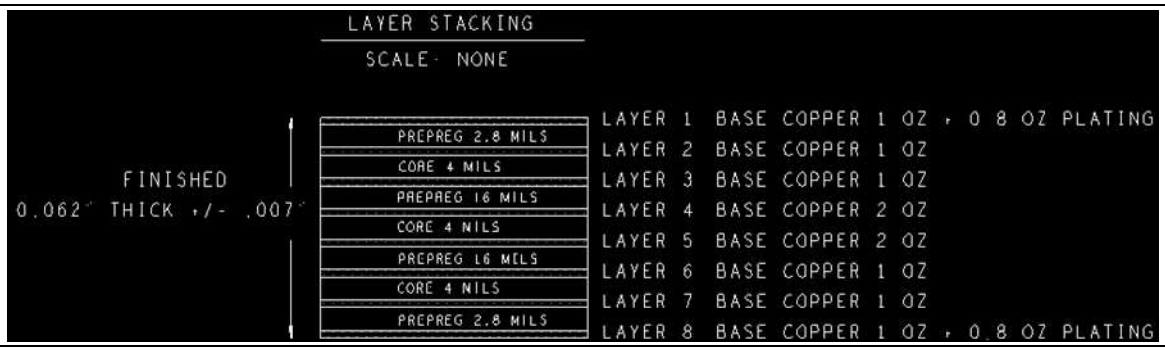


Figure 36 PCB construction details (8 layers, 11.6 oz total Cu Thickness)

12 PMBUS Commands

Table 26 PMBus commands (See UN0049 for more details)

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION	Default
PAGE	Read/Write Byte	00h	Allows access to each output via paging.	N/A
OPERATION	Read/Write Byte	01h	Enables or disables the output and controls margining.	00h
ON_OFF_CONFIG	Read/Write Byte	02h	Configures the combination of Enable pin and OPERATION command needed to turn the unit on and off.	17h
CLEAR FAULTS	Send Byte	03h	Clear contents of Fault registers	N/A
PAGE_PLUS_READ	Block Read	06h		N/A
WRITE_PROTECT	Read/Write Byte	10h	Provides protection from accidental changes	00h
RESTORE_DEFAULT_ALL	Send Byte	12h	Reloads the OTP	N/A
STORE_USER_ALL	Send Byte	15h	Stores the user OTP section	N/A
RESTORE_USER_ALL	Send Byte	16h	Reloads the user OTP section	N/A
CAPABILITY	Read Byte	19h	Returns 1010xxxx to indicate Packet Error Checking is supported and Maximum bus speed is 400kHz	N/A
SMBALERT_MASK	Block Write/ Block Read Process Call	1Bh	Set to prevent warning or fault conditions from asserting the SMBALERT# signal. Write command code for STATUS register to be masked in the low byte, the bit to be masked in the High byte.	N/A
VOUT_MODE	Read/Write Byte	20h	Sets the format for VOUT related commands. Linear mode, -8, -9, and -12 exponents supported. No LDO support	18h
VOUT_COMMAND	Read/Write Word	21h	Sets the voltage to which the device should set the output. Format according to VOUT_MODE. No LDO support	0000h
VOUT_TRIM	Read/Write Word	22h	Applies a fixed offset to the output voltage command value. Format according to VOUT_MODE. No LDO support	0000h
VOUT_MAX	Read/Write Word	24h	Sets an upper limit on the output voltage the unit can command. Format according to VOUT_MODE. No LDO support	0800h
VOUT_MARGIN_HIGH	Read/Write Word	25h	Sets the margin high voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE. No LDO support	0000h
VOUT_MARGIN_LOW	Read/Write Word	26h	Sets the margin low voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE. No LDO support	0000h
VOUT_TRANSITION_RATE	Read/Write Word	27h	Sets the rate at which the output changes voltage due to VOUT_COMMAND or	E808h

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION	Default
			OPERATION commands. mV/µs; Exp = -3. No LDO support	
VOUT_SCALE_LOOP	Read/Write Word	29h	Supports scale factor 1 and 0.5. No LDO support	E808h
FREQUENCY_SWITCH	Read/Write Word	33h	Sets the switching frequency in kHz. Exp = 0, 1. No LDO support	0320h
VIN_ON	Read/Write Word	35h	Sets the value of the input voltage at which the unit should begin power conversion. Exp = -2 for Switchers, -5 for LDO.	SW;F001h LDO;D808h
VIN_OFF	Read/Write Word	36h	Sets the value of the input voltage that the unit, once operation has started, should stop power conversion. Exp = -2 for Switchers, -5 for LDO	SW;F000h LDO;D800h
IOUT_CAL_OFFSET	Read/Write Word	39h	Used to null out any offsets in the output current sensing circuitry. Exp = -10 for LDO, -6 for Internal, -3 for External	SW:D000h LDO:B000h
VOUT_OV_FAULT_LIMIT	Read/Write Word	40h	Sets fault limit relative to VOUT… LDO=read only	8000h
VOUT_OV_FAULT_RESPONSE	Read/Write Byte	41h	Instructs the device on what action to take in response to an output over voltage fault. Only shutdown and ignore are supported.	00h
VOUT_OV_WARN_LIMIT	Read/Write Word	42h	Sets the value of the output voltage, measured at the sense or output pins, that causes an output overvoltage warning. Format as determined by VOUT_MODE… LDO=read only	8000h
VOUT_UV_WARN_LIMIT	Read/Write Word	43h	Sets the value of the output voltage, measured at the sense or output pins, that causes an output voltage low warning. Format as determined by VOUT_MODE… LDO=read only	0000h
VOUT_UV_FAULT_LIMIT	Read/Write Word	44h	Sets fault limit relative to VOUT… LDO=read only	0000h
VOUT_UV_FAULT_RESPONSE	Read/Write Byte	45h	Instructs the device on what action to take in response to an output under voltage fault. Only shutdown and ignore are supported.	00h
IOUT_OC_FAULT_LIMIT	Read/Write Word	46h	Sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. Set by writing this command in Linear format. Exp = -5 for internal and -2 for external … LDO=read only	SW:D900h LDO:C0B8h
IOUT_OC_FAULT_RESPONSE	Read/Write Byte	47h	Instructs the device on what action to take in response to an output overcurrent fault. Only C0h (latch off), F8h (hiccup forever), and F0h (hiccup 6 times then latch off) are supported…LDO supports C0h (latch off) and 00h (current limiting)	SW:F8h LDO:C0h

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION	Default
IOUT_OC_WARN_LIMIT	Read/Write Word	4Ah	Sets the value of the output current that causes an output over current warning. Set by writing this command in Linear format. Exp = -10 for LDO, -5 for internal and -2 for external.	SW:D900h LDO:C0B8h
OT_FAULT_LIMIT	Read/Write Word	4Fh	Sets the temperature in °C that would should indicate an over temperature fault. Linear format, Exp = 0.	0080h
OT_FAULT_RESPONSE	Read/Write Byte	50h	Instructs the device on what action to take in response to an over temperature fault. Only 80h (shutdown), 00h (ignore), and C0h (inhibit then restart) are supported.	00h
OT_WARN_LIMIT	Read/Write Word	51h	Sets the temperature in °C that would indicate an over temperature warning alarm. Linear format, Exp = 0.	0080h
VIN_OV_FAULT_LIMIT	Read/Write Word	55h	Sets the value of the input voltage that causes an input overvoltage fault. Exp = -4 for switchers, -7 for LDO	SW:E200h LDO:CAC0h
VIN_OV_FAULT_RESPONSE	Read/Write Byte	56h	Instructs the device on what action to take in response to an input overvoltage fault. Only 80h (shutdown) and 00h (ignore) are supported.	00h
VIN_UV_WARN_LIMIT	Read/Write Word	58h	Sets the value of the input voltage that causes an input voltage low warning. Exp = -4 for switchers, -7 for LDO	SW:E000h LDO:C800h
POWER_GOOD_ON	Read/Write Word	5Eh	Sets the output voltage at which the POWER_GOOD signal will be asserted. Format according to VOUT_MODE.	0000h
POWER_GOOD_OFF	Read/Write Word	5Fh	Sets the output voltage at which the POWER_GOOD signal will be de-asserted. Format according to VOUT_MODE.	0000h
TON_DELAY	Read/Write Word	60h	Sets the time, in milliseconds, from when a start condition is received until the output voltage starts to rise. Exp = -1.	F800h
TON_RISE	Read/Write Word	61h	Sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. Exp = -2. No LDO support	F004h
TON_MAX_FAULT_LIMIT	Read/Write Word	62h	Sets an upper limit, in milliseconds, on how long the unit can attempt to power up the output without reaching the output under voltage fault limit. Exp = -2.	F004h
TON_MAX_FAULT_RESPONSE	Read/Write Byte	63h	Instructs the device on what action to take in response to a TON_MAX fault. Only 80h (shutdown) and 00h (ignore) are supported.	00h
TOFF_DELAY	Read/Write Word	64h	Sets the time, in milliseconds, from when a stop condition is received until the unit starts ramping down to 0V. Exp = -1. No	F800h

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION	Default
			LDO support	
TOFF_FALL	Read/Write Word	65h	Sets the time, in milliseconds, for the output to ramp to 0V. Exp = -2. No LDO support	F004h
STATUS_BYTE	Read/Write Byte	78h	Returns 1 byte where the bit meanings are: Bit <7> Reserved Bit <6> Output off (due to fault or enable) Bit <5> Output over-voltage fault Bit <4> Output over-current fault Bit <3> Input Under-voltage fault Bit <2> Temperature fault Bit <1> Communication/Memory/Logic fault Bit <0>: None of the above	N/A
STATUS_WORD	Read/Write Word	79h	Returns 2 bytes where the Low byte is the same as the STATUS_BYTE data. The High byte has bit meanings are: Bit <7> Output high or low fault Bit <6> Output over-current fault Bit <5> Input under-voltage fault Bit <4> MFR_SPECIFIC Bit <3> POWER_GOOD# Bit <2:0> Reserved	N/A
STATUS_VOUT	Read/Write Byte	7Ah	Bit <7> Output Over voltage Fault Bit <6> Output Over voltage Warning Bit <5> Output Under voltage Warning Bit <4> Output Under voltage Fault Bit <3> VOUT_MAX Warning Bit <2> TON_MAX_FAULT Bit <1> Reserved Bit <0> Reserved	N/A
STATUS_IOUT	Read/Write Byte	7Bh	Bit <7> Output Over current Fault Bit <6> Reserved Bit <5> Output Over current Warning Bit <4:0> Reserved	N/A
STATUS_INPUT	Read/Write Byte	7Ch	Bit <7> Input Overvoltage Fault Bit <6> Reserved Bit <5> Input Under voltage Warning Bit <4> Reserved Bit <3> Unit Off For Insufficient Input Voltage Bit <2:0> Reserved	N/A
STATUS_TEMPERATURE	Read/Write Byte	7Dh	Bit <7> Over Temperature Fault Bit <6> Over Temperature Warning Bit <5:0> Reserved	N/A
STATUS_CML	Read/Write Byte	7Eh	Returns 1 byte where the bit meanings are: Bit <7> Invalid or unsupported command Bit <6> Invalid or unsupported data or send too may bytes	N/A

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION	Default
			Bit <5> PEC fault Bit <4:2> Reserved Bit <1> Other communication fault not listed here Bit <0> Reserved	
READ_VIN	Read Word	88h	Returns the input voltage in Volts. Exp = -5 for Switchers and -7 for LDO	N/A
READ_IIN	Read Word	89h	Returns the input current in Amperes. Exp = -7 for Internal, and -4 for External	N/A
READ_VOUT	Read Word	8Bh	Returns the output voltage in the format set by VOUT_MODE	N/A
READ_IOUT	Read Word	8Ch	Returns the output current in Amperes. Exp = -10 for LDO, -6 for Internal, and -3 for External	N/A
READ_TEMPERATURE_1	Read Word	8Dh	Returns the addressed loop temperature in °C. Switcher A and B have a common sensor, Switcher C, D and LDO have a common sensor. Exp = -2	N/A
READ_POUT	Read Word	96h	Returns the output power in Watts. Exp = -6 for LDO, -5 for Internal, and -2 for External	N/A
READ_PIN	Read Word	97h	Returns the input power in Watts. Exp = -6 for LDO, -5 for Internal, and -2 for External	N/A
PMBUS_REVISION	Read Byte	98h	Reports PMBus Part I rev 1.1 & PMBus Part II rev 1.2	22h
MFR_ID	Block Read/Write Byte count = 3	99h	The MFR_ID is set to IR (ASCII 52 49) unless programmed different in the USER registers of the controller.	004952h
MFR_MODEL	Block Read/Write byte count = 4	9Ah		00000052h
MFR_REVISION	Block Read/Write byte count = 4	9Bh		00000002h
IC_DEVICE_ID	Block Read byte count = 1	ADh	Returns a 1 byte code with the following values: 52h = IRPS5401	N/A
IC_DEVICE_REV	Block Read byte count = 1	AEh	The IC revision that is stored inside the IC	N/A
MFR_REG_ACCESS	Custom MFR protocol	D0h	Read/Write I2C registers	N/A
MFR_I2C_ADDRESS	Read/Write Byte	D6h	Reads I2C address	N/A
MFR_TPGDLY	Read/Write Word	B8h	Sets delay from PG threshold crossed to PG assertion.	0000h

COMMAND	PMBUS PROTOCOL	COMMAND CODE	DESCRIPTION	Default
			Exp = 0	
MFR_FCCM	Read/Write Byte	B9h	Write a 1 to force continuous current mode (CCM) and disable constant on time (COT) mode at light load. No LDO support	01h
MFR_VOUT_PEAK	Read Word	DBh	Reads maximum VOUT recorded since the last read. Reading the register automatically clears the value. Resolution set by VOUT_MODE	N/A
MFR_IOUT_PEAK	Read Word	DCh	Reads maximum IOUT recorded since the last read. Reading the register automatically clears the value. Exp = -10 for LDO, -6 for Internal, and -3 for External	N/A
MFR_TEMPERATURE_PEAK	Read Word	DDh	Reads maximum temp recorded since the last read. Reading the register automatically clears the value. Exp = 0, -2 for LDO	N/A
MFR_LDO_MARGINING	Read/Write Byte	DEh	Allows margining of the LDO output ± 15%	00h

Note:

1. *If a low to high to low transaction occurs on the DIO line while the CLK is low after the a START or RESTART and before the first CLK pulse occurs, the transaction will be NAK'd*
2. *The MFR_LDO_MARGIN command is readable and writeable but cannot be saved in the configuration file*
3. *The MFR_TPGDLY command is readable and writeable but cannot be saved in the configuration file*
4. *To avoid inadvertently setting the MFR_LDO_MARGIN and MFR_TPGDLY commands to non-0 values, the LDO VOUT_MODE command must be set to -8, the LDO POWER_GOOD_ON command must be set to 0.109V (or 0V), and the LDO POWER_GOOD_OFF command must be set to 0.063V (or 0V)*
5. *To avoid inadvertently masking LDO STATUS_INPUT register bits 5, 6, and 7 and LDO STATUS_TEMPURATURE bits 7 and 6, the LDO VIN_UV_WARN_LIMIT command must be set to a value no larger than 0.49V*

Table 27 PMBus Commands Saved to MTP

OPERATION	ON_OFF_CONFIG	WRITE_PROTECT	VOUT_MODE
VOUT_COMMAND	VOUT_MAX	VOUT_TRANSITION_RATE	VOUT_SCALE_LOOP
VOUT_MIN	FREQUENCY_SWITCH	POWER_MODE	VOUT_OV_FAULT_LIMIT
VIN_OFF	IOUT_CAL_GAIN	IOUT_CAL_OFFSET	VOUT_OV_FAULT_RESPONSE
VIN_ON	VOUT_OV_WARN_LIMIT	VOUT_UV_WARN_LIMIT	VOUT_UV_FAULT_LIMIT
VIN_UV_WARN_LIMIT	IOUT_OC_WARN_LIMIT	OT_FAULT_LIMIT	OT_FAULT_RESPONSE
OT_WARN_LIMIT	VIN_OV_FAULT_LIMIT	TON_DELAY	VIN_OV_FAULT_RESPONSE
IIN_OC_WARN_LIMIT	POWER_GOOD_ON	POWER_GOOD_OFF	TON_MAX_FAULT_RESPONSE
TON_RISE	TON_MAX_FAULT_LIMIT	TOFF_DELAY	IOUT_OC_FAULT_RESPONSE
TOFF_FALL	POUT_OP_WARN_LIMIT	PIN_OP_WARN_LIMIT	RESET_TRANSITION_RATE
VOUT_RESET	STATUS_INPUT (Mask)	STATUS_VOUT (Mask)	STATUS_TEMPERATURE (Mask)
	STATUS_CML (Mask)	STATUS_IOUT (Mask)	STATUS_MFR_SPECIFIC (Mask)

13 Marking Information

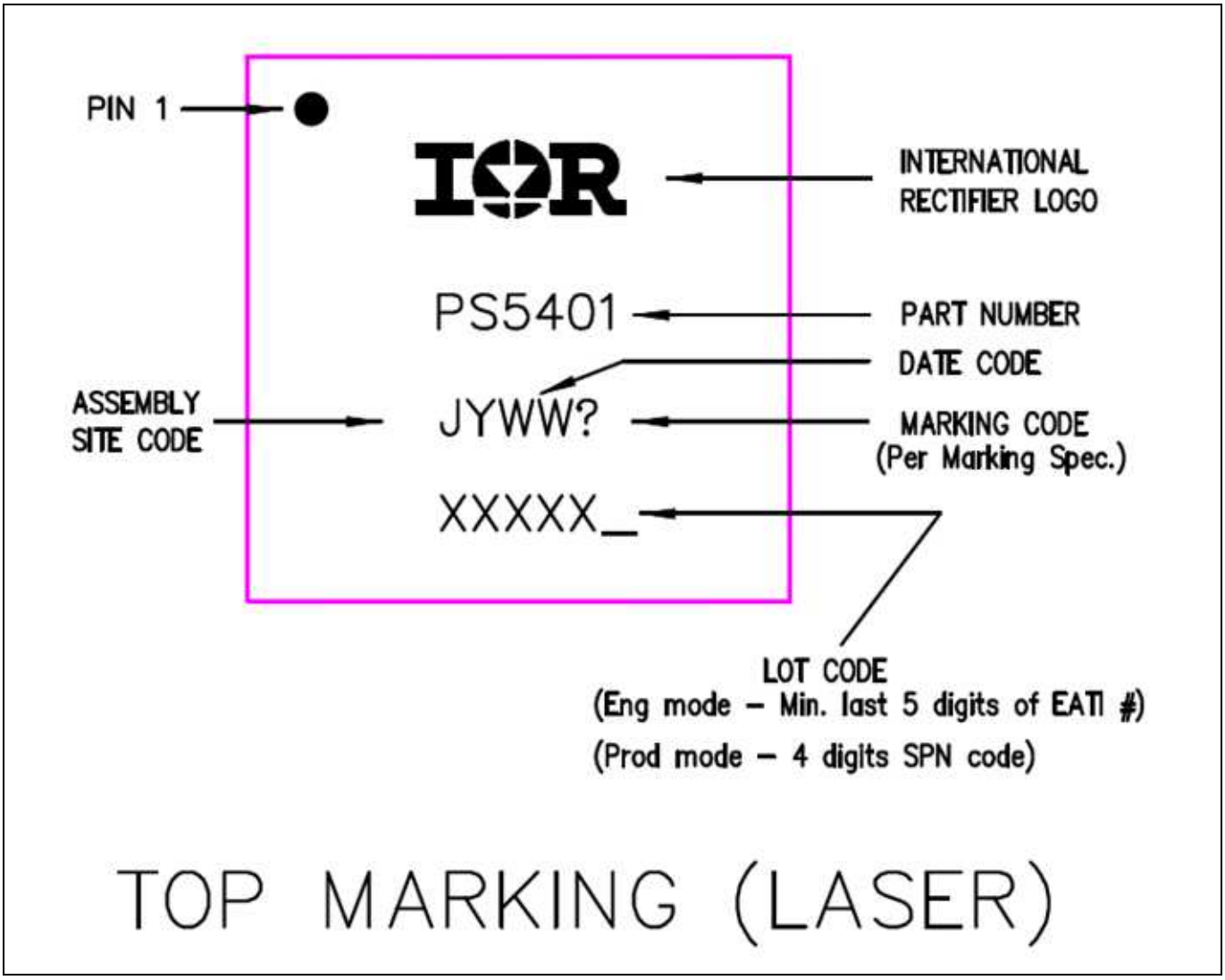
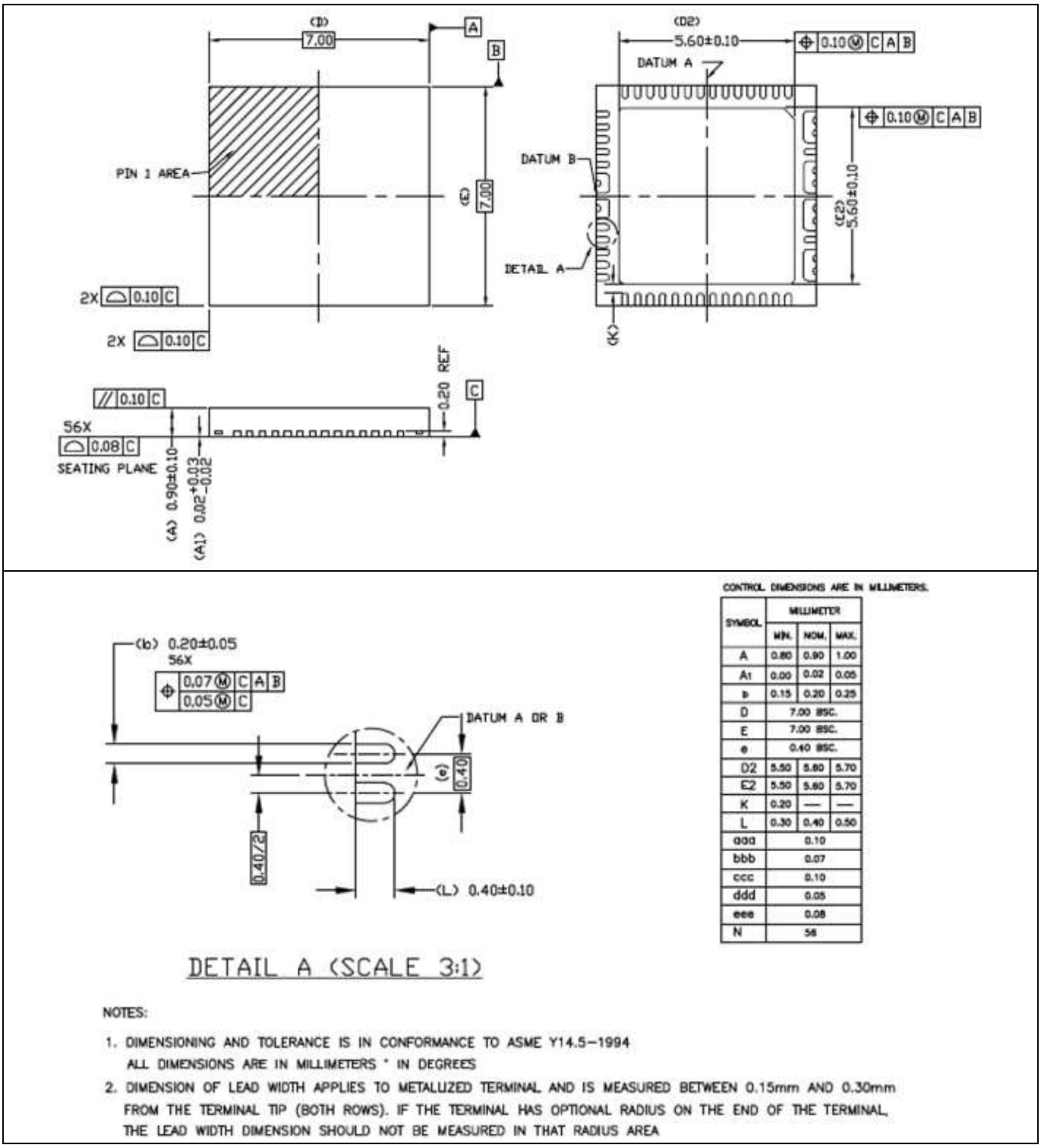


Figure 37 Package Marking

14 Package Information



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D		7.00 BSC.	
E		7.00 BSC.	
e		0.40 BSC.	
D2	5.50	5.60	5.70
E2	5.50	5.60	5.70
K	0.20	—	—
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
N		56	

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Figure 38 Package information

14.1 PCB Pad Size

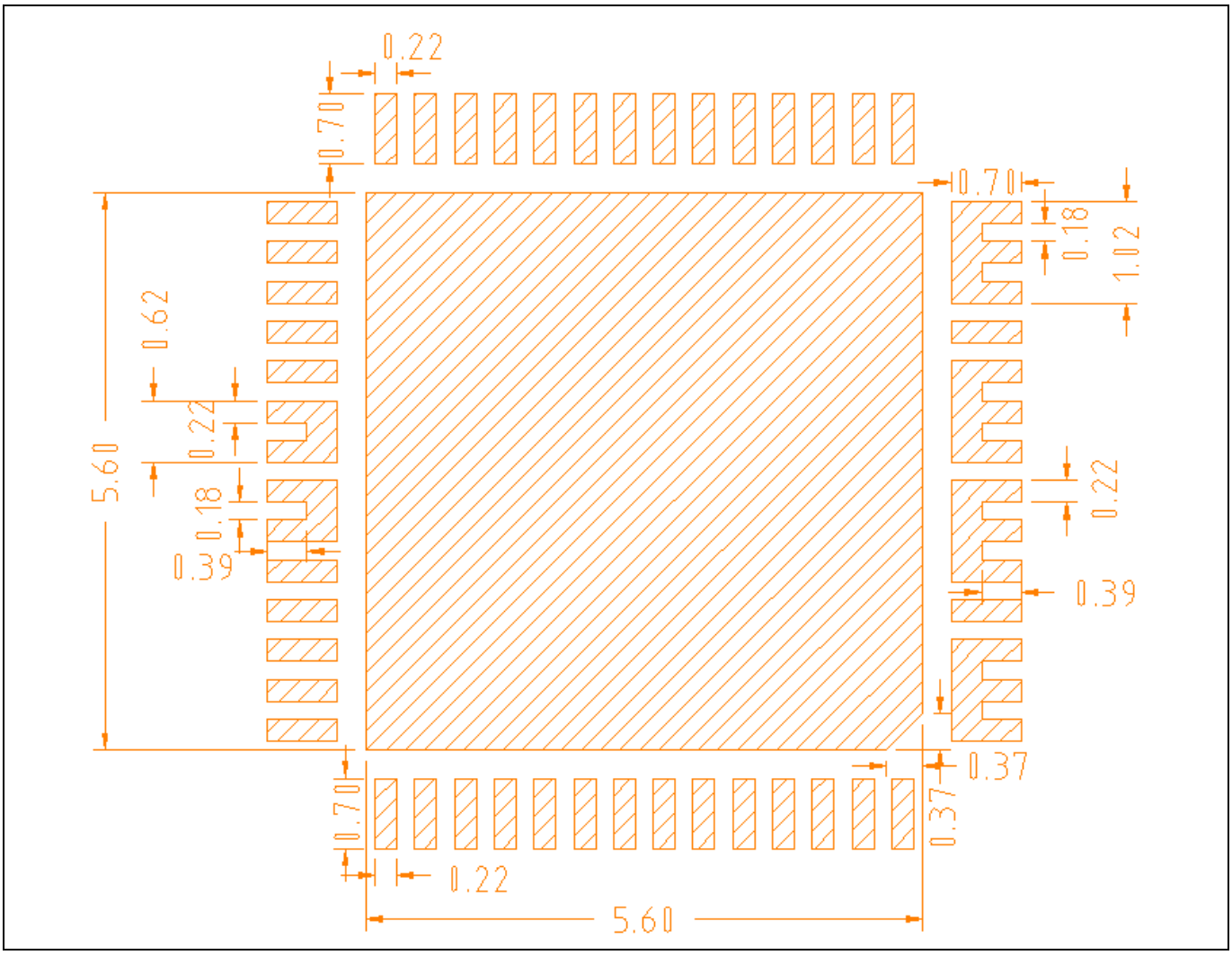


Figure 39 PCB PAD Size

14.2 PCB Pad Spacing

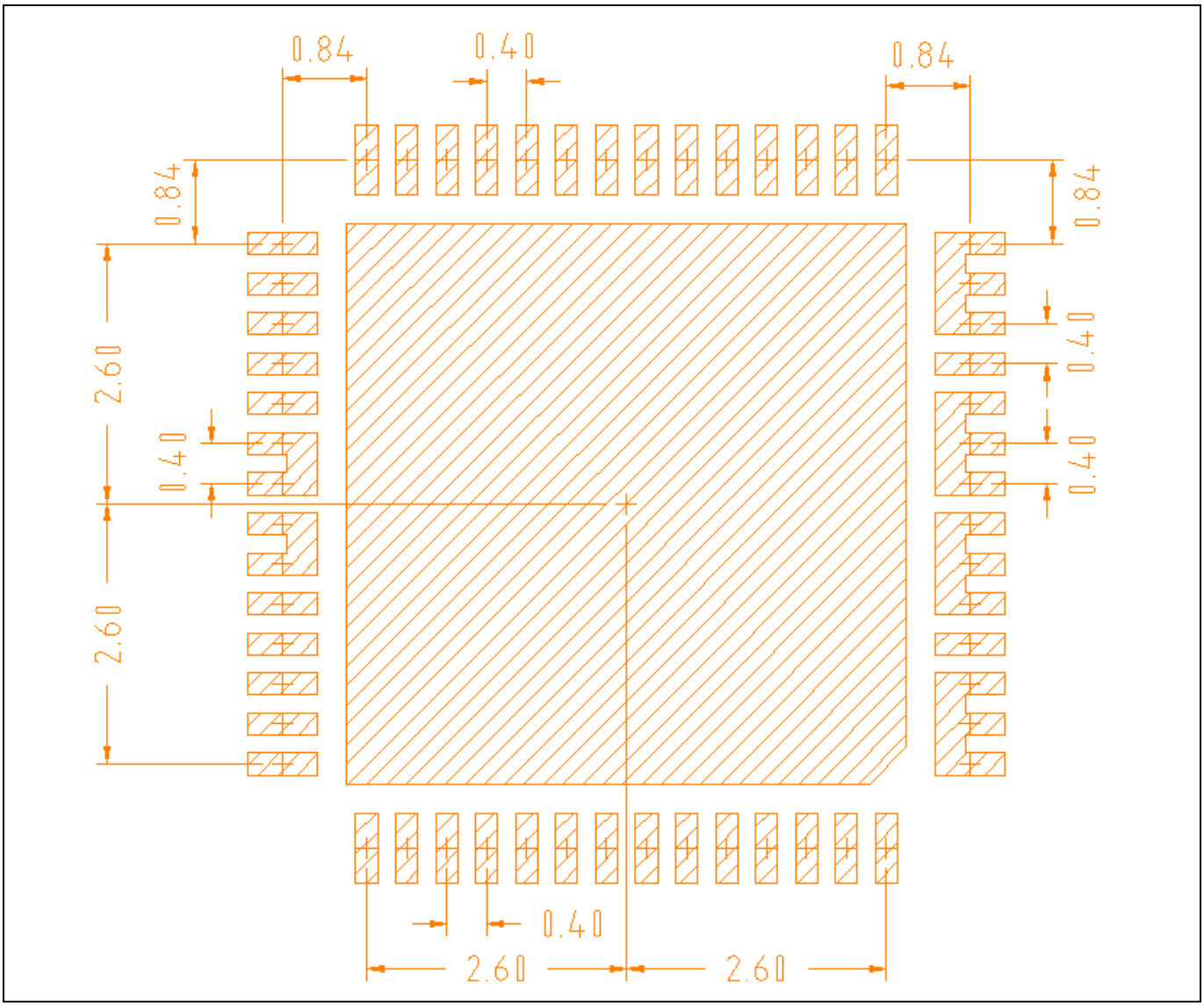


Figure 40 PCB PAD Spacing

14.3 Solder Paste Stencil Pad Size

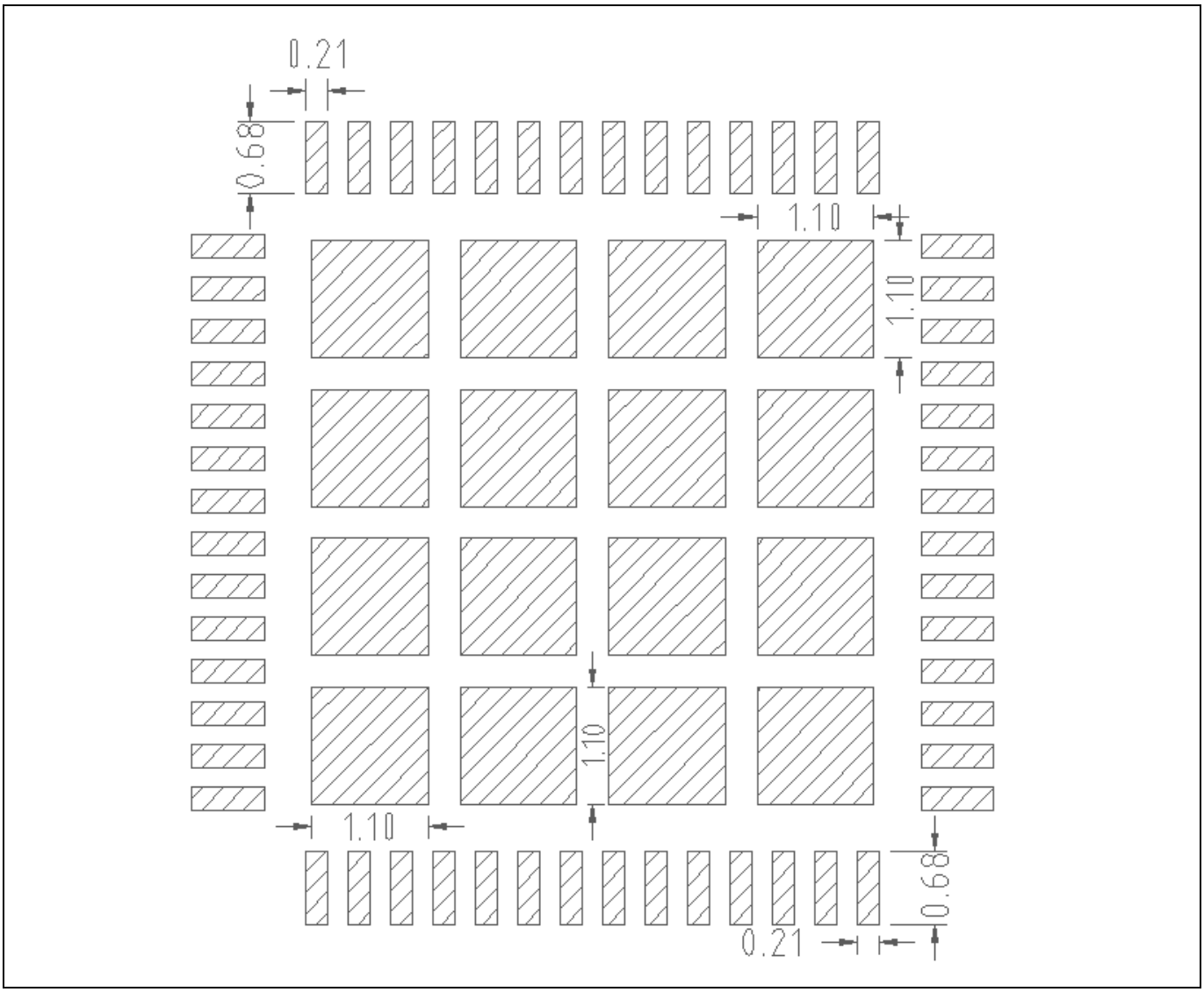


Figure 41 Solder paste stencil pad size

14.4 Solder Paste Stencil Pad Spacing

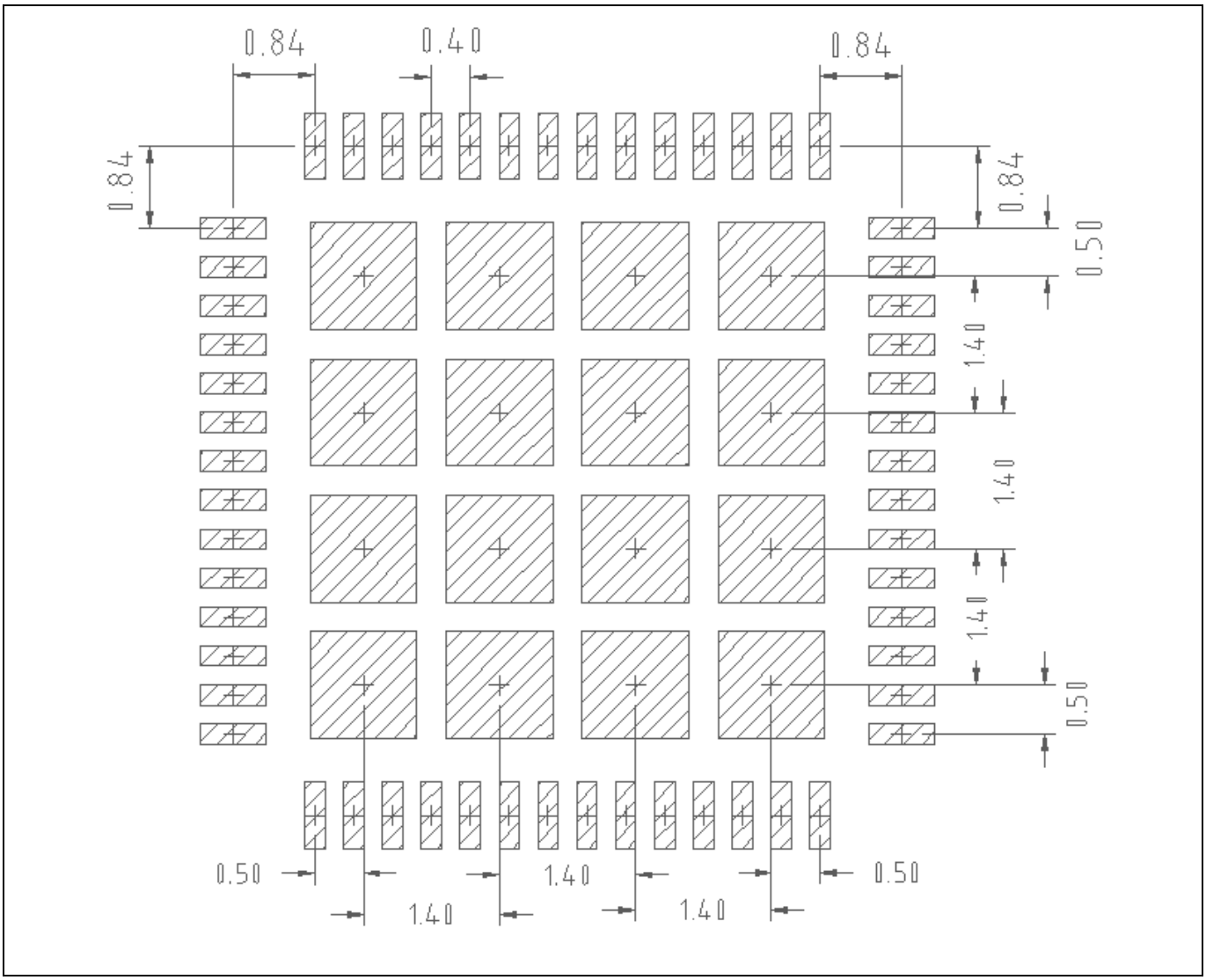


Figure 42 Solder paste stencil pad spacing

15 Environmental Qualifications

Qualification Level		Industrial	
Moisture Sensitivity Level		7mm x 7mm PQFN	JEDEC Level 2 @ 260°C
ESD	Human Body Model (JS-001-2014)	Class 1B	
		500V to <1000V	
	Charged Device Model (JESD22-C101F)	Class C3	
		>1000V	
RoHS2 Compliant		Yes (6/6)	

Revision History

IRPS5401

Revision: 2022-07-11, Rev. 2.8

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-08-11	Release of final version
2.1	2018-10-27	Correct PWM_A output HI Value
2.2	2018-12-21	Update pin descriptions
2.3	2019-05-09	Change LDO reference tolerance to 3%
2.4	2019-10-08	Add VDDIO note to section 9.3 Table 26; update reset value for command 5Eh, 5Fh, 62h Table 26; add reset values to command 99h, 9Ah and 9Bh to agree with PMBUS command document
2.5	2020-10-12	Add Table 27 to show PMBUS commands that are saved to OTP Add VDDIO info ABS MAX table, Table 5 and recommended table, Table 7 Update VDDIO voltage in FIG1 (application circuit) from 1V-5V to 1.8V-5V
2.6	2021-01-14	Add cold start delay requirement note to section 9.3 and update FIGURE 8. This change is only describing the operation of the controller. It is not a change in form fit or function. Fix Table 8 formatting, some categories were not BOLDed
2.7	2021-07-20	Update note in section 9.3 to specify internal switchers only
2.8	2022-07-11	update OPN in Table 1 from IRPS5401MXI04TRPAUMA to IRPS5401MXI04TRPXUMA11

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