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Evaluating the ADP5055 Triple Buck Regulator Integrated Power Solution

FEATURES

- Wide input voltage range: 2.75 V to 18 V
- Bias input voltage range: 4.5 V to 18 V
- Full-featured evaluation board for the ADP5055
  - Channel 1 and Channel 2: 7 A synchronous buck regulator, or 14 A output in parallel operation
  - Channel 3: 3 A synchronous buck regulator
- Selective PSM or FPWM operation
- 250 kHz to 2500 kHz adjustable switching frequency range
- Frequency synchronization input or output
- USB dongle and GUI software support

HARDWARE REQUIREMENTS

- USB to I²C dongle (USB-SDP-CABLEZ), which is not included in the evaluation kit and must be ordered separately

SOFTWARE REQUIREMENTS

- ADP5055 demonstration board GUI software
- USB to I²C dongle (USB-SDP-CABLEZ) driver

GENERAL DESCRIPTION

This user guide describes the evaluation of the ADP5055 and includes a detailed schematic and printed circuit board (PCB) layouts.

The ADP5055-EVALZ features the ADP5055, which combines three high performance buck regulators in a 43-terminal land grid array (LGA) to meet the demanding performance and board space requirements. The ADP5055-EVALZ connects to input voltages up to 18 V directly, without any preregulators.

The ADP5055 includes a PMBus®-compatible serial interface and the ADP5055-EVALZ can be used with an external USB dongle and graphical user interface (GUI) software to evaluate the power management functionalities and to read back system status.

Full details on the device are provided in the ADP5055 data sheet, available from Analog Devices, Inc. Consult this data sheet in conjunction with this user guide when evaluating the ADP5055.

ADP5055-EVALZ PHOTOGRAPH

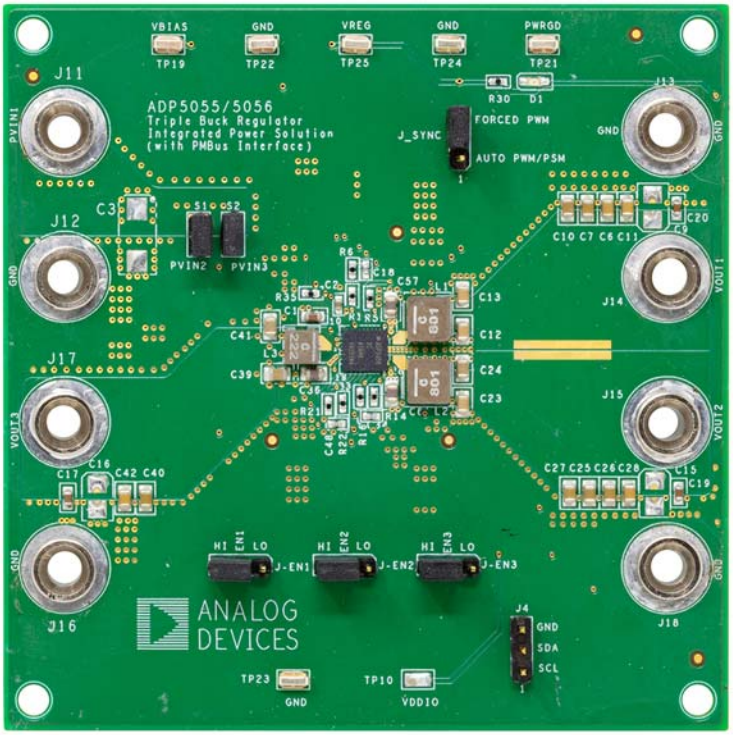

Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

1/2022—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The ADP5055-EVALZ is fully assembled and tested. Before applying power to the ADP5055-EVALZ, follow the procedures in this section.

ENABLE JUMPERS

Each channel has an enable pin (ENx) that must be pulled high to enable that channel (see Table 1). Pull the ENx pin low or leave it floating to disable the channel.

The enable control for each regulator has a 0.615 V precision enable threshold, which allows the ADP5055 to be sequenced between channels or other input and output supplies.

Table 1. Enable Pin Channels

Channel Number	Mnemonic	Enable Jumpers
Channel 1	EN1	J-EN1
Channel 2	EN2	J-EN2
Channel 3	EN3	J-EN3

POWER INPUT JUMPERS

Each channel has its own power input jumper, which supports separate input voltages or cascaded options for all channels.

The bias input voltage range for the three buck regulators is 4.5 V to 18 V. If separate power supplies are used for PVIN1 and VBIAS with R35 removed (on the ADP5055-EVALZ, PVIN1 and VBIAS are connected together through the R35, 0 Ω resistor by default), the wide input voltage range for the three buck regulators is 2.75 V to 18 V. The S1 and S2 shunts allow easy setup by using the same input voltages for the three buck regulators. See Table 2 for the power input details.

Table 2. Power Input Pin Channels

Channel Number	Mnemonic	Input Jumper	Input Range (V)
Channel 1	PVIN1	J11	4.5 to 18
Channel 2	PVIN2	S1	4.5 to 18
Channel 3	PVIN3	S2	4.5 to 18

J_SYNC JUMPER (SYNC/MODE)

The J_SYNC jumper, as shown in Figure 1, is used to connect the SYNC/MODE pin of the device to either low (GND) or high (VREG).

1. Shunt the center contact of J_SYNC (SYNC_MODE) to the top pin header, which pulls the SYNC/MODE pin high to VREG (4.8 V) to allow the three buck regulators into forced pulse-width modulation (FPWM) operation.
2. Shunt the center contact of J_SYNC to the bottom pin header, which pulls the SYNC/MODE pin low to force the three buck regulators to operate in automatic pulse-width modulation/power saving mode (PWM/PSM) operation.

INPUT POWER SOURCE

Use the following steps to connect the ADP5055-EVALZ to the input power source:

1. Ensure that the ADP5055-EVALZ is disabled by connecting the enable jumpers (J-EN1 to J-EN3) to the low position before connecting the power source to the ADP5055-EVALZ.
2. If the input power source includes a current meter, use the meter to monitor the input current.
3. Connect the positive terminal of the power source to the PVIN1 terminal (J11) on the ADP5055-EVALZ and connect the negative terminal of the power source to the GND terminal (J12) of the ADP5055-EVALZ.
4. If the power source does not include a current meter, connect a current meter in series with the input source voltage.
5. Connect the positive terminal of the power source to the positive lead of the current meter, the negative terminal of the power source to the GND terminal (J12) on the ADP5055-EVALZ, and the negative lead of the current meter to the PVIN1 terminal (J11) on the ADP5055-EVALZ.

OUTPUT LOAD

Use the following steps to connect the ADP5055-EVALZ to the output load:

1. Ensure that the ADP5055-EVALZ is off before connecting the load.
2. Connect an electronic load or resistor to set the load current. If the load includes an ammeter, or if the current is not measured, connect the load directly to the ADP5055-EVALZ with the positive load connected to one of the channels. For example, connect the positive load terminal to the Channel 1 buck regulator output, J14 (VOUT1) and connect the negative load terminal to J13 (GND).
3. If an ammeter is used, connect it in series with the load.
4. Connect the positive ammeter terminal to the Channel 1 buck regulator output, J14 (VOUT1), connect the negative ammeter terminal to the positive load terminal, and connect the negative load terminal to J13 (GND).

INPUT AND OUTPUT VOLTMETERS

Use the following steps to measure the input and output voltages with voltmeters:

1. Ensure that the voltmeters are connected to the appropriate ADP5055-EVALZ terminals and not to the load or power sources themselves. If the voltmeters are not connected directly to the ADP5055-EVALZ, the measured voltages are inaccurate due to the voltage drop across the leads and/or connections between the ADP5055-EVALZ, the power source, and/or the load.
2. Connect the voltmeter positive terminal measuring the input voltage to J11 (PVIN1) and connect the voltmeter negative terminal measuring the input voltage to J12 (GND).
3. Connect the voltmeter positive terminal measuring the output voltage of the Channel 1 buck regulator to J14 (VOUT1) and connect the voltmeter negative terminal measuring the output voltage to J13 (GND).

QUICK STARTUP

Verify the following before powering up the ADP5055-EVALZ:

- The power source voltage for the three buck regulators (PVIN1, PVIN2, and PVIN3) is within the 4.5 V to 18 V range. In addition, shunt the S1 and S2 jumpers to use the same input voltage for all three buck regulators
- Use the J-EN1, J-EN2, and J-EN3 jumpers to enable or disable the desired channel.

When the power source and load are connected to the ADP5055-EVALZ, the evaluation board can be powered for operation. If the load is not enabled, enable the load. Check that the load is drawing the proper current and that the output voltage maintains voltage regulation.

After power-up, the following output voltages (VOUTx) are measured:

- VOUT1 = 1.0 V, supply up to 7 A continuous load current
- VOUT2 = 1.3 V, supply up to 7 A continuous load current
- VOUT3 = 1.8 V, supply up to 3 A continuous load current

EVALUATION BOARD SOFTWARE

The ADP5055-EVALZ can be powered up and placed in standalone operation without the GUI software. The GUI software and the USB to I²C dongle (USB-SDP-CABLEZ), which is not included in the evaluation kit and must be ordered separately, are optional to access the advanced functionalities of the ADP5055 through the PMBus serial interface.

Ensure that the ADP5055-EVALZ is not connected to the USB port of the PC before starting the software installation.

INSTALLING THE GUI SOFTWARE

To install the **ADP5055_GUI** software on the PC, take the following steps:

1. Download the GUI software installation file, **ADP5055_GUI_Install**, from the ADP5055 product page. Unzip the **ADP5055_GUI_Install** file.
2. Launch the **Setup.exe** file located within the **ADP5055_GUI_Install\Volume** folder. The dialog box shown in Figure 2 then appears.

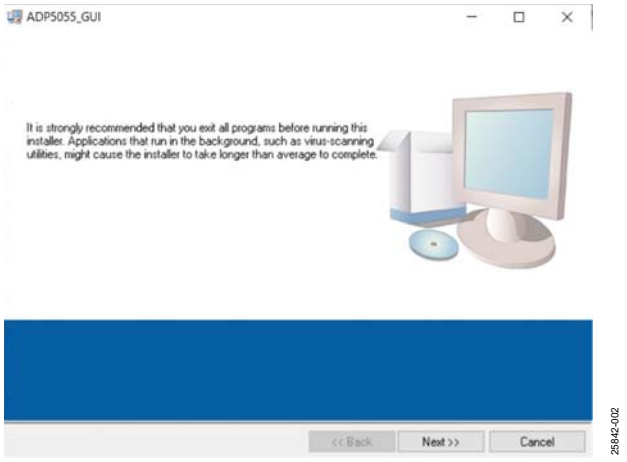

*Figure 2. **ADP5055_GUI** Software Installation Dialog*

3. Click **Next > >** to install the files to the default destination folders or click **Browse** to choose a different destination folder (see Figure 3).

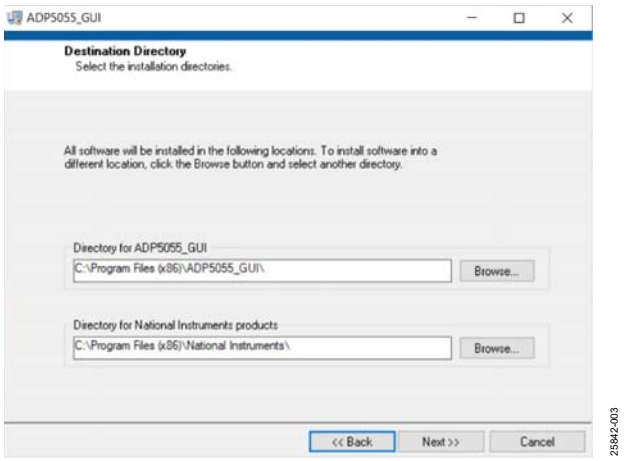

Figure 3. Choose Installation Destination Locations

4. Click **Next > >** to install the **ADP5055_GUI** software program (see Figure 4).

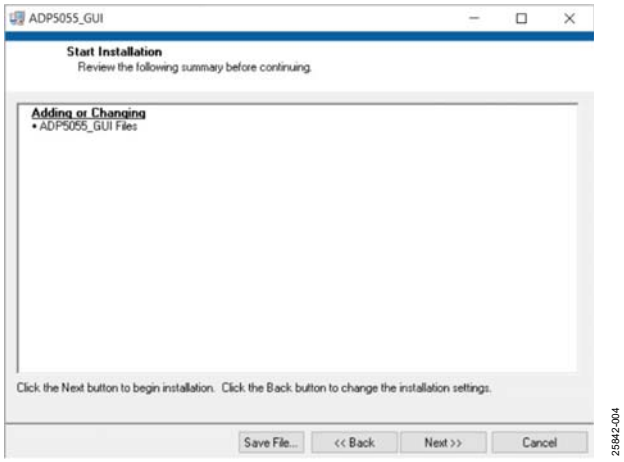

*Figure 4. **Start Installation** Window*

5. Click **Finish** to complete the installation (see Figure 5).

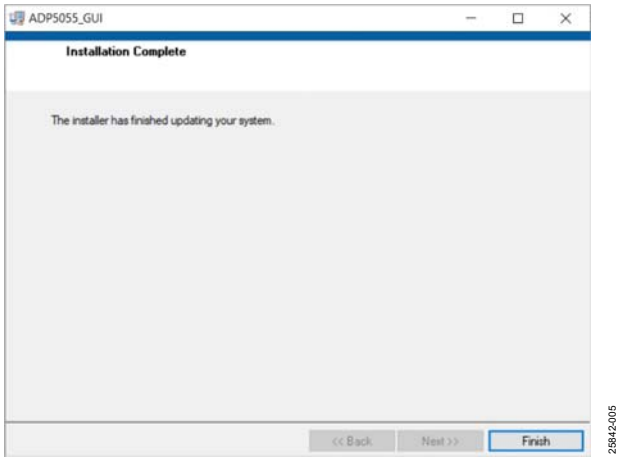

*Figure 5. **ADP5055_GUI Installation Complete** Window*

After GUI software installation, the PC may require a restart to compete the installation.

INSTALLING THE ADI SDP DRIVERS

For the PC to communicate with the USB to I²C dongle (USB-SDP-CABLEZ), install the driver installation package on the PC. To install the ADI SDP drivers, take the following steps:

1. Download the **SDPDriversNET40.exe** driver installation file from the ADP5055 web page and launch the installation file.
2. Click **Next >** to start the installation (see Figure 6).

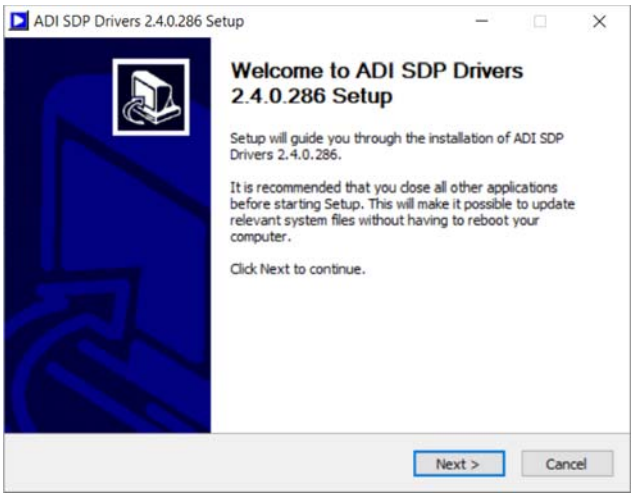

*Figure 6. **ADI SDP Drivers 2.4.0.286 Setup** Install Wizard*

3. Accept the License Agreement, and click **Next >** (see Figure 7).

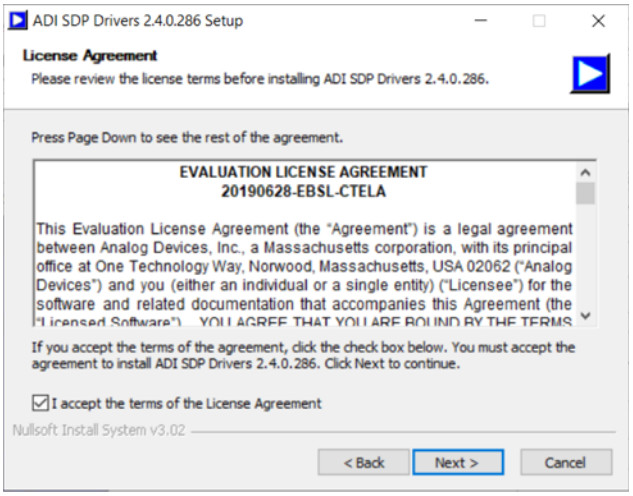

*Figure 7. **ADI SDP Drivers 2.4.0.286 Setup License Agreement***

4. Choose the components to install. The **PreRequisites** components are enough only for the ADP5055-EVALZ to use the USB-SDP-CABLEZ dongle.

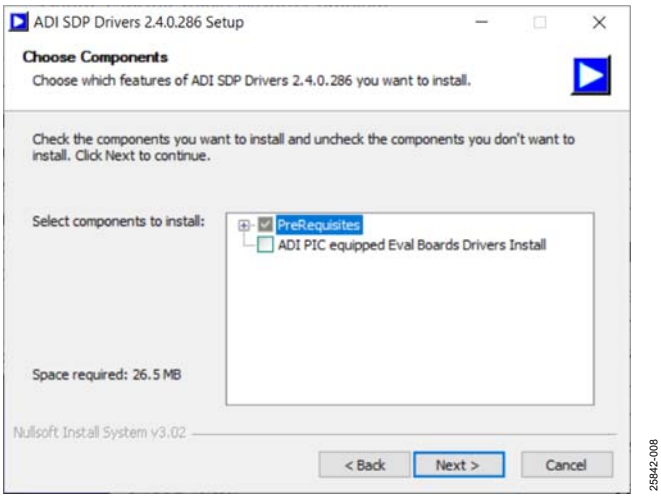

*Figure 8. **ADI SDP Drivers 2.4.0.286 Setup Choose Components** Window*

5. Click **Next >** to install the files to the default destination folder or click **Browse** to choose a different destination folder (see Figure 9).

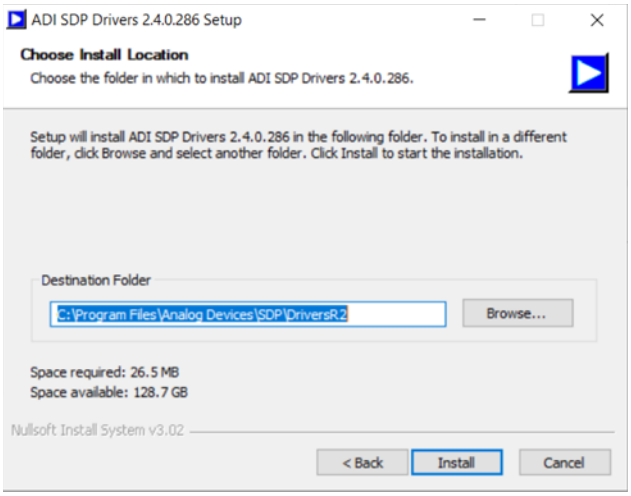

*Figure 9. **ADI SDP Drivers 2.4.0.286 Setup Choose Install Location** Window*

6. Click **Close** when the installation is complete.

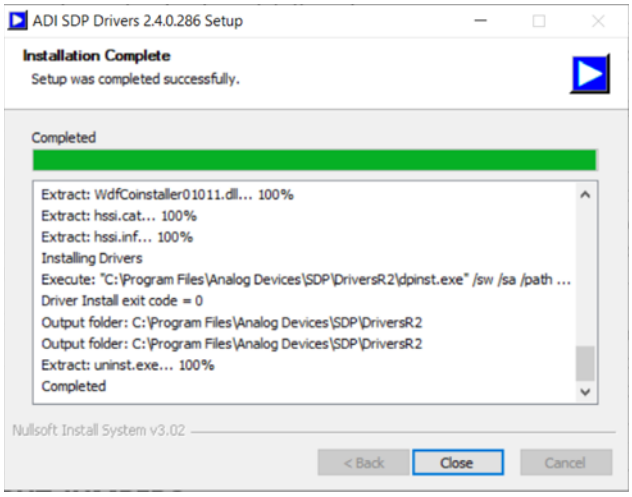

Figure 10. ***ADI SDP Drivers 2.4.0.286 Setup Installation Complete*** *Window*

7. To verify that the USB-SDP-CABLEZ installed properly, open the **Device Manager** on the PC. With the USB-SDP-CABLEZ dongle connected to PC, verify that the USB-SDP-CABLEZ appears under the **ADI Development Tools**, as shown in Figure 11.

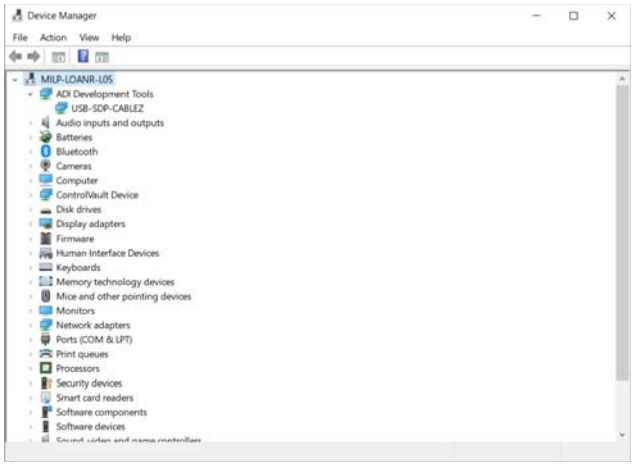

Figure 11. ***Device Manager*** *Window*

USE THE ADP5055 GUI SOFTWARE

Figure 12 shows the optional ADP5055-EVALZ connection diagram for using the ADP5055_GUI software to evaluate the advanced functionalities through the PMBus serial interface. Besides the power supply, the following items are also necessary for using the ADP5055_GUI software:

- A PC with the ADP5055_GUI software and the USB-SDP-CABLEZ dongle driver properly installed
- A 1 m USB Standard A to Mini B cable (included in the USB-SDP-CABLEZ package)
- An USB-I2C-ADPTZ adapter board that can convert the 10-pin Micro-MaTch connector to a 3-pin 0.1" I²C header, which is also included in the USB-SDP-CABLEZ package

To run the ADP5055_GUI, go to **Start > ADP5055_GUI > ADP5055_GUI**. If the program starts properly, and the ADP5055-EVALZ is detected, the ADP5055 GUI appears as shown in Figure 13.

Choose the proper ADP5055 device PMBus address. (Note that the default address with 23.7 kΩ on the CFG2 pin resistor is 0x70). Click **Read all Registers** to view the default values of all registers initialized in the GUI.

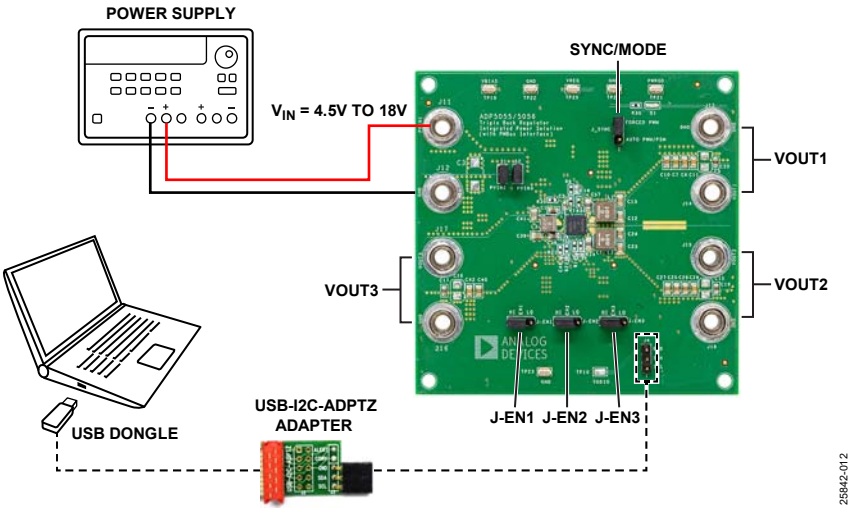

Figure 12. Optional ADP5055-EVALZ Connection Diagram

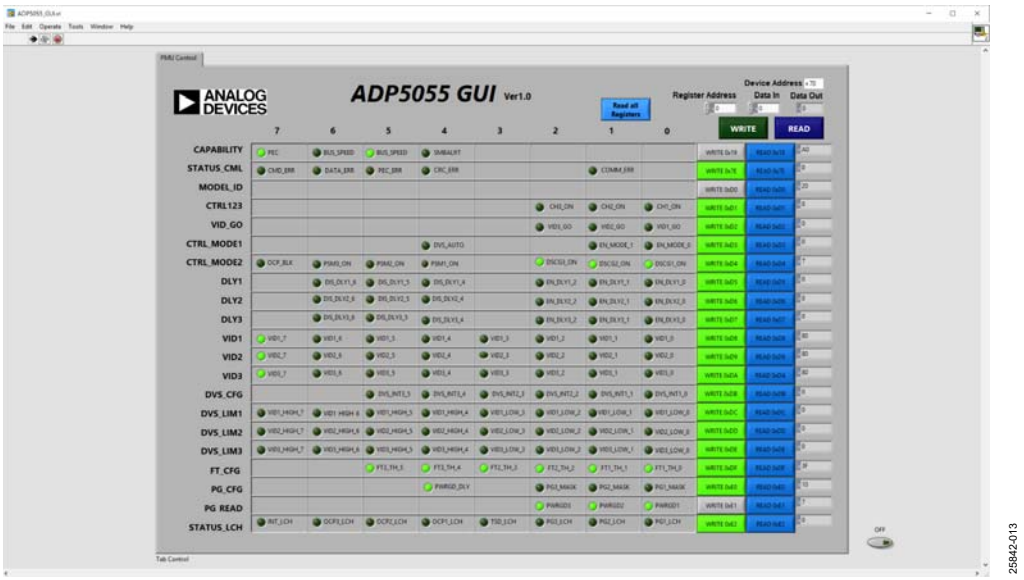

Figure 13. ADP5055 GUI Default Values

MEASURING EVALUATION BOARD PERFORMANCE

MEASURING THE OUTPUT VOLTAGE RIPPLE OF THE BUCK REGULATOR

To observe the output voltage ripple of Channel 1, place an oscilloscope probe across the output capacitor (C_{OUT1}) with the probe ground lead at the negative capacitor terminal and the probe tip at the positive capacitor terminal.

Set the oscilloscope to ac coupling and a 1 µs/division time base, with the bandwidth set to 20 MHz to avoid noise that interferes with the measurements. It is recommended to shorten the ground loop of the oscilloscope probe to minimize coupling.

An accurate output voltage ripple measurement can be performed across C11 or C20 using the proper measurement technique as shown in Figure 14.

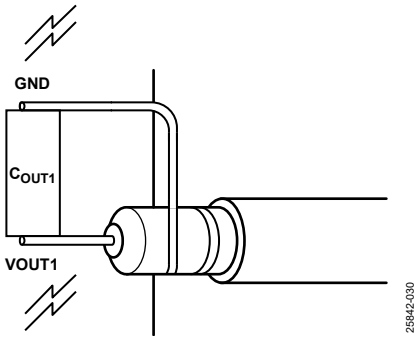

Figure 14. Measure Output Voltage Ripple

MEASURING THE SWITCHING WAVEFORM OF THE BUCK REGULATOR

To observe the switching waveform using an oscilloscope, place the oscilloscope probe tip at the exposed copper trace at the SWx terminal of the inductor with the probe ground at GND. Set the oscilloscope to dc coupling, a 5 V/division, and a 1 µs/division time base.

When the SYNC/MODE pin is set to high, the buck regulators operate in FPWM mode. When the SYNC/MODE pin is set to low, the buck regulators operate in PSM, improving the light load efficiency.

EVALUATING THE SYNCHRONIZATION INPUT OR OUTPUT

The SYNC/MODE pin can be configured as the clock output by the CFG1 pin. A clock pulse with a 50% duty cycle is generated at the SYNC/MODE pin with the frequency equal to the internal frequency set by the RT pin.

When the SYNC/MODE pin is configured as the input, the ADP5055 can be synchronized to an external clock applied to the SYNC/MODE pin. The internal switching frequency (f_{SW}) set by the RT pin must be programed to a value close to the external clock value.

EVALUATING EFFICIENCY

Measure the efficiency, η, by comparing the input power with the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

where:
V_{OUT} is the output voltage.
I_{OUT} is the output current.
V_{IN} is the input voltage.
I_{IN} is the input current.

Measure the input and output voltages as close as possible to the input and output capacitors to reduce the effect of the trace voltage drops.

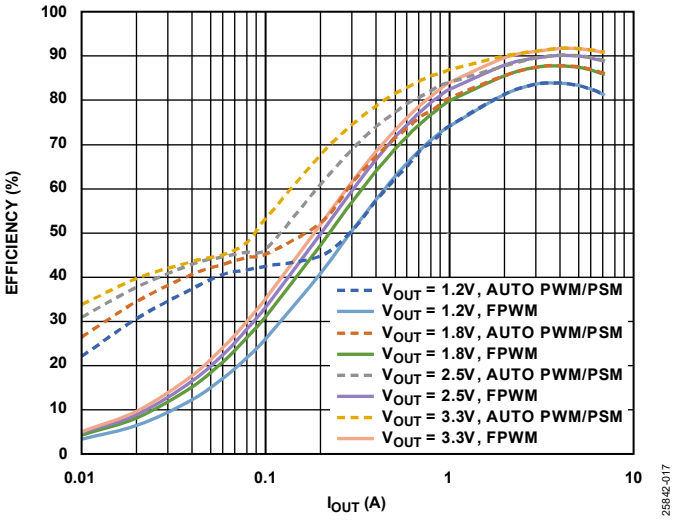

Figure 15. Typical Channel 1 and Channel 2 Efficiency, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and Automatic PSM Mode

MODIFYING THE ADP5055-EVALZ

Setting the Output Voltages

The output voltage (VOUTx) of the three buck regulators are set through external resistor dividers, as shown in Figure 16, for Channel 1. The equation for setting the output voltage is

$$VOUTx = V_{REF} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

where:

V_{REF} is the reference voltage, V_{REF} = 0.6 V.

R_{TOP} is the top resistor in the feedback voltage divider.

R_{BOT} is the bottom resistor in the feedback voltage divider.

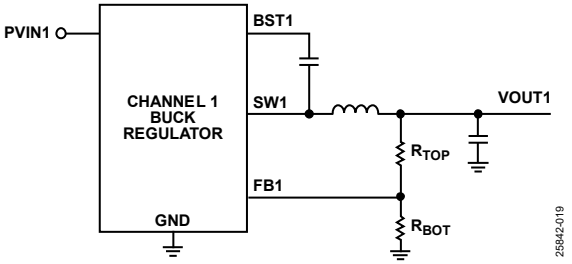

Figure 16. Channel 1 Output Voltage Setting

When the output voltage of the buck regulator is changed, the values of the inductors, the output capacitors, and the compensation networks may require recalculation and changes for stable operation. Refer to the ADP5055 data sheet for details on the selection of the external components.

The ADP5055-EVALZ is supplied with resistor dividers for setting target output voltages. Table 3 shows the external resistor divider components for each channel.

Table 3. External Resistor Dividers in Each Channel

Resistor Divider	Channel 1	Channel 2	Channel 3
R_{TOP}	R2	R13	R23
R_{BOT}	R7	R17	R25

Changing f_{SW}

The f_{SW} of ADP5055-EVALZ is programmed to be 600 kHz by default. To change the f_{SW} (within the range of 250 kHz to 2500 kHz), replace the R1 resistor connected to the RT pin with a different value. Refer to the ADP5055 data sheet for the relationship between f_{SW} and the RT resistor. When the f_{SW} changes, the values of the inductors, output capacitors, and the compensation networks may need recalculation and change for stable operation. Refer to the ADP5055 data sheet for more details on external components selection.

Setting Channel 1 and Channel 2 to Interleaved Parallel Operation

Channel 1 and Channel 2 are configured as individual outputs on the ADP5055-EVALZ by default. To configure Channel 1 and Channel 2 to operate in interleaved parallel single output mode, take the following steps:

1. Short J14 and J15.
2. Ensure that S1 is shunted.
3. Change R26 to 23.7 kΩ on the CFG1 pin.
4. Remove R16 and C34 on the COMP2 pin.
5. Remove R13 and replace R17 with 0 Ω on the FB2 pin.
6. Shunt the J-EN2 jumper to low.
7. Use the Channel 1 feedback resistor dividers, R2 and R7, to set the output voltage.
8. Use J-EN1 (EN1 pin) to enable or disable the regulator.

During parallel operation, the input voltage and current-limit threshold for both channels are the same, and FPWM mode operation on both Channel 1 and Channel 2 is recommended. Refer to the ADP5055 data sheet for more details on inphase parallel operation and interleaved parallel operation.

Phase Shift (0°, 120°, 240°) in the Three Buck Regulators

In the ADP5055-EVALZ, the phase shift is 120° between Channel 1, Channel 2, and Channel 3. This value provides the benefits of out of phase operation by reducing the input ripple current and lowering the ground noise.

Changing the Power Good Output Options

In the ADP5055-EVALZ, the PWRGD output becomes active high when the regulated output voltage of the buck regulator is greater than 95% (typical) and less than 105% (typical) of the nominal output. The PWRGD hardware output is logically ANDed of the internal unmasked PWRGD signal. By default, the PWRGD pin monitors the output voltage on three channels.

The immediate PWRGD signal in each individual buck regulator channel can be read back by the PWRGDx bits in Register 0xE1 in the ADP5055 GUI software. Use the ADP5055 GUI software to configure the PGx_MASK bits in Register 0xE0 to mask or unmask the PWRGD signal of the individual channel to the external PWRGD hardware pin.

Enabling the Dynamic Voltage Scaling (DVS)

The ADP5055 provides a DVS function for Channel 1 to Channel 3. These reference voltages can be programmed in real time via the PMBus serial interface in Register 0xDC (DVS_LIM1) to Register 0xDE (DVS_LIM3). The DVS_INTVALx bits in Register 0xDB (DVS_CFG) are used to set the step interval during the transition for individual channels.

Figure 17 shows a typical DVS voltage transition.

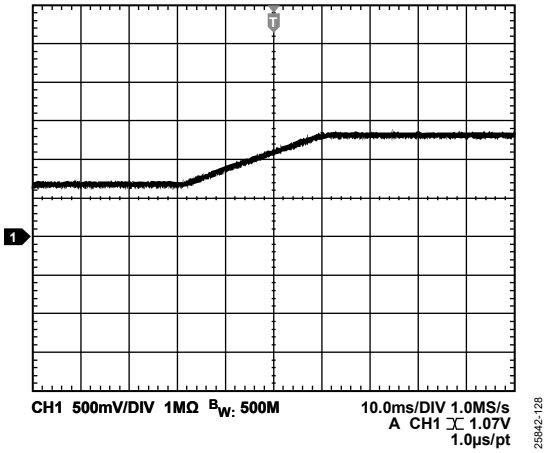

Figure 17. Channel 1 DVS from 0.62 V to 1.24 V, 12 mV/ms, V_{IN} = 12 V

EVALUATION BOARD SCHEMATIC AND ARTWORK

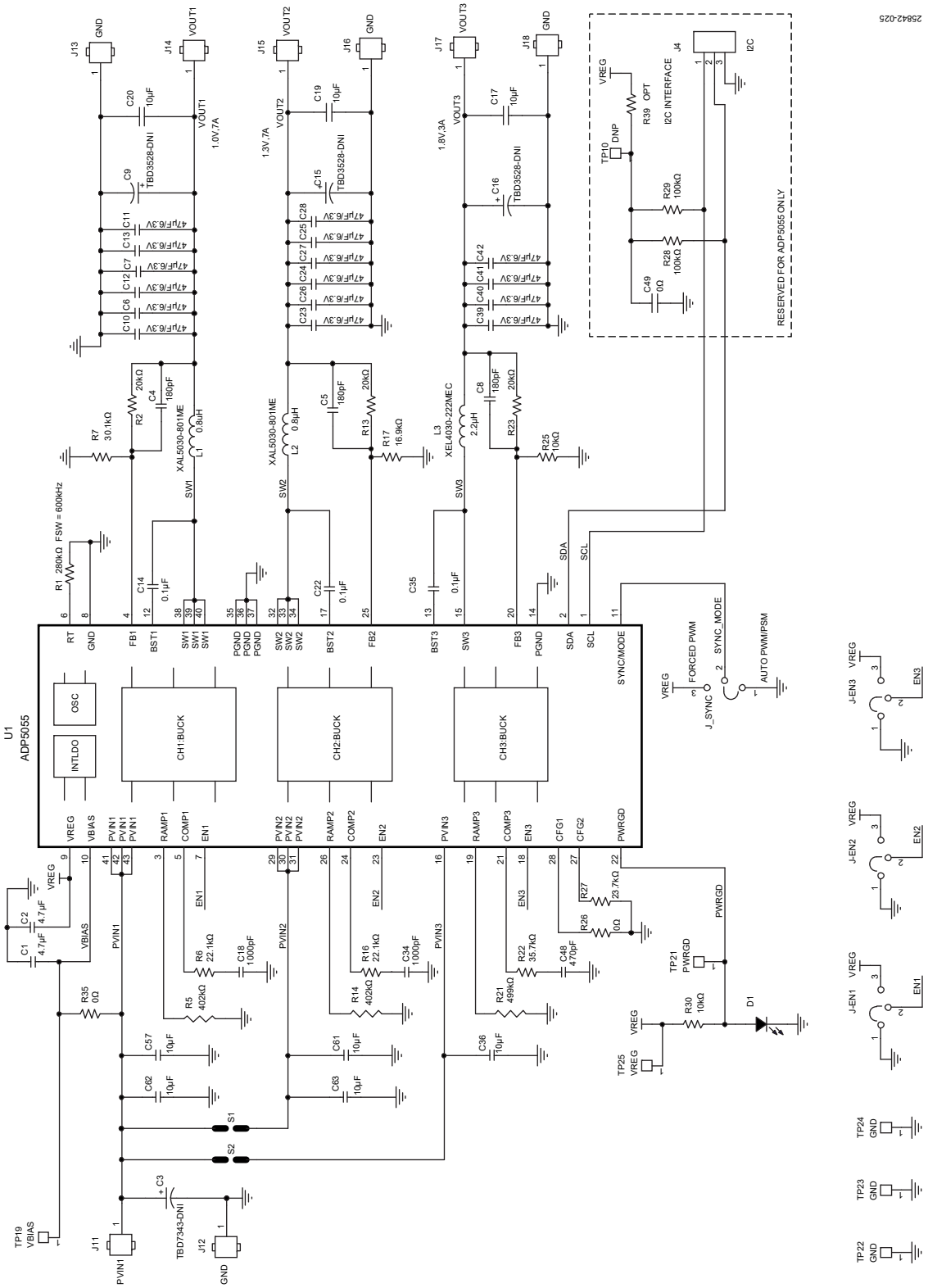

Figure 18. ADP5055-EVALZ Evaluation Board Schematic

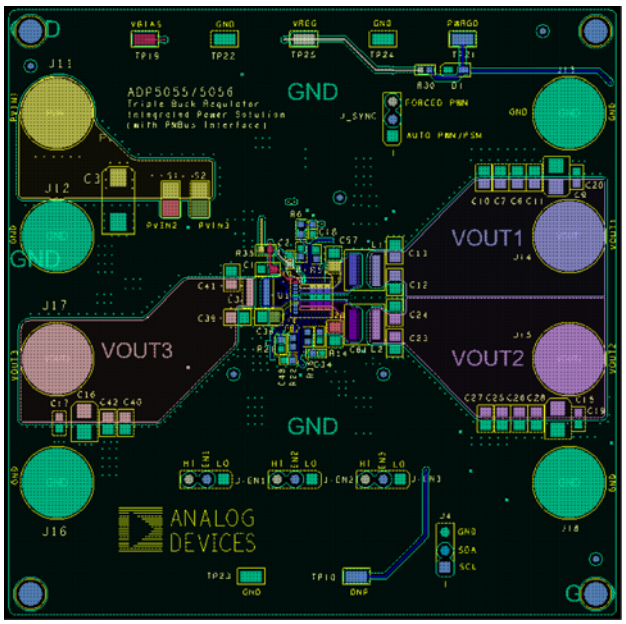

Figure 19. ADP5055-EVALZ Top Layer, Recommended Layout

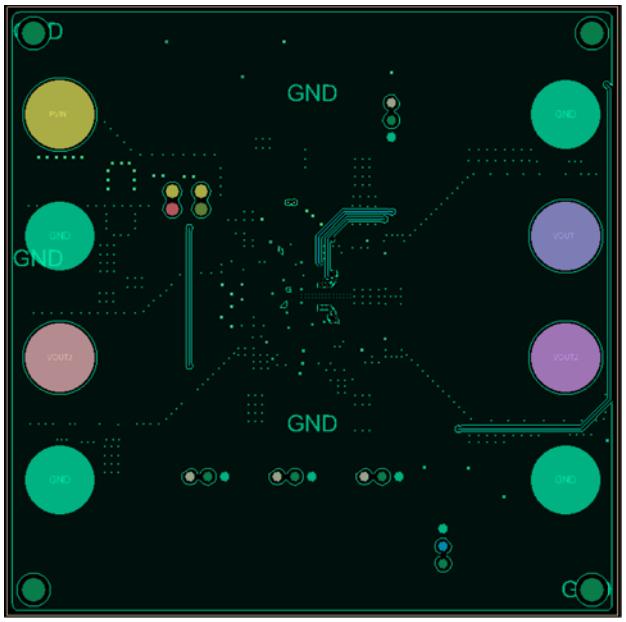

Figure 20. ADP5055-EVALZ Second Layer, Recommended Layout

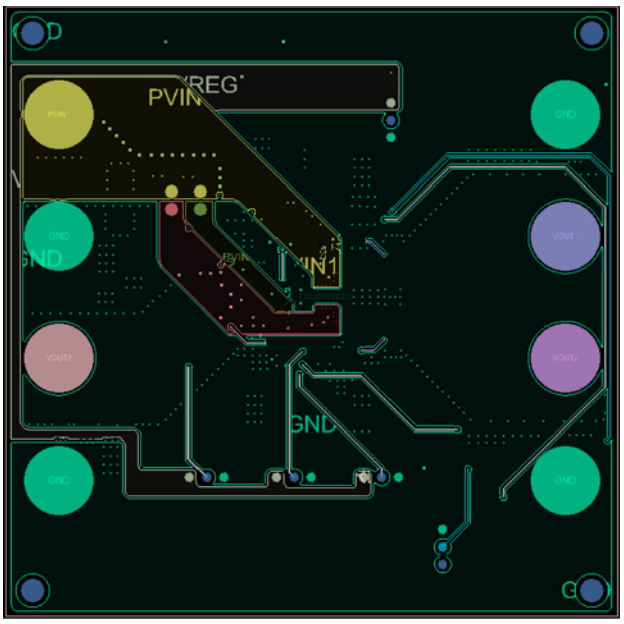

Figure 21. ADP5055-EVALZ Third Layer, Recommended Layout

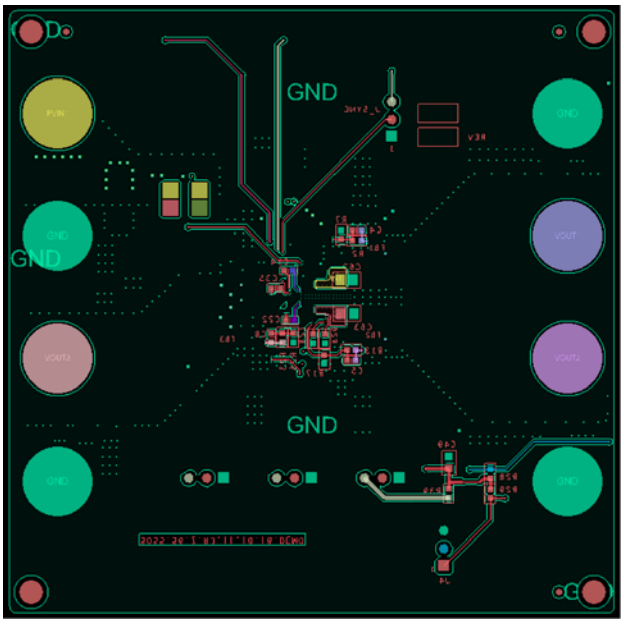

Figure 22. ADP5055-EVALZ Bottom Layer, Recommended Layout

ORDERING INFORMATION

BILL OF MATERIALS

Table 4.

Qty.	Reference Designator	Description	Manufacturer	Part Number
1	C1	Ceramic capacitor, 4.7 µF, X6S, 25 V, 10%, 0603	Murata	GRM188C81E475KE11
1	C2	Ceramic capacitor, 4.7 µF, X6S, 6.3 V, 20%, 0402	Murata	GRM155C80J475MEAA
3	C4, C5, C8	Ceramic capacitors, 180 pF, C0G, 50 V, 1%, 0402	Murata	GCM1555C1H181FA16D
16	C6, C7, C10 to C13, C23 to C28, C39 to C42	Ceramic capacitors, 47 µF, 6.3 V, 20%, 0805	Murata/Taiyo Yuden	GRM21BR60J476ME11, MK212BJ476MG-T
3	C14, C22, C35	Ceramic capacitors, 0.1 µF, X7R, 16 V, 10%, 0402	KEMET	C0402C104K4RACTU
2	C18, C34	Ceramic capacitors, 1 nF, 50 V, 5%, 0402	Murata	GRM1555C1H102JA01
5	C36, C57, C61 to C63	Ceramic capacitors, 10 µF, X7S, 25 V, 10%, 0805	Murata	GRM21BC71E106KE11
3	C17, C19, C20	Ceramic capacitors, 10 µF, X5R, 10 V, 10%, 0603	Murata	GRM188R61A106KAAL
4	C3, C9, C15, C16	Capacitors, do not install (DNI)	Not applicable	Not applicable
1	C48	Ceramic capacitor, 470 pF, C0G, 50 V, 5%, 0402	Murata	GRT1555C1H471JA02
1	C49	Resistor, SMD 0 Ω jumper, 1/10 W, 0603	Vishay Dale	CRCW06030000Z0EA
1	D1	Clear green LED, 0603, surface-mount device (SMD)	LITE-ON	LTST-C191KGKT
4	J-EN1, J-EN2, J-EN3, J_SYNC	2.54 mm, 3-pin headers	Wurth	61300311121
2	S1, S2	2.54 mm, 2-pin headers	Wurth	61300311121
8	J11 to J18	Noninsulated jacks, .218 inches	Keystone Electronics	575-4
2	L1, L2	Inductors, 0.8 µH	Coilcraft	XAL5030-801ME
1	L3	Inductor, 2.2 µH	Coilcraft	XEL4030-222ME
1	R1	Resistor, SMD, 280 kΩ, 1%, 1/16 W, 0402	Vishay Dale	CRCW0402280KFKED
3	R2, R13, R23	Resistors, SMD, 20 kΩ, 1%, 1/16 W, 0402	Vishay Dale	CRCW040220K0FKED
2	R5, R14	Resistors, SMD, 402 kΩ, 1%, 1/16 W, 0402	Vishay Dale	CRCW0402402KFKED
2	R6, R16	Resistors, SMD, 22.1 kΩ, 1%, 1/16 W, 0402	Vishay Dale	CRCW040222K1FKED
1	R7	Resistor, SMD, 30.1 kΩ, 1%, 1/16 W, 0402	Vishay Dale	CRCW040230K1FKED
1	R17	Resistor, SMD, 16.9 kΩ, 1%, 1/16 W, 0402	Vishay Dale	CRCW040216K9FKED

Qty.	Reference Designator	Description	Manufacturer	Part Number
1	R21	Resistor, SMD, 499 kΩ, 1%, 1/16 W, 0402	Vishay Dale	CRCW0402499KFKED
1	R22	Resistor, SMD, 35.7 kΩ, 1%, 1/16 W, 0402	Vishay Dale	CRCW040235K7FKED
2	R25, R30	Resistors, SMD,10 kΩ, 1%, 1/16 W, 0402	Vishay Dale	CRCW040210K0FKED
2	R26, R35	Resistors, SMD, 0 Ω, jumper, 1/10 W, 0603	Vishay Dale	CRCW04020000Z0ED
1	R27	Resistors, SMD, 23.7 kΩ, 1%, 1/16 W, 0402	Vishay Dale	CRCW040223K7FKED
2	R28, R29	Resistors, SMD, 100 kΩ, 1%, 1/16 W, 0402	Vishay Dale	CRCW0402100KFKED
1	R39	Resistors, 0402, DNI	Not applicable	Not applicable
6	TP19, TP21 to TP25	Test points, miniature	Keystone Electronics	5019
1	TP10	Test point, DNI	Not applicable	Not applicable
1	U1	Triple buck regulator integrated power solution	Analog Devices	ADP5055

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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