ISO721EVM

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1 Introduction

This user's guide details the evaluation module (EVM) operation of the ISO721 and ISO721M digital isolators. The same EVM board is used for each device. Configuration requirements are presented as well as user optional I/O loads. This document is intended to aid designers with isolator parameter performance evaluation within a particular system.

1.1 Overview

The ISO721 and ISO721M digital isolators have a logic input and output buffer separated by a silicon oxide (SiO_2) insulation barrier. Used with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, and then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received for more than 4 µs, the input is assumed to be unpowered or not functional, and the fail-safe circuit drives the output to a logic-high state.

CAUTION

Note that although these devices provide galvanic isolation of up to 4000 V, this EVM cannot be used for isolation voltage testing. It is designed for the examination of device operating parameters only and will be damaged if high voltage (> 5.5 V) is applied anywhere in the circuit.

1.2 Functional Configuration of the ISO721 and ISO721M

The EVM is configured for the pinout displayed in Figure 1. The additional I/Os on the EVM are provided for future development.

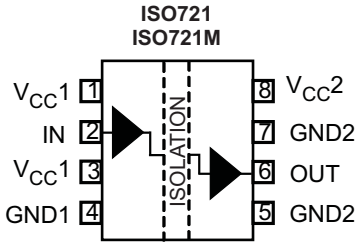

Figure 1. The ISO721 and ISO721M Pinout

The ISO721 has TTL input thresholds and a input noise filter that prevents transient pulses of up to 2 ns in duration from being passed to the output of the device.

The ISO721M has a CMOS $V_{CC}/2$ input threshold and does not have the noise filter and the additional propagation delay. These features of the ISO721M also provide for a 0-Mbps to 150-Mbps signaling rate rather than the ISO721's 0-Mbps to 100-Mbps signaling rate.

1.3 EVM Signal Paths of the ISO721 and ISO721M Isolators

This multifunctional EVM is designed with signal paths shown in Figure 2 for the analysis of the ISO721 and ISO721M, as well as future isolator configurations.

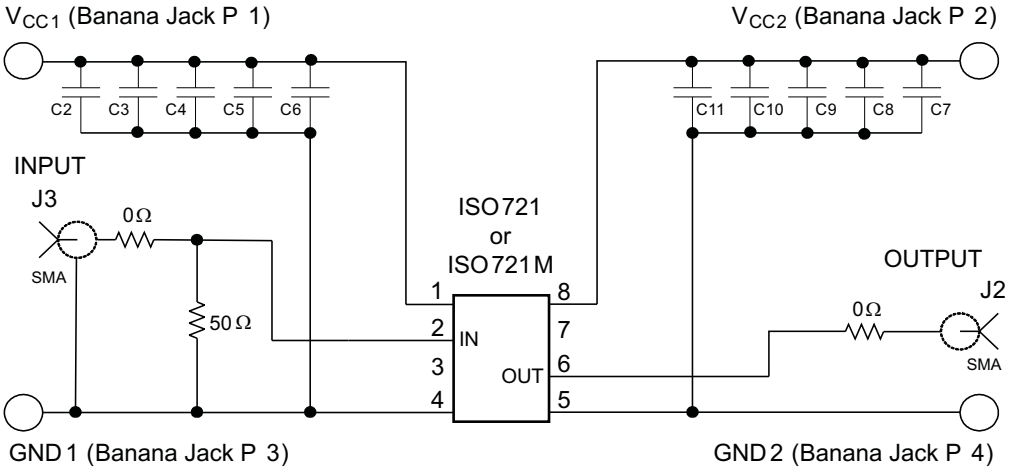

Figure 2. The ISO721 and ISO721M EVM Schematic

Table 1. EVM Connections

Connection	Label	Description
J1		SMA connector (unused)
J2		SMA connector to the output pin 6
J3		SMA connector to the input pin 2
J4		SMA connector (unused)
P1	V_{CC1}	Input power supply banana jack
P2	V_{CC2}	Output power supply banana jack
P3	GND1	Input power ground connection banana jack
P4	GND2	Output power ground connection banana jack

Table 1. EVM Connections (continued)

Connection	Label	Description
JMP1		3-pin jumper (unused)
JMP2		3-pin jumper (unused)
JMP3		3-pin jumper – V_{CC1}, input, GND1
JMP4		3-pin jumper (unused)

1.4 The EVM Configuration

The ISO721EVM configuration has an SMA connector J3 set up as the input to pin 2, the IN pin of the ISO721 in Figure 1 and Figure 2. A 0-Ω input series resistor, R8, is located next to the J3 input connector, and a 50-Ω R5 from the input to ground is located on the bottom of the board.

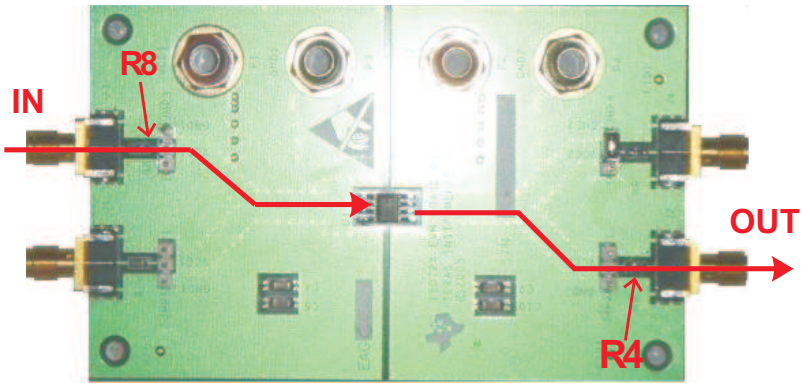

Figure 3. ISO721 and ISO721M EVM, Top

The output channel configuration of the ISO721EVM has the OUT pin (pin 6) of Figure 1 and Figure 2 connected to SMA connector J2 through a 0- Ω series resistor R4.

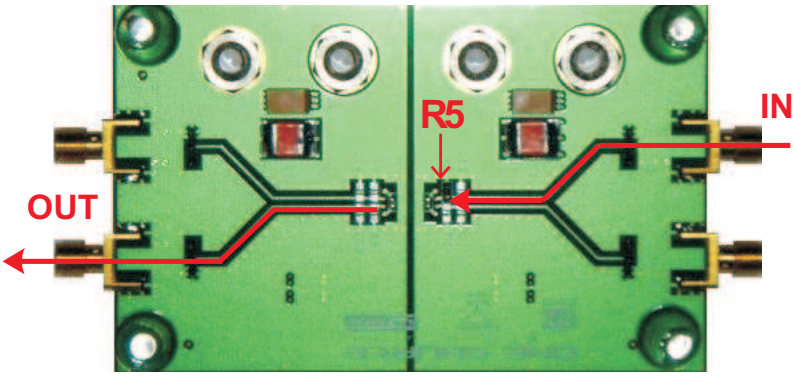

Figure 4. ISO721 and ISO721M EVM, Bottom

The pads for R3, C12, and C13 are available on the bottom of the EVM for varied loading conditions if desired by a user.

2 EVM Setup and Operation

This section includes the setup and operation of the EVM for parameter performance evaluation. Typical waveforms are included.

2.1 Overview

The basic setup in Figure 5 has the two power supplies required to evaluate isolator performance with 3.3-V on one side and 5-V on the other. If both sides are to be evaluated at the same supply voltage, only one power supply is required and can be used to power both sides of the EVM.

CAUTION

Note that this EVM is for operating parameter performance evaluation only and not designed for isolation voltage testing. Any voltage applied above the 5.5-V maximum recommended operating voltage of the ISO721 will damage the EVM.

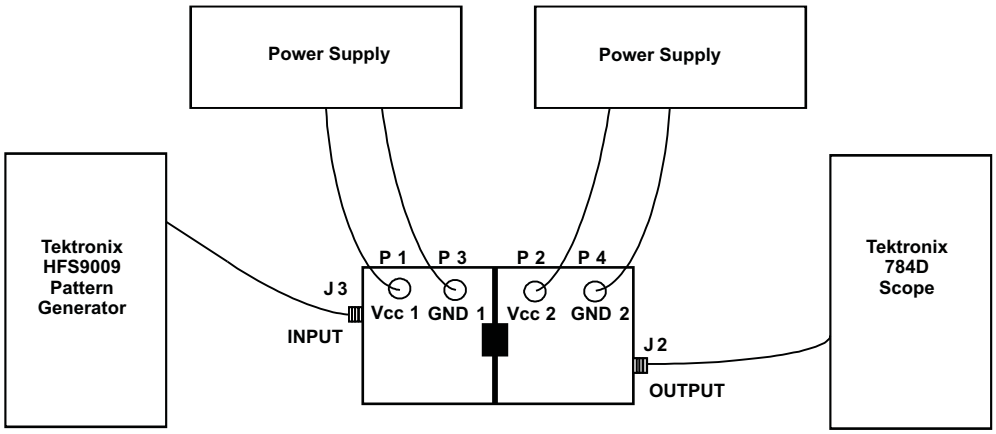

Figure 5. Basic EVM Operation

The input to the EVM is a 20-MHz pulse displayed on channel 1 in Figure 6. The output of the EVM is channel 2.

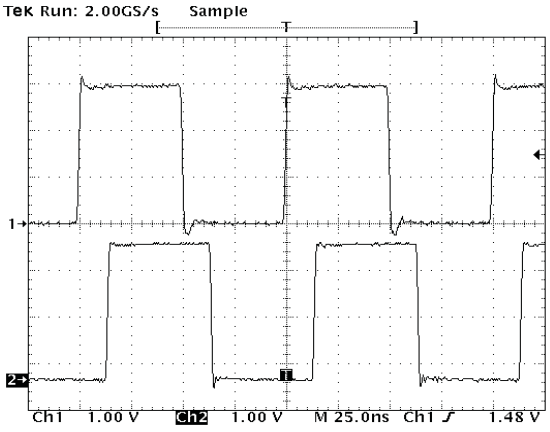

Figure 6. Typical Input and Output Waveforms

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 5.5 V and the output voltage range of 0 V to 6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°CC as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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