# Dual, Simultaneous Sampling, 16-Bit/14-Bit, 4 MSPS, SAR ADCs, Pseudo Differential Input

Data Sheet **AD7383/AD7384**

## FEATURES

- Dual 16-bit/14-bit ADC family
- Dual simultaneous sampling
- Pseudo differential analog inputs
- 4 MSPS throughput conversion rate
- SNR (typical)
  - 87.5 dB, $V_{REF}$ = 3.3 V external for 16-bit AD7383
  - 83.5 dB, $V_{REF}$ = 3.3 V external for 14-bit AD7384
  - 93.4 dB with RES = 1 and OSR = 8
- On-chip oversampling function
- Resolution boost function
- INL error (maximum)
  - 2.5 LSBs for 16-bit AD7383
  - 1.0 LSB for 14-bit AD7384
- 2.5 V internal reference
- High speed serial interface
- −40°C to +125°C operation
- 16-lead LFCSP, 3 mm × 3 mm
- Alert function

## APPLICATIONS

- Motor control position feedback
- Motor control current sense
- Sonar
- Power quality
- Data acquisition systems
- Erbium doped fiber amplifier (EDFA) applications
- I and Q demodulation

## GENERAL DESCRIPTION

The 16-bit AD7383 and the 14-bit AD7384 are a pin-compatible family of dual simultaneous sampling, high speed, low power, successive approximation register (SAR), analog-to-digital converters (ADCs) that operate from a 3.0 V to 3.6 V power supply and feature throughput rates up to 4 MSPS. The analog input type is pseudo differential and is sampled and converted on the falling edge of $\overline{CS}$.

Integrated on-chip oversampling blocks improve dynamic range and reduce noise at lower bandwidths. A buffered internal 2.5 V reference is included. Alternatively, an external reference up to 3.3 V can be used.

## FUNCTIONAL BLOCK DIAGRAM

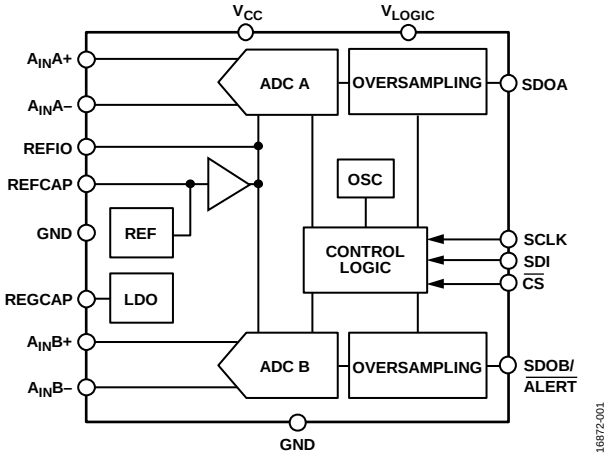


*Figure 1.*

The conversion process and data acquisition use standard control inputs that allow simple interfacing to microprocessors or digital signal processors (DSPs). The devices are compatible with 1.8 V, 2.5 V, and 3.3 V interfaces, using a separate logic supply.

The AD7383 and the AD7384 are available in a 16-lead lead frame chip scale package (LFCSP) with operation specified from −40°C to +125°C.

Multifunction pin names may be referenced by their relevant function only.

## PRODUCT HIGHLIGHTS

1. Dual simultaneous sampling and conversion with two complete ADC functions.
2. Pin-compatible product family.
3. High 4 MSPS throughput rate.
4. Space saving 3 mm × 3 mm LFCSP.
5. Integrated oversampling block to increase dynamic range, reduce noise, and reduce SCLK speed requirements.
6. Pseudo differential analog inputs.
7. Small sampling capacitor reduces amplifier drive burden.

**Table 1. Related Devices in the Family**

| Channels | Analog Input | 16-Bit | 14-Bit | 12-Bit |
|---|---|---|---|---|
| 2 | Differential | AD7380 | AD7381 | |
| | Pseudo differential | AD7383 | AD7384 | |
| | Single-ended | AD7386 | AD7387 | AD7388 |

Rev. 0 Document Feedback


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## REVISION HISTORY

**7/2020—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{CC}$ = 3.0 V to 3.6 V, $V_{LOGIC}$ = 1.65 V to 3.6 V, reference voltage ($V_{REF}$) = 2.5 V internal, sampling frequency ($f_{SAMPLE}$) = 4 MSPS, $T_A$ = −40°C to +125°C, and no oversampling enabled, unless otherwise noted.

**Table 2. AD7383**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESOLUTION | | 16 | | | Bits |
| THROUGHPUT | | | | | |
| Conversion Rate | | | | 4 | MSPS |
| DC ACCURACY | | | | | |
| No Missing Codes | | 16 | | | Bits |
| Differential Nonlinearity (DNL) Error | | −1.0 | −0.5 | +1.0 | LSB |
| Integral Nonlinearity (INL) Error | | −2.5 | ±1.0 | +2.5 | LSB |
| Gain Error | $T_{MIN}$ to $T_{MAX}$ | −0.06 | ±0.02 | +0.06 | % FS |
| Gain Error Temperature Drift | | −3 | ±1 | +3 | ppm/°C |
| Gain Error Match | $T_{MIN}$ to $T_{MAX}$ | | 0.025 | ±0.07 | % FS |
| Offset Error | $T_{MIN}$ to $T_{MAX}$ | −0.5 | ±0.05 | +0.5 | mV |
| Offset Temperature Drift | | −1 | ±0.25 | +1 | µV/°C |
| Offset Error Match | $T_{MIN}$ to $T_{MAX}$ | | 0.05 | 0.5 | mV |
| AC ACCURACY | Input frequency ($f_{IN}$) = 1 kHz | | | | |
| Dynamic Range | $V_{REF}$ = 3.3 V external | | 87.9 | | dB |
| | | | 86.1 | | dB |
| Oversampled Dynamic Range | OSR = 4 | | 91.8 | | dB |
| Signal-to-Noise Ratio (SNR) | $V_{REF}$ = 3.3 V external | 85 | 87.5 | | dB |
| | | 84 | 86 | | dB |
| | OS_MODE = 1, OSR = 8, RES = 1 | | 93.4 | | dB |
| | $f_{IN}$ = 100 kHz | | 85.3 | | dB |
| Spurious-Free Dynamic Range (SFDR) | | | 101 | | dB |
| Total Harmonic Distortion (THD) | | | −100 | | dB |
| | $f_{IN}$ = 100 kHz | | −97 | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | $V_{REF}$ = 3.3 V external | 84.5 | 87 | | dB |
| | | 83.5 | 85.5 | | dB |
| Channel to Channel Isolation | | | −110 | | dB |
| POWER SUPPLIES | Normal mode (operational) | | | | |
| Power Dissipation | | | | | |
| Total Power ($P_{TOTAL}$) | | | 87 | 107 | mW |
| $V_{CC}$ Power ($P_{VCC}$) | | | 74.3 | 94 | mW |
| $V_{LOGIC}$ Power ($P_{VLOGIC}$) | Sinewave input at 1 kHz | | 12.6 | 13 | mW |
| $V_{CC}$ Current ($I_{VCC}$) | | | 22.5 | 26 | mA |
| $V_{LOGIC}$ Current ($I_{VLOGIC}$) | Sinewave input at 1 kHz | | 3.5 | 3.6 | mA |

$V_{CC}$ = 3.0 V to 3.6 V, $V_{LOGIC}$ = 1.65 V to 3.6 V, $V_{REF}$ = 2.5 V internal, $f_{SAMPLE}$ = 4 MSPS, $T_A$ = −40°C to +125°C, and no oversampling enabled, unless otherwise noted.

**Table 3. AD7384**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESOLUTION | | 14 | | | Bits |
| THROUGHPUT | | | | | |
| Conversion Rate | | | | 4 | MSPS |
| DC ACCURACY | | | | | |
| No Missing Codes | | 14 | | | Bits |
| DNL Error | | −1.0 | −0.5 | +1.0 | LSB |
| INL Error | | −1.0 | ±0.4 | +1.0 | LSB |
| Gain Error | $T_{MIN}$ to $T_{MAX}$ | −0.06 | ±0.02 | +0.06 | % FS |
| Gain Error Temperature Drift | | −3 | ±1 | +3 | ppm/°C |
| Gain Error Match | $T_{MIN}$ to $T_{MAX}$ | | 0.025 | ±0.07 | % FS |
| Offset Error | $T_{MIN}$ to $T_{MAX}$ | −2 | ±0.5 | +2 | LSB |
| Offset Temperature Drift | | −5 | ±0.003 | +5 | µV/°C |
| Offset Error Match | $T_{MIN}$ to $T_{MAX}$ | | 0.5 | 2.5 | LSB |
| AC ACCURACY | $f_{IN}$ = 1 kHz | | | | |
| Dynamic Range | $V_{REF}$ = 3.3 V external | | 84.1 | | dB |
| | | | 83.2 | | dB |
| Oversampled Dynamic Range | OSR = 4 | | 89 | | dB |
| SNR | $V_{REF}$ = 3.3 V external | 82.5 | 83.5 | | dB |
| | | 82 | 83 | | dB |
| | OS_MODE = 1, OSR = 8, RES = 1 | | 90.7 | | dB |
| | $f_{IN}$ = 100 kHz | | 82.7 | | dB |
| SFDR | | | 101 | | dB |
| THD | | | −100 | | dB |
| | $f_{IN}$ = 100 kHz | | −96.7 | | dB |
| SINAD | $V_{REF}$ = 3.3 V | 82 | 83 | | dB |
| | | 81.5 | 82.5 | | dB |
| Channel to Channel Isolation | | | −110 | | dB |
| POWER SUPPLIES | Normal mode (operational) | | | | |
| Power Dissipation | | | | | |
| $P_{TOTAL}$ | | | 84.2 | 105.6 | mW |
| $P_{VCC}$ | | | 73 | 94 | mW |
| $P_{VLOGIC}$ | Sinewave input at 1 kHz | | 11.2 | 11.6 | mW |
| $I_{VCC}$ | | | 22 | 26 | mA |
| $I_{VLOGIC}$ | Sinewave input at 1 kHz | | 3.1 | 3.2 | mA |

**Table 4. All Devices**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ANALOG INPUT | | | | | |
| Voltage Range | ($A_{IN}$x+) to ($A_{IN}$x−) | $-V_{REF}/2$ | | $+V_{REF}/2$ | V |
| Absolute Input Voltage Range | $A_{IN}$x+ | −0.1 | | $+V_{REF}$ + 0.1 | V |
| Common-Mode Input Range | $A_{IN}$x− | | $V_{REF}/2 \pm 0.075$ | | V |
| Common-Mode Rejection Ratio (CMRR) | $f_{IN}$ = 500 kHz | | −70 | | dB |
| DC Leakage Current | | | 0.1 | 1 | µA |
| Input Capacitance | When in track mode | | 18 | | pF |
| | When in hold mode | | 5 | | pF |
| SAMPLING DYNAMICS | | | | | |
| Input Bandwidth | At −0.1 dB | | 6 | | MHz |
| | At −3 dB | | 25 | | MHz |
| Aperture Delay | | | 2 | | ns |
| Aperture Delay Match | | | 26 | 100 | ps |
| Aperture Jitter | | | 20 | | ps |
| REFERENCE INPUT AND OUTPUT | | | | | |
| $V_{REF}$ Input | | | | | |
| Voltage Range | External reference | 2.49 | | 3.4 | V |
| Current | External reference | | 0.47 | 0.51 | mA |
| $V_{REF}$ Output Voltage | −40°C to +125°C | 2.495 | 2.5 | 2.505 | V |
| $V_{REF}$ Temperature Coefficient | | | 5 | 10 | ppm/°C |
| $V_{REF}$ Noise | | | 7 | | µV rms |
| DIGITAL INPUTS (SCLK, SDI, AND $\overline{CS}$) | | | | | |
| Logic Levels | | | | | |
| Input Voltage | | | | | |
| Low ($V_{IL}$) | | | | $0.2 \times V_{LOGIC}$ | V |
| High ($V_{IH}$) | | $0.8 \times V_{LOGIC}$ | | | V |
| Input Current | | | | | |
| Low ($I_{IL}$) | | −1 | | +1 | µA |
| High ($I_{IH}$) | | −1 | | +1 | µA |
| DIGITAL OUTPUTS (SDOA AND SDOB/$\overline{ALERT}$) | | | | | |
| Output Coding | | | Twos complement | | Bits |
| Output Voltage | | | | | |
| Low ($V_{OL}$) | Sink current ($I_{SINK}$) = 300 µA | | | 0.4 | V |
| High ($V_{OH}$) | Source current ($I_{SOURCE}$) = −300 µA | $V_{LOGIC}$ − 0.3 | | | V |
| Floating State | | | | | |
| Leakage Current | | | | ±1 | µA |
| Output Capacitance | | | 10 | | pF |
| POWER SUPPLIES | | | | | |
| $V_{CC}$ | | | | | |
| | | 3.0 | 3.3 | 3.6 | V |
| | External reference = 3.3 V | 3.2 | 3.3 | 3.6 | V |
| $V_{LOGIC}$ | | 1.65 | | 3.6 | V |
| $I_{VCC}$ | | | | | |
| Normal Mode (Static) | | | 2.3 | 2.8 | mA |
| Shutdown Mode | | | 101 | 200 | µA |
| $V_{LOGIC}$ Current ($I_{VLOGIC}$) | | | | | |
| Normal Mode (Static) | | | 10 | 200 | nA |
| Shutdown Mode | | | 10 | 200 | nA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Dissipation | | | | | |
| $P_{VCC}$ | | | | | |
| Normal Mode (Static) | | | 8 | 11 | mW |
| Shutdown Mode | | | 365 | 720 | µW |
| $P_{VLOGIC}$ | | | | | |
| Normal Mode (Static) | | | 36 | 720 | nW |
| Shutdown Mode | | | 36 | 720 | nW |

## TIMING SPECIFICATIONS

$V_{CC}$ = 3.0 V to 3.6 V, $V_{LOGIC}$ = 1.65 V to 3.6 V, $V_{REF}$ = 2.5 V internal, and $T_A$ = −40°C to +125°C, unless otherwise noted. See Figure 2 to Figure 6, Figure 36, and Figure 38 for the timing diagrams.

**Table 5.**

| Parameter | Min | Typ | Max | Unit | Description |
|---|---|---|---|---|---|
| $t_{CYC}$ | 250 | | | ns | Time between conversions |
| $t_{SCLKED}$ | 0.4 | | | ns | $\overline{CS}$ falling edge to first SCLK falling edge |
| $t_{SCLK}$ | 12.5 | | | ns | SCLK period |
| $t_{SCLKH}$ | 5 | | | ns | SCLK high time |
| $t_{SCLKL}$ | 5 | | | ns | SCLK low time |
| $t_{CSH}$ | 10 | | | ns | $\overline{CS}$ pulse width |
| $t_{QUIET}$ | 10 | | | ns | Interface quiet time prior to conversion |
| $t_{SDOEN}$ | | | | | $\overline{CS}$ low to SDOA and SDOB/$\overline{ALERT}$ enabled |
| | | | 6 | ns | $V_{LOGIC} \geq 2.25$ V |
| | | | 8 | ns | 1.65 V ≤ $V_{LOGIC}$ < 2.3 V |
| $t_{SDOH}$ | 2 | | | ns | SCLK rising edge to SDOx hold time |
| $t_{SDOS}$ | | | | | SCLK rising edge to SDOx setup time |
| | | | 6 | ns | $V_{LOGIC} \geq 2.25$ V |
| | | | 8 | ns | 1.65 V ≤ $V_{LOGIC}$ < 2.3 V |
| $t_{SDOT}$ | | | 8 | ns | $\overline{CS}$ rising edge to SDOx high impedance |
| $t_{SDIS}$ | 1 | | | ns | SDI setup time prior to SCLK falling edge |
| $t_{SDIH}$ | 1 | | | ns | SDI hold time after SCLK falling edge |
| $t_{SCLKCS}$ | 0 | | | ns | SCLK rising edge to $\overline{CS}$ rising edge |
| $t_{CONVERT}$ | | | 190 | ns | Conversion time |
| $t_{ACQUIRE}$ | 110 | | | ns | Acquire time |
| $t_{RESET}$ | | | | | Valid time to start conversion after software reset |
| | | 250 | | ns | Valid time to start conversion after soft reset |
| | | 800 | | ns | Valid time to start conversion after hard reset |
| $t_{POWERUP}$ | | | | | Supply active to conversion |
| | | | 5 | ms | First conversion allowed |
| | | | 11 | ms | Settled to within 1% with internal reference |
| | | | 5 | ms | Settled to within 1% with external reference |
| $t_{REGWRITE}$ | | | 5 | ms | Supply active to register read write access allowed |
| $t_{STARTUP}$ | | | | | Exiting shutdown mode to conversion |
| | | | 11 | ms | Settled to within 1% with internal reference |
| | | | 10 | µs | Settled to within 1% with external reference |
| $t_{CONVERT0}$ | 4 | 7 | 10 | ns | Conversion start time for first sample in normal average oversampling mode |
| $t_{CONVERTx}$ | | | | | Conversion start time for $x^{th}$ sample in normal average oversampling mode |
| | $t_{CONVERT0}$ + (330 × (x − 1)) | | | ns | For AD7383 at 3 MSPS |
| | $t_{CONVERT0}$ + (250 × (x − 1)) | | | ns | For AD7384 at 4 MSPS |
| $t_{ALERTS}$ | | | 200 | ns | Time from $\overline{CS}$ to $\overline{ALERT}$ indication |
| $t_{ALERTC}$ | | | 12 | ns | Time from $\overline{CS}$ to $\overline{ALERT}$ clear |
| $t_{ALERTS\_NOS}$ | | | 12 | ns | Time from internal conversion with exceeded threshold to $\overline{ALERT}$ indication |

### *Timing Diagrams*

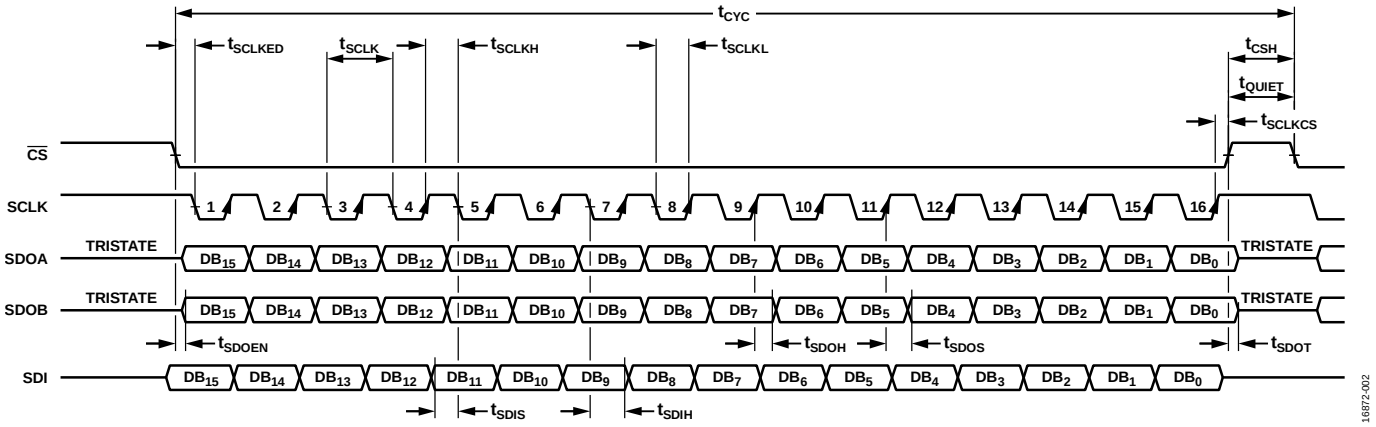


*Figure 2. Serial Interface Timing Diagram*

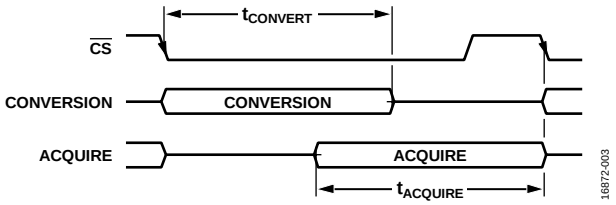


*Figure 3. Internal Conversion Acquire Timing*

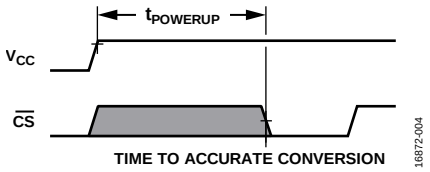


*Figure 4. Power-Up Time to Conversion*

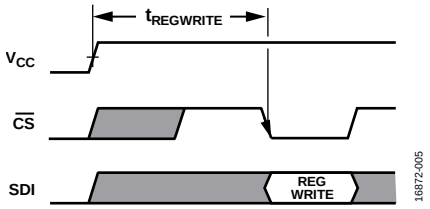


*Figure 5. Power-Up Time to Register Read Write Access*

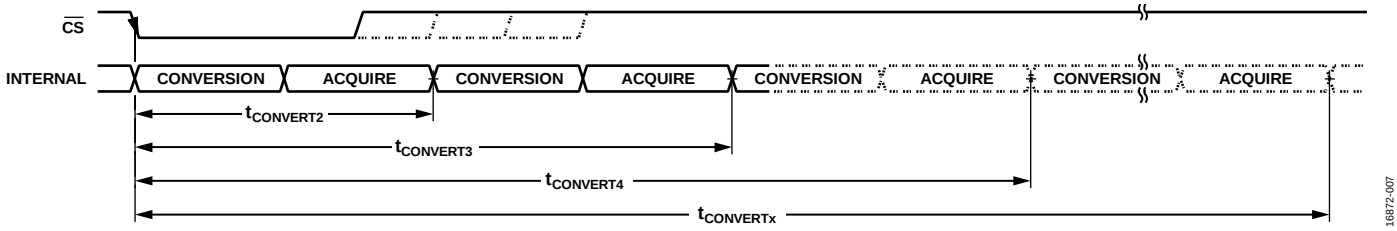


*Figure 6. Conversion Timing During Normal Average Oversampling Mode*

# ABSOLUTE MAXIMUM RATINGS

**Table 6.**

| Parameter | Rating |
|---|---|
| $V_{CC}$ to GND | −0.3 V to +4 V |
| $V_{LOGIC}$ to GND | −0.3 V to +4 V |
| Input Voltage | |
| Analog to GND | −0.3 V to $V_{REF}$ + 0.3 V and less than $V_{CC}$ + 0.3 V and less than +4 V |
| Digital to GND | −0.3 V to $V_{LOGIC}$ + 0.3 V and less than +4 V |
| Digital Output Voltage to GND | −0.3 V to $V_{LOGIC}$ + 0.3 V and less than +4 V |
| REFIO Input to GND | −0.3 V to $V_{CC}$ + 0.3 V |
| Input Current to Any Pin Except Supplies | ±10 mA |
| Temperature | |
| Operating Range | −40°C to +125°C |
| Storage Range | −65°C to +150°C |
| Junction | 150°C |
| Pb-Free Soldering Reflow | 260°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$ is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. $\theta_{JC}$ is the junction to case thermal resistance.

**Table 7. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| CP-16-45[1] | 55.4 | 12.7 | °C/W |

[1] Test Condition 1: thermal impedance simulated values are based on JEDEC 2S2P thermal test board four thermal vias. See JEDEC JESDS-51.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charge device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

### *ESD Ratings for AD7383 and AD7384*

**Table 8. AD7383 and AD7384, 16-Lead LFCSP**

| ESD Model | Withstand Threshold (V) | Class |
|---|---|---|
| HBM | ±4000 | 3A |
| FICDM | ±1250 | C3 |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

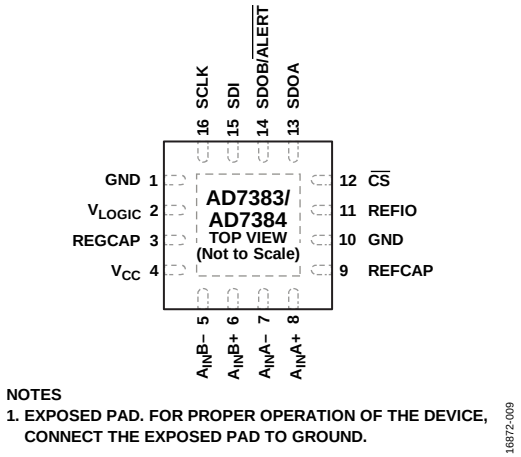


*Figure 7. Pin Configuration*

**Table 9. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 10 | GND | Ground Reference Points. The GND pins are the ground reference points for all circuitry on the device. |
| 2 | $V_{LOGIC}$ | Logic Interface Supply Voltage, 1.65 V to 3.6 V. Decouple $V_{LOGIC}$ to GND with a 1 µF capacitor. |
| 3 | REGCAP | Decoupling Capacitor Pin for Voltage Output from the Internal Regulator. Decouple REGCAP to GND with a 1 µF capacitor. The voltage at REGCAP is 1.9 V typical. |
| 4 | $V_{CC}$ | Power Supply Input Voltage, 3.0 V to 3.6 V. Decouple $V_{CC}$ to GND using a 1 µF capacitor. |
| 5, 6 | $A_{IN}B–$, $A_{IN}B+$ | Analog Inputs of ADC B. The $A_{IN}B–$ and $A_{IN}B+$ analog inputs form a pseudo differential pair. $A_{IN}B–$ is typically connected to $V_{REF}/2$, and the $A_{IN}B+$ voltage range is from 0 V to $V_{REF}$. |
| 7, 8 | $A_{IN}A–$, $A_{IN}A+$ | Analog Inputs of ADC A. The $A_{IN}A–$ and $A_{IN}A+$ analog inputs form a pseudo differential pair. $A_{IN}A–$ is typically connected to $V_{REF}/2$, and the $A_{IN}A+$ voltage range is from 0 V to $V_{REF}$. |
| 9 | REFCAP | Decoupling Capacitor Pin for Band Gap Reference. Decouple REFCAP to GND with a 0.1 µF capacitor. The voltage at REFCAP is 2.5 V typical. |
| 11 | REFIO | Reference Input and Output. The on-chip reference of 2.5 V is available as an output on REFIO for external use if the device is configured accordingly. Alternatively, an external reference of 2.5 V to 3.3 V can be input to REFIO. Set the REFSEL bit in the CONFIGURATION1 register to 1 when using the external reference and apply the REFSEL bit after $V_{CC}$ and $V_{LOGIC}$. Decoupling is required on REFIO for both the internal and external reference options. Apply a 1 µF capacitor from REFIO to GND. |
| 12 | $\overline{CS}$ | Chip Select Input. Active low, logic input. This input provides the dual function of initiating conversions on the AD7383 and the AD7384 and framing the serial data transfer. |
| 13 | SDOA | Serial Data Output A. SDOA functions as a serial data output pin to access the ADC A or ADC B conversion results or data from any of the on-chip registers. |
| 14 | SDOB/$\overline{ALERT}$ | Serial Data Output B/Alert Indication Output. The SDOB/$\overline{ALERT}$ pin can operate as a serial data output pin or an alert indication output.<br>SDOB functions as a serial data output pin to access the ADC B conversion results.<br>$\overline{ALERT}$ operates as an alert pin going low to indicate that a conversion result exceeded a configured threshold. When using $\overline{ALERT}$, set the SDO bit in the CONFIGURATION2 register to 1, and set the ALERT_EN bit to 1 in the CONFIGURATION1 register. |
| 15 | SDI | Serial Data Input. SDI provides the data written to the on-chip control registers. |
| 16 | SCLK | Serial Clock Input. SCLK is for data transfers to and from the ADC. |
| | EPAD | Exposed Pad. For proper operation of the device, connect the exposed pad to ground. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{REF}$ = 2.5 V internal, $V_{CC}$ = 3.6 V, $V_{LOGIC}$ = 2.7 V, $f_{SAMPLE}$ = 4 MSPS, $f_{IN}$ = 1 kHz, and $T_A$ = 25°C, unless otherwise noted.

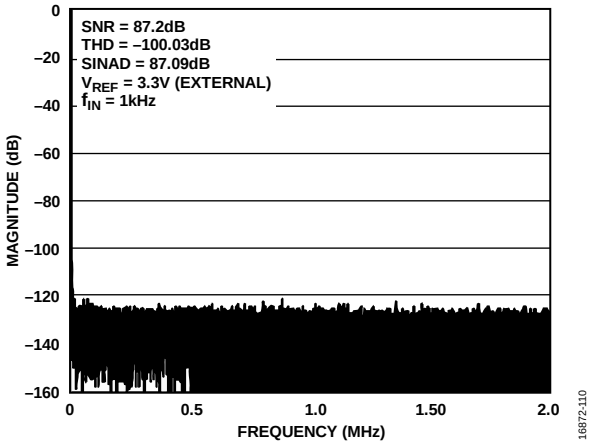


Figure 8. AD7383 Fast Fourier Transform (FFT), $V_{REF}$ = 3.3 V External

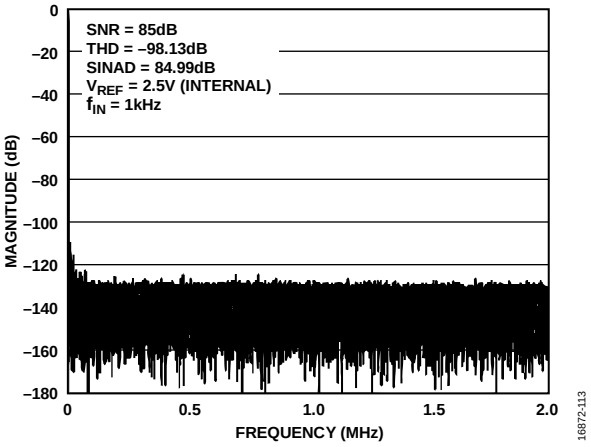


Figure 11. AD7383 FFT, $V_{REF}$ = 2.5 V Internal

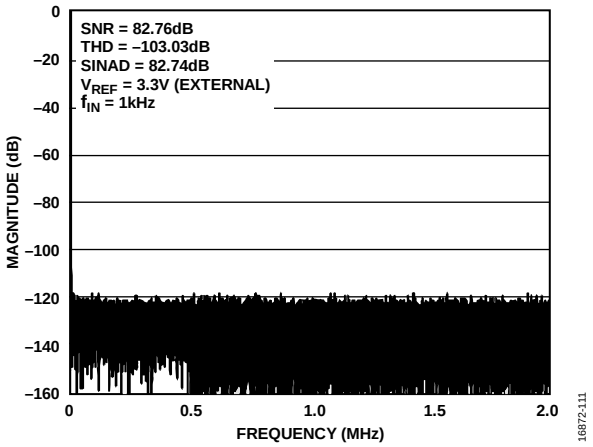


Figure 9. AD7384 FFT, $V_{REF}$ = 3.3 External

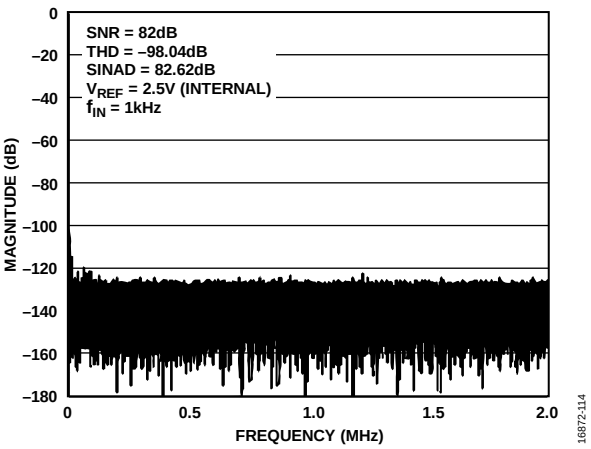


Figure 12. AD7384 FFT, $V_{REF}$ = 2.5 V Internal

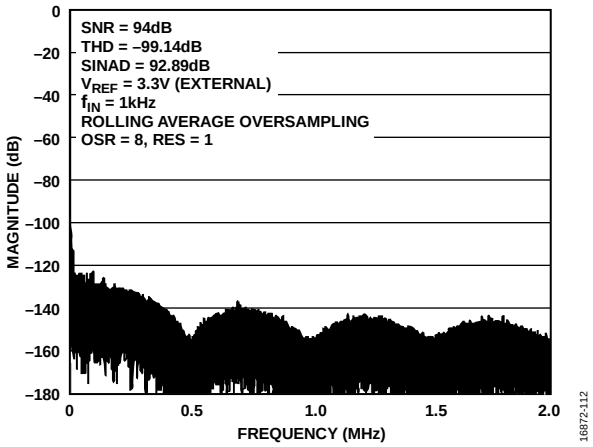


Figure 10. AD7383 FFT, Rolling Average Oversampling

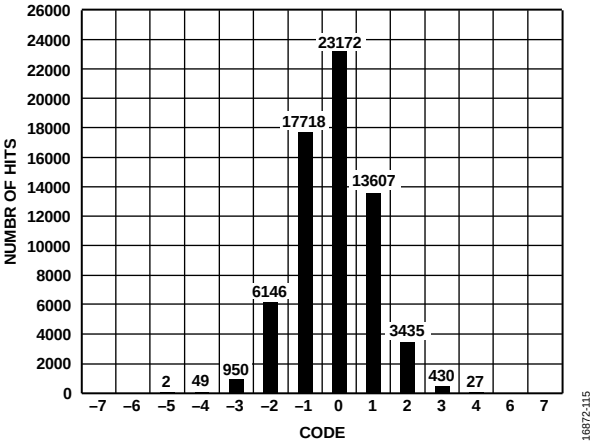


Figure 13. DC Histogram at Code Center

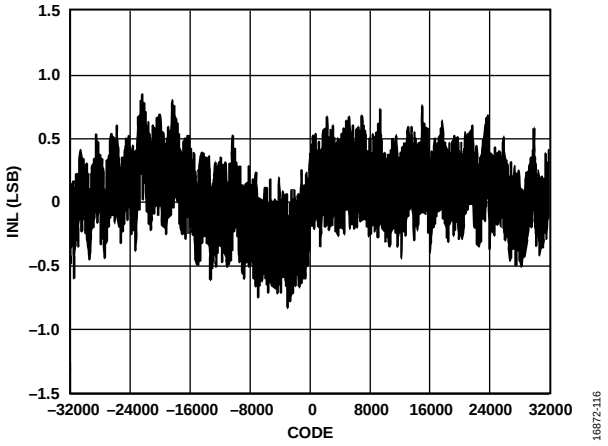


Figure 14. Typical INL Error

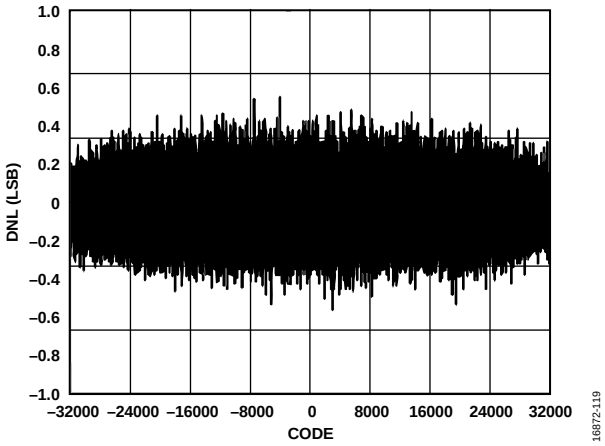


Figure 17. Typical DNL Error

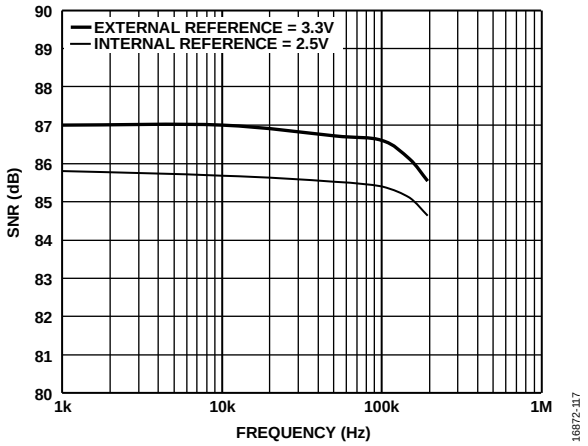


Figure 15. AD7383 SNR vs. Frequency

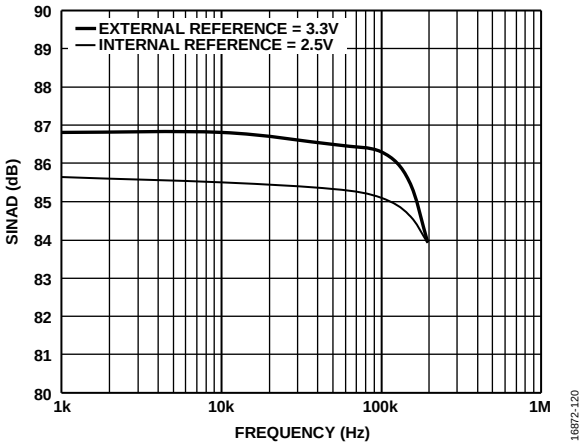


Figure 18. AD7383 SINAD vs. Frequency

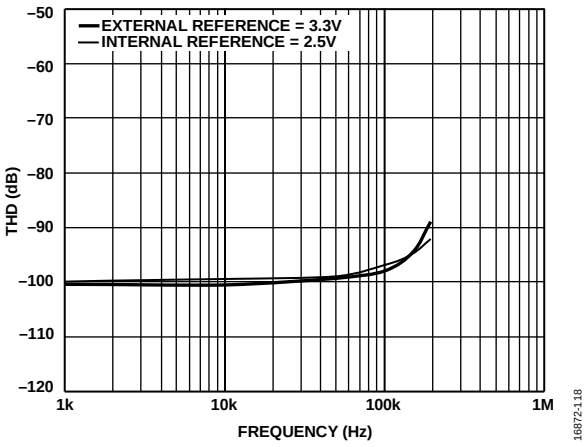


Figure 16. AD7383 THD vs. Frequency

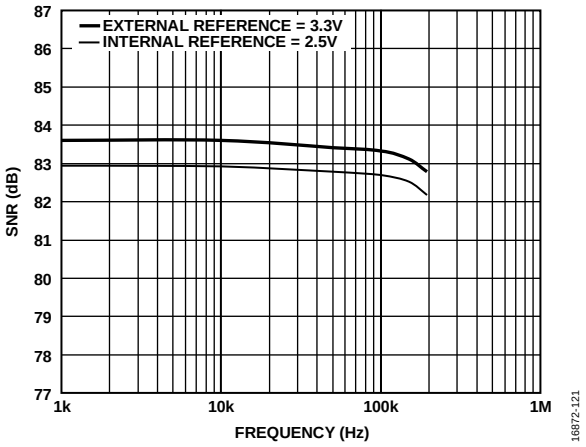


Figure 19. AD7384 SNR vs. Frequency

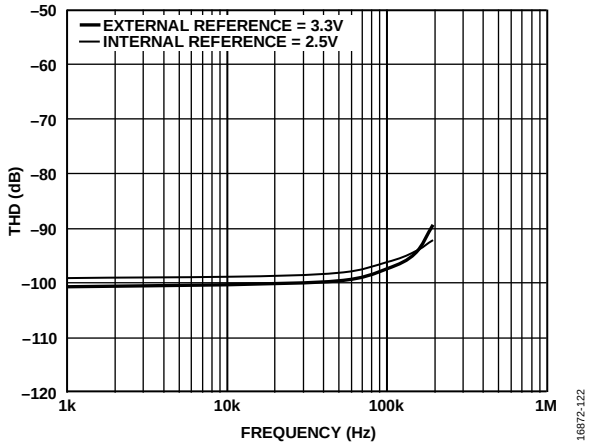


Figure 20. AD7384 THD vs. Frequency

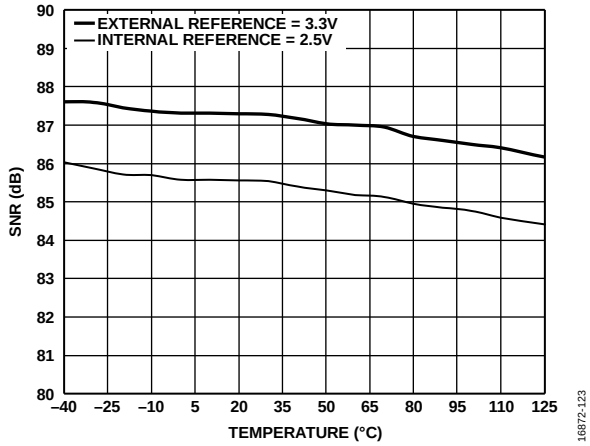


Figure 21. AD7383 SNR vs. Temperature

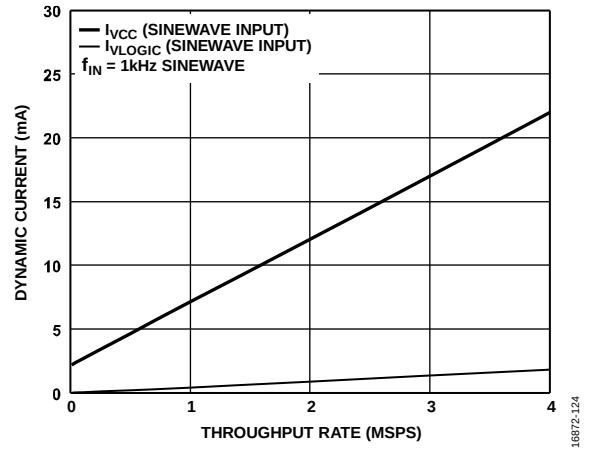


Figure 22. Dynamic Current vs. Throughput Rate

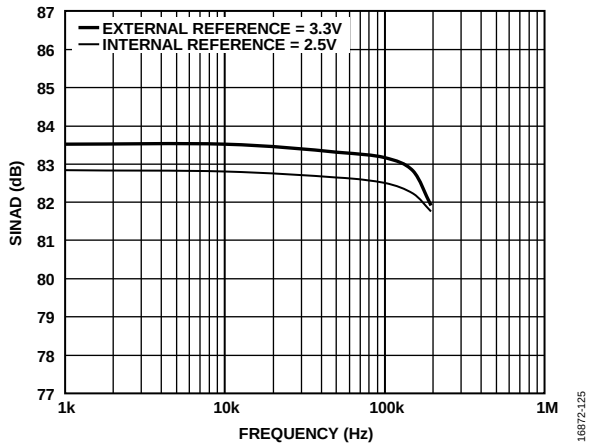


Figure 23. AD7384 SINAD vs. Frequency

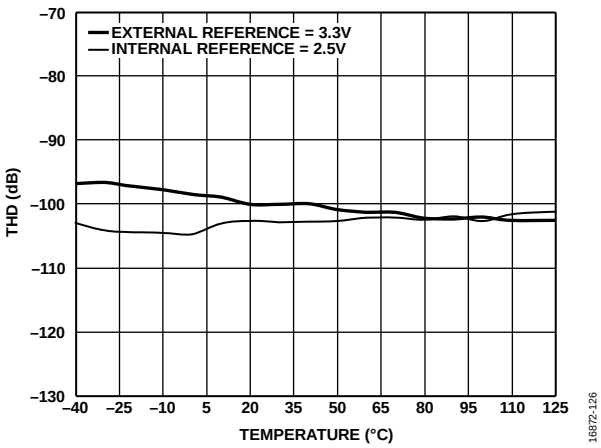


Figure 24. AD7383 THD vs. Temperature

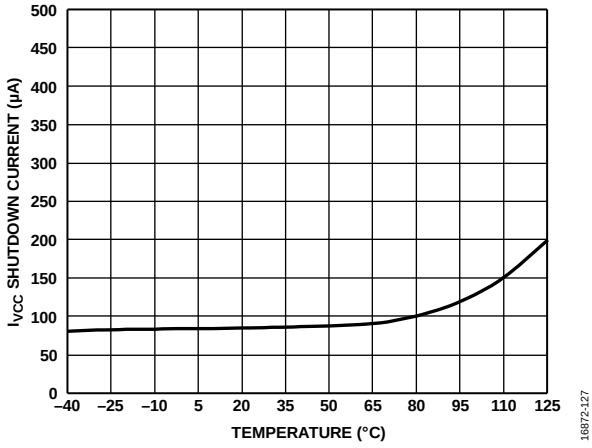


Figure 25. $I_{VCC}$ Shutdown Current vs. Temperature

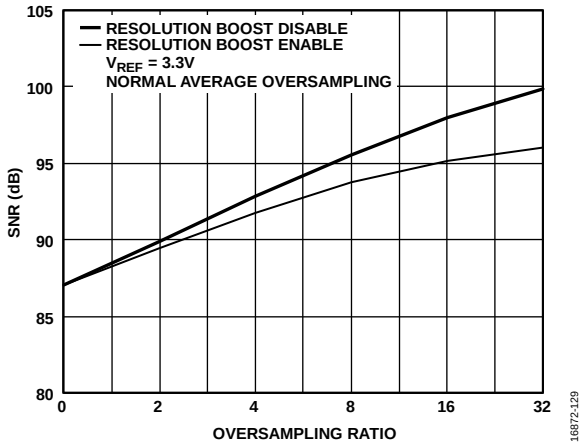


*Figure 26. SNR vs. Oversampling Ratio, Normal Average Oversampling (AD7383)*

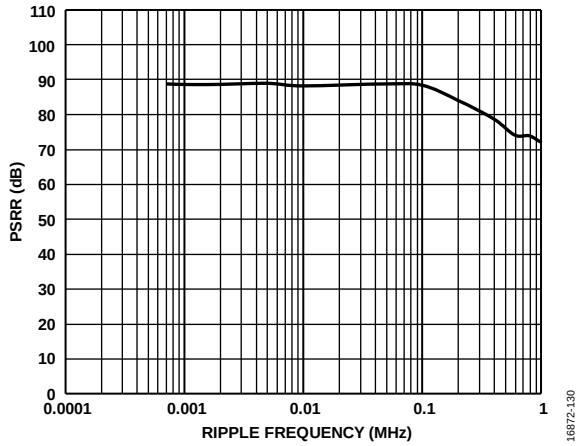


*Figure 27. Power Supply Rejection Ratio (PSRR) vs. Ripple Frequency*

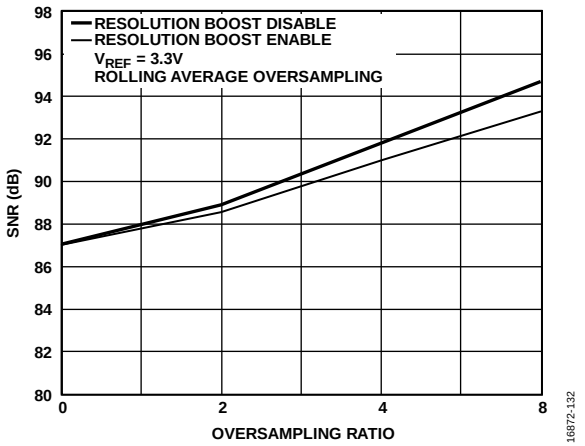


*Figure 28. SNR vs. Oversampling Ratio, Rolling Average Oversampling (AD7383)*

# TERMINOLOGY

**Differential Nonlinearity (DNL)**
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

**Integral Nonlinearity (INL)**
INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

**Gain Error**
The first transition (from 100 … 000 to 100 … 001) occurs at a level ½ LSB above nominal negative full scale. The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

**Gain Error Temperature Drift**
Gain error drift is the gain error change due to a temperature change of 1°C.

**Gain Error Match**
Gain error matching is the difference in negative full-scale error between the input channels and the difference in positive full-scale error between the input channels.

**Offset Error**
Offset error is the difference between the ideal midscale voltage, 0 V, and the actual voltage producing the midscale output code, 0 LSB.

**Offset Temperature Drift**
Offset error drift is the zero error change due to a temperature change of 1°C.

**Offset Error Match**
Offset error match is the difference in zero error between the input channels.

**Signal-to-Noise Ratio (SNR)**
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

**Spurious-Free Dynamic Range (SFDR)**
SFDR is the difference, in dB, between the rms amplitude of the input signal and the peak spurious signal.

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

**Signal-to-(Noise + Distortion) (SINAD)**
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

**Common-Mode Rejection Ratio (CMRR)**
CMRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 200 mV p-p sine wave applied to the common-mode voltage of $A_{IN}x+$ and $A_{IN}x-$ of frequency, f.

$$CMRR\ (dB) = 10log(P_{ADC\_IN}/P_{ADC\_OUT})$$

where:
$P_{ADC\_IN}$ is the common-mode power at the frequency, f, applied to the $A_{IN}x+$ and $A_{IN}x-$ inputs.
$P_{ADC\_OUT}$ is the power at the frequency, f, in the ADC output.

**Aperture Delay**
Aperture delay is the measure of the acquisition performance and is the time between the falling edge of the $\overline{CS}$ input and when the input signal is held for a conversion.

**Aperture Delay Match**
Aperture delay match is the difference of the aperture delay between ADC A and ADC B.

**Aperture Jitter**
Aperture jitter is the variation in aperture delay.

# THEORY OF OPERATION

## CIRCUIT INFORMATION

The 16-bit AD7383 and the 14-bit AD7384 are high speed, dual, simultaneous sampling, pseudo differential, SAR ADCs. The AD7383 and the AD7384 operate from a 3.0 V to 3.6 V power supply and feature throughput rates up to 4 MSPS.

The AD7383 and the AD7384 contain two SAR ADCs and a serial peripheral interface (SPI) with two separate data output pins. The devices are housed in a 16-lead LFCSP, offering the user considerable space-saving advantages over alternative solutions.

Data is accessed from the devices via the SPI. The SPI can operate with one or two serial output(s). The AD7383 and the AD7384 have an on-chip 2.5 V internal reference, $V_{REF}$. If an external reference is required, disable the internal reference, supply a reference value that ranges from 2.5 V to 3.3 V, and set the REFSEL bit in the CONFIGURATION1 register to 1. If the internal reference is used elsewhere in the system, buffer the reference output. The pseudo differential analog input range for the AD7383 and the AD7384 is the common mode voltage ($V_{CM}$) ± $V_{REF}$/2.

The AD7383 and the AD7384 feature an on-chip oversampling block to improve performance. Normal average and rolling average oversampling modes and power-down options that allow power saving between conversions are also available. Configuration of the devices is implemented via the standard SPI (see the Interface section).

## CONVERTER OPERATION

The AD7383 and the AD7384 have two SAR ADCs, each based around two capacitive digital-to-analog converters (DACs). Figure 29 and Figure 30 show the simplified schematics of one of these ADCs in acquisition and conversion phases, respectively. The ADC comprises control logic, an SAR, and two capacitive DACs. In Figure 29 (the acquisition phase), SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor ($C_S$) arrays can acquire the pseudo differential signal on the input.

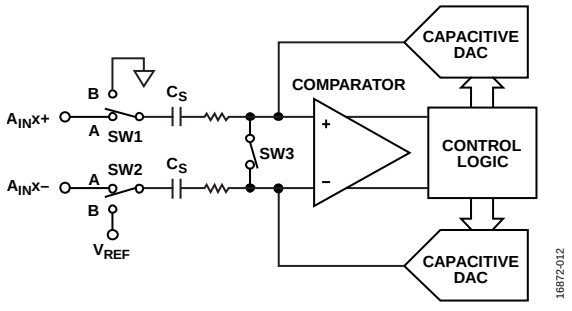


*Figure 29. ADC Acquisition Phase*

When the ADC starts a conversion (see Figure 30), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected when the conversion begins. The control logic and charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion completes. The control logic generates the ADC output code. The output impedances of the sources driving the $A_{IN}x+$ and $A_{IN}x-$ pins must be matched. Otherwise, the two inputs have different settling times, which results in errors.

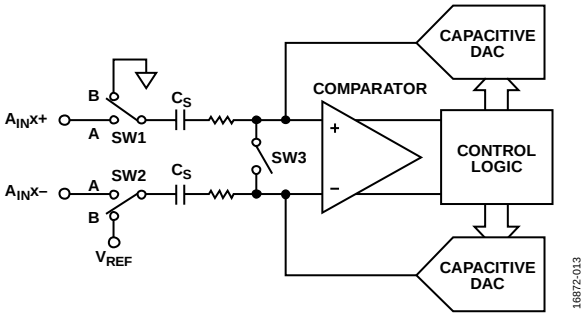


*Figure 30. ADC Conversion Phase*

## ANALOG INPUT STRUCTURE

Figure 31 shows the equivalent analog input circuit of the AD7383 and the AD7384. The four diodes (D) provide ESD protection for the analog inputs. Ensure that the analog input signals do not exceed the supply rails by more than 300 mV. Exceeding the limit causes these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the devices.

The C1 capacitors in Figure 31 are typically 3 pF and can primarily be attributed to pin capacitance. The R1 resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 200 Ω. The C2 capacitors are sampling capacitors of the ADC with a capacitance of 15 pF typically.

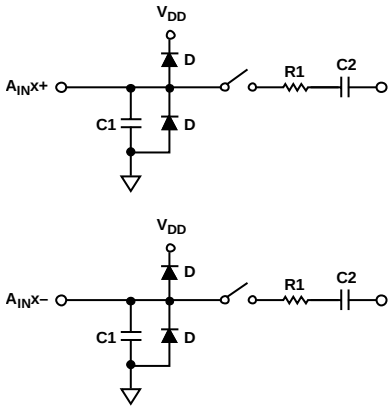


*Figure 31. Equivalent Analog Input Circuit, Conversion Phase—Switches Open, Track Phase—Switches Closed*

## ADC TRANSFER FUNCTION

The AD7383 and the AD7384 can use a typical 2.5 V to 3.3 V $V_{REF}$. The AD7383 and the AD7384 convert the differential voltage of the analog inputs ($A_{IN}A+$, $A_{IN}A-$, $A_{IN}B+$, and $A_{IN}B-$) into a digital output.

The conversion result is MSB first, twos complement. The LSB size is $V_{REF}/2^N$, where N is the ADC resolution. The ADC resolution is determined by the resolution of the device chosen, and if resolution boost mode is enabled. Table 10 outlines the LSB size expressed in μV for different resolutions and reference voltage options.

The ideal transfer characteristics for the AD7383 and the AD7384 are shown in Figure 32.

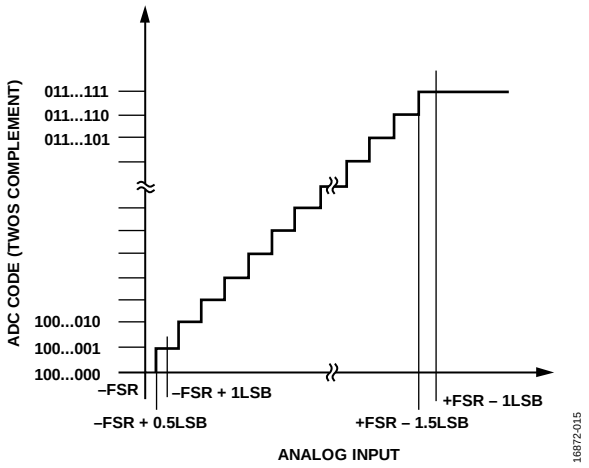


*Figure 32. ADC Ideal Transfer Function (FSR = Full-Scale Range)*

**Table 10. LSB Size**

| Resolution (Bit) | 2.5 V Reference (μV) | 3.3 V Reference (μV) |
|---|---|---|
| 14 | 152.6 | 201.4 |
| 16 | 38.1 | 50.3 |
| 18 | 9.5 | 12.6 |

# APPLICATIONS INFORMATION

Figure 33 shows an example of the typical connection diagram for the AD7383 and the AD7384. Decouple the $V_{CC}$, $V_{LOGIC}$, REGCAP, and REFIO pins with suitable decoupling capacitors as shown in Figure 33.

The exposed pad is a ground reference point for circuitry on the devices and must be connected to the PCB ground.

Place an RC filter on the analog inputs to ensure optimal performance is achieved. For a typical application, it is recommended that R = 33 Ω and C1 = 68 pF.

The performance of the AD7383 and the AD7384 devices may be impacted by noise on the digital interface. This impact is dependent on the on-board layout and design. Keep a minimal distance between the digital line to the digital interface or place a 100 Ω resistor in series and close to the SDOA pin and the SDOB/$\overline{\text{ALERT}}$ pin to reduce noise from the digital interface coupling of the AD7383 and the AD7384.

The two pseudo differential ADC channels of the AD7383 and the AD7384 can accept an input voltage range from 0 V to $V_{REF}$ on $A_{IN}A+$ and $A_{IN}B+$, and a $V_{REF}/2$ voltage on $A_{IN}A-$ and $A_{IN}B-$. The $A_{IN}A+$, $A_{IN}B+$, $A_{IN}A-$, and $A_{IN}B-$ analog input pins can be driven with an amplifier. Table 11 lists the recommended driver amplifiers that best fit and add value to the application. The AD7383 and the AD7384 have a buffered internal 2.5 V reference that is accessed via the REFIO pin. The buffered internal 2.5 V reference must use an external buffer, like the ADA4807-2, before connecting the reference to the external circuitry. The AD7383 and AD7384 have an option to use an ultralow noise, high accuracy voltage reference as an external voltage source ranging from 2.5 V to 3.3 V, such as the ADR4533 and ADR4525.

## POWER SUPPLY

The typical application circuit in Figure 33 can be powered by a single 5 V voltage source (V+) that supplies the entire signal chain. The 5 V supply can come from a low noise, CMOS low dropout (LDO) regulator (ADP7105). The driver amplifier supply is supplied by the +5 V (V+) and −2.5 V negative supply rail (V−), which is derived from the inverter (ADM660). The inverter converts the +5 V to −5 V and supplies the voltage to the ADP7182 low noise voltage regulator to output the −2.5 V. The two independent supplies of the AD7383 and the AD7384, $V_{CC}$ and $V_{LOGIC}$, that supply the analog circuitry and digital interface, respectively, can be supplied by a low quiescent current LDO regulator, such as the ADP166. The ADP166 is a suitable supply with a fixed output voltage range from 1.2 V to 3.3 V for typical $V_{CC}$ and $V_{LOGIC}$ levels. Decouple both the $V_{CC}$ supply and the $V_{LOGIC}$ supply separately with a 1 µF capacitor. Additionally, there is an internal LDO regulator that supplies the AD7383 and the AD7384. The on-chip regulator provides a 1.9 V supply for internal use on the device only. Decouple the REGCAP pin with a 1 µF capacitor connected to GND.

### *Power-Up*

The AD7383 and the AD7384 are robust to power supply sequencing. $V_{CC}$ and $V_{LOGIC}$ can be applied in any sequence. Apply an external reference after $V_{CC}$ and $V_{LOGIC}$ are applied.

The AD7383 and the AD7384 require a $t_{POWERUP}$ time from applying $V_{CC}$ and $V_{LOGIC}$ until the ADC conversion results are stable. Applying $\overline{\text{CS}}$ pulses or interfacing with the AD7383 and the AD7384 prior to the setup time elapsing does not have a negative impact on ADC operation. Conversion results are not guaranteed to meet data sheet specifications during this time, however, and must be ignored.

**Table 11. Signal Chain Components**

| Companion Parts | Part Name | Description | Typical Application |
|---|---|---|---|
| ADC Driver | ADA4896-2 | 1 nV/√Hz, rail-to-rail output amplifier | Precision, low noise, high frequency |
| | ADA4940-2 | Ultra low power, full differential, low distortion | Precision, low density, low power |
| | ADA4807-2 | 1 mA, rail-to-rail output amplifier | Precision, low power, high frequency |
| | LTC6227 | Low distortion rail-to-rail output op amp | Precision, low noise, high frequency |
| External Reference | ADR4525 | Ultralow noise, high accuracy 2.5 V voltage reference | 2.5 V reference voltage |
| | ADR4533 | Ultralow noise, high accuracy 3.3 V voltage reference | 3.3 V reference voltage |
| LDO | ADP166 | Very low quiescent, 150 mA, LDO regulator | 3.0 V to 3.6 V supply for $V_{CC}$ and $V_{LOGIC}$ |

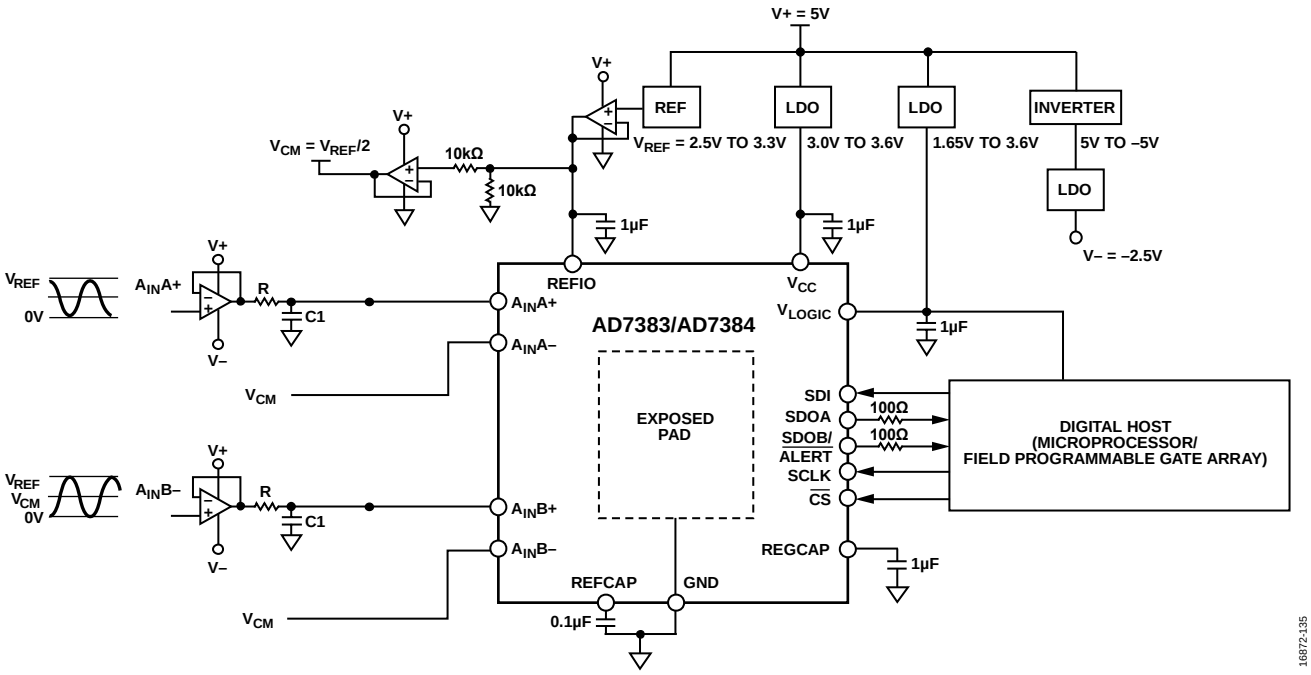


*Figure 33. Typical Application Circuit*

# MODES OF OPERATION

The AD7383 and the AD7384 have several on-chip configuration registers for controlling the operational mode of the device.

## OVERSAMPLING

Oversampling is a common method used in analog electronics to improve the accuracy of the ADC result. Multiple samples of the analog input are captured and averaged to reduce the noise component from the quantization noise and the thermal noise (kTC) of the ADC. The AD7383 and the AD7384 offer an oversampling function on chip and have two user configurable oversampling modes, normal average and rolling average.

The oversampling functionality is configured by programming the OS_MODE bit, Bit 9, and the OSR bits, Bits[8:6], in the CONFIGURATION1 register.

### *Normal Average Oversampling*

Normal average oversampling mode can be used in applications where slower output data rates are allowable and where higher SNR or dynamic range is required. Normal average oversampling involves taking a number of samples, adding the samples together, and dividing the result by the number of samples taken. This result is then output from the AD7383 or the AD7384. The sample data is cleared after the process completes.

Normal average oversampling mode is configured by setting the OS_MODE bit to Logic 0 and having a valid nonzero value in the OSR bits. Writing to the OSR bits has a two cycle latency before the register gets updated. The oversampling ratio of the digital filter is controlled using the oversampling bits, OSR, which provides the oversampling bit decoding to select the different oversample rates (see Table 12 and Table 13). The output result is decimated to 16-bit resolution for the AD7383 and 14-bit resolution for the AD7384. If additional resolution is required, configure the resolution boost bit in the CONFIGURATION1 register. See the Resolution Boost section for more details.

The number of samples, n, defined by the OSR bits are taken, added together, and the result is divided by n. The initial ADC conversion is initiated by the falling edge of $\overline{CS}$ and the AD7383 and the AD7384 control all subsequent samples in the oversampling sequence internally. The sampling rate of the additional n samples is 3 MSPS. The oversampled conversion result is ready for read back on the next serial interface access. After the technique is applied, the sample data used in the calculation is discarded. This process is repeated every time the application needs a new conversion result and is initiated by the falling edge of $\overline{CS}$.

As the output data rate is reduced by the oversampling ratio, the SPI SCLK frequency required to transmit the data is also reduced accordingly.

**Table 12. AD7383 Normal Average Oversampling Performance Overview**

| | | SNR (dB Typical) | | | | |
|---|---|---|---|---|---|---|
| | | $V_{REF}$ = 2.5 V | | $V_{REF}$ = 3.3 V | | |
| OSR, Bits[8:6] | Oversampling Ratio | RES = 0 | RES = 1 | RES = 0 | RES = 1 | Output Data Rate (kSPS Maximum) |
| 000 | Disabled | 85.4 | 85.4 | 87.1 | 87.1 | 4000 |
| 001 | 2 | 87.9 | 88.3 | 89.4 | 89.9 | 1500 |
| 010 | 4 | 90.5 | 91.3 | 91.8 | 92.8 | 750 |
| 011 | 8 | 92.7 | 94.1 | 93.7 | 95.5 | 375 |
| 100 | 16 | 94.4 | 96.6 | 95.2 | 97.9 | 187.5 |
| 101 | 32 | 95.6 | 98.4 | 96 | 99.8 | 93.75 |

**Table 13. AD7384 Normal Average Oversampling Performance Overview**

| | | SNR (dB Typical) | | |
|---|---|---|---|---|
| OSR, Bits[8:6] | Oversampling Ratio | RES = 0 | RES = 1 | Output Data Rate (kSPS Maximum) |
| 000 | Disabled | 82.8 | 82.8 | 4000 |
| 001 | 2 | 83.4 | 85.7 | 1500 |
| 010 | 4 | 84.3 | 88.7 | 750 |
| 011 | 8 | 85.04 | 90.9 | 375 |
| 100 | 16 | 85.5 | 93.0 | 187.5 |
| 101 | 32 | 85.7 | 94.5 | 93.75 |

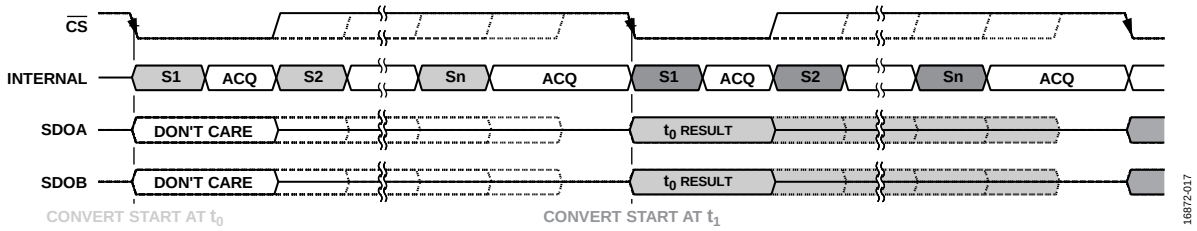


*Figure 34. Normal Average Oversampling Operation*

### *Rolling Average Oversampling*

Rolling average oversampling mode can be used in applications where higher output data rates are required and where higher SNR or dynamic range is required. Rolling average oversampling involves taking a number of samples, adding the samples together, and dividing the result by the number of samples taken. This result is then output from the AD7383 or the AD7384. The sample data is not cleared after the process completes. The rolling average oversampling mode uses a first in, first out (FIFO) buffer of the most recent samples in the averaging calculation, allowing the ADC throughput rate and output data rate to stay the same.

Rolling average oversampling mode is configured by setting the OS_MODE bit to Logic 1 and having a valid nonzero value in the OSR bits. The oversampling ratio of the digital filter is controlled using the oversampling bits, OSR (see Table 14 and Table 15). The output result is decimated to 16-bit resolution for the AD7383 and 14-bit resolution for the AD7384. If additional resolution is required, configure the resolution boost bit in the CONFIGURATION1 register. See the Resolution Boost section for further details.

In rolling average oversampling mode, all ADC conversions are controlled and initiated by the falling edge of $\overline{CS}$. After a conversion is complete, the result is loaded into the FIFO. The FIFO length is 8, regardless of the oversampling ratio set. The FIFO is filled on the first conversion after a power-on reset, the first conversion after a software controlled hard or soft reset, or the first conversion after the REFSEL bit is toggled. A new conversion result is shifted into the FIFO on completion of every ADC conversion, regardless of the status of the OSR bits and the OS_MODE bit. This conversion allows a seamless transition from no oversampling to rolling average oversampling or different rolling average oversampling ratios without waiting for the FIFO to fill.

The number of samples, n, defined by the OSR bits are taken from the FIFO, added together, and the result is divided by n. The time between $\overline{CS}$ falling edges is the cycle time, which can be controlled by the user, depending on the required data output rate.

## RESOLUTION BOOST

The default conversion result output data size for the AD7383 is 16 bits and for the AD7384 is 14 bits. When the on-chip oversampling function is enabled, the performance of the ADC can exceed the 16-bit level for the AD7383 or the 14-bit level for the AD7384. To accommodate the performance boost achievable, it is possible to enable an additional two bits of resolution. If the RES bit in the CONFIGURATION1 register is set to Logic 1, and the AD7383 and the AD7384 are in a valid oversampling mode, the conversion result size for the AD7383 is 18 bits and for the AD7384 is 16 bits. In this mode, 18 SCLKs are required to propagate the data for the AD7383, and 16 SCLKs are required for the AD7384.

**Table 14. AD7383 Rolling Average Oversampling Performance Overview**

| | | SNR (dB Typical) | | | | |
|---|---|---|---|---|---|---|
| | | $V_{REF}$ = 2.5 V | | $V_{REF}$ = 3.3 V | | |
| OSR, Bits[8:6] | Oversampling Ratio | RES = 0 | RES = 1 | RES = 0 | RES = 1 | Output Data Rate (kSPS Maximum) |
| 000 | Disabled | 85.4 | 85.4 | 87.0 | 87.0 | 4000 |
| 001 | 2 | 87.3 | 87.5 | 88.5 | 88.9 | 4000 |
| 010 | 4 | 89.9 | 90.5 | 91.0 | 91.8 | 4000 |
| 011 | 8 | 92.2 | 93.3 | 93.2 | 94.6 | 4000 |

**Table 15. AD7384 Rolling Average Oversampling Performance Overview**

| | | SNR (dB Typical) | | |
|---|---|---|---|---|
| OSR, Bits[8:6] | Oversampling Ratio | RES = 0 | RES = 1 | Output Data Rate (kSPS Maximum) |
| 000 | Disabled | 82.8 | 82.8 | 4000 |
| 001 | 2 | 83.2 | 85.3 | 4000 |
| 010 | 4 | 84.2 | 88.3 | 4000 |
| 011 | 8 | 84.9 | 90.6 | 4000 |

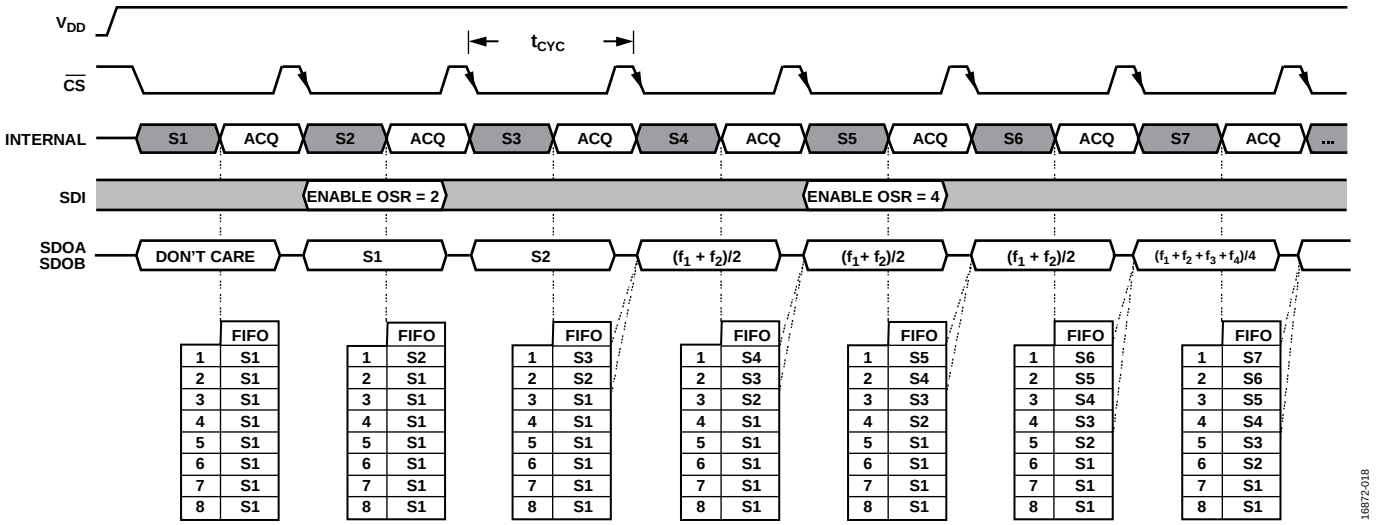


*Figure 35. Rolling Average Oversampling Mode Configuration*

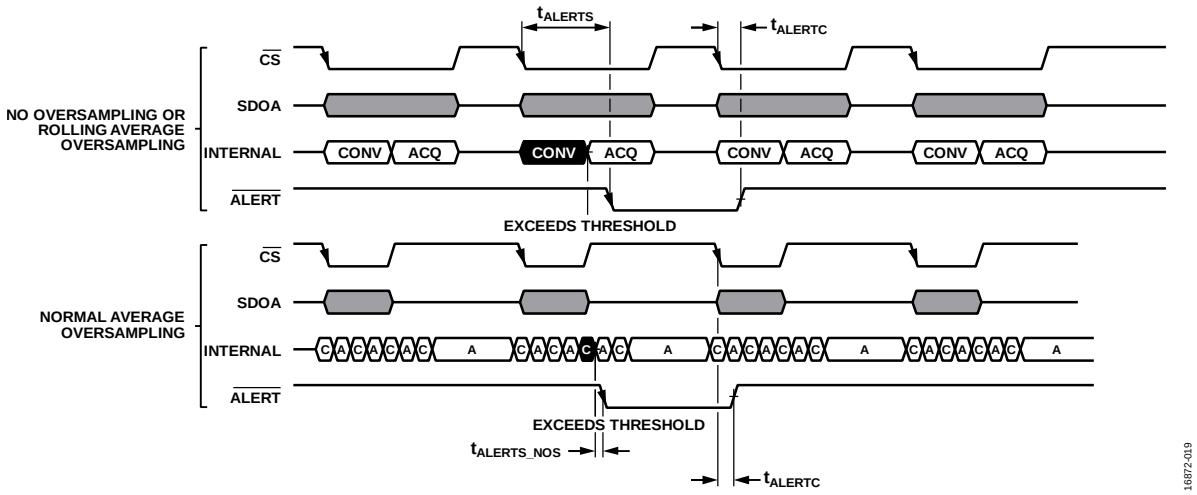


*Figure 36. Alert Operation*

## ALERT

The alert functionality is an out of range indicator and can be used as an early indicator of an out of bounds conversion result. An alert event triggers when the conversion result value register exceeds the alert high limit value in the ALERT_HIGH_THRESHOLD register or falls below the alert low limit value in the ALERT_LOW_THRESHOLD register. The ALERT_HIGH_THRESHOLD register and ALERT_LOW_THRESHOLD register are common to all ADCs. When setting the threshold limits, the alert high threshold must always be greater than the alert low threshold. Detailed alert information is accessible in the $\overline{\text{ALERT}}$ register.

The $\overline{\text{ALERT}}$ register contains two status bits per ADC, one corresponding to the high limit, and the other to the low limit. A logical OR of alert signals for all ADCs creates a common alert value. This value can be configured to drive out on the $\overline{\text{ALERT}}$ function of the SDOB/$\overline{\text{ALERT}}$ pin. The SDOB/$\overline{\text{ALERT}}$ pin is configured as $\overline{\text{ALERT}}$ by configuring the following bits in the CONFIGURATION1 and CONFIGURATION2 registers:

- Set the SDO bit to 1.
- Set the ALERT_EN bit to 1.
- Set a valid value to the ALERT_HIGH_THRESHOLD register and the ALERT_LOW_THRESHOLD register.

The alert indication function is available in oversampling, both rolling average and normal average, and in nonoversampling modes.

The $\overline{\text{ALERT}}$ function of the SDOB/$\overline{\text{ALERT}}$ pin gets updated at the end of the conversion. The alert indication status bits in the $\overline{\text{ALERT}}$ register get updated as well and must be read before the end of the next conversion. The $\overline{\text{ALERT}}$ function of the SDOB/$\overline{\text{ALERT}}$ pin is cleared with a falling edge of $\overline{\text{CS}}$. Issuing a software reset also clears the alert status in the $\overline{\text{ALERT}}$ register.

## POWER MODES

The AD7383 and the AD7384 have two power modes, normal and shutdown. These modes of operation provide flexible power management options, allowing optimization of the power dissipation and throughput rate ratio for different application requirements.

Program the PMODE bit in the CONFIGURATION1 register to configure the power modes in the AD7383 and the AD7384. Set the PMODE bit to Logic 0 for normal mode and Logic 1 for shutdown mode.

### *Normal Mode*

Keep the AD7383 and the AD7384 in normal mode to achieve the fastest throughput rate. All blocks within the AD7383 and the AD7384 remain fully powered at all times, and an ADC conversion can be initiated by a falling edge of $\overline{CS}$, when required. When the AD7383 and the AD7384 are not converting, the devices are in static mode and power consumption is automatically reduced. Additional current is required to perform a conversion. Therefore, power consumption on the AD7383 and the AD7384 scales with throughput.

### *Shutdown Mode*

When slower throughput rates and lower power consumption are required, use shutdown mode by either powering down the ADC between each conversion, or by performing a series of conversions at a high throughput rate and then powering down the ADC for a relatively long duration between these burst conversions. When the AD7383 and the AD7384 are in shutdown mode, all analog circuitry powers down, including the internal reference, if enabled. The SPI remains active during shutdown mode to allow the AD7383 and the AD7384 to exit shutdown mode.

To enter shutdown mode, write to the PMODE bit in the CONFIGURATION1 register. The AD7383 and the AD7384 shut down and current consumption reduces.

To exit shutdown mode and return to normal mode, set the PMODE bit in the CONFIGURATION1 register to Logic 0. All register configuration settings remain unchanged entering or exiting shutdown mode. After exiting shutdown mode, allow sufficient time for the circuitry to turn on before starting a conversion. If the internal reference is enabled, allow the reference to settle for accurate conversions to happen.

## INTERNAL AND EXTERNAL REFERENCE

The AD7383 and the AD7384 have a buffered 2.5 V internal reference primarily used for internal device operation. When using the buffered internal 2.5 V reference externally, the reference must use an external buffer before connecting to the external circuitry. Alternatively, if a more accurate reference or higher dynamic range is required, an external reference can be supplied. An externally supplied reference can range from 2.5 V to 3.3 V.

Reference selection, internal or external, is configured by the REFSEL bit in the CONFIGURATION1 register. If the REFSEL bit is set to 0, the internal reference buffer is enabled. If the REFSEL bit is set to 1, the internal reference buffer is disabled. If an external reference is preferred, set the REFSEL bit to 1 and supply an external reference to the REFIO pin.

## SOFTWARE RESET

The AD7383 and the AD7384 have two reset modes, a soft reset and a hard reset. To initiate a reset, write to the RESET bits, Bits[7:0], in the CONFIGURATION2 register.

A soft reset maintains the contents of the configurable registers but refreshes the interface and the ADC blocks. Any internal state machines are reinitialized, and the oversampling block and FIFO are flushed. The $\overline{ALERT}$ register is then cleared. The reference and LDO remain powered.

A hard reset, in addition to the blocks reset by a soft reset, resets all user registers to default status, resets the reference buffer, and resets the internal oscillator block.

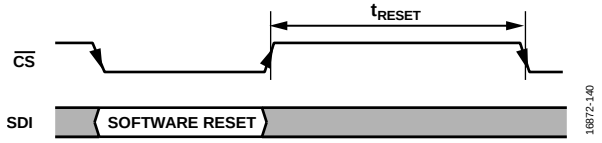


*Figure 37. Software Reset Operation*

## DIAGNOSTIC SELF TEST

The AD7383 and the AD7384 run a diagnostic self test after a power-on reset or after a software hard reset to ensure the proper configuration is loaded into the device.

The result of the self test is displayed in the SETUP_F bit in the $\overline{ALERT}$ register. If the SETUP_F bit is set to Logic 1, the diagnostic self test fails. If the self test fails, perform a software hard reset to reset the AD7383 and the AD7384 registers to the default status.

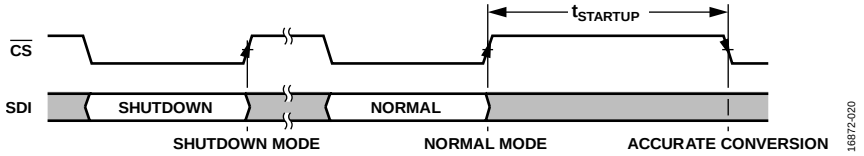


*Figure 38. Shutdown Mode Operation*

# INTERFACE

The interface to the AD7383 and the AD7384 is via an SPI. The interface consists of the $\overline{CS}$, SCLK, SDOA, SDOB, and SDI pins.

The $\overline{CS}$ signal frames a serial data transfer and initiates an ADC conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, at which point, the analog input is sampled, and the bus is taken out of three-state.

The SCLK signal synchronizes data in and out of the devices via the SDOA, SDOB, and SDI signals. A minimum of 16 SCLKs are required for a write to or read from a register. The minimum number of SCLKs for a conversion read is dependent on the resolution of the devices and the configuration settings (see Table 16).

The ADC conversion operation is driven internally by an on-board oscillator and is independent of the SCLK signal.

The AD7383 and the AD7384 have two serial output signals, SDOA and SDOB. To achieve the highest throughput of the devices, use both SDOA and SDOB, 2-wire mode, to read conversion results. If a reduced throughput is required or oversampling is used, it is possible to use 1-wire mode, SDOA signal only, for reading conversion results. Programming the SDO bit in the CONFIGURATION2 register configures 2-wire mode or 1-wire mode.

Configuring a cyclic redundancy check (CRC) operation for SPI reads or SPI writes alters the operation of the interface. Consult the relevant CRC Read, CRC Write, and CRC Polynomial sections to ensure proper operation.

## READING CONVERSION RESULTS

The $\overline{CS}$ signal initiates the conversion process. A high to low transition on the $\overline{CS}$ signal initiates a simultaneous conversion of both ADCs, ADC A and ADC B. The AD7383 and the AD7384 have a one cycle readback latency. Therefore, the conversion results are available on the next SPI access. Take the $\overline{CS}$ signal low, and the conversion result clocks out on the serial output pins. The next conversion also initiates at this point.

The conversion result shifts out of the device as a 16-bit result for the AD7383 and a 14-bit result for the AD7384. The MSB of the conversion result shifts out on the $\overline{CS}$ falling edge. The remaining data shifts out of the device under the control of the SCLK input. The data shifts out on the rising edge of the SCLK, and the data bits are valid on both the falling edge and the rising edge. After the final SCLK falling edge, take $\overline{CS}$ high again to return the SDOx pins to a high impedance state.

The number of SCLK cycles to propagate the conversion results on the SDOx pins is dependent on the serial mode of operation configured and if resolution boost mode is enabled (see Figure 39 and Table 16 for details). If CRC reading is enabled, this reading requires additional SCLK pulses to propagate the CRC information (see the CRC section for more details).

As the $\overline{CS}$ signal initiates a conversion and frames the data, any data access must be completed within a single frame.

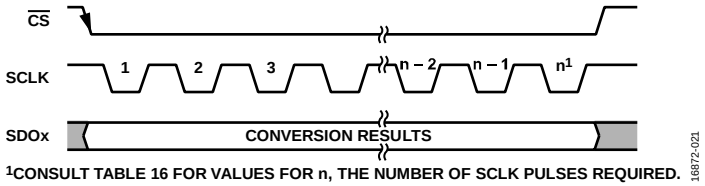


*Figure 39. Reading Conversion Results*

**Table 16. Number of SCLKs, n, Required for Reading Conversion Results**

| Interface Configuration | Resolution Boost Mode | CRC Read | AD7383 SCLKs | AD7384 SCLKs |
|---|---|---|---|---|
| 2-Wire | Disabled | Disabled | 16 | 14 |
| | | Enabled | 24 | 22 |
| | Enabled | Disabled | 18 | 16 |
| | | Enabled | 26 | 24 |
| 1-Wire | Disabled | Disabled | 32 | 28 |
| | | Enabled | 40 | 36 |
| | Enabled | Disabled | 36 | 32 |
| | | Enabled | 44 | 40 |

### Serial 2-Wire Mode

Configure 2-wire mode by setting the SDO bit in the CONFIGURATION1 register to 0. In 2-wire mode, the conversion result for ADC A is output on the SDOA pin, and the conversion result for ADC B is output on the SDOB/ALERT pin (see Figure 40).

### Serial 1-Wire Mode

In applications where slower throughput rates are allowed, or normal average oversampling is used, the serial interface can be configured to operate in 1-wire mode. In 1-wire mode, the conversion results from ADC A and ADC B are output on the serial output, SDOA. Additional SCLK cycles are required to propagate all of the data. The ADC A data is output first, followed by the ADC B conversion results (see Figure 41).

### Resolution Boost Mode

The default resolution and output data size for the AD7383 is 16 bits and for the AD7384 is 14 bits. Enabling the on-chip oversampling function reduces noise and improves device performance. To accommodate the performance boost achievable, it is possible to enable an additional two bits of resolution in the conversion output data. If the RES bit in the CONFIGURATION1 register is set to Logic 1, and the AD7383 and the AD7384 are in a valid oversampling mode, the conversion result size for the AD7383 is 18 bits and for the AD7384 is 16 bits.

When the resolution boost mode is enabled, 18 SCLKs are required for the AD7383 and 16 SCLKs are required for the AD7384 to propagate the data.

## LOW LATENCY READBACK

The interface on the AD7383 and the AD7384 has a one cycle latency, as shown in Figure 42. For applications that operate at lower throughput rates, the latency of reading the conversion result can be reduced. When the conversion time elapses, a second $\overline{CS}$ pulse after the initial $\overline{CS}$ pulse that initiates the conversion can readback the conversion result. This operation is shown in Figure 42.

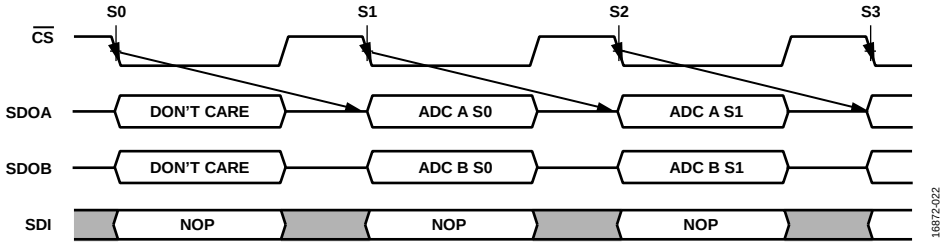


Figure 40. Reading Conversion Results for 2-Wire Mode

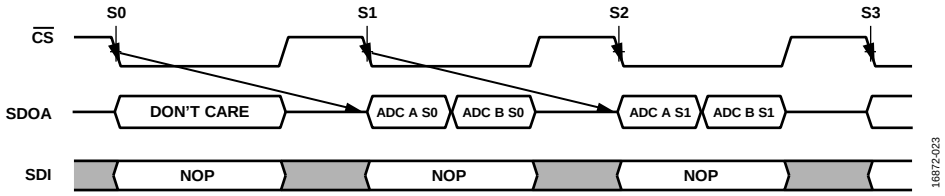


Figure 41. Reading Conversion Results for 1-Wire Mode

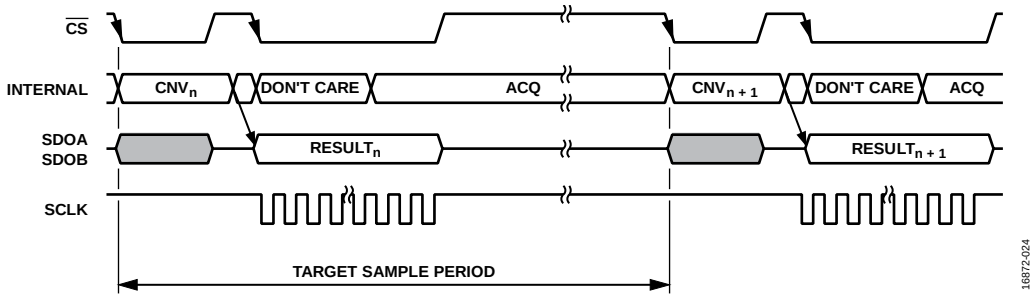


Figure 42. Low Throughput Low Latency

## READING FROM DEVICE REGISTERS

All of the registers in the AD7383 and the AD7384 can be read over the SPI. To perform a register read, issue a register read command followed by an additional SPI command that can be either a valid command or a no operation (NOP) command. The format for a read command is shown in Table 19. Set Bit D15 to 0 to select a read command. Bits[D14:D12] contain the register address, and the subsequent twelve bits, Bits[D11:D0], are ignored.

## WRITING TO DEVICE REGISTERS

All of the read and write registers in the AD7383 and the AD7384 can be written to over the SPI. The length of an SPI write access is determined by the CRC write function. An SPI access is 16 bits if CRC write is disabled and 24 bits when CRC write is enabled. The format for a write command is shown in Table 19. Set Bit D15 to 1 to select a write command. Bits[D14:D12] contain the register address, and the subsequent twelve bits, Bits[D11:D0], contain the data to be written to the selected register.

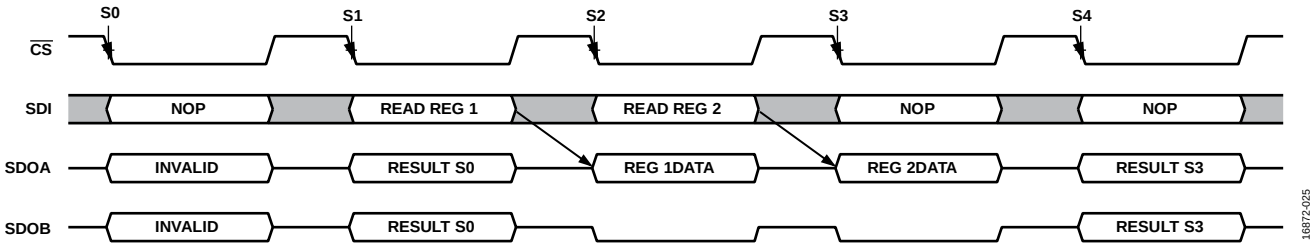


*Figure 43. Register Read*

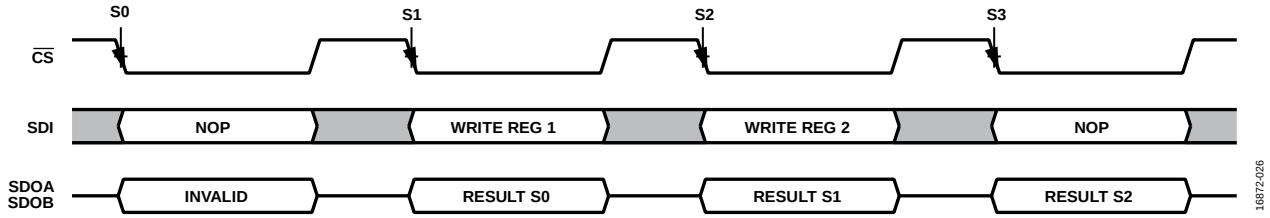


*Figure 44. Register Write*

## CRC

The AD7383 and the AD7384 have CRC checksum modes that can improve interface robustness by detecting errors in data transmissions. The CRC feature is independently selectable for SPI reads and SPI writes. For example, the CRC function for SPI writes can be enabled to prevent unexpected changes to the device configuration but disabled on SPI reads, therefore maintaining a higher throughput rate. The CRC feature is controlled by the programming of the CRC_W bit and CRC_R bits in the CONFIGURATION1 register.

### *CRC Read*

If enabled, a CRC is appended to the conversion result or register reads and consists of an 8-bit word. The CRC is calculated in the conversion result for ADC A and ADC B and is output on SDOA. A CRC is also calculated and appended to register read outputs.

The CRC read function can be used in 2-wire SPI mode, 1-wire SPI mode, and resolution boost mode.

### *CRC Write*

To enable the CRC write function, set the CRC_W bit in the CONFIGURATION1 register to 1. To set the CRC_W bit to 1 to enable the CRC feature, ensure the request frame has a valid CRC appended to the frame.

After the CRC feature is enabled, all register write requests are ignored unless the requests are accompanied by a valid CRC command, requiring a valid CRC to both enable and disable the CRC write feature.

### *CRC Polynomial*

For CRC checksum calculations, the following polynomial is always used: $x^8 + x^2 + x + 1$.

To generate the checksum on a conversion read, the 16-bit data conversion result of the two channels is combined to produce 32-bit data. The 8 MSBs of the 32-bit data are inverted and then left shifted by eight bits to create a number ending in eight logic zeros. The polynomial is aligned such that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned such that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum. For example, this polynomial is 100000111.

Let the original data of two channels be 0xAAAA and 0x5555, that is, 1010 1010 1010 1010 and 0101 0101 0101 0101. The data of the two channels is then appended, including eight zeros on the right. The data then becomes 1010 1010 1010 1010 0101 0101 0101 0101 0000 0000.

Table 17 shows the CRC calculation of 16-bit two-channel data. In the final XOR operation, the reduced data is less than the polynomial. Therefore, the remainder is the CRC for the assumed data.

The same process is followed for the AD7384, but instead of dealing with 32-bit data (the combined result of two channels), it is 28-bit data. For reading data like the registers, CRC computation is based on 16-bit register data, and the same process is performed as described for 32-bit data.

**Table 17. Example CRC Calculation for 16-Bit Two-Channel Data**

| **Data** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **X[1]** | **X[1]** | **X[1]** | **X[1]** | **X[1]** | **X[1]** | **X[1]** | **X[1]** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Process Data** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | | | | | |
| | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | | | |
| | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | | | |
| | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | |
| | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | | |
| | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | |
| | | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | | | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | | | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | | | | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | | | | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | |
| **CRC** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | | |

[1]X = don't care

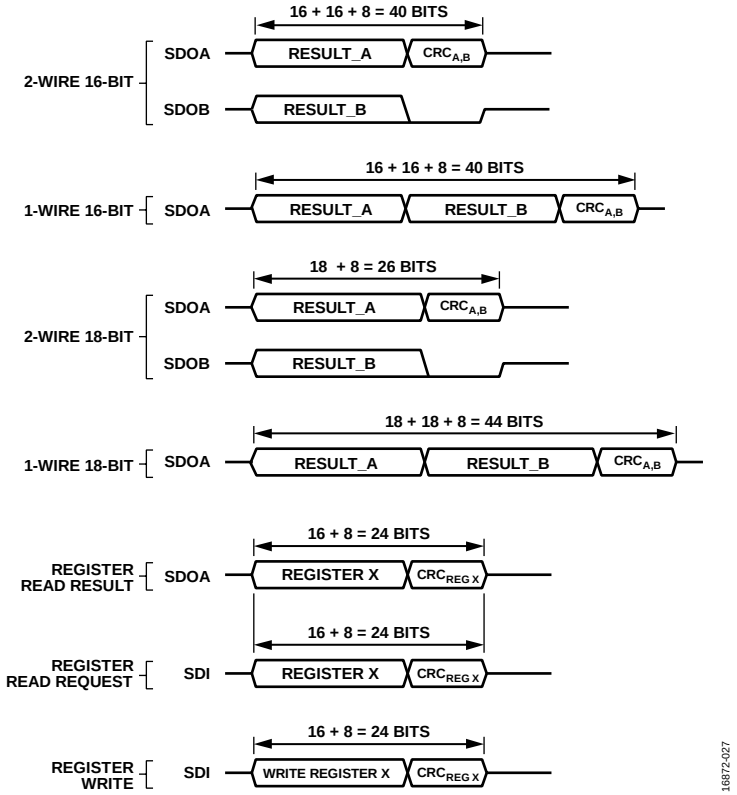


*Figure 45. CRC Operation*

# REGISTERS

The AD7383 and the AD7384 have user programmable on-chip registers for configuring the device.

Table 18 shows a complete overview of the registers available on the AD7383 and the AD7384. The registers are either read and write (R/W) or read only (R). Any read request to a write only register is ignored, and any write request to a read only register is ignored. Writes to any other register address are considered an NOP and are ignored. Any read request to a register address, other than those listed in Table 18, is considered an NOP, and the data transmitted in the next SPI frame are the conversion results.

**Table 18. Register Summary**

| Address | Register Name | Bits | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | | |
| 0x1 | CONFIGURATION1 | [15:8] | ADDRESSING | | | | RESERVED | | OS_MODE | OSR[2] | 0x0000 | R/W |
| | | [7:0] | OSR[1:0] | | CRC_W | CRC_R | ALERT_EN | RES | REFSEL | PMODE | | |
| 0x2 | CONFIGURATION2 | [15:8] | ADDRESSING | | | | RESERVED | | | SDO | 0x0000 | R/W |
| | | [7:0] | RESET | | | | | | | | | |
| 0x3 | $\overline{\text{ALERT}}$ | [15:8] | ADDRESSING | | | | RESERVED | | CRCW_F | SETUP_F | 0x0000 | R |
| | | [7:0] | RESERVED | | AL_B_HIGH | AL_B_LOW | RESERVED | | AL_A_HIGH | AL_A_LOW | | |
| 0x4 | ALERT_LOW_THRESHOLD | [15:8] | ADDRESSING | | | | ALERT_LOW[11:8] | | | | 0x0800 | R/W |
| | | [7:0] | ALERT_LOW[7:0] | | | | | | | | | |
| 0x5 | ALERT_HIGH_THRESHOLD | [15:8] | ADDRESSING | | | | ALERT_HIGH[11:8] | | | | 0x07FF | R/W |
| | | [7:0] | ALERT_HIGH[7:0] | | | | | | | | | |

## ADDRESSING REGISTERS

A serial register transfer on the AD7383 and the AD7384 consists of 16 SCLK cycles. The 4 MSBs written to the AD7383 and the AD7384 are decoded to determine which register is addressed. The 4 MSBs consist of the register address (REGADDR), Bits[D14:D12], and the read and write bit (WR), Bit D15. The register address bits determine which on-chip register is selected. The WR bit determines if the remaining 12 bits of data on the SDI input are loaded into the addressed register, if the addressed register is a valid write register. If the WR bit is 1, the bits load into the register addressed by the register select bits. If the WR bit is 0, the command is seen as a read request. The addressed register data is available to be read during the next read operation.

**Table 19. Addressing Register Format**

| MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| WR | REGADDR | | | DATA | | | | | | | | | | | |

**Table 20. Bit Descriptions for Addressing Registers**

| Bit | Mnemonic | Description |
|---|---|---|
| D15 | WR | If a 1 is written to the WR bit, Bits[D11:D0] of this register are written to the register specified by REGADDR, if the register is a valid address. Alternatively, if a 0 is written, the next data sent out on the SDOA pin is a read from the designated register, if the register is a valid address. |
| D14 to D12 | REGADDR | When WR = 1, the contents of REGADDR determine the register for selection as outlined in Table 18.<br>When WR = 0 and REGADDR contains a valid register address, the contents on the requested register are output on the SDOA pin during the next interface access.<br>When WR = 0 and REGADDR contains 0x0, 0x6, or 0x7, the contents on the SDI line are ignored. The next interface access results in the conversion results being read back. |
| D11 to D0 | DATA | The DATA bits are written into the corresponding register specified by the REGADDR data bits when WR is equal to 1 and the REGADDR data bits contain a valid address. |

## CONFIGURATION1 REGISTER

**Address: 0x1, Reset: 0x0000, Name: CONFIGURATION1**

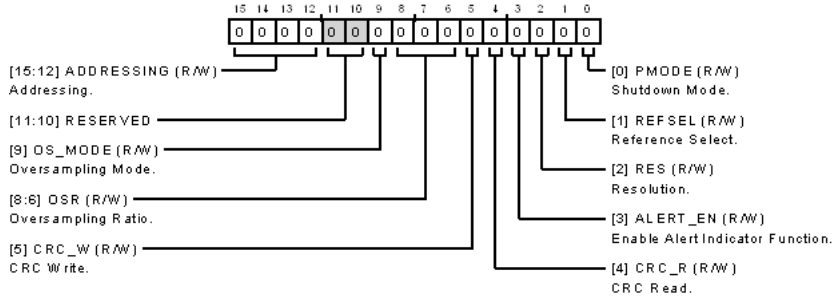


**Table 21. Bit Descriptions for CONFIGURATION1**

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details. | 0x0 | R/W |
| [11:10] | RESERVED | Reserved. | 0x0 | R |
| 9 | OS_MODE | Oversampling Mode. Sets the oversampling mode of the ADC.<br>0: normal average.<br>1: rolling average. | 0x0 | R/W |
| [8:6] | OSR | Oversampling Ratio. Sets the oversampling ratio for all the ADCs in the relevant mode. Normal average mode supports oversampling ratios of ×2, ×4, ×8, ×16, and ×32. Rolling average mode supports oversampling ratios of ×2, ×4, and ×8.<br>000: disabled.<br>001: ×2.<br>010: ×4.<br>011: ×8.<br>100: ×16.<br>101: ×32.<br>110: disabled.<br>111: disabled. | 0x0 | R/W |
| 5 | CRC_W | CRC Write. Controls the CRC functionality for the SDI interface. When setting the CRC_W bit from a 0 to a 1, follow the command with a valid CRC to set this configuration bit. If a valid CRC is not received, the entire frame is ignored. If the CRC_W bit is set to 1, the bit requires a CRC to clear it to 0.<br>0: no CRC function.<br>1: CRC function. | 0x0 | R/W |
| 4 | CRC_R | CRC Read. Controls the CRC functionality for the SDOA and SDOB/$\overline{\text{ALERT}}$ interface.<br>0: no CRC function.<br>1: CRC function. | 0x0 | R/W |
| 3 | ALERT_EN | Enable Alert Indicator Function. This register functions when the SDO bit = 1. Otherwise, the ALERT_EN bit is ignored.<br>0: SDOB.<br>1: $\overline{\text{ALERT}}$. | 0x0 | R/W |
| 2 | RES | Resolution. Sets the size of the conversion result data. If OSR = 0, the RES bit is ignored, and the resolution is set to default resolution.<br>0: normal resolution.<br>1: 2-bit higher resolution. | 0x0 | R/W |
| 1 | REFSEL | Reference Select. Selects the ADC reference source.<br>0: selects internal reference.<br>1: selects external reference. | 0x0 | R/W |
| 0 | PMODE | Shutdown Mode. Sets the power modes.<br>0: normal mode.<br>1: shutdown mode. | 0x0 | R/W |

## CONFIGURATION2 REGISTER

**Address: 0x2, Reset: 0x0000, Name: CONFIGURATION2**

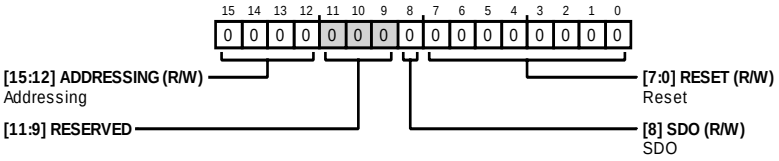


**Table 22. Bit Descriptions for CONFIGURATION2**

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details. | 0x0 | R/W |
| [11:9] | RESERVED | Reserved. | 0x0 | R |
| 8 | SDO | SDO. Conversion results in the serial data output.<br>0: 2-wire. Conversion data are output on both the SDOA and SDOB/$\overline{\text{ALERT}}$ pins.<br>1: 1-wire. Conversion data are output on the SDOA pin only. | 0x0 | R/W |
| [7:0] | RESET | Reset.<br>0x3C performs a soft reset that resets some blocks. Register contents remain unchanged. Clears the $\overline{\text{ALERT}}$ register and flushes any oversampling stored variables or any active state machines.<br>0xFF performs a hard reset that resets all possible blocks in the AD7383 or the AD7384. Register contents are set to defaults. All other values are ignored. | 0x0 | R/W |

## $\overline{\text{ALERT}}$ REGISTER

**Address: 0x3, Reset: 0x0000, Name: $\overline{\text{ALERT}}$**

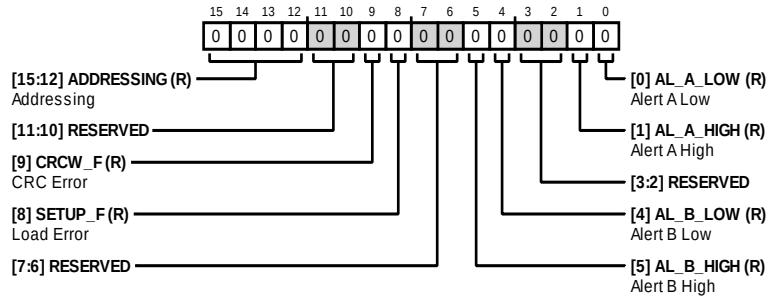


**Table 23. Bit Descriptions for $\overline{\text{ALERT}}$**

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details. | 0x0 | R |
| [11:10] | RESERVED | Reserved. | 0x0 | R |
| 9 | CRCW_F | CRC Error. Indicates that a register write command failed due to a CRC error. This fault bit is sticky and remains set until the register is read.<br>0: no CRC error.<br>1: CRC error. | 0x0 | R |
| 8 | SETUP_F | Load Error. The SETUP_F bit indicates that the device configuration data did not load properly on startup. The SETUP_F bit does not clear on an $\overline{\text{ALERT}}$ register read. A hard reset via the CONFIGURATION2 register is required to clear the SETUP_F bit and restart the device setup again.<br>0: no setup error.<br>1: setup error. | 0x0 | R |
| [7:6] | RESERVED | Reserved. | 0x0 | R |

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| 5 | AL_B_HIGH | Alert B High. The alert indication high bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication. | 0x0 | R |
| 4 | AL_B_LOW | Alert B Low. The alert indication low bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication. | 0x0 | R |
| [3:2] | RESERVED | Reserved. | 0x0 | R |
| 1 | AL_A_HIGH | Alert A High. The alert indication high bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>0: no alert indication.<br>1: alert indication. | 0x0 | R |
| 0 | AL_A_LOW | Alert A Low. The alert indication low bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read.<br>1: alert indication.<br>0: no alert indication. | 0x0 | R |

## ALERT_LOW_THRESHOLD REGISTER

**Address: 0x4, Reset: 0x0800, Name: ALERT_LOW_THRESHOLD**

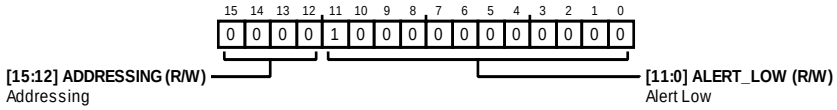


**Table 24. Bit Descriptions for ALERT_LOW_THRESHOLD**

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details. | 0x0 | R/W |
| [11:0] | ALERT_LOW | Alert Low. Bits[D11:D0] from ALERT_LOW move to the MSBs of the internal alert low register, Bits[D15:D4]. The remaining bits, Bits[D3:D0], are fixed at 0x0, which sets an alert when the converter result is below ALERT_LOW_THRESHOLD and disables when the converter result is above ALERT_LOW_THRESHOLD. | 0x800 | R/W |

## ALERT_HIGH_THRESHOLD REGISTER

**Address: 0x5, Reset: 0x07FF, Name: ALERT_HIGH_THRESHOLD**

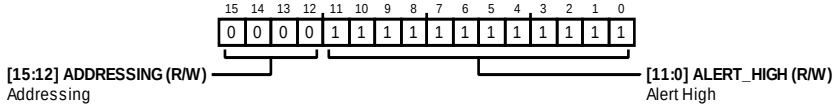


**Table 25. Bit Descriptions for ALERT_HIGH_THRESHOLD**

| Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|
| [15:12] | ADDRESSING | Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details. | 0x0 | R/W |
| [11:0] | ALERT_HIGH | Alert High. Bits[D11:D0] from ALERT_HIGH move to the MSBs of the internal alert high register, Bits[D15:D4]. The remaining bits, Bits[D3:D0], are fixed at 0xF, which sets an alert when the converter result is above ALERT_HIGH_THRESHOLD and disables when the converter result is below ALERT_HIGH_THRESHOLD. | 0x7FF | R/W |

# OUTLINE DIMENSIONS

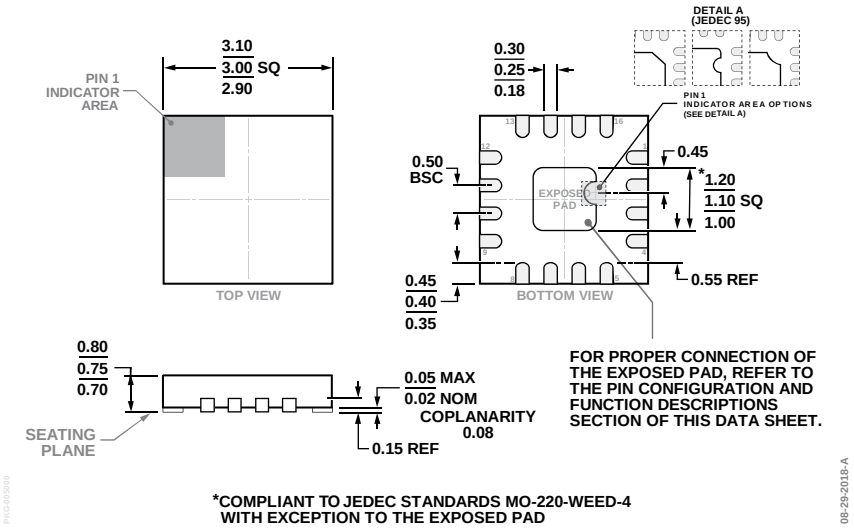


*Figure 46. 16-Lead Lead Frame Chip Scale Package [LFCSP]*
*3 mm × 3 mm Body and 0.75 mm Package Height*
*(CP-16-45)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1, 2] | Resolution (Bit) | Temperature Range | Package Description | Package Option | Marking Code |
|---|---|---|---|---|---|
| AD7383BCPZ-RL | 16 | −40°C to +125°C | 16-Lead LFCSP | CP-16-45 | C96 |
| AD7383BCPZ-RL7 | 16 | −40°C to +125°C | 16-Lead LFCSP | CP-16-45 | C96 |
| AD7384BCPZ-RL | 14 | −40°C to +125°C | 16-Lead LFCSP | CP-16-45 | CA1 |
| AD7384BCPZ-RL7 | 14 | −40°C to +125°C | 16-Lead LFCSP | CP-16-45 | CA1 |
| EVAL-AD7383FMCZ | | | AD7383 Evaluation Board | | |

[1] Z = RoHS Compliant Part.
[2] Use the EVAL-AD7383FMCZ to evaluate the AD7384.