# Product / Process Change Notice

PCN No.: Q000-PCN-DL201512-01 Date: 2015-12-02.

**Change Title: Version Changed for NAU88L25YG.**

Change Classification: ☑ Major ☐ Minor

Change item: ☑ Design ☐ Raw Material ☐ Wafer FAB ☐ Package Assembly ☐ Testing ☐ Others: _____.

***Affected Product(s) :***

The affected product is NAU88L25YG.

***Description of Change(s) :***

Chip design had been revised from rev. A to rev. B.to improve the issues below:

| NAU88L25YG (Rev A) | NAU88L25YGB (Rev B) |
|---|---|
| Device generates an audible "pop" on HPR and HPL when powering up or down the supply. | Pop in inaudible in Rev B. |
| The I2C SDA IO driver pull-down is not strong enough (~470 Ohm to 3.3V) to pull-down these pull-ups close to ground. This results in "ACK" detection of the I2C host to detect a "high" instead of "low". Regx80[11] default =0. | Changed the default drive strength of the SDA IO to "high drive" Regx80[11] default =1. |
| Silicon Revision ID is REGx58[4:2]=7. | Silicon Revision ID is REGx58[4:2]=5. |
| Microphone & Ground terminal Switch resistance is ~160 mOhms. | Design improvements to reduce the Microphone & Ground terminal Switch resistance. It is now ~90 mOhms. |
| Soft-Mute was designed to ramp the signal down to zero at 32 clocks per step. | The Soft-Mute now ramps the signal down to zero at 512 clocks per step. |
| Jack detection interrupt logic requires ADCEN or DACEN to be set in order to see the interrupt at the pin. | Jack detection interrupt can be implemented without ADCEN or DACEN to simplify the sequence. |
| Jack detection interrupt, with no external clocks running, does not get generated unless one FS master mode cycle is executed. FS & BCLK IO become outputs in master mode. | Removed the restriction of the one FS clock in Master mode, thereby simplifying the sequence. |
| Humming Noise from AC main supply is audible on an AC powered line-in speaker when the power supply to the part is off. | Used MICBIAS, to pull down the supply, eliminating the need for external components. |

***Reason for Change(s) :***

Silicon change to improve the performance of the part in the customer application.

***Impact of Change(s) : ( positive & negative )***

Form: No change.

Fit: No change.

Function: Changes described in the change list above.

Reliability: No concern.

***Qualification Plan/ Results :***

1. Passed the products' performeance verification by Nuvoton's evaluation board test, please refer to appendix A for the details.
2. Samples are available for customer qualification and evaluation.

***Implementation Plan :***

☐ Date Code: _____ onward ☐ Lot No.: _____ onward ☐ Implemented date: Feb. 29, 2016 (scheduled)

| | | | |
|---|---|---|---|
| ***Originator:*** | ***H.Y. Lai / Q100*** | ***Approval:(QA Director)*** | ***K.L. Lin/ Q000*** |
| ***Contact for Questions & Concerns*** | Name: HYLai TEL: 886-3-5770066 (ext. 31226) FAX: 886-3-5792673.<br>Address: No.4, Creation Rd. III Science-Based Industrial Park Hsinchu, Taiwan, R.O.C..<br>E-mail: hylai0@nuvoton.com. | | |

***Customer Comments:***

*Note: Please sign this notice, and return to **Nuvoton** contact within **30** days. If no response is received within **30** days, this Change Request will be assumed to meet your approval.*

☐ Approval ☐ Disapproval ☐ Conditional Approval: _____.

Date: _____ Dept. name:_____ Person in charge:_____.

***Follow-up and Tracing:***

**A. copies to**

**FAB:** ☐ Integration _____☐_____☐_____☐_____☐_____.

**Test / Product:** ☐ _____☐_____☐_____☐_____☐_____.

**Design/ Marketing:** ☐ _____☐_____☐_____☐_____☐_____.

**Production control/ Others:** ☐ _____☐_____☐_____☐_____☐_____.

**B. Changes:**

1. Document / Test program:

| Document No/ test program | Document name/ test program name | Version | | Responsible | Completed date | Remark |
|---|---|---|---|---|---|---|
| | | before | after | | | |
| NA | NA | NA | NA | NA | NA | NA |

Verifed by: _____.

Appendix A: Performeance verified result

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| NO.: | VERSION: | PAGE: 1 |
|---|---|---|

# NAU88L25YGB (Rev B) Verification Report

The NAU88L25YGB is the revision B device of NAU88L25YG. This verification report shows list of changes from the Rev A device (NAU88L25YG), possible impacts to customer application, and test results on Nuvoton's evaluation board for verification.

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1. **Headphone Left & Right audible 'pop' during power up and power down**

   NAU88L25YG (Rev A) device may generate a small audible 'pop' on HPR and HPL during powering up or down the supply.

   The internal DAC circuits are powered down by an internal register bit PD_DAC. The PD_DAC signal is supposed to be '1' at power on reset, but it is actually '0', which powers up the DACs. Since the output drivers are powered off at power on reset, the DAC output signals are coupled to the outputs HPL & HPR, which is causing the 'pop'.

2. **SDA IO Driver Strength**

   Increased drive strength of SDA IO in Rev B

   The SDA drive strength register bit is now hard wired such that the IO is always pulling down strong.

3. **Silicon Revision ID**

   Silicon Revision ID will change from revision A to revision B.

   The NAU88L25YGB (Rev B) version will have a different ID register value. Bit [2] is changed to '1'.
   If there is any driver change required, then the same driver can be used for both devices by using the ID bits to distinguish between the parts and apply the correct piece of driver code.

| | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 58 | I2C_DEVICE_ID | I2C_DEVICE_ID[6:1] | | | | | | | | | | | | | | | I2C Device ID read in |
| | | I2C_DEVICE_ID[0] | | | | | | | | | | | | | | | I2C Device ID Lsb read in set by GPIO1/CSB pin |
| | | GPIO2JD1 | | | | | | | | | | | | | | | Jack detect 1 GPIO2 status bit |
| | | GPIO3JD2 | | | | | | | | | | | | | | | Jack detect 2 GPIO3 status bit |
| | | JKDETL | | | | | | | | | | | | | | | Jack Tip insertion detect status bit |
| | | Silicon Revision ID | | | | | | | | | | | | | | | Silicon revision bits |
| | | Software ID | | | | | | | | | | | | | | | Software ID 00=NAU88L25 |
| | | **Default** | **X** | **0** | **0** | **1** | **1** | **0** | **1** | **X** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **Read Only** |

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4. **Switch Resistance Reduction and Crosstalk**

On NAU88L25YG (Rev A), the switch resistance may cause increased echo in a network communication application if echo cancellation is not sufficient.

The resistances of the internal FET (30milliOhm), metal routing (70milliOhm) and bond wires ( 50 milliOhm) all add up to about 150 milli Ohm of switch resistance on NAU88L25YG. If the external flex cable adds another 200 milli Ohm, then it can be a total of 350 milli Ohm, which may create poor echo performance to the microphone audio path.

There are two revised methods:

1) Generating equal amplitude output signals with inverse phase on the left and right headphone outputs by generating (Left+Right)/2 and -(Left+Right)/2. This allows the crosstalk signal to be cancelled out;
2) Reduction of the switch resistance by improved metal routing, reducing the bond wire length by shifting the dice up and WLCSP package option (no bond wires).

5. **Soft un-Mute Function**

Increase the soft-unmute ramp up time from 32 clocks per step on NAU88L25YG (Rev A) to 512 clocks per step on NAU88L25YGB (Rev B).

6. **Jack detect interrupt logic requires ADCEN or DACEN to be set in order to see the interrupt at the pin**

In NAU88L25YGB (Rev B), the clock gating of the interrupt modules is removed such that there is no need to turn on ADC/DAC and enable the master mode for Frame Sync. MSB0 (output enable for FS/BCLK) is ORed with CFG_REG0x73[15]. Set to "1" to disable the output driving of FS & BCLK.

7. **Jack detection interrupt with no external clocks running does not get generated unless one FS master mode cycle is executed. FS & BCLK IO's become outputs in master mode**

Removed the clock gating of the interrupt modules, so no need to turn on ADC/DAC enable and master mode for Frame Sync. MSB0 (output enable for FS/BCLK) is ORed with CFG_REG0x73[15]. Set to "1" to disable the output driving of FS & BCLK.

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8. **Humming Noise from AC mains supply audible on an AC powered line in speaker when the NAU88L25 supply is off**

If an AC powered line-in speaker instead of a headphone is hooked up to NAU88L25YG (Rev A), a 60Hz or 50Hz humming noise can be heard if the NAU88L25YG is powered off.

When the NAU88L25YG power is off, the switches that ground the jack terminals can no longer be controlled and these terminals will become high impedance and floating, which makes it easier to pick up noise that is coupled through the ground terminals. Since this is a new requirement we found from NAU88L25YG customer evaluation, the NAU88L25YGB now contains a feature to support this, other than a full power up state.

A 3.3V standby voltage was found within the system easily, that could be used when the system is powered off. However, only a small current (< 1uA) can be consumed from this supply. A circuit, using three FETs was identified and proven to work on the system.

Conclusion:

All proposed changes have been implemented and verified successfully.
Recommend that the part be released to production.

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