

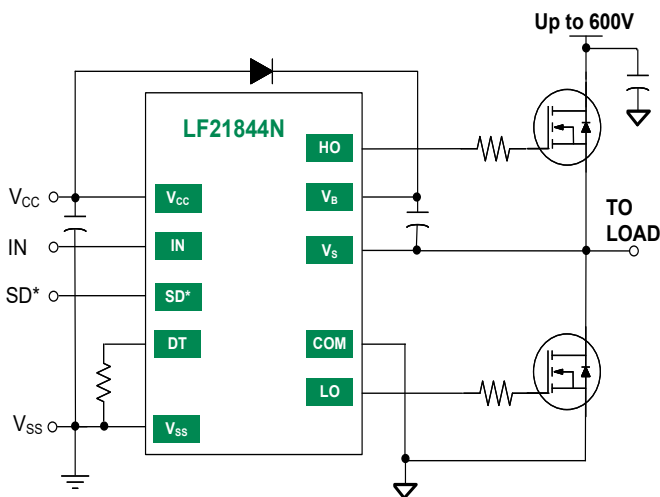
## Features

- Floating high-side driver in bootstrap operation to 600V
- Drives two N-channel MOSFETs or IGBTs in a half-bridge configuration
- 1.4A source / 1.7A sink output current capability
- Outputs tolerant to negative transients
- Programmable dead time to protect MOSFETs
- Wide low-side gate driver supply voltage: 10V to 20V
- Wide logic supply voltage offset voltage: -5V to 5V
- Logic input (IN and SD\*) 3.3V capability
- Schmitt triggered logic inputs with internal pull up and pull down
- Under Voltage Lockout (UVLO) for high-side and low side drivers
- Extended temperature range:-40°C to +125°C

## Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

## Typical Application



# LF21844N

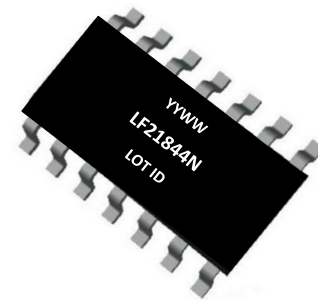
## Half-Bridge Gate Driver

## Description

LF21844N is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half bridge configuration. The high voltage technology enables the LF21844N's high side to switch to 600V in a bootstrap operation.

The LF21844N logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. Programmable dead time, by an external resistor, provides more system level flexibility.

The LF21844N is offered in SOIC(N)-14 package. It operates over the extended temperature range of -40 °C to +125 °C .



SOIC(N)-14

## Ordering Information

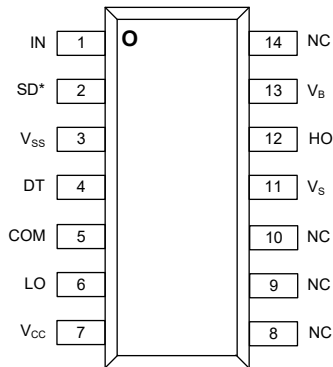
Year Year Week Week

Part #	Package	Pack / Qty	Mark
LF21844NTR	SOIC(N)-14	T&R / 2500	YYWW LF21844N Lot ID



## 1 Specifications

### 1.1 Pin Diagrams



**Top View: SOIC(N)-14  
LF21844N**

### 1.2 Pin Descriptions

Pin #	Pin Name	Pin Type	Description
1	IN	Input	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO
2	SD*	Input	Logic input for shutdown, active low.
3	V <sub>SS</sub>	Power	Logic ground
4	DT	Output	Programmable deadtime lead
5	COM	Power	Low-side return
6	LO	Output	Low-side gate drive output
7	V <sub>CC</sub>	Power	Low-side and logic fixed supply
11	V <sub>S</sub>	Power	High-side floating supply return
12	HO	Output	High-side gate drive output
13	V <sub>B</sub>	Power	High-side floating supply
8, 9, 10, 14	NC	No Connect	Not connected internally

### 1.3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
High side floating supply voltage	$V_B$	-0.3	+624	V
High side floating supply offset voltage	$V_S$	$V_B - 24$	$V_B + 0.3$	V
High side floating output voltage	$V_{HO}$	$V_S - 0.3$	$V_B + 0.3$	V
Offset supply voltage transient	$dV_S/dt$	--	50	V/ns
Programmable dead time voltage	$V_{DT}$	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V
Low side fixed supply voltage	$V_{CC}$	-0.3	+24	V
Low side output voltage	$V_{LO}$	-0.3	$V_{CC} + 0.3$	V
Logic Supply offset voltage	$V_{SS}$	$V_{CC} - 24$	$V_{CC} + 0.3$	V
Logic input voltage (IN and SD*)	$V_{IN}$	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V
Package power dissipation	$P_D$	--	1.0	W
Junction Operating Temperature	$T_J$	--	+150	°C
Storage Temperature	$T_{STG}$	-55	+150	°C

Unless otherwise specified all voltages are referenced to COM. All electrical ratings are at  $T_A = 25^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 1.4 Thermal Characteristics

Parameter	Symbol	Rating	Unit
Junction to ambient	$\theta_{JA}$	120	°C/W

Thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

### 1.5 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High side floating supply absolute voltage	$V_B$	$V_S + 10$	$V_S + 20$	V
High side floating supply offset voltage	$V_S$	<b>NOTE1</b>	600	V
High side floating output voltage	$V_{HO}$	$V_S$	$V_B$	V
Logic and Low side fixed supply voltage	$V_{CC}$	10	20	V
Low side output voltage	$V_{LO}$	0	$V_{CC}$	V
Logic input voltage (IN & SD*)	$V_{IN}$	$V_{SS}$	5	V
Programmable deadtime voltage	$V_{DT}$	$V_{SS}$	<b>Note2</b>	V
Logic ground	$V_{SS}$	-5	+5	V
Ambient temperature	$T_A$	-40	125	°C

Unless otherwise specified all voltages are referenced to COM

**NOTE1** High-side driver remains operational for  $V_S$  transients down to -5V

**NOTE2** Recommended pull down resistor to  $V_{SS}$ : 0 - 200K, minimum 1/8W suggested

### 1.6 DC Electrical Characteristics

$V_{CC} = V_{BS} = 15V$ ,  $V_{SS} = V_{COM} = 0V$ , and  $T_A = 25^\circ C$ , unless otherwise specified.

The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to both logic input pins: IN and SD\*. The  $V_O$  and  $I_O$  parameters are applicable to the respective output pins: HO and LO and are referenced to COM.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Logic "1" input voltage	$V_{IH}$	$V_{CC} = 10V$ to $20V$ <b>NOTE3</b>	2.5	--	--	V
Logic "0" input voltage	$V_{IL}$		--	--	0.8	
Logic input voltage hysteresis	$V_{IN(HYS)}$		--	0.3	--	
High level output voltage, $V_{BIAS} - V_O$	$V_{OH}$	$I_O = 0A$	--	--	1.4	V
Low level output voltage, $V_O$	$V_{OL}$	$I_O = 20mA$	--	--	0.2	
Offset supply leakage current	$I_{LK}$	$V_B = V_S = 600V$	--	--	50	$\mu A$
Quiescent $V_{BS}$ supply current	$I_{BSQ}$	$V_{IN} = 0V$ or $5V$	20	60	150	
Quiescent $V_{CC}$ supply current	$I_{CCQ}$	$V_{IN} = 0V$ or $5V$	0.4	1.0	1.8	mA
Logic "1" input bias current	$I_{IN+}$	$V_{IN} = 5V$	--	25	60	$\mu A$
	$I_{SD+}$		--	--	1	
Logic "0" input bias current	$I_{IN-}$	$V_{IN} = 0V$	--	--	1	
	$I_{SD-}$		--	25	60	
$V_{CC}, V_{BS}$ UVLO off, positive going threshold	$V_{UV+}$	--	8	8.9	9.8	V
$V_{CC}, V_{BS}$ UVLO enable, negative going threshold	$V_{UV-}$	--	7.4	8.2	9	
UVLO hysteresis	$V_{UV(HYS)}$	--	--	0.7	--	
Output high short circuit pulsed current	$I_{O+}$	$V_O = 0V$ , $t \leq 10 \mu s$	1.4	1.9	--	A
Output low short circuit pulsed current	$I_{O-}$	$V_O = 15V$ , $t \leq 10 \mu s$	1.7	2.3	--	

**NOTE3** For optimal operation, it is recommended the input pulse to IN should have a minimum amplitude of 2.5V with a minimum pulse width of  $2 \times t_{DT}$  (deadtime)

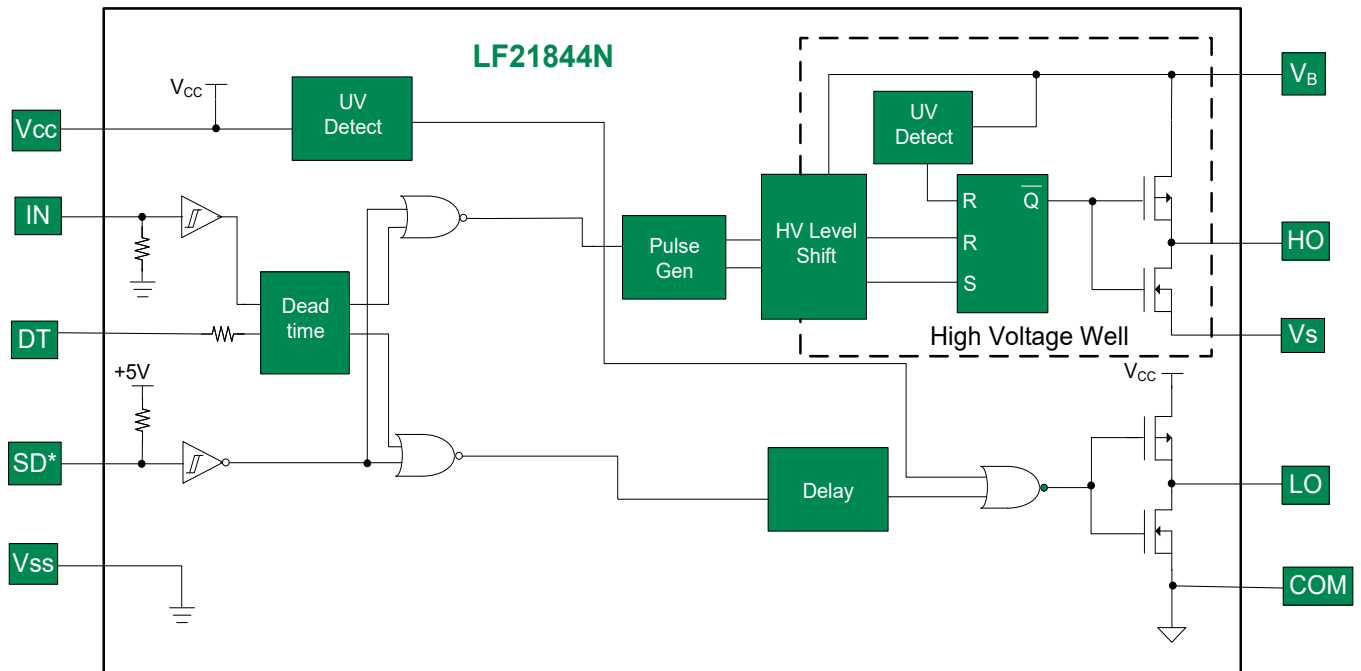
### 1.7 AC Electrical Characteristics

$V_{CC}=V_{BS}=15V, V_{SS}=V_{COM}=0V, C_L=1000\text{ pF}$ , and  $T_A=25\text{ }^\circ\text{C}$  unless otherwise specified.

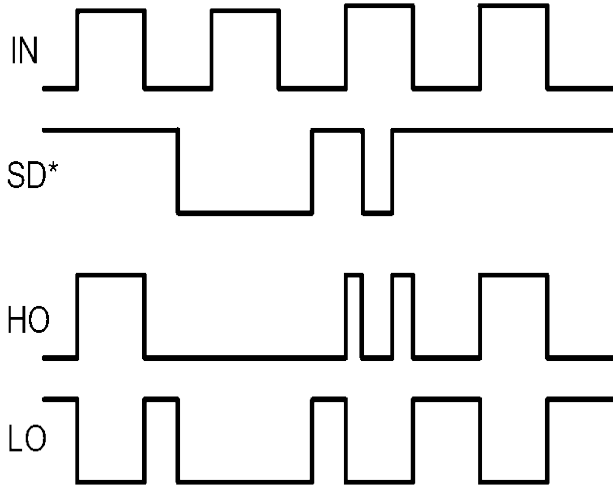
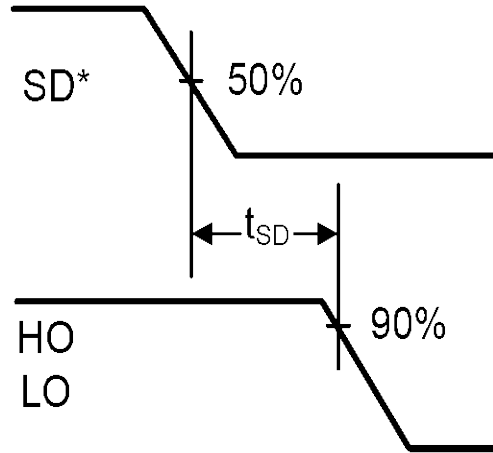
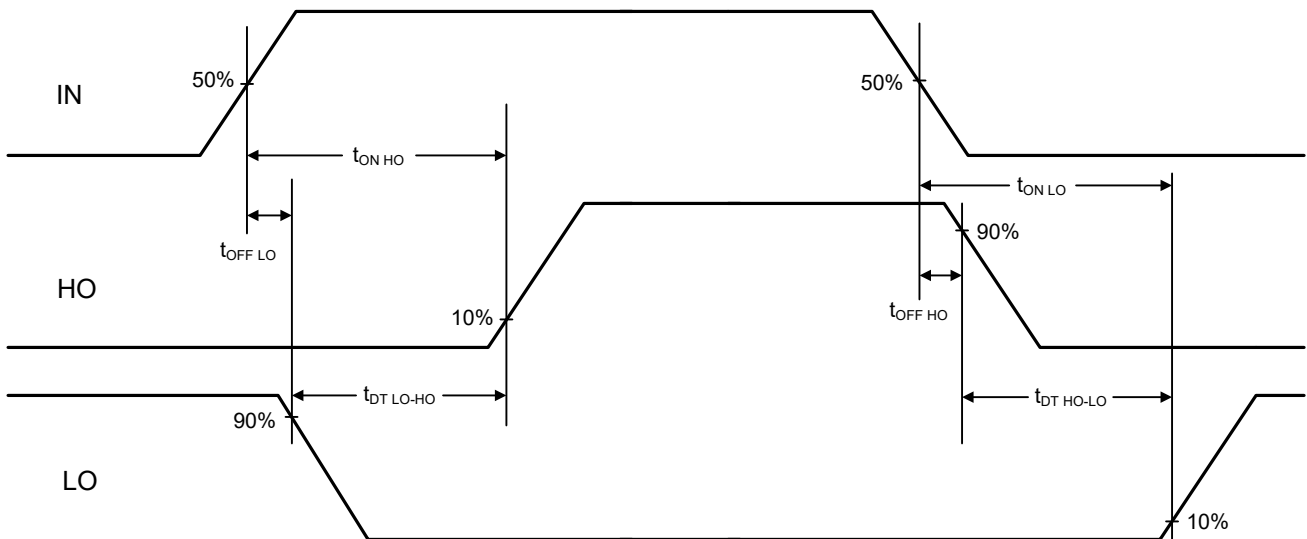
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-on propagation delay	$t_{ON}$	$V_S = 0V$	--	680	900	ns
Turn-off propagation delay	$t_{OFF}$	$V_S = 0V$ or $600V$	--	270	400	
Shut-down propagation delay	$t_{SD}$	--	--	180	270	
Propagation delay matching, HO & LO turn-on	$t_{DMON}$	--	--	--	90	
Propagation delay matching, HO & LO turn-off	$t_{DMOFF}$	--	--	--	40	
Turn-on rise time	$t_r$	$V_S = 0V$	--	40	60	
Turn-off fall time	$t_f$		--	20	35	
Deadtime	$t_{DT}$	$R_{DT}=0\Omega$	280	400	520	ns
		$R_{DT}=200k\Omega$	4	5	6	$\mu s$
Deadtime matching	$t_{DTMT}$	$R_{DT}=0\Omega$	--	0	50	ns
		$R_{DT}=200k\Omega$	--	0	600	

## 2 Functional Description

### 2.1 Functional Block Diagram



### 2.2 Timing Waveforms

**Figure 1. Input / Output Logic Diagram**

**Figure 2. Shutdown Waveform Definitions**

**Figure 3. Input-to-Output Delay Timing Diagram**


$$\text{Deadtime } t_{DT\ LO-HO} = t_{ON\ HO} - t_{OFF\ LO}$$

$$t_{DT\ HO-LO} = t_{ON\ LO} - t_{OFF\ HO}$$

Deadtime matching

$$t_{MDT} = t_{DT\ LO-HO} - t_{DT\ HO-LO}$$

Delay matching

$$t_{DM\ OFF} = t_{OFF\ LO} - t_{OFF\ HO}$$

$$t_{DM\ ON} = t_{ON\ LO} - t_{ON\ HO}$$

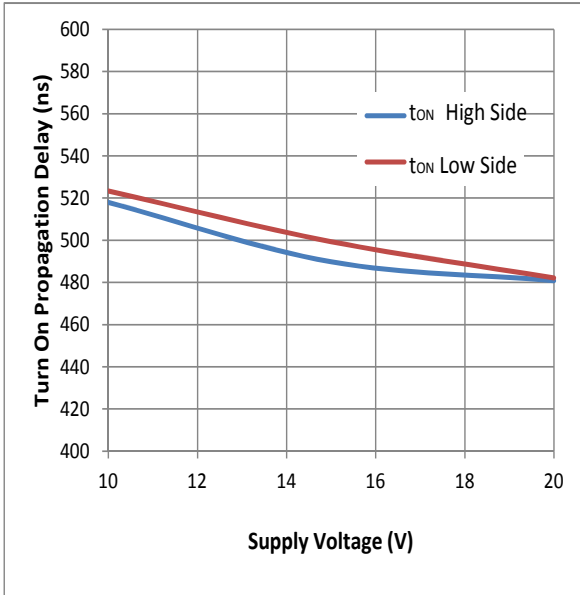




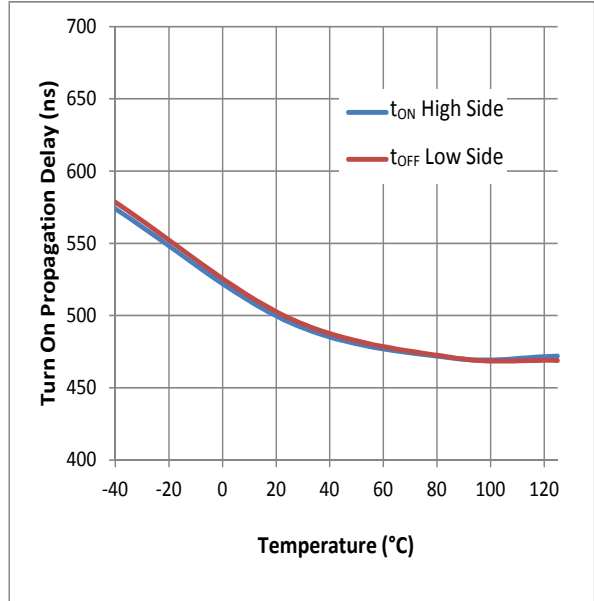
### 3 Performance Data

Unless otherwise noted  $V_{CC} = V_{BS} = 15V$ ,  $T_A = 25^\circ C$ ,  $V_{COM} = 0V$  and values are typical.

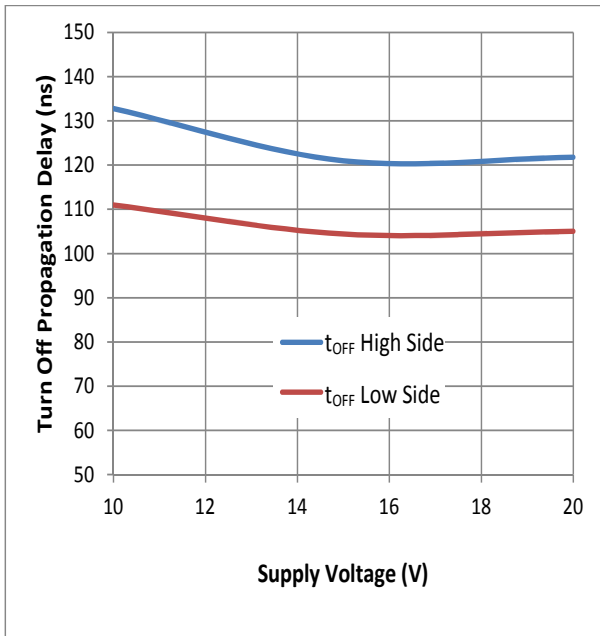
**Figure 5.** Turn-on Propagation Delay vs. Supply Voltage



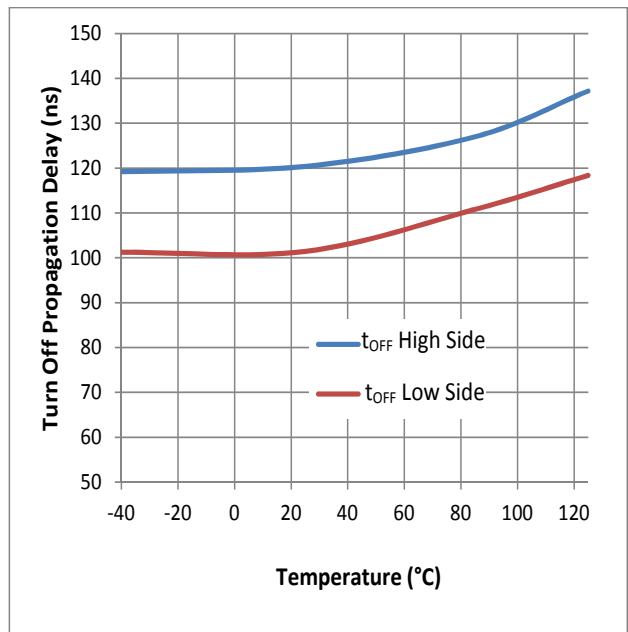
**Figure 6.** Turn-on Propagation Delay vs. Temperature

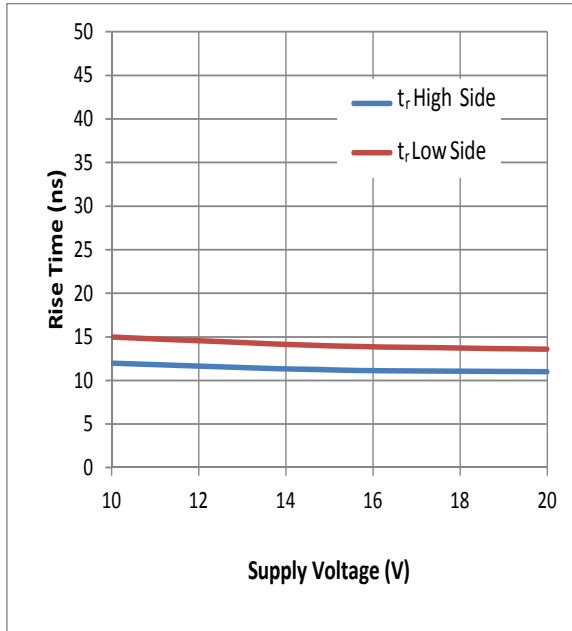
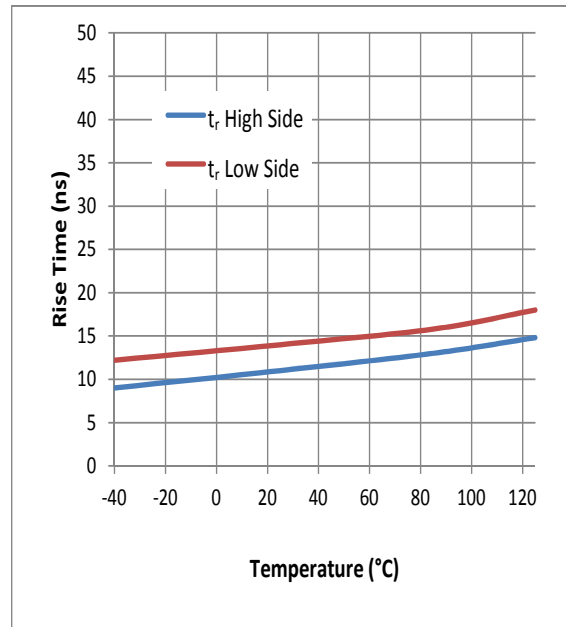
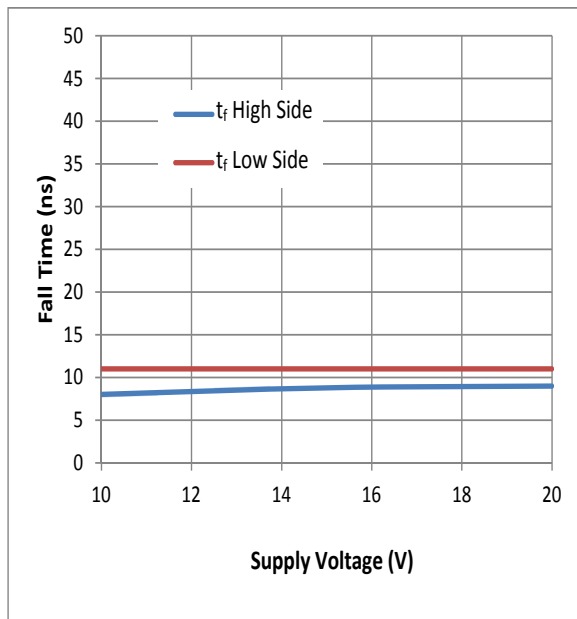
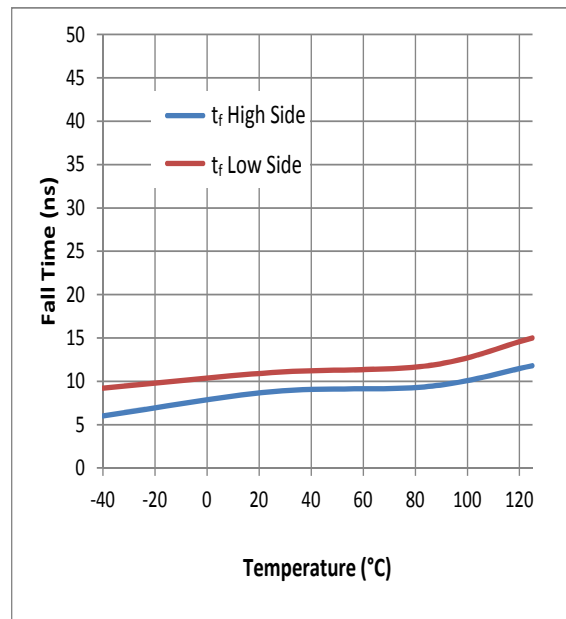


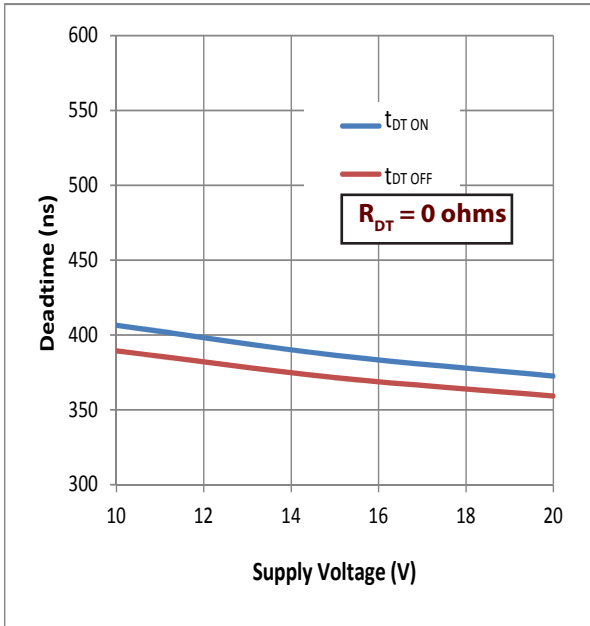
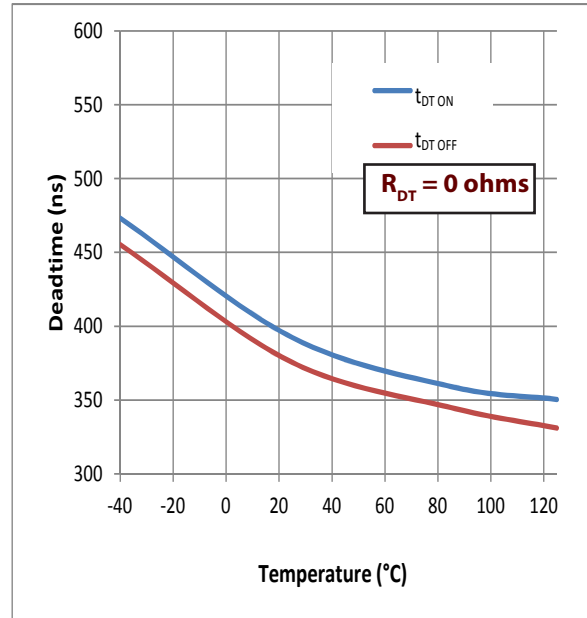
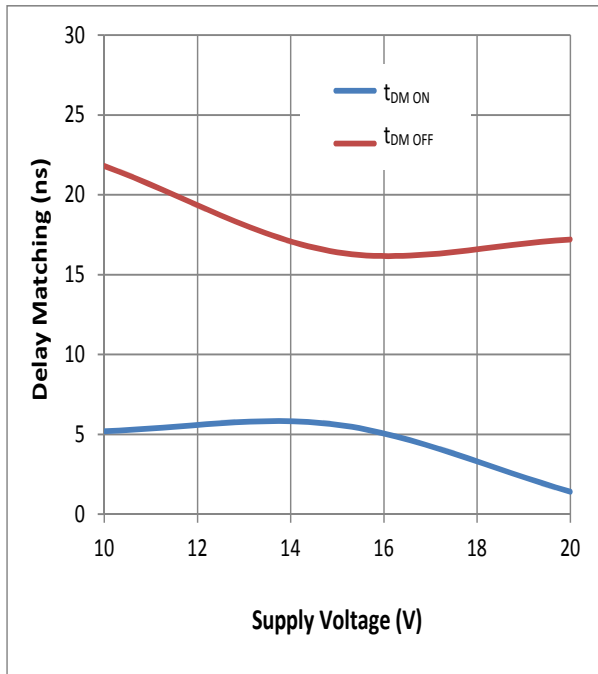
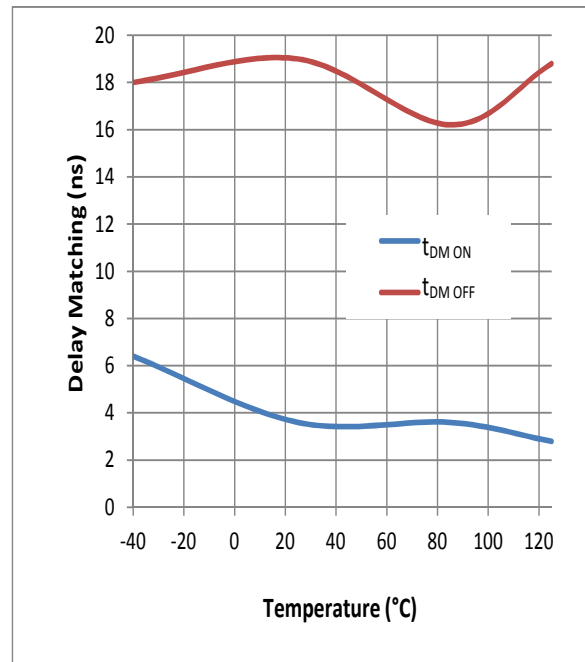
**Figure 7.** Turn-off Propagation Delay vs. Supply Voltage

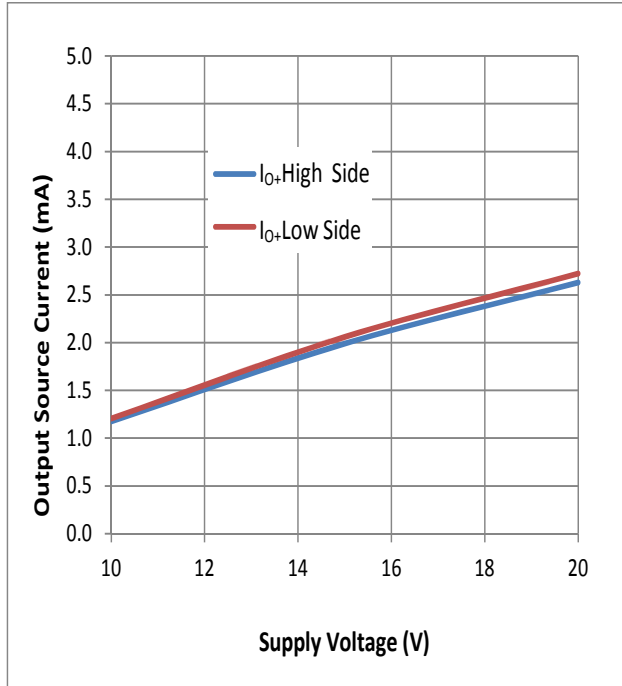
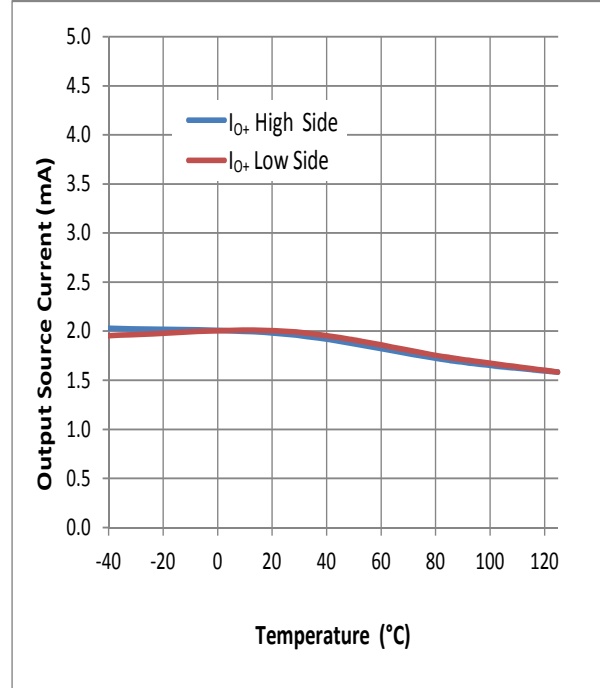
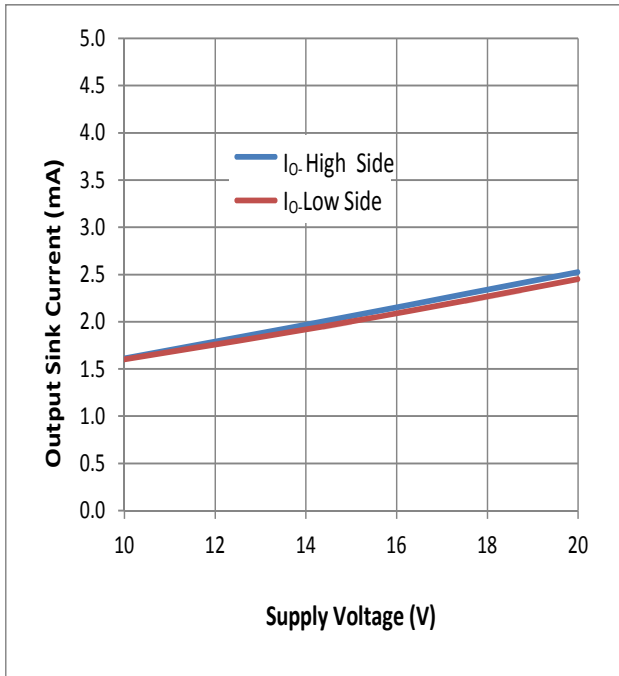
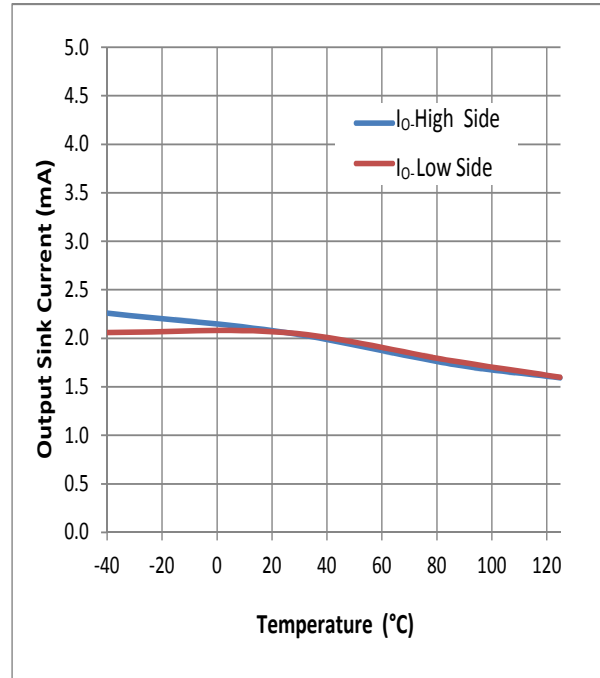


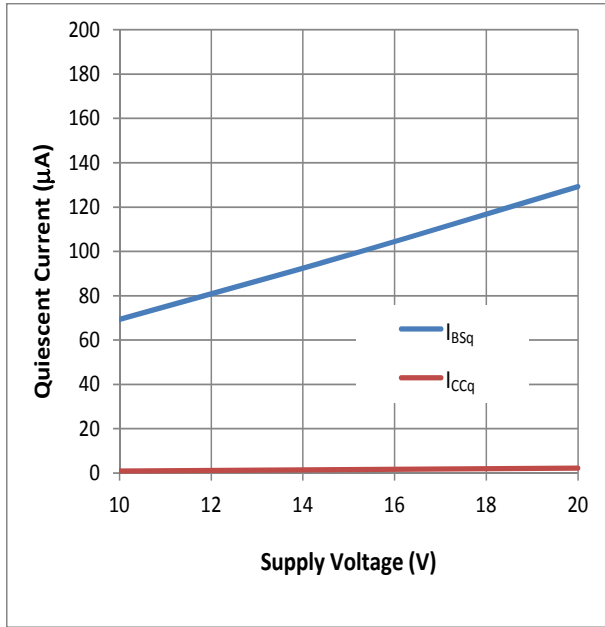
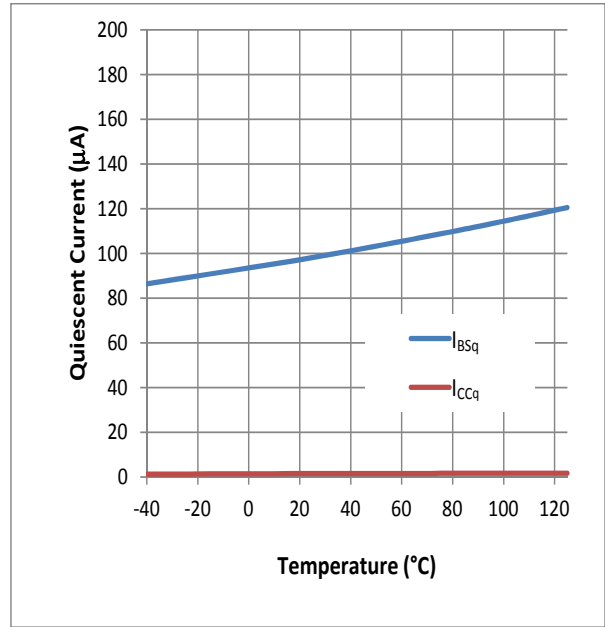
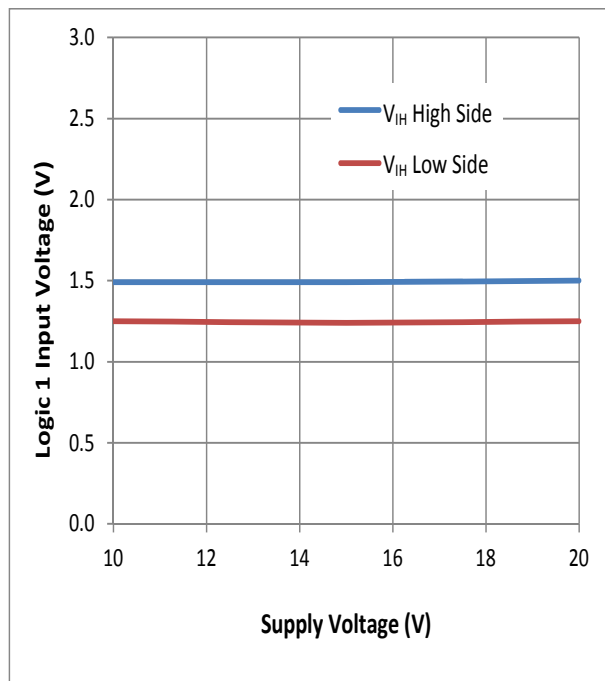
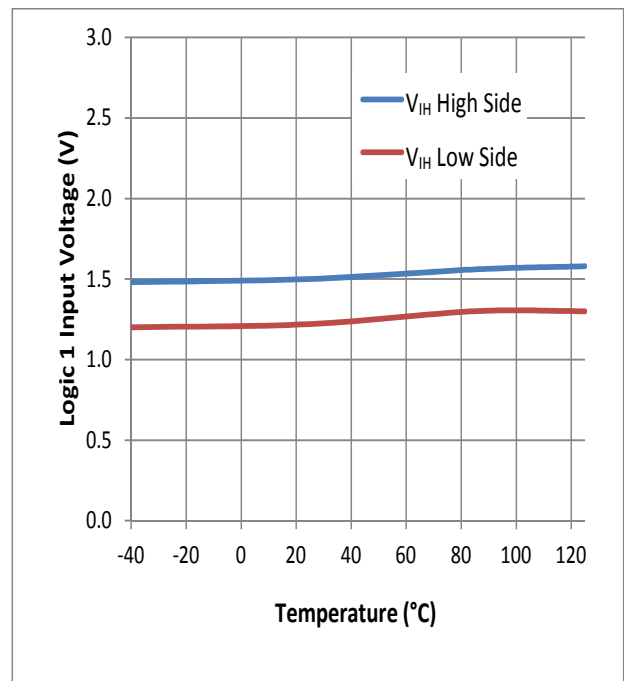
**Figure 8.** Turn-off Propagation Delay vs. Temperature

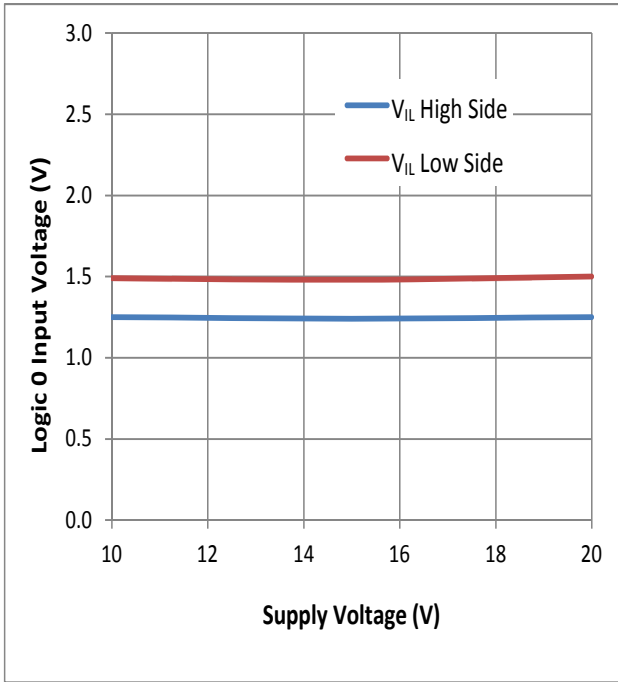
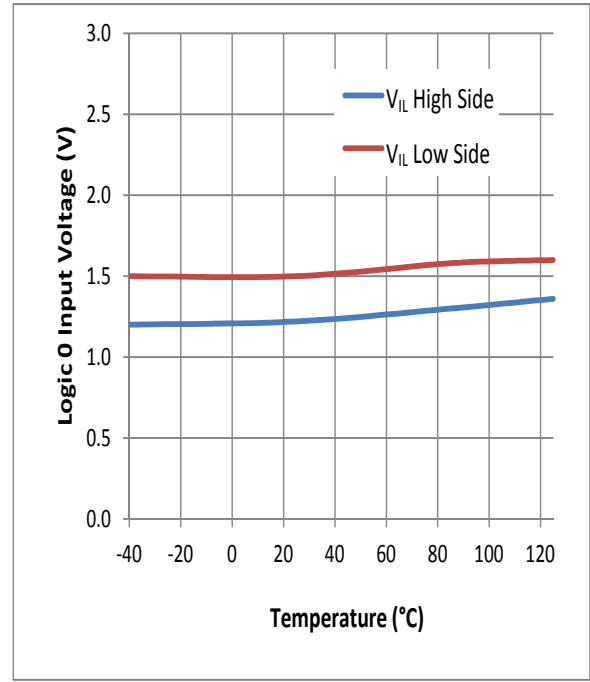
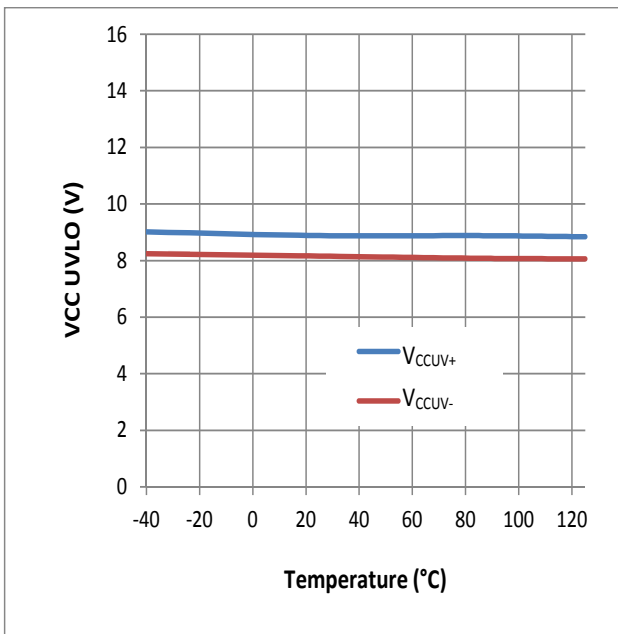
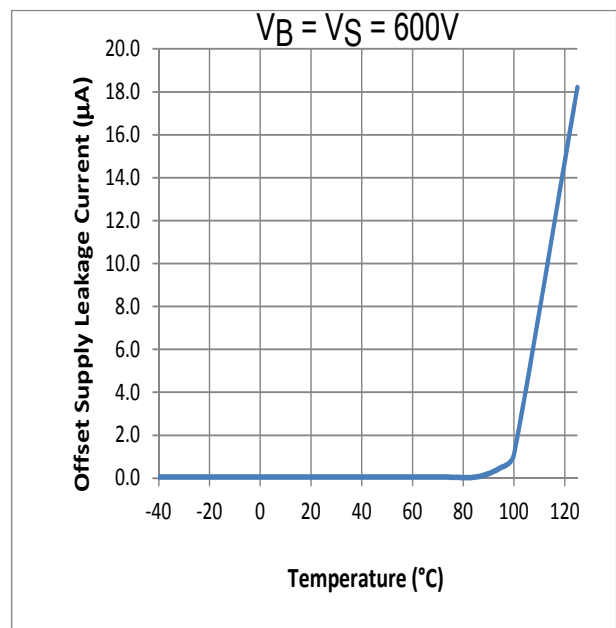


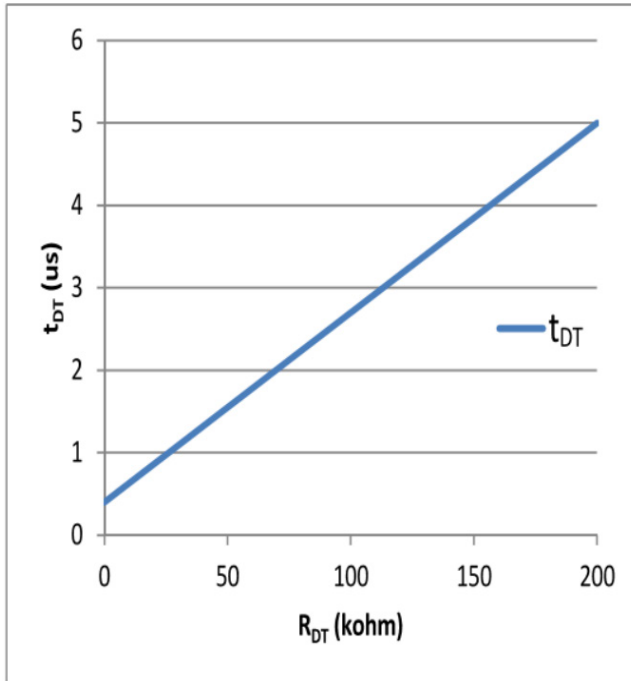
**Figure 9. Rise Time vs. Supply Voltage**

**Figure 10. Rise Time vs. Temperature**

**Figure 11. Fall Time vs. Supply Voltage**

**Figure 12. Fall Time vs. Temperature**


**Figure 13.** Deadtime vs. Supply Voltage

**Figure 14.** Deadtime vs. Temperature

**Figure 15.** Delay Matching vs. Supply Voltage

**Figure 16.** Delay Matching vs. Temperature


**Figure 17. Output Source Current vs. Supply Voltage**

**Figure 18. Output Source Current vs. Temperature**

**Figure 19. Output Sink Current vs. Supply Voltage**

**Figure 20. Output Sink Current vs. Temperature**


**Figure 21.** Quiescent Current vs. Supply Voltage

**Figure 22.** Quiescent Current vs. Temperature

**Figure 23.** Logic 1 Input Voltage vs. Supply Voltage

**Figure 24.** Logic 1 Input Voltage vs. Temperature


**Figure 25.** Logic 0 Input Voltage vs. Supply Voltage

**Figure 26.** Logic 0 Input Voltage vs. Temperature

**Figure 27.** V<sub>CC</sub> UVLO vs. Temperature

**Figure 28.** Offset Supply Leakage Current Temperature


**Figure 29.**  $t_{DT}$  vs  $R_{DT}$ 



### 4 Manufacturing Information

#### 4.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. Littelfuse Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** rating as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
LF21844N	MSL3

#### 4.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

#### 4.3 Reflow Profile

Provided in the table below is the IPC/JEDEC J-STD-020 Classification Temperature ( $T_c$ ) and the maximum dwell time the body temperature of these surface mount devices may be ( $T_c - 5$ )°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

Device	Classification Temperature ( $T_c$ )	Dwell Time ( $t_p$ )	Max Reflow Cycles
LF21844N	260°C	30 seconds	3

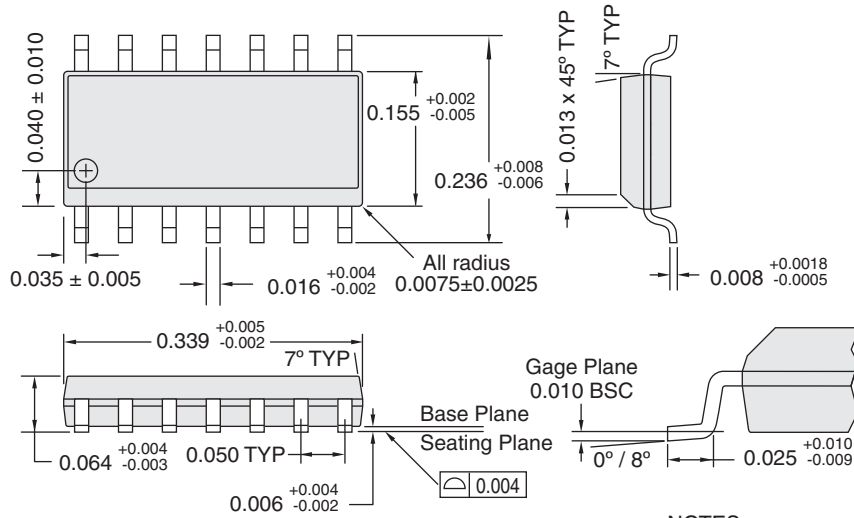


#### 4.4 Board Wash

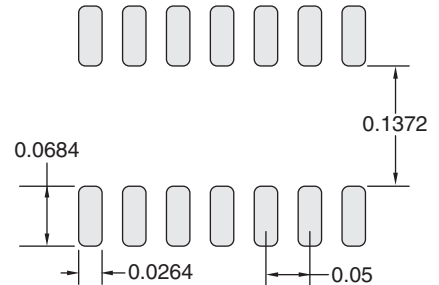
Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.



### 5 Package Dimensions: SOIC(N)-14



#### Recommended PCB Land Pattern



#### NOTES:

1. Controlling dimension: inches
2. Molded package dimensions do not include mold flash or protrusion. Mold flash or protrusion shall not exceed 6 mils per side.
3. Formed leads shall be planar with respect to one another within 4 mils referenced from the seating plane.
4. The bottom package lead side may be bigger than the top package lead side by 4 mils (2 mils per side). Bottom package dimension shall follow dimension stated in this drawing.
5. This drawing conforms to JEDEC REF. MS-012 Rev. E.

### Important Notice

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