NUP1301U

Ultra low capacitance ESD protection array

14 April 2023 **Product data sheet**

1. General description

Ultra low capacitance ElectroStatic Discharge (ESD) protection array in a small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package designed to protect one signal line in rail-to-rail configuration from the damage caused by ESD and other transients.

2. Features and benefits

- ESD protection of one signal line (rail-to-rail configuration)
- Ultra low diode capacitance: C_d = 0.6 pF
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); I_{PP} = 11 A

3. Applications

- Telecommunication networks
- Video line protection
- Microcontroller protection
- I²C-bus protection
- Antenna power supply
- Analog audio
- Class-D amplifier

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage			-	-	80	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	0.6	0.75	pF
I_R	reverse current	V_R = 80 V; T_{amb} = 25 °C		-	-	100	nA

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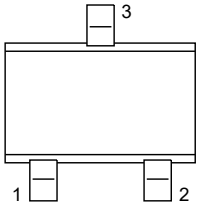
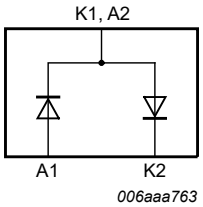
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND	ground	 SC-70 (SOT323)	
2	V_{CC}	supply voltage		
3	I/O	input/output		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NUP1301U	SC-70	plastic, surface-mounted package; 3 leads; 1.3 mm pitch; 2 mm x 1.25 mm x 0.95 mm body	SOT323

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
NUP1301U	%VU

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RRM}	repetitive peak reverse voltage			-	80	V
V_R	reverse voltage			-	80	V
I_F	forward current		[1]	-	215	mA
I_{FRM}	repetitive peak forward current	$t_p \leq 1$ ms; $\delta \leq 0.25$		-	500	mA
P_{PPM}	rated peak pulse power	t_p = 8/20 µs	[2] [3]	-	220	W
I_{PPM}	rated peak pulse current		[2] [3]	-	11	A
I_{FSM}	non-repetitive peak forward current	square wave; t_p = 1 µs	[4]	-	4	A
		square wave; t_p = 1 ms	[4]	-	1.5	A
		square wave; t_p = 1 s	[4]	-	0.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[5] [6]	-	200	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge)	[3] [7]	-	30	kV
		machine model		-	400	V
		MIL-STD-883 (human body model)		-	10	kV

[1] Pulse test: $t_p \leq 300$ µs; $\delta \leq 0.02$.
[2] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[3] Measured from pin 3 to pins 1 and 2 (pins 1 and 2 are connected).
[4] T_j = 25 °C prior to surge.
[5] Single diode loaded.
[6] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[7] Device stressed with ten non-repetitive ESD pulses.

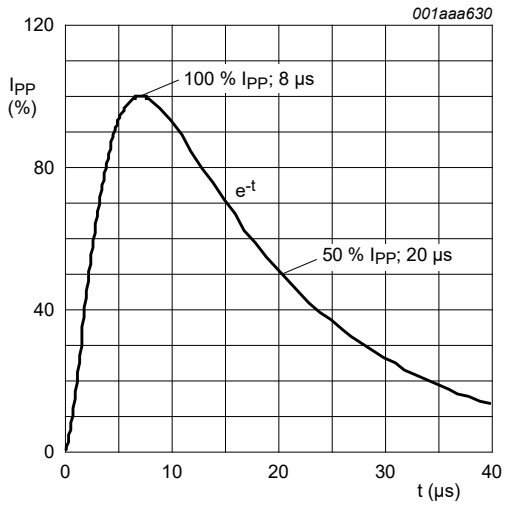


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5

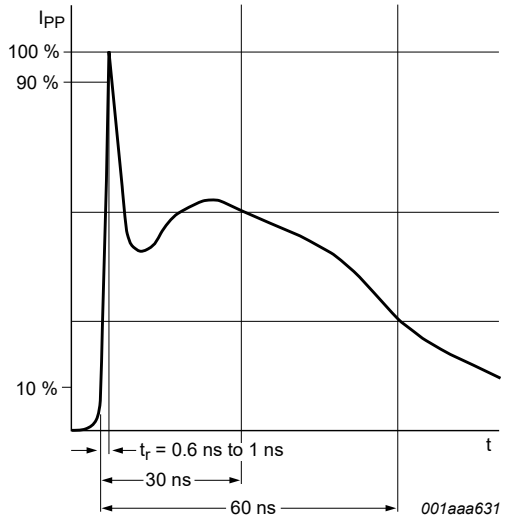


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	625	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	300	K/W

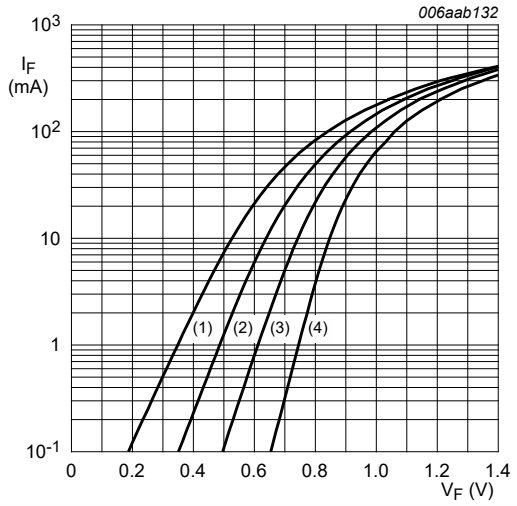
[1] Single diode loaded.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

10. Characteristics

Table 7. Characteristics

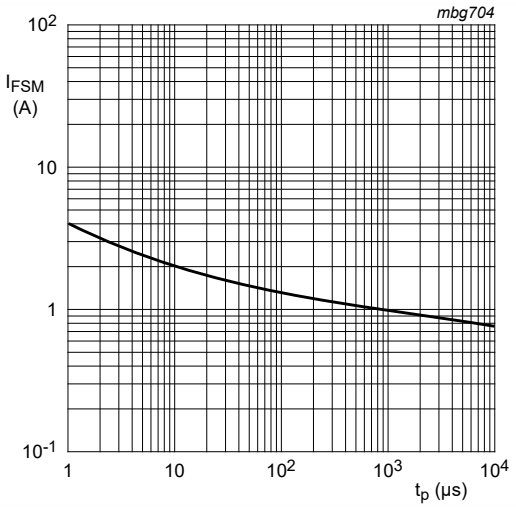
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_F	forward voltage	I_F = 1 mA; T_{amb} = 25 °C	[1]	-	-	715	mV
		I_F = 10 mA; T_{amb} = 25 °C	[1]	-	-	855	mV
		I_F = 50 mA; T_{amb} = 25 °C	[1]	-	-	1	V
		I_F = 150 mA; T_{amb} = 25 °C	[1]	-	-	1.25	V
V_{BR}	breakdown voltage	I_R = 100 µA; T_{amb} = 25 °C		100	-	-	V
I_R	reverse current	V_R = 25 V; T_{amb} = 25 °C		-	-	30	nA
		V_R = 80 V; T_{amb} = 25 °C		-	-	100	nA
		V_R = 25 V; T_j = 150 °C		-	-	25	µA
		V_R = 80 V; T_j = 150 °C		-	-	35	µA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	0.6	0.75	pF
V_{CL}	clamping voltage	I_{PP} = 1 A; T_{amb} = 25 °C	[2] [3]	-	-	3	V
		I_{PPM} = 11 A; T_{amb} = 25 °C	[2] [3]	-	-	20	V

[1] Pulse test: $t_p \leq 300$ µs; $\delta \leq 0.02$.
[2] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[3] Measured from pin 3 to pins 1 and 2 (pins 1 and 2 are connected).



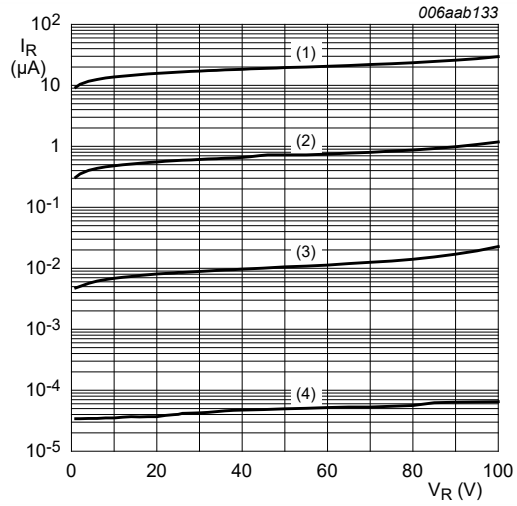
(1) T_{amb} = 150 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 3. Forward current as a function of forward voltage; typical values



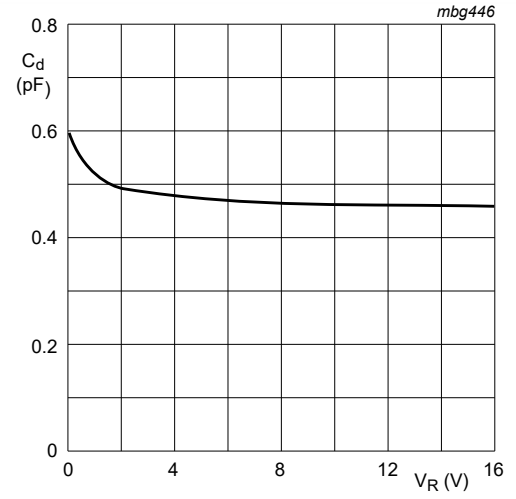
Based on square wave currents.
$T_{j(init)}$ = 25 °C

Fig. 4. Non-repetitive peak forward current as a function of pulse duration; typical values



(1) T_{amb} = 150 °C
(2) T_{amb} = 85 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 5. Reverse current as a function of reverse voltage; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig. 6. Diode capacitance as a function of reverse voltage; typical values

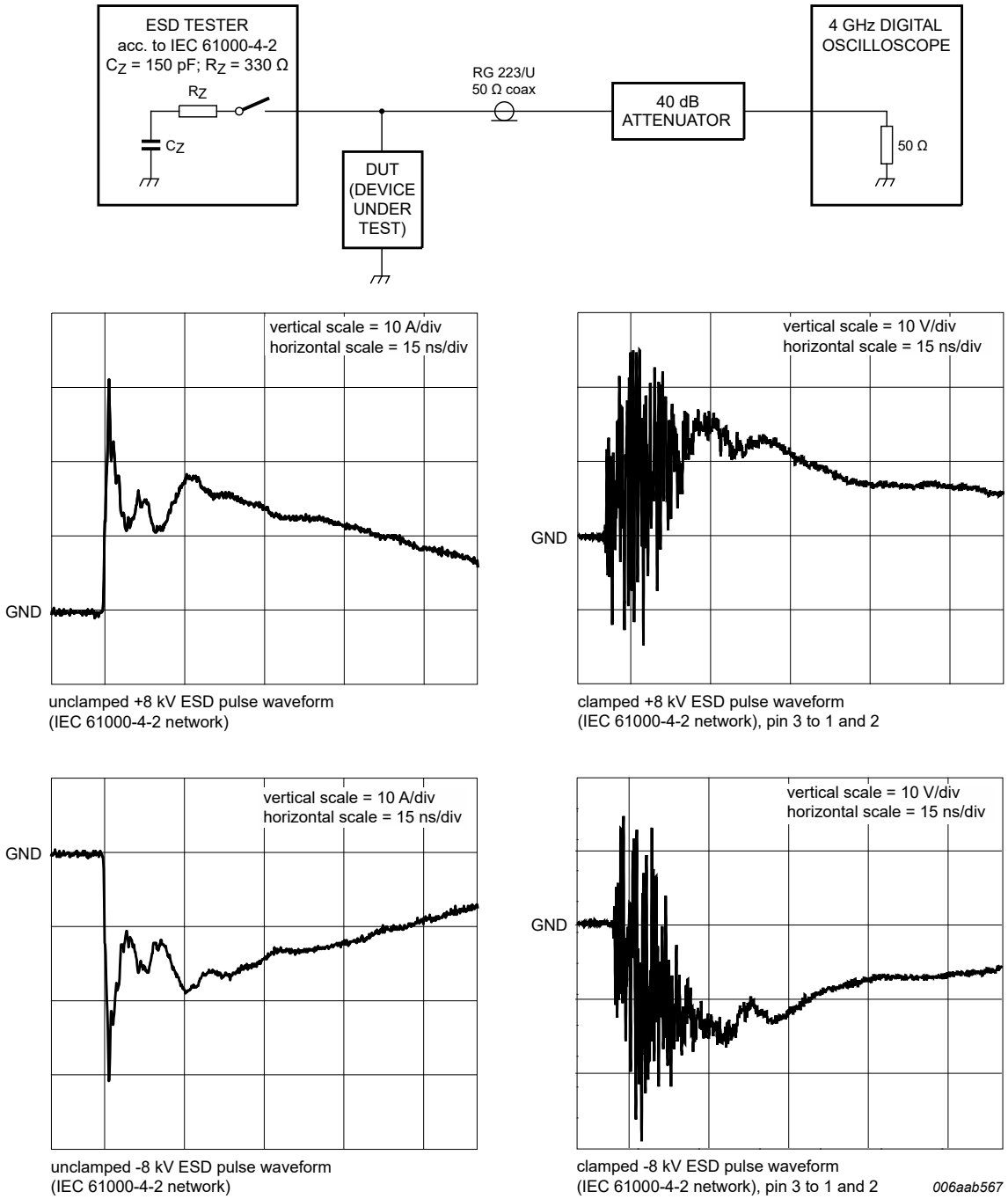


Fig. 7. ESD clamping test setup and waveforms

11. Application information

Protection of a single (high-speed) data line in rail-to-rail configuration. The protected data line is connected to pin 3. Pin 1 is connected to ground (GND) and pin 2 is connected to the supply rail (supply voltage V_{CC}). When the transient voltage exceeds the forward voltage drop of one diode, the transient is directed either to the supply rail or to GND.

The advantages of these solutions are: low line capacitance (0.6 pF typically), fast response time, and low clamping voltage.

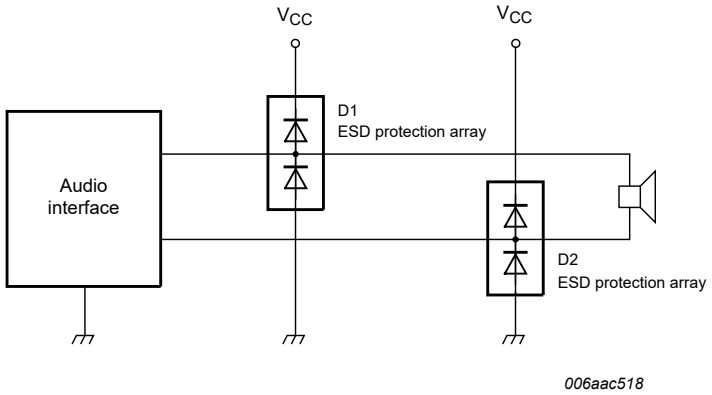


Fig. 8. Application diagram

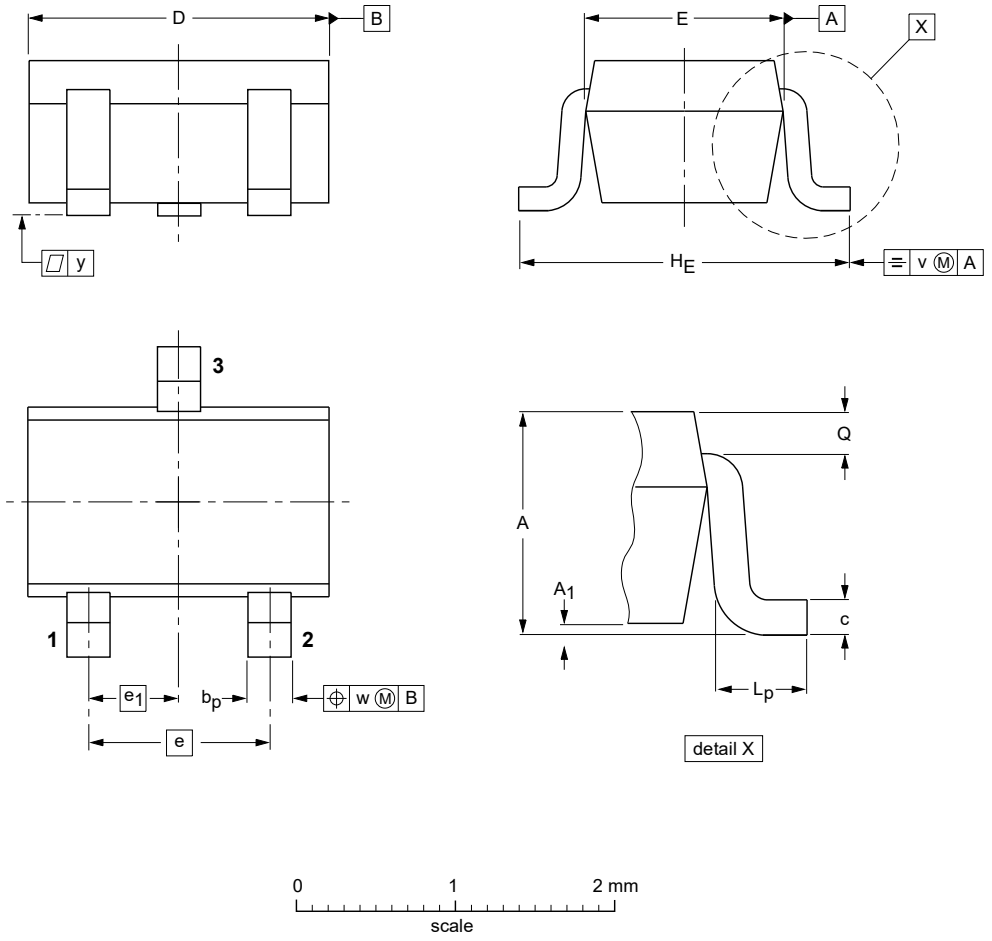
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

12. Package outline

Plastic surface-mounted package; 3 leads **SOT323**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT323			SC-70			~~04-11-04~~ 06-03-16

Fig. 9. Package outline SC-70 (SOT323)

13. Soldering

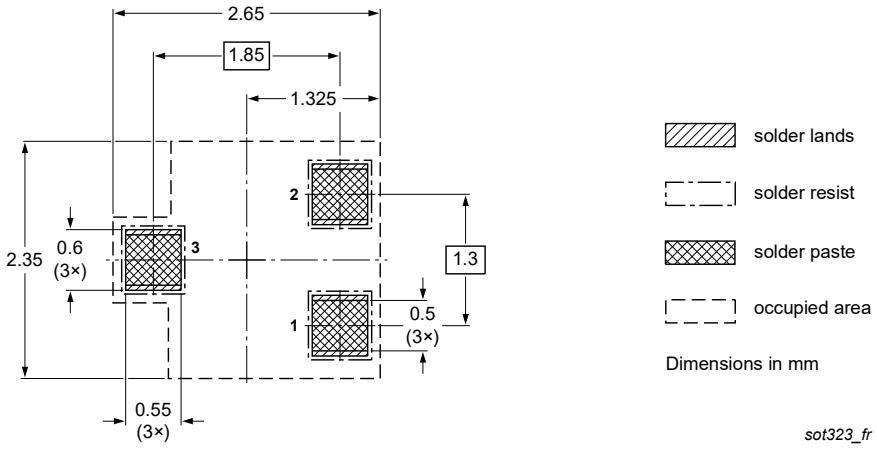


Fig. 10. Reflow soldering footprint for SC-70 (SOT323)

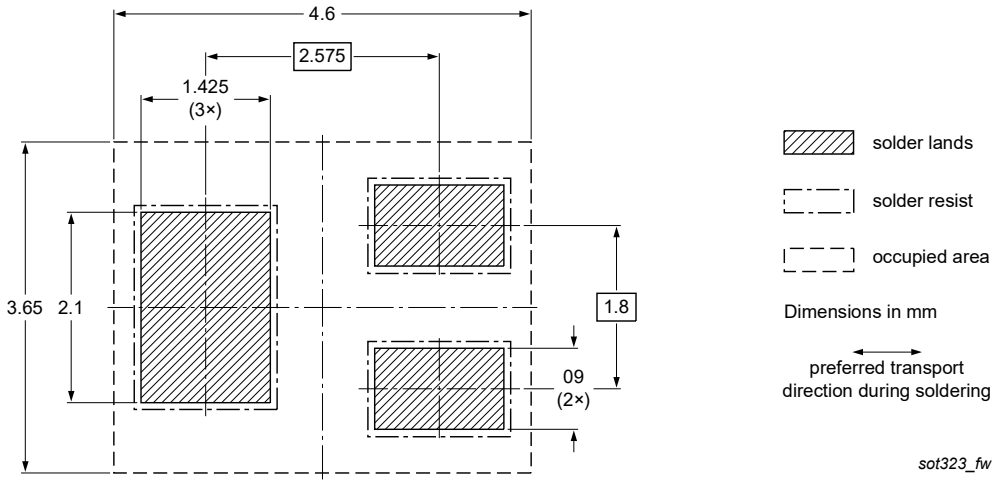


Fig. 11. Wave soldering footprint for SC-70 (SOT323)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NUP1301U v.2	20230414	Product data sheet	-	NUP1301U-Q v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia • Legal texts have been adapted to the new company name where appropriate • Removed table "ESD standards compliance" • Product changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s).			
NUP1301U v.1	20110128	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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