NCL30059

High-Voltage Half-Bridge Controller for LED Lighting Applications

The NCL30059 is a self−oscillating high voltage MOSFET driver primarily tailored for LED driver applications using half−bridge topology. LLC and LCC configurations are supported with optimized wide range control offered by the latter for Constant Current (CC) applications. Due to its proprietary 600 V technology, the driver is useful for bulk voltages utilized in 277 VAC lighting applications. Operating frequency of the driver can be adjusted from 25 kHz to 250 kHz using a single resistor. Adjustable brown−out protection assures correct bulk voltage operating range. An internal 100 ms PFC delay timer ensures the converter is enabled after the bulk voltage is fully stabilized. The device provides fixed dead−time which helps to lower the shoot−through current.

Features

- Wide Operating Frequency Range − from 25 kHz to 250 kHz
- Minimum Frequency Adjust Accuracy ±3%
- Fixed Dead Time − 0.6 μs
- Adjustable Brown−out Protection for a Simple PFC Association
- 100 ms PFC Delay Timer
- Latched Input for Severe Fault Conditions, e.g. Overtemperature or OVP
- Internal 16 V V_{CC} Clamp
- Low Startup Current of 50 μA Maximum
- 1 A / 0.5 A Peak Current Sink / Source Drive Capability
- Operation up to 600 V Bulk Voltage
- Internal Temperature Shutdown
- Supports Outdoor Use: −40°C to +125°C
- PSR Current Regulation ±2%
- Efficiency up to 92%
- SOIC−8 Package
- These are Pb−Free Devices

Typical Applications

- Low Cost Resonant Converters
- Low Parts Count
- CV and CC LED Drivers
- Wide Output Voltage Range LCC Drivers
- Wallpack and Bollard LED Drivers
- High Bay and Streetlight LED Drivers

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MARKING DIAGRAM

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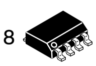

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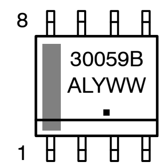
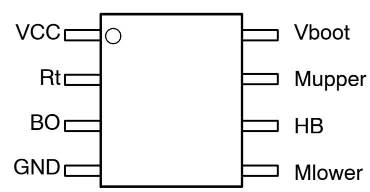
SOIC−8
CASE 751



A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
WW	=	Work Week
▪	=	Pb−Free Package

PINOUT DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NCL30059BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

December, 2018 − Rev. 0

Publication Order Number:
NCL30059/D

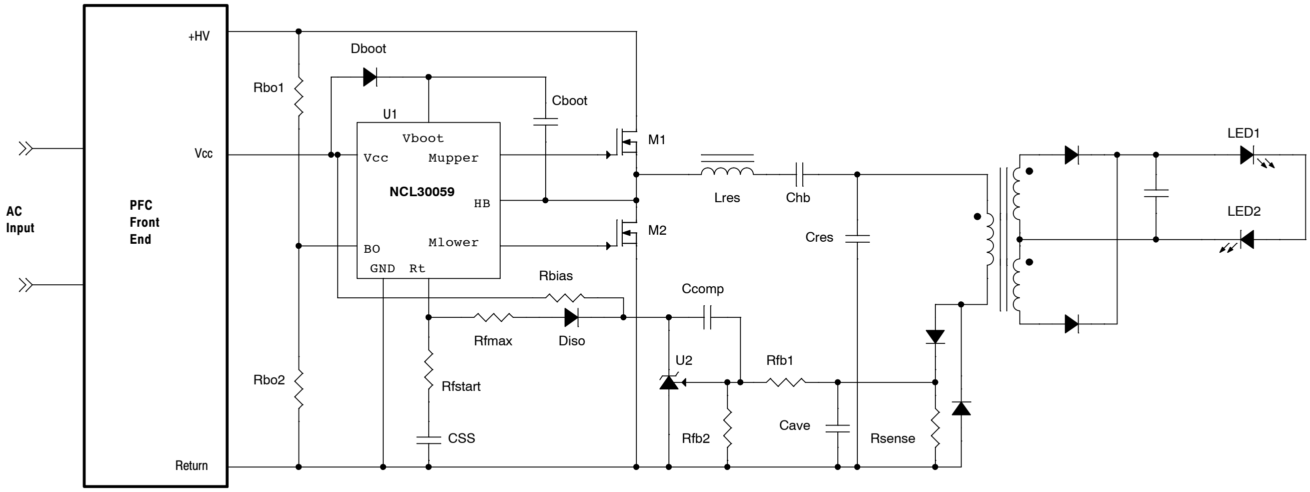


Figure 1. Typical LCC Application Example

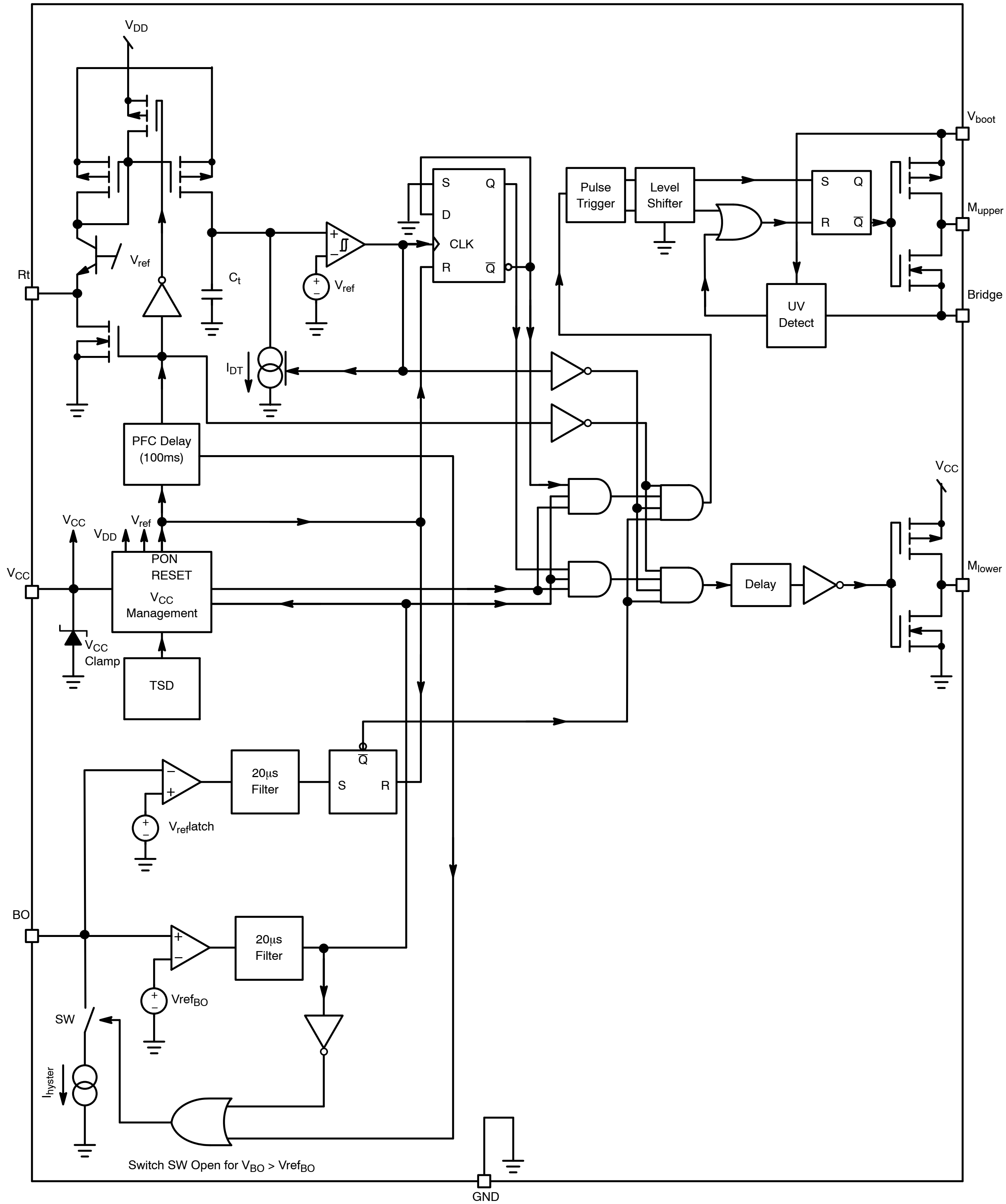


Figure 2. Internal Circuit Architecture

PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Function	Pin Description
1	V_{CC}	Supplies the Driver	The driver accepts up to 16 V (given by internal zener clamp).
2	Rt	Timing Resistor	Connecting a resistor between this pin and GND, sets the operating frequency
3	BO	Brown−Out	Detects low input voltage conditions. When brought above V_{latch}, it fully latches off the driver.
4	GND	IC Ground	−
5	M_{lower}	Low−Side Driver Output	Drives the lower side MOSFET.
6	HB	Half−Bridge Connection	Connects to the half−bridge output.
7	M_{upper}	High−Side Driver Output	Drives the higher side MOSFET.
8	V_{boot}	Bootstrap Pin	The floating supply terminal for the upper stage.

MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
V_{bridge}	High Voltage Bridge Pin − Pin 6	−1 to +600	V
Vboot − Vbridge	Floating Supply Voltage	0 to 20	V
VDRV_HI	High−Side Output Voltage	Vbridge − 0.3 to Vboot + 0.3	V
VDRV_LO	Low−Side Output Voltage	−0.3 to V_{CC} +0.3	V
dVbridge/dt	Allowable Output Slew Rate	±50	V/ns
I_{CC}	Maximum Current that Can Flow into V_{CC} Pin (Pin 1), (Note 1)	20	mA
V_Rt	Rt Pin Voltage	−0.3 to 5	V
	Maximum Voltage, All Pins (Except Pins 4 and 5)	−0.3 to 10	V
$R_{\theta JA}$	Thermal Resistance Junction−to−Air, IC Soldered on 50 mm^2 Cooper 35 μm	178	°C/W
$R_{\theta JA}$	Thermal Resistance Junction−to−Air, IC Soldered on 200 mm^2 Cooper 35 μm	147	°C/W
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, Human Body Model (All Pins Except Pins 1 , 6, 7 and 8)	2	kV
	ESD Capability, Machine Model (All Pins Except Pins 1, 6, 7 and 8)	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains internal zener clamp connected between V_{CC} and GND terminals. Current flowing into the V_{CC} pin has to be limited by an external resistor when device is supplied from supply which voltage is higher than VCC_{clamp} (16 V typically). The I_{CC} parameter is specified for VBO = 0 V.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION						
Turn−On Threshold Level, V_{CC} Going Up	1	VCC_{ON}	10	11	12	V
Minimum Operating Voltage after Turn−On	1	VCC_{min}	8	9	10	V
Startup Voltage on the Floating Section	1	$Vboot_{ON}$	7.8	8.8	9.8	V
Cutoff Voltage on the Floating Section	1	$Vboot_{min}$	7	8	9	V
V_{CC} Level at which the Internal Logic gets Reset	1	VCC_{reset}	–	6.5	–	V
Startup Current, $V_{CC} < VCC_{ON}$, 0°C ≤ T_{amb} ≤ +125°C	1	I_{CC}	–	–	50	μA
Startup Current, $V_{CC} < VCC_{ON}$, −40°C ≤ T_{amb} < 0°C	1	I_{CC}	–	–	65	μA
Internal IC Consumption, No Output Load on Pins 8/7 − 5/4, Fsw = 100 kHz	1	$I_{CC}1$	–	2.2	–	mA
Internal IC Consumption, 1 nF Output Load on Pins 8/7 − 5/4, Fsw = 100 kHz	1	$I_{CC}2$	–	3.4	–	mA
Consumption in Fault Mode (Drivers Disabled, $V_{CC} > V_{CC(min)}$, R_T = 3.5 kΩ)	1	$I_{CC}3$	–	2.56	–	mA
Consumption During PFC Delay Period, 0°C ≤ T_{amb} ≤ +125°C		$I_{CC}4$	–	–	400	μA
Consumption During PFC Delay Period, −40°C ≤ T_{amb} < 0°C		$I_{CC}4$	–	–	470	μA
Internal IC Consumption, No Output Load on Pin 8/7 F_{WS} = 100 kHz	8	I_{boot1}	–	0.3	–	mA
Internal IC Consumption, 1 nF Output Load on Pin 8/7 F_{WS} = 100 kHz	8	I_{boot2}	–	1.44	–	mA
Consumption in Fault Mode (Drivers Disabled, $V_{boot} > Vboot_{min}$)	8	I_{boot3}	–	0.1	–	mA
V_{CC} Zener Clamp Voltage @ 20 mA	1	VCC_{clamp}	15.4	16	17.5	V
INTERNAL OSCILLATOR						
Minimum Switching Frequency, R_t = 35 kΩ on Pin 2, D_T = 600 ns	2	F_{SW} min	24.25	25	25.75	kHz
Maximum Switching Frequency, R_t = 3.5 kΩ on Pin 2, D_T = 600 ns	2	F_{SW} max	208	245	282	kHz
Reference Voltage for all Current Generations	2	V_{ref} RT	3.33	3.5	3.67	V
Internal Resistance Discharging $C_{soft−start}$	2	$Rt_{discharge}$	–	500	–	Ω
Operating Duty Cycle Symmetry	5, 7	DC	48	50	52	%

NOTE: Maximum capacitance directly connected to Pin 2 must be under 100 pF.

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
DRIVE OUTPUT						
Output Voltage Rise Time @ CL = 1 nF, 10−90% of Output Signal	5, 7	T_r	–	40	–	ns
Output Voltage Fall Time @ CL = 1 nF, 10−90% of Output Signal	5, 7	T_f	–	20	–	ns
Source Resistance	5, 7	R_{OH}	–	12	–	Ω
Sink Resistance	5, 7	R_{OL}	–	5	–	Ω
Dead−Time (Measured Between 50% of Rise and Fall Edge)	5,7	T_dead	540	610	720	ns
Leakage Current on High Voltage Pins to GND (600 Vdc)	6,7,8	IHV_Leak	–	–	5	μA
PROTECTION						
Brown−Out Input Bias Current	3	IBO_{bias}	–	0.01	–	μA
Brown−Out Level	3	V_{BO}	0.95	1	1.05	V
Hysteresis Current, V_{pin3} < VBO	3	I_{BO}	15.6	18.2	20.7	μA
Latching Voltage on BO Pin	3	V_{latch}	1.9	2	2.1	V
Propagation Delay Before Drivers are Stopped	3	EN Delay	–	20	–	μs
Delay Before Any Driver Restart	–	PFC Delay	–	100	–	ms
Temperature Shutdown (Guaranteed by design)	–	TSD	140	–	–	°C
Hysteresis	–	TSD_{hyste}	–	30	–	°C

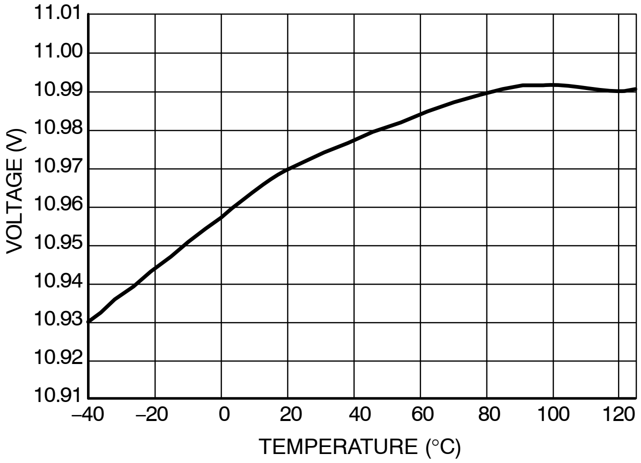


Figure 3. V_{CCon}

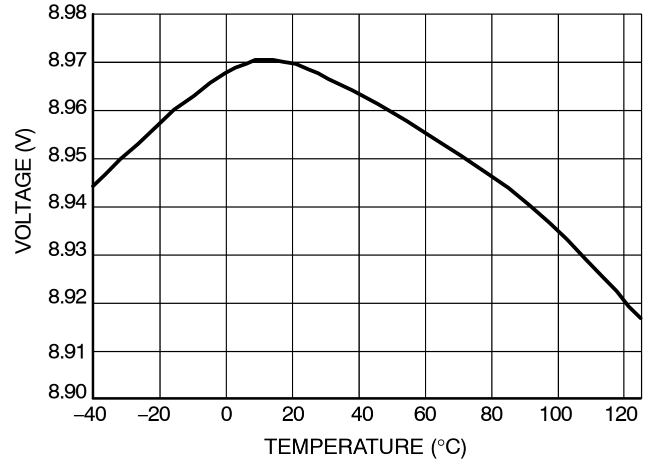


Figure 4. V_{CCmin}

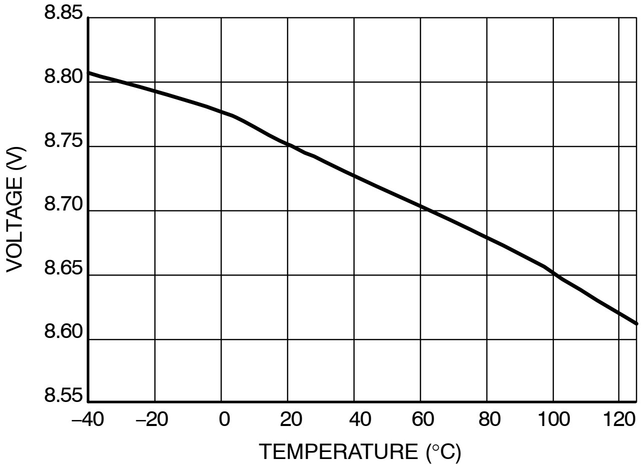


Figure 5. V_{BOOTon}

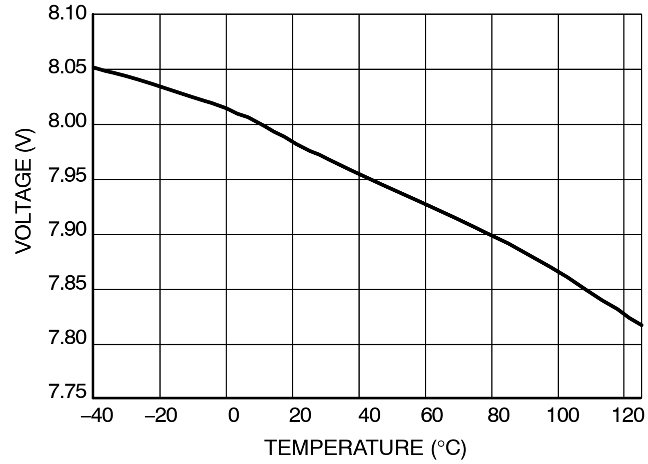


Figure 6. $V_{BOOTmin}$

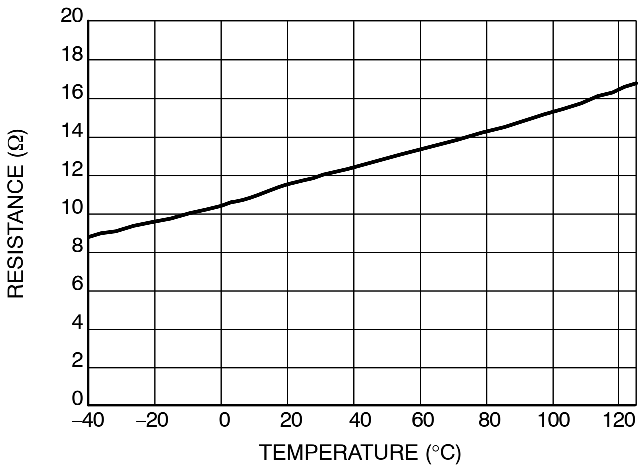


Figure 7. R_{OH}

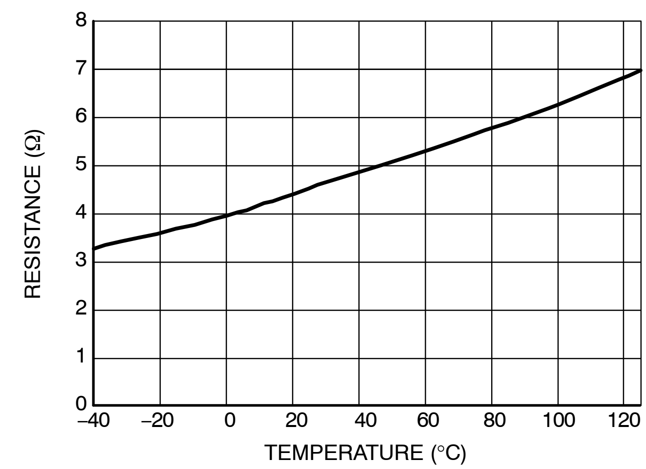


Figure 8. R_{OL}

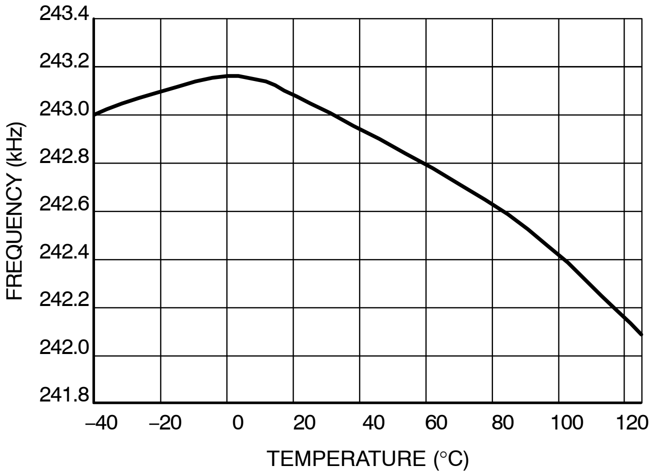


Figure 9. F_{SWmax}

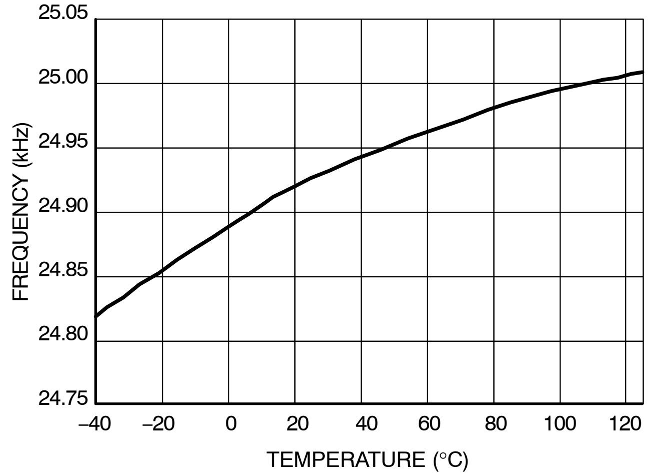


Figure 10. F_{SWmin}

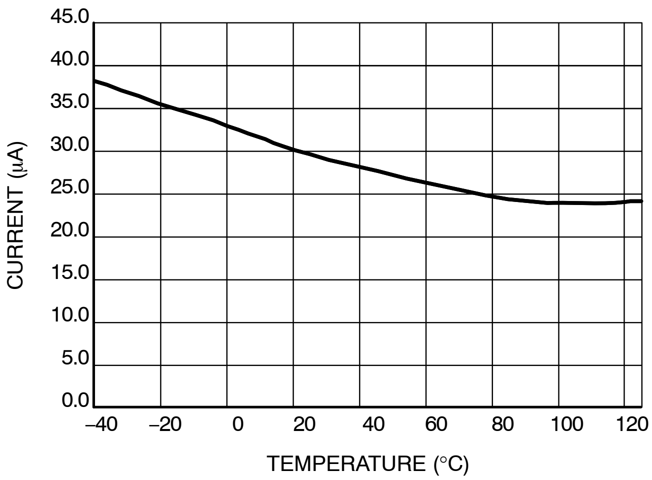


Figure 11. $I_{CC\_startup}$

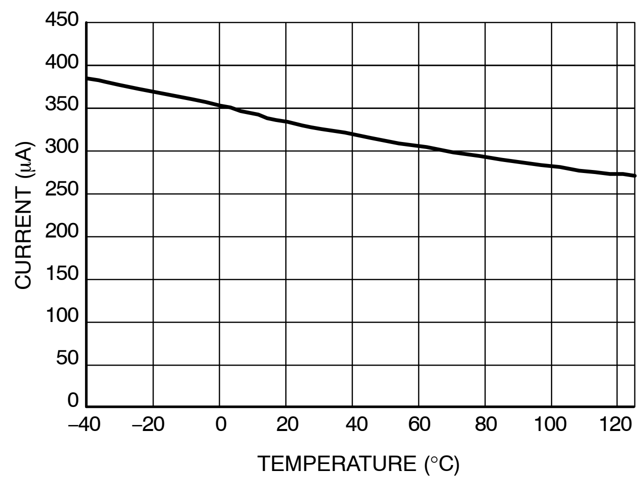


Figure 12. I_{CC4}

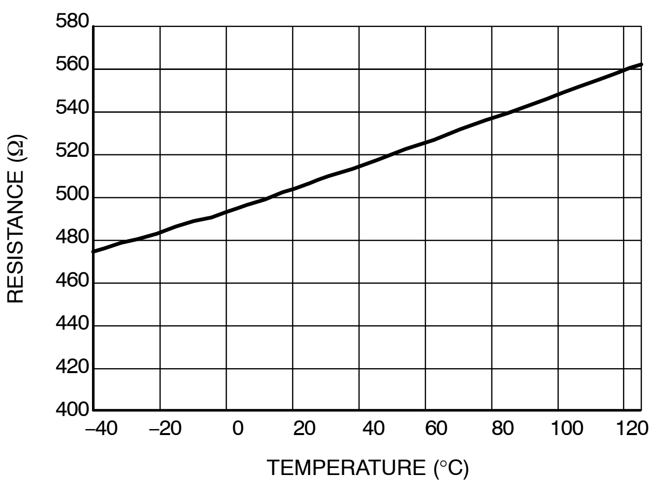


Figure 13. $R_{t\_discharge}$

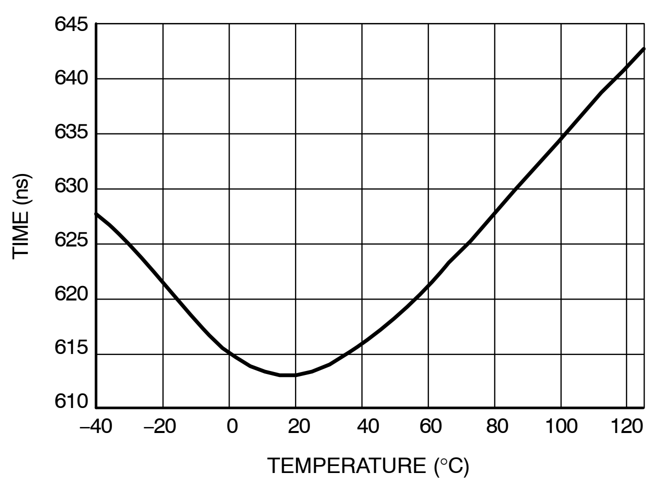


Figure 14. T_{dead}

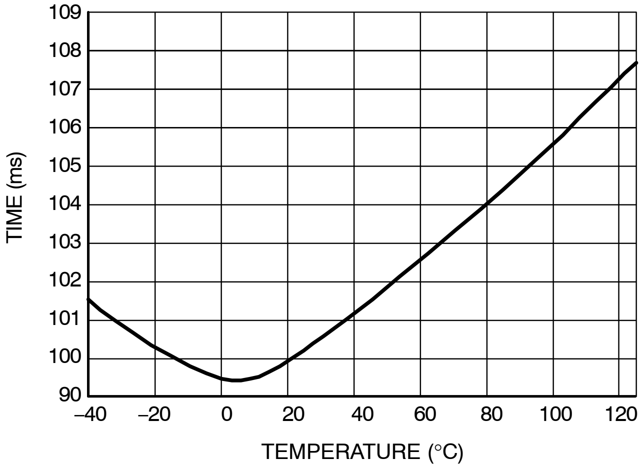


Figure 15. PFC_{delay}

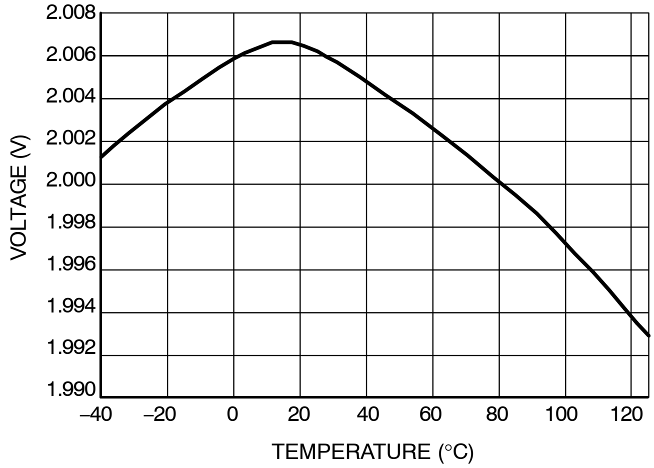


Figure 16. V_{LATCH}

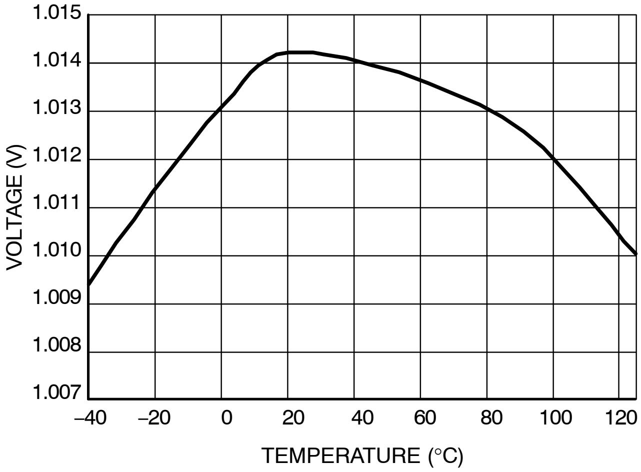


Figure 17. V_{BO}

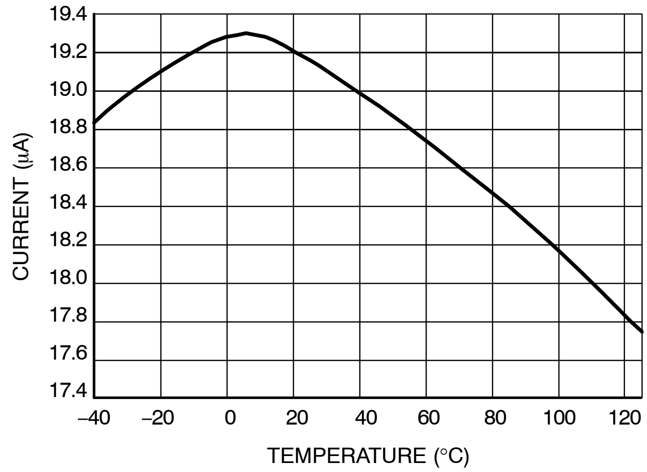


Figure 18. I_{BO}

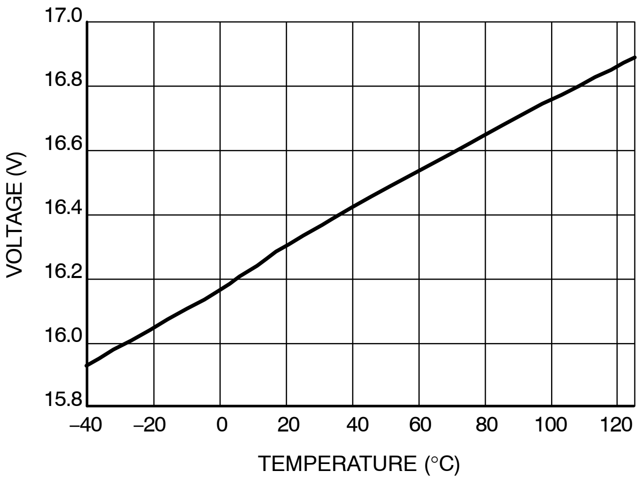


Figure 19. V_{CC_clamp}

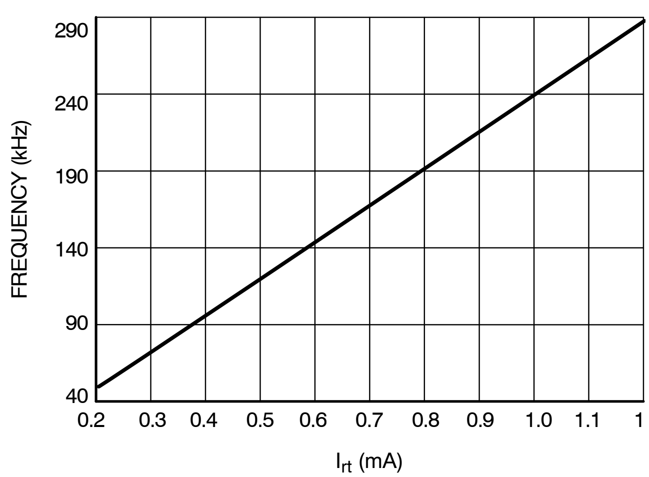


Figure 20. I_{rt} and Appropriate Frequency

APPLICATION INFORMATION

The NCL30059 is primarily intended to drive low cost half−bridge applications. It supports LLC and optimized LCC topologies offering wide output voltage range in constant current (CC) mode making it ideal for LED drivers. The IC includes several features that help the designer to cope with resonant SPMS design. All features are described thereafter:

- **Wide Operating Frequency Range**: The internal current controlled oscillator is capable to operate over wide frequency range up to 250 kHz. Minimum frequency accuracy is ±3%.
- **Fixed Dead−Time**: Internal dead−time control is optimized to avoid cross conduction or shoot−through during transitions between low and high side conduction.
- **100 ms PFC Timer**: Fixed delay is placed to IC operation whenever the driver restarts (VCC_{ON} or BO_OK detect events). This delay assures that the bulk voltage will be stabilized prior to switching operation. Another benefit of this delay is that the soft start capacitor will be fully discharged before any restart.
- **Brown−Out Detection**: The BO input monitors bulk voltage level via resistor divider and thus assures that the application is working only for wanted bulk voltage band. The BO input sinks current of 18.2 μA until the $Vref_{BO}$ threshold is reached. Designer can thus adjust the bulk voltage hysteresis according to the application needs.
- **Latched Input**: The latched comparator input is connected in parallel to the BO terminal to allow the designer latch the IC if necessary − overvoltage or overtemperature shutdown can be implemented using this latch. The supply voltage has to be cycled down below VCC_{reset} threshold, or V_{BO} diminished under V_{BO} level to reset the latch and enable restart.
- **Internal V_{CC} Clamp**: The internal zener clamp offers a way to prepare passive voltage regulator to maintain V_{CC} voltage at 16 V in case the controller is supplied from unregulated power supply or from bulk capacitor.
- **Low Startup Current**: This device features maximum startup current of 50 μA which allows the designer to use high value startup resistor for applications when driver is supplied from the auxiliary winding. Power dissipation of startup resistor is thus significantly reduced.

Current Controlled Oscillator

The current controlled oscillator features a high−speed circuitry allowing operation from 50 kHz up to 500 kHz. However, as a division by two internally creates the two Q and $\overline{Q}$ outputs, the final effective signal on output Mlower and Mupper switches between 25 kHz and 250 kHz. The VCO is configured in such a way that if the current that flows out from the Rt pin increases, the switching frequency also goes up. Figure 21 shows the architecture of this oscillator.

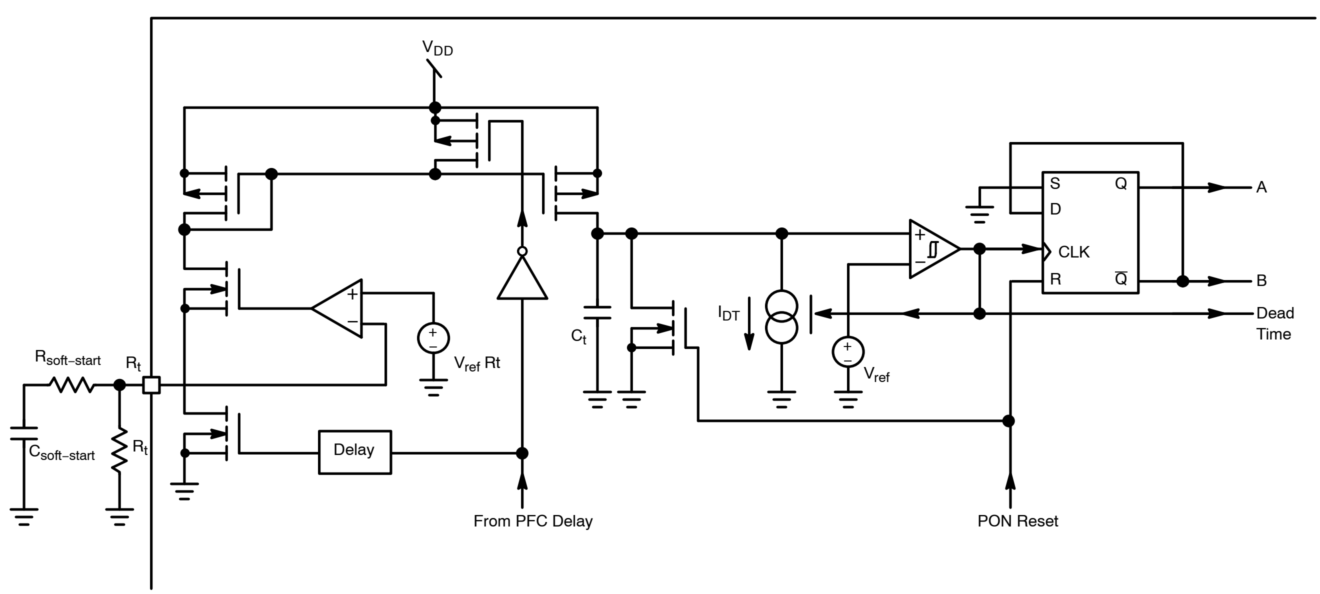


Figure 21. The Internal Current Controlled Oscillator Architecture

The internal timing capacitor Ct is charged by current which is proportional to the current flowing out from the Rt pin. The discharging current I_{DT} is applied when voltage on this capacitor reaches 2.5 V. The output drivers are disabled during discharge period so the dead time length is given by the discharge current sink capability. Discharge sink is disabled when voltage on the timing capacitor reaches zero and charging cycle starts again. The charging current and thus also whole oscillator is disabled during the PFC delay period to keep the IC consumption below 400 μA. This is valuable for applications that are supplied from auxiliary winding and V_{CC} capacitor is supposed to provide energy during PFC delay period.

For resonant LED driver applications it is necessary to adjust minimum operating frequency with high accuracy. The designer also needs to limit maximum operating and startup frequency. All these parameters can be adjusted using few external components connected to the Rt pin as depicted in Figure 22.

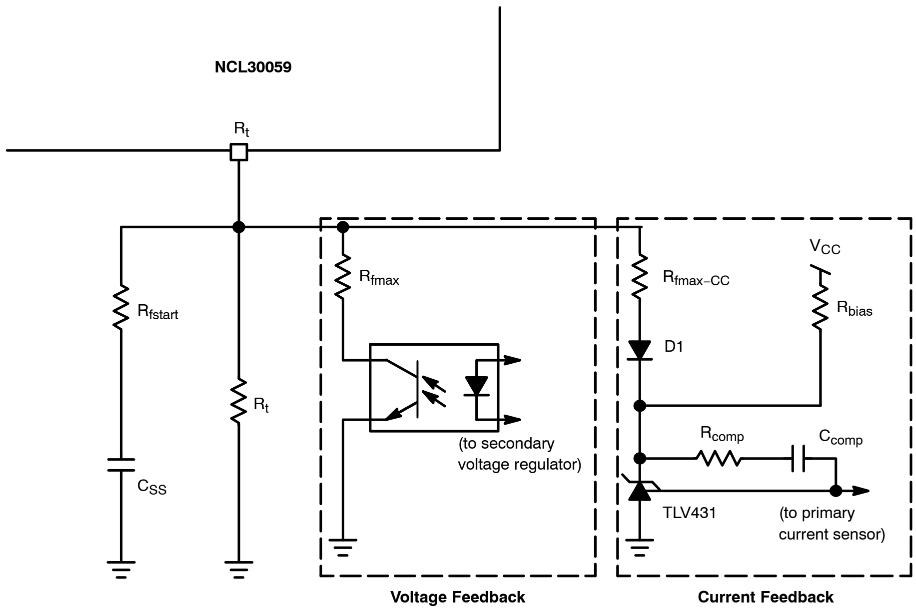


Figure 22. Typical Rt Pin Connection

The minimum switching frequency is given by the Rt resistor value. This frequency is reached if there is no optocoupler or current feedback action and soft start period has been already finished. The maximum switching frequency excursion is limited by the Rf_{max} selection. Note that the F_{max} value is influenced by the optocoupler saturation voltage value. Resistor Rf_{start} together with capacitor C_{SS} prepares the soft start period after PFC timer elapses. The Rt pin is grounded via an internal switch during the PFC delay period to assure that the soft start capacitor will be fully discharged via Rfstart resistor.

Constant LED current is achieved using a feedback loop monitoring the primary current. The sensing voltage must be scaled by the turns ratio of the transformer. The Rt pin reference voltage is $Vref_{Rt}$ = 3.5 V. The control regulator operates on the difference between the Rt pin reference voltage and the minimum voltage compliance of the regulator. This voltage difference is applied across $R_{fmax-CC}$.

The TLV431 shunt regulator is used in Figure 22 as the constant current control regulator. Diode D1 is used to establish minimum regulator bias current via resistor R_{bias}. Total saturation voltage of this solution is 1.25 + 0.6 = 1.85 V for room temperature. Shottky diode will further decrease saturation voltage. The Rf_{max-CC} resistor limits the maximum frequency delivered by this regulation loop. This parameter is affected by D1 temperature drift.

Brown−Out Protection

The Brown−Out circuitry (BO) offers a way to protect the application from low DC input voltages. Operation is blocked below a set threshold. Hysteresis is provided by the switched current source providing stable operation. The internal circuitry, depicted by Figure 23, offers a way to monitor the high−voltage (HV) rail.

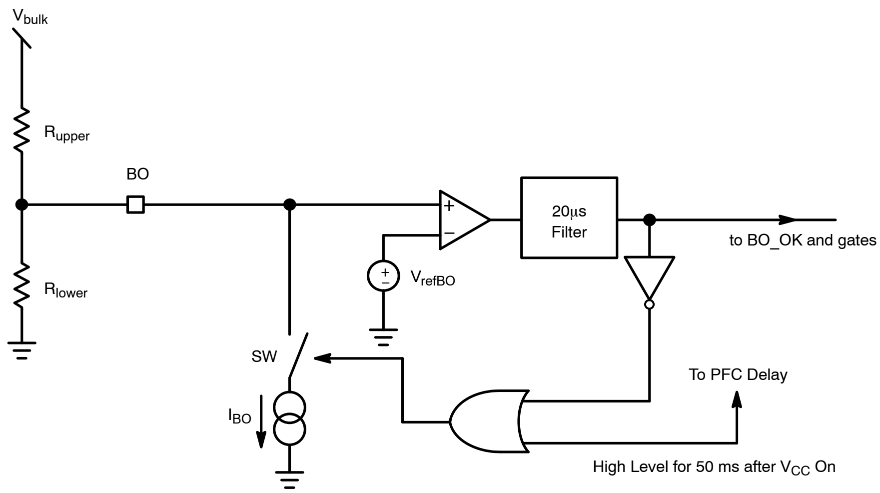


Figure 23. The internal Brown−Out Configuration with an Offset Current Sink

A resistive divider made of R_{upper} and R_{lower}, brings a portion of the HV rail on Pin 3. Below the turn−on level, the 18.2 µA current sink (I_{BO}) is on. Therefore, the turn−on level is higher than the level given by the division ratio brought by the resistive divider. To the contrary, when the internal BO_OK signal is high (PFC timer runs or Mlower and Mupper pulse), the I_{BO} sink is deactivated. As a result, it becomes possible to select the turn−on and turn−off levels via a few lines of algebra:

I_{BO} is ON

$$Vref_{BO} = V_{bulk1} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} - I_{BO} \cdot \left(\frac{R_{lower} \cdot R_{upper}}{R_{lower} + R_{upper}}\right) \quad \text{(eq. 1)}$$

I_{BO} is OFF

$$Vref_{BO} = V_{bulk2} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} \quad \text{(eq. 2)}$$

We can extract R_{lower} from Equation 2 and plug it into Equation 1, then solve for R_{upper}:

$$R_{lower} = Vref_{BO} \cdot \frac{V_{bulk1} - V_{bulk2}}{I_{BO} \cdot \left(V_{bulk2} - Vref_{BO}\right)} \quad \text{(eq. 3)}$$

$$R_{upper} = R_{lower} \cdot \frac{V_{bulk2} - Vref_{BO}}{Vref_{BO}} \quad \text{(eq. 4)}$$

If we decide to turn−on our converter for V_{bulk1} equals 350 V and turn it off for V_{bulk2} equals 250 V, then for I_{BO} = 18.2 µA and $Vref_{BO}$ = 1.0 V we obtain:

R_{upper} = 5.494 MΩ

R_{lower} = 22.066 V

The bridge power dissipation is 400^2 / 5.517 MΩ = 29 mW when front−end PFC stage delivers 400 V. Figure 24 simulation result confirms our calculations.

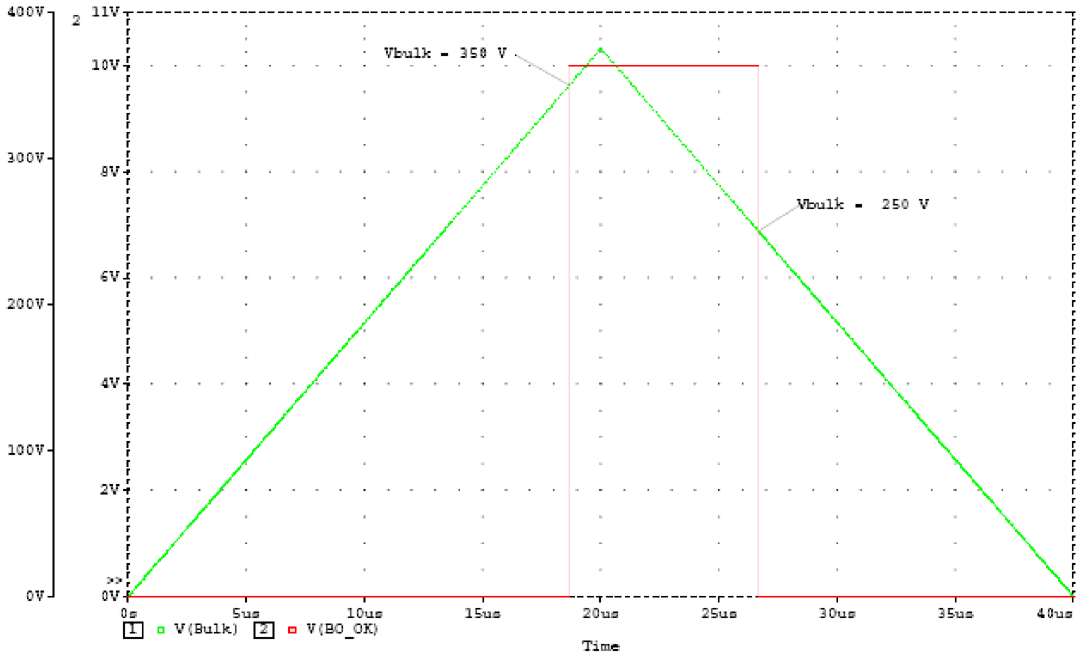


Figure 24. Simulation Results for 350/250 ON/OFF Brown−Out Levels

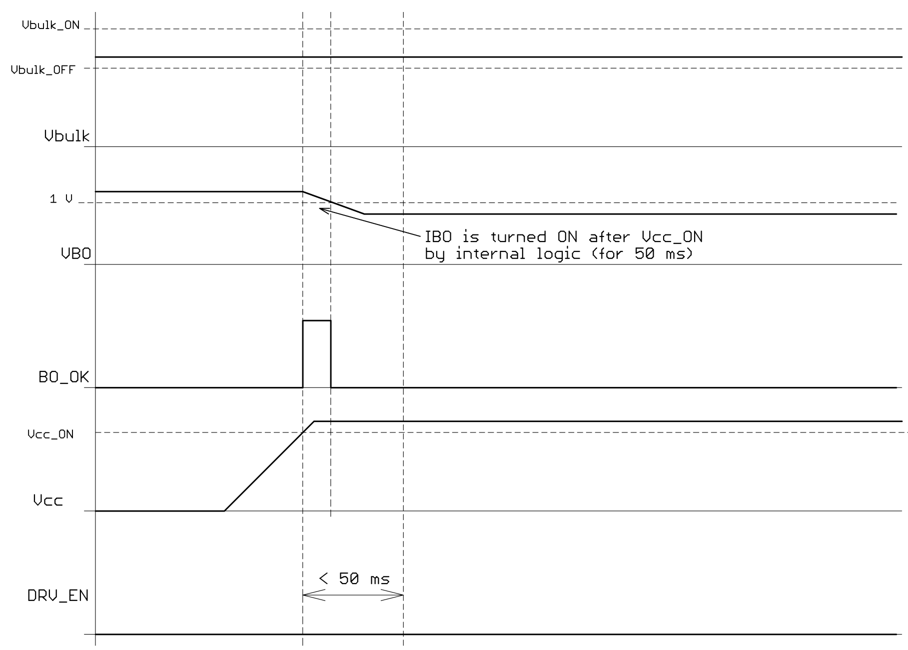


Figure 25. BO Input Functionality − $V_{bulk2} < V_{bulk} < V_{bulk1}$

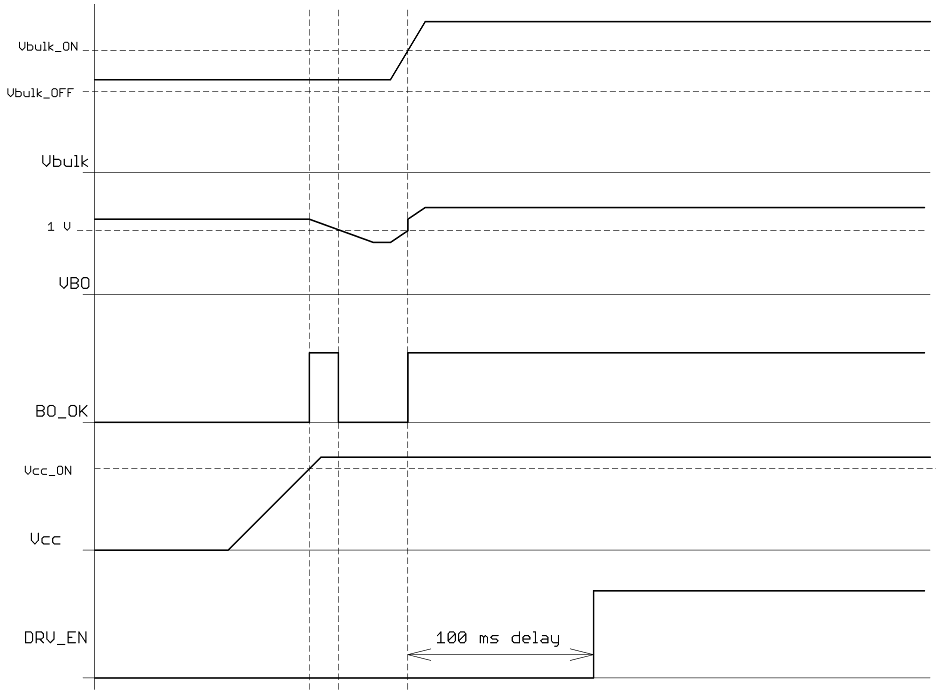


Figure 26. BO Input Functionality –V_{bulk2} < V_{bulk} < V_{bulk1}, PFC Start Follows

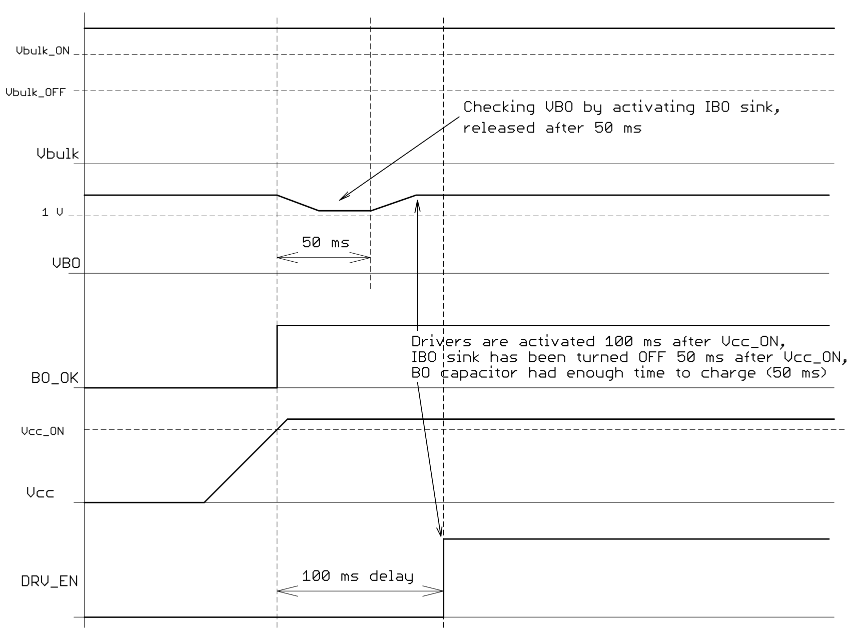


Figure 27. BO Input Functionality – V_{bulk} > V_{bulk1}

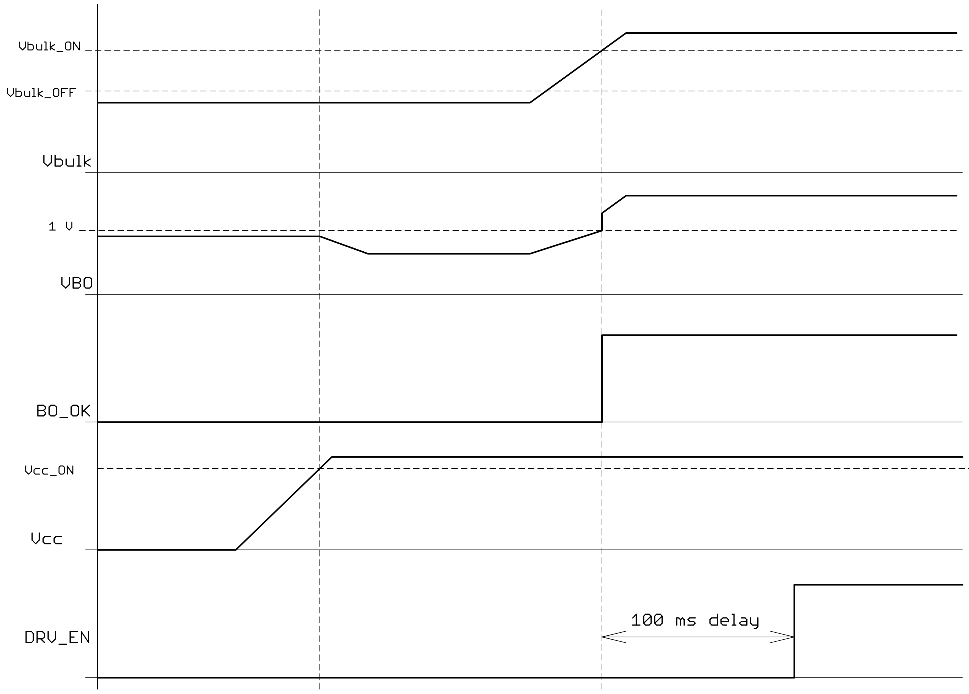


Figure 28. BO Input Functionality – V_{bulk} < V_{bulk2}, PFC Start Follows

The I_{BO} current sink is turned ON for 50 ms after any controller restart to let the BO input voltage stabilize (there can be connected big capacitor to the BO input and the I_{BO} is only 18.2 μA so it will take some time to discharge). Once the 50 ms one shoot pulse ends the BO comparator is supposed to either hold the I_{BO} sink turned ON (if the bulk voltage level is not sufficient) or let it turned OFF (if the bulk voltage is higher than V_{bulk1}). See Figures 25 through 28 for better understanding on how the BO input works.

Latched−Off Protection

There are some situations where the converter shall be fully turned−off and stay latched. This can happen in presence of an overvoltage (the feedback loop is drifting) or when an overtemperature is detected. Due to the addition of a comparator on the BO Pin, a simple external circuit can lift up this pin above V_{latch} (2 V typical) and permanently disable pulses. The V_{CC} needs to be cycled down below 6.5 V typically to reset the controller.

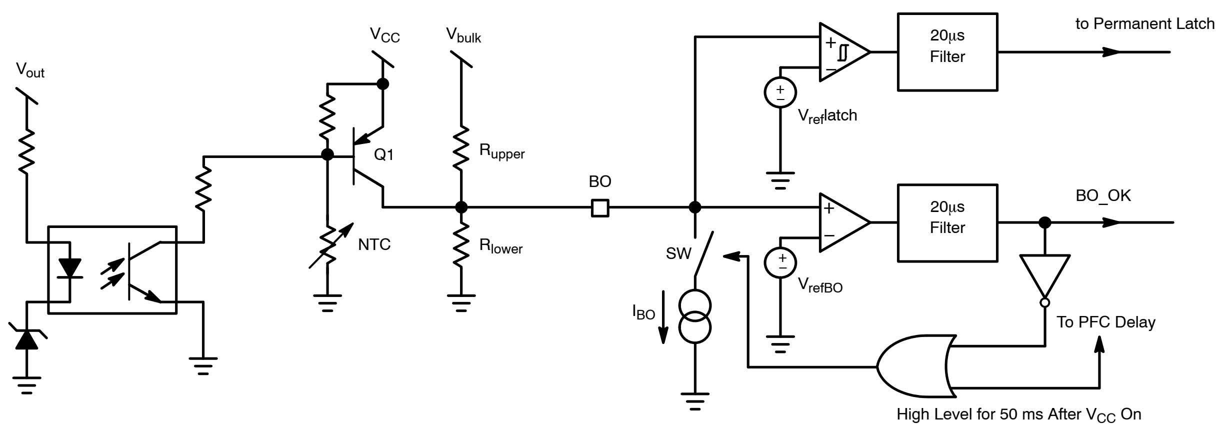


Figure 29. Adding a Comparator on the BO Pin Offers a Way to Latch−Off the Controller

On Figure 29, Q1 is biased off and does not affect the BO measurement as long as the NTC and the optocoupler are not activated. As soon as the secondary optocoupler senses an OVP condition, or the NTC reacts to a high ambient temperature, Q1 base is biased on and the BO Pin goes up, permanently latching off the controller.

The High−Voltage Driver

Figure 30 shows the internal architecture of the high−voltage section. The device incorporates an upper UVLO circuitry that makes sure enough V_{gs} is available for the upper side MOSFET. The V_{CC} for floating driver section is provided by C_{boot} capacitor that is refilled by external bootstrap diode.

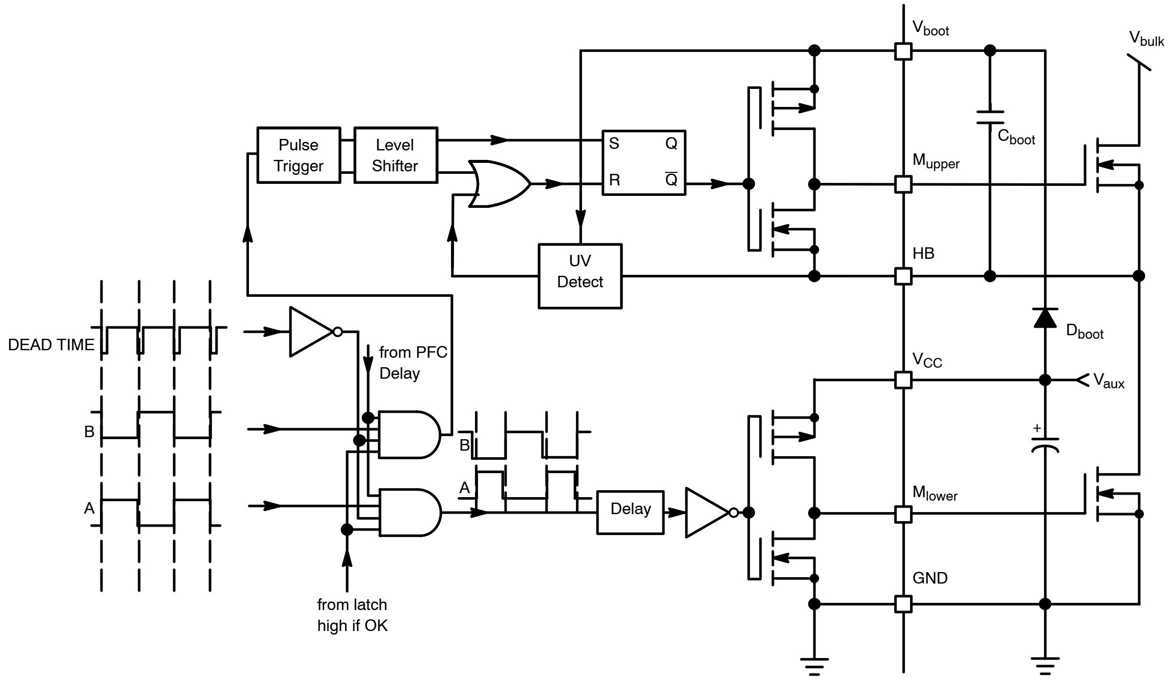
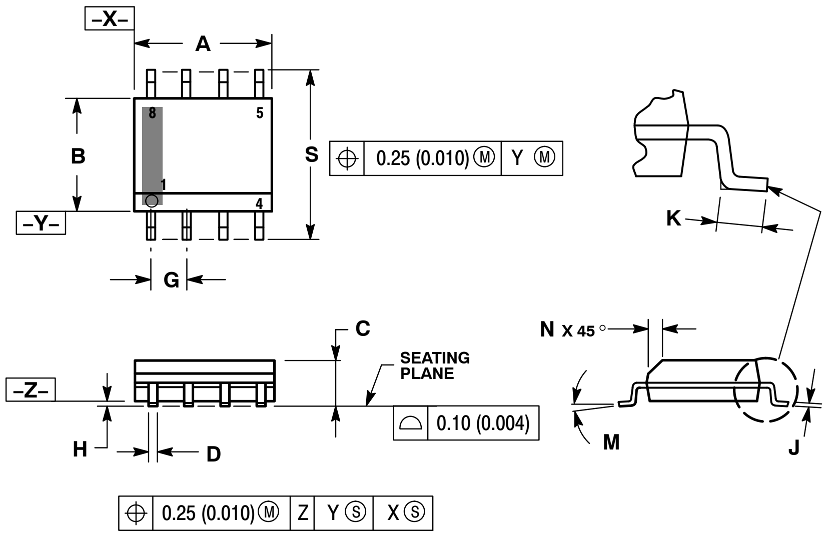


Figure 30. The Internal High−Voltage Section of the NCL30059

The A and B outputs are delivered by the internal logic, as depicted in block diagram. This logic is constructed in such a way that the M_{lower} driver starts to pulse firs after any driver restart. The bootstrap capacitor is thus charged during first pulse. A delay is inserted in the lower rail to ensure good matching between these propagating signals. As stated in the maximum rating section, the floating portion can go up to 600 Vdc and makes the IC perfectly suitable for offline applications featuring a 400 V PFC front−end stage.

PACKAGE DIMENSIONS

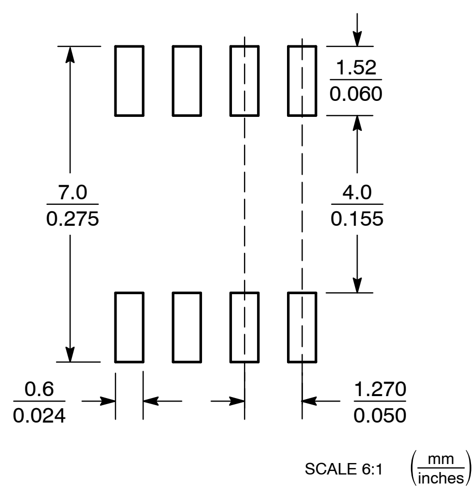
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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