MityDSP™ Document

Document: MityDSP-L138F, MitySOM-1808F, and MityDSP-6748F Carrier Board Design Guide

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1 Overview

1.1 Fast Facts for Getting Started

Facts	MityDSP-L138F, MitySOM-1808F, MityDSP-6748F
Required socket connector	FCI 10033853-152FSLF
Voltages required	3.3V
Supported I/O standards	LVTTL, LVCMOS33, LVCMOS25*, LVDS25*, LVCMOS18*
Total number of FPGA I/O's	96
Number of LVDS capable I/O's	48 pairs
SOC Peripherals**	3x UART, 2x SPI, EMAC (MII or RMII), 2x I2C, McASP, 2x McBSP
*Requires external bank voltage supply according to standard **SOC peripherals share pins, see SOC datasheet for specific pin-multiplexing options	

1.2 Introduction

The MityDSP-L138F, MitySOM-1808F, and MityDSP-6748F modules are System On Modules (SOMs) designed to be easy to integrate into an end-user embedded system. The modules integrate many crucial elements of an embedded system, and do so with an established design framework utilizing a common set of core libraries. End-user design of the application PCB is also intended to be as simple as possible, allowing the PCB designer to concentrate on the custom I/O interfaces – especially analog & mixed-signal – instead of getting distracted with the learning curve of designing a brand new embedded digital system from scratch.

1.3 MityDSP-L138F Family Modules

The MityDSP-L138F, MitySOM-1808F, and MityDSP-6748F family of modules represents a 3rd generation SOM in the MityDSP product line. These modules are based on a Texas Instruments OMAP-L138, Sitara-1808, and the TMS320C6748 System On Chip (SOC) modules, respectively. Each of these SOC modules are pin compatible devices that employ one or both of an ARM 9 core and a DSP 674x floating point DSP core according to the table below.

Core	OMAP-L138	Sitara-1808	TMS320C6748
ARM926EJ-S 300/375/456 MHz	Y	Y	N
DSP 674X Floating Point DSP 300/375/456 MHz	Y	N	Y

Each module includes power management, DDR2 SDRAM, NAND and NOR Flash memories, and is interfaced by a 200-pin low-profile SO-DIMM card-edge connector. The modules also integrate a Xilinx Spartan6 FPGA for end-user customizable logic and I/O interfaces beyond the capability of the SOC device. Carrier board design for these types of MityDSP is the main focus of this document.

The 2nd generation module, the MityDSP-Pro (MityDSP-6455), is based on a Texas Instruments TMS320C645x DSP, includes DDR2 SDRAM and Flash memories, and is interfaced by the same 200-pin SO-DIMM card-edge connector and a 100-pin high-density, low-profile Hirose connector. The module integrates a large Xilinx Spartan3 FPGA for implementing required on-board logic and I/O interfaces, and also for end-user customizable logic and I/O interfaces. The module also incorporates a number of high bandwidth I/O interfaces including: PCI/HPI, Serial RapidIO, and Gigabit Ethernet interfaces provided by the DSP; and DDR SDRAM dedicated to the FPGA.

The 1st generation family of modules, the MityDSP and MityDSP-XM (MityDSP-6711 and MityDSP-6711XM), are based on a Texas Instruments TMS3206711 DSP, include SDRAM and Flash memories, and are interfaced using a 144-pin SO-DIMM card edge connector. The module integrates a Xilinx Spartan 3 FPGA for implementing required on-board logic and I/O interfaces.

All types of MityDSP are available with options for speed grade, memory size, FPGA size (or complete removal), operating temperature ranges, and RoHS / non-RoHS compliance. Please contact Critical Link for the current list of MityDSP and MitySOM variants.

1.4 MityDSP-L138 Family Modules (No FPGA)

An available option to the MityDSP-L138F family of modules is a module with no Spartan6 FPGA. This unit is slightly less expensive than its sister module that includes the FPGA and has been reduced in size. The unit also requires less power to run. The IO pins previously reserved for the FPGA have been routed to additional peripheral interfaces on the SOC processor. The difference in the part name is the lack of the “F” at the end. See the datasheets and design guide for these parts for pin-out information.

1.5 Module Dimensions

A dimensioned drawing of module is included below in Figure 1.

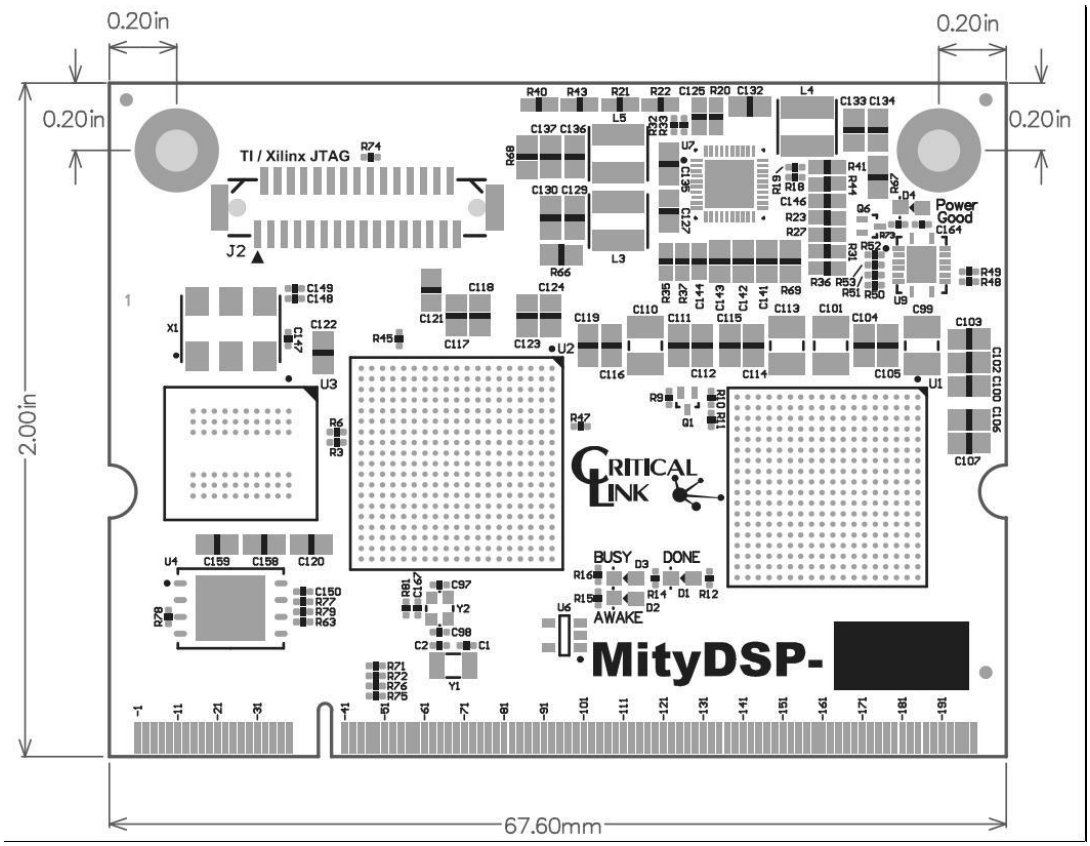

Figure 1: MityDSP-L138F, MitySOM-1808F, MityDSP-6748F Mechanical Drawing

2 Connectors

All types of MityDSP utilize SO-DIMM style edge-connectors for main connectivity with the end user application PCB. These connectors were chosen for their high density, compact size, ease of procurement, and low cost. With edge connectors, a physical socket component is only required on one side – the main PCB side. The SO-DIMM standard also allows the MityDSP module to lay flat, in parallel with the main PCB, as they were intended for use by memory modules in compact equipment, such as laptops.

2.1 Card-edge compatibility

The original MityDSP-L138F family of SOMs is designed to plug into a 200-pin SO-DIMM DDR2 RAM socket. These sockets are used for memory on PC laptop systems. Please note that the MityDSP is NOT electrically compatible with the DDR2 socket standard, and intermixing modules/sockets from the two standards would very possibly cause permanent damage to one or both sides.

2.2 MityDSP-L138F Module Pin-out

Table 1: MityDSP-L138F, MitySOM-1808F, and MityDSP-6748F Card-edge (J100) Pin-out

Pin	I/O	Signal	Pin	I/O	Signal
1	-	+3.3 V in	2	-	+3.3 V in
3	-	+3.3 V in	4	-	+3.3 V in
5	-	+3.3 V in	6	-	+3.3 V in
7	-	GND	8	-	GND
9	-	GND	10	-	GND
11	I	RESET_IN#	12		EXT_BOOT#
13	O	SATA_TX_P	14	I/O	GP0_7
15	O	SATA_TX_N	16	I/O	GP0_10
17	I	SATA_RX_P	18	I/O	GP0_11
19	I	SATA_RX_N	20	I/O	GP0_15
21	I	USB0_ID	22	I/O	GP0_6
23	I/O	USB1_D_N	24	I/O	GP0_14
25	I/O	USB1_D_P	26	I/O	GP0_12
27	O	USB0_VBUS	28	I/O	GP0_5
29	I/O	USB0_D_N	30	I/O	GP0_13
31	I/O	USB0_D_P	32	I/O	GP0_1
33	O	USB0_DRVVBUS	34	I/O	GP0_4
35	-	3V RTC Battery	36	I/O	GP0_3
37	-	+3.3 V in	38	-	+3.3 V in
39	-	+3.3 V in	40	-	+3.3 V in
41	-	GND	42	-	GND
43	I/O	SPI1_MISO	44	I/O	GP0_2

Pin	I/O	Signal	Pin	I/O	Signal
45	I/O	SPI1_MOSI	46	I/O	GP0_0
47	I/O	SPI1_ENA	48	I/O	GP0_8
49	I/O	SPI1_CLK	50	I/O	GP0_9
51	I/O	SPI1_SCS1	52	I/O	MMCSD0_DAT7
53	I/O	Reserved	54	I/O	MMCSD0_DAT6
55	I/O	I2C0_SCL	56	I/O	MMCSD0_DAT5
57	I/O	I2C0_SDA	58	I/O	MMCSD0_DAT4
59	I/O	UART2_TXD / I2C1_SDA	60	I/O	MMCSD0_DAT3
61	I/O	UART2_RXD / I2C1_SCL	62	I/O	MMCSD0_DAT2
63	I/O	GND	64	I/O	GND
65	I/O	UART1_TXD	66	I/O	MMCSD0_DAT1
67	I/O	UART1_RXD	68	I/O	MMCSD0_DAT0
69	I/O	MDIO_CLK	70	I/O	MMCSD0_CMD
71	I/O	MDIO_DAT	72	I/O	MMCSD0_CLK
73	I/O	MII_RXCLK	74	I/O	MII_TXCLK
75	I/O	MII_RXDV	76	I/O	MII_TXD3
77	I/O	MII_RXD0	78	I/O	MII_TXD2
79	I/O	MII_RXD1	70	I/O	MII_TXD1
81	I/O	MII_RXD2	82	I/O	MII_TXD0
83	I/O	MII_RXD3	84	I/O	MII_TXEN
85	-	GND	86	-	GND
87	I/O	MII_CRS	88	I/O	MII_COL
89	I/O	MII_RXER	80	I/O	FPGA_SUSPEND
91	I/O	B1 _47_P.U17	92	I/O	B1 _48_P.M14
93	I/O	B1_ 47_N.U18	94	I/O	B1_ 48_N.N14
95	I/O	B1 _45_P.T17	96	I/O	B1 _46_P.N15
97	I/O	B1_ 45_N.T18	98	I/O	B1_ 46_N.N16
99	I/O	B1_43_P.P17	100	I/O	B1 _44_P.L12
101	I/O	B1_43_N.P18	102	I/O	B1_ 44_N.L13
103	I/O	B1_41_P.N17	104	I/O	B1 _42_P.K12
105	I/O	B1_41_N.N18	106	I/O	B1_ 42_N.K13
107	-	GND	108	-	GND
109	I/O	B1_39_P.M16	110	I/O	B1 _40_P.L15
111	I/O	B1_39_N.M18	112	I/O	B1_ 40_N.L16
113	I/O	B1_37_P.L17	114	I/O	B1 _38_P.K15
115	I/O	B1_37_N.L18	116	I/O	B1_ 38_N.K16
117	I/O	B1_35_P.K17	118	I/O	B1 _36_P.J13
119	I/O	B1_35_N.K18	120	I/O	B1_ 36_N.K14
121	I/O	B1_33_P.J16	122	I/O	B1 _34_P.H15
123	I/O	B1_33_N.J18	124	I/O	B1_ 34_N.H16
125	I/O	B1_31_P.H17	126	I/O	B1 _32_P.H13

Pin	I/O	Signal	Pin	I/O	Signal
127	I/O	B1_31_N.H18	128	I/O	B1_ 32_N.H14
129	-	GND	130	-	GND
131	I/O	B1_29_P.G16	132	I/O	B1 _30_P.F15
133	I/O	B1_29_N.G18	134	I/O	B1_ 30_N.F16
135	I/O	B1_27_P.F17	136	I/O	B1 _28_P.H12
137	I/O	B1_27_N.F18	138	I/O	B1_ 28_N.G13
139	I/O	B1_25_P.E16	140	I/O	B1 _26_P.F14
141	I/O	B1_25_N.E18	142	I/O	B1_ 26_N.G14
143	I/O	B1_23_P.D17	144	I/O	B0 _24_P.F13
145	I/O	B1_23_N.D18	146	I/O	B0_ 24_N.E13
147	I/O	B1_21_P.C17	148	I/O	B0 _22_P.D14
149	I/O	B1_21_N.C18	150	I/O	B0_ 22_N.C14
151	-	GND	152	-	GND
153	I/O	B0_19_P.B16	154	I/O	B0 _20_P.F12
155	I/O	B0_19_N.A16	156	I/O	B0_ 20_N.E12
157	I/O	B0_17_P.C15	158	I/O	B0 _18_P.D12
159	I/O	B0_17_N.A15	160	I/O	B0_ 18_N.C12
161	I/O	B0_15_P.B14	162	I/O	B0 _16_P.F11
163	I/O	B0_15_N.A14	164	I/O	B0_ 16_N.E11
165	I/O	B0_13_P.C13	166	I/O	B0 _14_P.D11
167	I/O	B0_13_N.A13	168	I/O	B0_ 14_N.C11
169	I/O	B0_11_P.B12	170	I/O	B0 _12_P.E7
171	I/O	B0_11_N.A12	172	I/O	B0_ 12_N.E8
173	-	GND	174	-	GND
175	I/O	B0_9_P.B11	176	I/O	B0 _10_P.D9
177	I/O	B0_9_N.A11	178	I/O	B0_ 10_N.C9
179	I/O	B0_7_P.C10	180	I/O	B0 _8_P.D8
181	I/O	B0_7_N.A10	182	I/O	B0_ 8_N.C8
183	I/O	B0_5_P.B9	184	I/O	B0 _6_P.D6
185	I/O	B0_5_N.A9	186	I/O	B0_ 6_N.C6
187	I/O	B0_3_P.B8	188	I/O	B0 _4_P.B6
189	I/O	B0_3_N.A8	190	I/O	B0_ 4_N.A6
191	I/O	B0_1_P.C7	192	I/O	B0 _2_P.C5
193	I/O	B0_1_N.A7	194	I/O	B0_ 2_N.A5
195	-	GND	196	-	GND
197	-	VCCO_1	198	-	VCCO_0
199	-	VCCO_1	200	-	VCCO_0

Table 2: MityDSP-L138F, MitySOM-1808F, MityDSP-6748F Signal Group Description

Signal / Group	Type	Description
3.3 V in	N/A	3.3 volt input power referenced to GND.
EXT_BOOT#	I	Bootstrap configuration pin. Pull low to configure booting from external UART1.
RESET_IN#	I	Manual Reset. When pulled to GND for a minimum of 1 usec, resets the DSP processor.
SPI_XXXX	I/O	The pins with an SPI_ prefix are direct connections to the OMAP-L138 pins supporting the SPI1 interface. The SPI1_CLK, SPI1_ENA, SPI1_MISO, SPI1_MOSI pins must remain configured for the SPI function in order to support interfacing to the on-board SPI boot ROM. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.
MII_XXXX	I/O	The pins with an MII_ prefix are direct connections to the OMAP-L138 pins supporting the media independent interface (MII) function. The MII pins provide multiplex capability and may alternately be used as UART, GPIO, and SPI control pins. For details please refer to the OMAP-L138, Sitara-1808, or TMS320C6748 processor specifications.
MDIO_XX	I/O	The MDIO_CLK and MDIO_DAT signals are direct connects to the corresponding MDIO signals on the OMAP-L138 processor. These pins may be configured for GPIO.
GP0_X	IO	General Purpose / multiplexed pins. These pins are direct connects to the corresponding GP0[X] pins on the OMAP-L138 processor. The include support for the McASP, general purpose I/O, UART flow control, and McBSP 1. For details please refer to the OMAP-L138 processor specifications.
SATA_TX_P/N	O	These pins are direct connects to the OMAP-L138 SATA_TX differential Serial ATA controller pins.
SATA_RX P/N	I	These pins are direct connects to the OMAP-L138 SATA_TX differential Serial ATA controller pins.
GND	N/A	System Digital Ground.
BX_Y_P.ZZ, BX_Y_N.ZZ	IO	FPGA I/O pins. These pins are routed directly to FPGA pins ZZ. The "X" indicates which FPGA bank the pin is allocated. The bank is either 0 or 1. The FPGA fabric supports routing pins in differential pairs, the Y_P and Y_N portion of the name indicates the pair number and polarity. The pins have been routed in pairs with phase matched line lengths.

Signal / Group	Type	Description
VCCO_X	I	FPGA Bank interface power input. These pins must be tied to the desired voltage used for the FPGA Bank 0 or 1 interface pins. Please refer to the VCCO input pin specifications for the Xilinx Spartan 6 family of devices for further information. Typical values are 3.3V and 2.5 volts.
USB0_XXXX, USB1_XXXX	I/O	The USBN_ prefixed pins are direct connects to the corresponding pins on the OMAP-L138 processor. For details please refer to the OMAP-L138 processor specifications.

3 Electrical Requirements

The following sections describe the various electrical requirements for the MityDSP-L138F, MitySOM-1808F, and MityDSP-6748F modules.

3.1 Power Supplies

The MityDSP-L138F, MitySOM-1808F, and MityDSP-6748F module requires only one regulated power supply for the main +3.3V I/O power rail. All other required power rails are generated on-module by a combination of switching and linear, high-efficiency voltage regulators. The main +3.3V power rail can be sourced by either a linear or switching regulator as system requirements dictate. Table 3 describes the specifications of the input voltage, allowed ripple, and current requirements.

Table 3: Module Voltage and Current Specifications

Module	Spec.	Minimum	Typical	Maximum	Units
MityDSP-L138F	$V_{3.3}$	3.14	3.3	3.46	V
	$I_{3.3}$	TBD	120	2200	mA

3.2 Recommended Capacitance

All MityDSP-L138F family modules include some power supply rail bypass capacitors on-board, however additional capacitance is recommended on the carrier board to minimize the ripple effect caused by changing load currents. It is common practice to place one 10uF tantalum capacitor nearby each power supply pin pair. Please note that this is the minimum recommended amount of additional capacitance, and even more is always better.

3.3 I/O Interfaces

All I/O pins directly connected to the CPU SOC are compliant to only 3.3V I/O standards. The FPGA I/O pins can support 3.3V I/O standards as well as LVCMOS25 and LVDS25 compliant if a given bank VCCO is run at 2.5V, or LVCMOS18 standards if a given bank VCCO is run at 1.8V. See section 2.2 and section 3.3.12, and consult the device datasheets for more information.

The following sections describe I/O interfaces that are found on all MityDSP-L138F, MitySOM-1808F, and MityDSP-6748F types.

3.3.1 Module Reset

On the MityDSP-L138F module, the main 3.3V input supply and all on-module generated power supplies are monitored and will trigger a module hard-reset if any of them fails or goes unstable. Also included on this module is a manual-reset (MRESET#) input pin that can be connected to carrier board system reset and power supply monitoring circuitry. Note that module resets will result in the FPGA being reset as well.

3.3.2 Emulator/JTAG

All modules include connectivity for DSP emulation and FPGA JTAG. There is a dedicated on-module Hirose header that is intended for use with a Critical Link supplied breakout cable/adaptor.

The DSP emulator connection is used for code download to RAM, and real-time debugging with TI's Code Composer Studio. The FPGA JTAG connection is used for the download of images directly into the FPGA, and for debug with tools such as Xilinx's Chipscope Pro. All on-module signals are directly connected to the DSP and FPGA pins. Connection to the emulator/JTAG pods via appropriate headers should be direct and made as short as possible, within reason.

3.3.3 McASP Port

All modules include a Multi-Channel Audio Serial Port provided by the SOC. The McASP supports audio generation in Time Division Multiplexed (TDM) mode and Inter-IC Sound (I2S) format for as many as 16 stereo audio channels at standard professional audio frequencies. The McASP signals are direct connects to the SOC and are configured for 3.3 V I/O logic. For more information, please consult the DSP device datasheets and McASP user guide documents provided by Texas Instruments. The McASP pins are shared with other peripherals on the SOC. Refer to the SOC datasheet for more details.

3.3.4 McBSP Ports

All modules include two Multi-channel Buffered Serial Ports provided by the SOC. These ports support a variety of synchronous serial communication protocols including TDM and SPI types. They can be used for connectivity to a wide array of data converters (DACs and ADCs), other DSPs, and other communications equipment. The signals are connected directly to the CPU SOC device pins and are configured for 3.3 V I/O logic. For more information, please consult the DSP device datasheets and McBSP user guide documents provided by Texas Instruments. The McBSP pins are shared with other peripherals on the SOC. Refer to the SOC datasheet for more details.

3.3.5 Serial UARTs

All modules include support for up to 3 UARTs directly connected to the processor. UART1 should be configured as a UART as that is the factory default console port used to support the bootloading application as well as the console for most higher level operating systems. The other UARTs may be configured per application needs. The UARTs share pins with other peripherals on the SOC processor. Refer to the SOC datasheet for more details.

In addition, soft UARTs can also be added to the FPGA fabric if needed.

3.3.6 Serial ATA (SATA)

The SOC device on the MityDSP-L138F, MitySOM-1808F, and MityDSP-6748F includes a serial ATA bus controller. The bus controller lines have been routed to the edge connector for application use. For details, refer to the SOC datasheet.

3.3.7 SPI Ports

All modules include support for up to 2 SPI ports each having up to 8 chip selects directly controlled by the peripheral and may also use general GPIO pins as chip select pins if necessary. SPI1 chip select 0, however, is reserved in order to support booting from the on-board NOR flash. After bootloading, access to the NOR flash is typically not required, and the SPI port may be used with other chip selects if required. The SPI ports share pins with other peripherals on the SOC processor. Refer to the SOC datasheet for more details.

In addition, SPI ports (or custom serializer ports) can also be added to the FPGA fabric if required.

3.3.8 I2C Ports

All modules include support for up to 2 Inter-Integrated Circuit (I2C) ports. I2C0 is connected to an on-board prom (address 1010XXXb) that is used to hold factory configuration data (serial number, MAC address, etc.) and is therefore dedicated to this function. I2C0 is also connected to an on-board Power Management Integrated Circuit (PMIC), the TPS65023 (address 1001000b). Users may use the I2C0 port however, to interface to other devices having different addresses than those mentioned on this bus. The I2C ports share pins with other peripherals on the SOC processor. Refer to the SOC datasheet for more details.

In addition, soft I2C ports can also be added to the FPGA fabric if needed.

3.3.9 10/100 Ethernet

Ethernet on the MityDSP-L138F, MitySOM-1808F, or MityDSP-6748F is available as a MAC core in the CPU SOC. This Ethernet MAC is capable of full and half duplex 10/100 Mbit operation. To complete the interface, the MAC core requires a physical-layer device (PHY), an Ethernet isolation transformer (H1102 or equivalent), and an RJ-45 style connector (RJHSE-5381 or equivalent) on the carrier board.

All of the SOCs in this family of MityDSP (OMAP-L138, Sitara-1808, and DSP6748) provide support for both standard Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) formats. The MityDSP-L138F family of SOMs expose the RMII SOC interface directly to the edge connector. For devices that include the Spartan6 FPGA, the RMII interface is connected internally to the FPGA (it shares I/O pins with one of the UPP channels). In general, designs requiring Ethernet should use the MII interface with MityDSP-L138F family SOMS. However, the RMII interface may still be used by routing the RMII interface through the FPGA and to the edge connector. Provisions are available to load the FPGA with the necessary logic during boot time to support use of the RMII interface for bootloading and early startup operations.

The PHY IC most commonly used by Critical Link is the National Semiconductor DP83848 family, although many other suitable ICs exist on the market today. It is also possible to connect the MAC core directly to an Ethernet

Switch IC, such as the Micrel KS8995, via its standard Ethernet MII port. This option gives the carrier board the flexibility of easily making connections with several other Ethernet devices, without the need for additional networking equipment.

3.3.10 USB

The SOC provides 2 Universal Serial Bus (USB) interfaces that are mapped directly to the edge connector of the module. One port is capable of running as a host controller using USB 1.1 compliant protocols. The second port is capable of operating using the On-The-Go (OTG) protocol and is USB 2.0 compliant. OTG protocols support dynamic switching from host mode (e.g., for controlling USB mass storage devices such as thumb drives) to client mode (e.g., for interfacing to a PC) based on application software. For details in implementing the USB physical interface, refer to the TI SOC datasheets. The USB functions are not multiplexed with any other interfaces on the module.

3.3.11 Customizable GPIO

The majority of the main interface connector pins on all MityDSP platforms are General-Purpose I/O (GPIO) pins routed from the FPGA that can be customized for any end-user purpose. This is not to say that on any given end-user application board the majority of MityDSP I/O will be fully customized. Most of the MityDSP I/O required by the majority of customer platforms actually falls into the category of "off-the-shelf" core modules already designed and tested by Critical Link. These modules include, but are not limited to: UART, Ethernet MAC, High-speed USB, I^2C controller, stepper motor controller, DACs, ADCs, LCD display, Camera-Link interfaces, and simple CPU controlled GPIO. Any desired interface that is not covered by Critical Link's library of modules can either be custom designed by Critical Link, or the end customer.

3.3.12 LVDS

All of the FPGA I/O on the MityDSP-L138F, MitySOM-1808F, and MityDSP-6748F modules are capable of Low-Voltage-Differential-Signaling (LVDS). These pins are routed in differential pairs. Each of the two banks can be individually configured for 3.3V operation, 2.5V, or 1.8V operation, which may be required by the Xilinx FPGA for the LVDS or other I/O standards. With careful I/O planning, the board designer can allocate all LVDS signal pairs to one or more FPGA banks, as required. Please note that once a bank has been configured for 2.5V operation, all I/O pins within that bank can only be used with 2.5V I/O standards, such as LVDS25 or LVCMOS25 – LVTTL or LVCMOS33 is not interoperable within a bank. Likewise, a bank configured for 3.3V operation cannot be used with the 2.5V I/O standards, LVDS25 or LVCMOS25.

LVDS communication allows for faster and more reliable communication between devices that support it. Critical Link has frequently used this feature of the MityDSP FPGA for communication with SERDES (Serializer-Deserializer) ICs for high-speed I/O expansion, LCD display connections, and for custom board-to-board communication protocols.

3.3.13 FPGA I/O Pin Power-up & Boot-up States

There are a couple of issues relating to FPGA I/O pin states on power-up and boot-up that the system and carrier board designer(s) need to be aware of. The first is that immediately upon power-up, all of the FPGA I/O's are configured to float, with no pull-ups or pull-downs. Once the FPGA is loaded by the system (which defined by the application, and may occur during the bootloading phase, or during the final application execution phase), the I/O pins are configured as designed into the FPGA's bitstream configuration data.

For many designs, this boot-up sequence is just fine. However, for some designs it may present problems with some carrier board interfaces connected to FPGA pins. In these instances, it may be necessary to take measures such as adding pull-ups / pull-downs on the carrier board.

3.4 OMAP-L138 Pin-out

This section shows in table format the OMAP-L138 pins that are connected to the FPGA and the corresponding signal or signals that can be accessed at each pin. This table should be helpful to developers, who are working with the FPGA or OMAP-L138 and need to know the signal name of their connected pins.

Table 4: OMAP-L138 Pin-out to FPGA

L138 Pin Number	L138 Signal Name	FPGA Pin Number
P17	VP_DIN[8]/UHPI_HD[0]/UPP_D[0]/GP6[5]/PRU1_R31[0]	L7
R15	VP_DIN[9]/UHPI_HD[1]/UPP_D[1]/PRU0_R30[9]/PRU0_R31[9]	K5
R19	VP_DIN[10]/UHPI_HD[2]/UPP_D[2]/PRU0_R30[10]/PRU0_R31[10]	H6
R18	VP_DIN[11]/UHPI_HD[3]/UPP_D[3]/PRU0_R30[11]/PRU0_R31[11]	J6
T16	VP_DIN[12]/UHPI_HD[4]/UPP_D[4]/PRU0_R30[12]/PRU0_R31[12]	L6
U19	VP_DIN[13]_FIELD/UHPI_HD[5]/UPP_D[5]/PRU0_R30[13]/PRU0_R31[13]	G6
V19	VP_DIN[14]_HSYNC/UHPI_HD[6]/UPP_D[6]/PRU0_R30[14]/PRU0_R31[14]	F6
V18	VP_DIN[15]_VSYNC/UHPI_HD[7]/UPP_D[7]/PRU0_R30[15]/PRU0_R31[15]	F5
W19	VP_DIN[0]/UHPI_HD[8]/UPP_D[8]/RMI_CRS_DV/PRU1_R31_[29]	F1
W18	VP_DIN[1]/UHPI_HD[9]/UPP_D[9]/RMI_MHZ_50_CLK/PRU0_R31[23]	E4
W17	VP_DIN[2]/UHPI_HD[10]/UPP_D[10]/RMI_RXER/PRU0_R31[24]	D1
V17	VP_DIN[3]/UHPI_HD[11]/UPP_D[11]/RMI_RXD[0]/PRU0_R31[25]	E3
W16	VP_DIN[4]/UHPI_HD[12]/UPP_D[12]/RMI_RXD[1]/PRU0_R31[26]	D2
R14	VP_DIN[5]/UHPI_HD[13]/UPP_D[13]/RMI_TXEN/PRU0_R31[27]	M5
V16	VP_DIN[6]/UHPI_HD[14]/UPP_D[14]/RMI_TXD[0]/PRU0_R31[28]	D3

U18	VP_DIN[7]/UHPI_HD[15]/UPP_D[15]/RMI_TXD[1]/PRU0_R31[29]	F3
W1	VP_DOUT[0]/LCD_D[0]/UPP_XD[8]/GP7[8]/PRU1_R31[8]	J1
W2	VP_DOUT[1]/LCD_D[1]/UPP_XD[9]/GP7[9]/PRU1_R31[9]	K1
W3	VP_DOUT[2]/LCD_D[2]/UPP_XD[10]/GP7[10]/PRU1_R31[10]	H1
V1	VP_DOUT[3]/LCD_D[3]/UPP_XD[11]/GP7[11]/PRU1_R31[11]	K2
V2	VP_DOUT[4]/LCD_D[4]/UPP_XD[12]/GP7[12]/PRU1_R31[12]	L1
V3	VP_DOUT[5]/LCD_D[5]/UPP_XD[13]/GP7[13]/PRU1_R31[13]	H2
U1	VP_DOUT[6]/LCD_D[6]/UPP_XD[14]/GP7[14]/PRU1_R31[14]	L2
U2	VP_DOUT[7]/LCD_D[7]/UPP_XD[15]/GP7[15]/PRU1_R31[15]	M1
U3	VP_DOUT[8]/LCD_D[8]/UPP_XD[0]/GP7[0]/BOOT[0]	G3
T1	VP_DOUT[9]/LCD_D[9]/UPP_XD[1]/GP7[1]/BOOT[1]	N2
T2	VP_DOUT[10]/LCD_D[10]/UPP_XD[2]/GP7[2]/BOOT[2]	N1
T3	VP_DOUT[11]/LCD_D[11]/UPP_XD[3]/GP7[3]/BOOT[3]	H3
R1	VP_DOUT[12]/LCD_D[12]/UPP_XD[4]/GP7[4]/BOOT[4]	P2
R2	VP_DOUT[13]/LCD_D[13]/UPP_XD[5]/GP7[5]/BOOT[5]	P1
R3	VP_DOUT[14]/LCD_D[14]/UPP_XD[6]/GP7[6]/BOOT[6]	H4
P4	VP_DOUT[15]/LCD_D[15]/UPP_XD[7]GP7[7]/BOOT[7]	L4
G4	MMCSD1_DAT[4]/LCD_VSYNC/PRU1_R30[4]/GP8[8]/PRU1_R31[5]	P4
H4	MMCSD1_DAT[5]/LCD_HSYNC/PRU1_R30[5]/GP8[9]/PRU1_R31[6]	N4
F2	MMCSD1_DAT[6]/LCD_MCLK/PRU1_R30[6]/GP8[10]/PRU1_R31[7]	U2
F1	MMCSD1_DAT[7]/LCD_PCLK/PRU1_R30[7]/GP8[11]	U1
R5	LCD_AC_ENB_CS/GP6[0]/PRU1_R31[28]	J3
H3	VP_CLKIN2/MMCSD1_DAT[3]/PRU1_R30[3]/GP6[4]/PRU1_R31[4]	N3
K3	VP_CLKOUT2/MMCSD1_DAT[2]/PRU1_R30[2]/GP6[3]/PRU1_R31[3]	K3
J3	VP_CLKIN3/MMCSD1_DAT[1]/PRU1_R30[1]/GP6[2]/PRU1_R31[2]	L3
K4	VP_CLKOUT3/PRU1_R30[0]/GP6[1]/PRU1_R31[1]	K4
V15	VP_CLKIN1/UHPI_HDS1/PRU1_R30[9]/GP6[6]/PRU1_R31[16]	C2
W14	VP_CLKIN0/UHPI_HCS/PRU1_R30[10]/GP6[7]/UPP_2xTXCLK	F4
T15	PRU0_R30[26]/UHPI_HRW/UPP_CHA_WAIT/GP6[8]/PRU1_R31[17]	L5
U16	PRU0_R30[27]/UHPI_HHWL/UPP_CHA_ENABLE/GP6[9]	H5

W15	PRU0_R30[28]/UHPI_HCNTL1/UPP_CHA_START/GP6[10]	C1
U17	PRU0_R30[29]/UHPI_HCNTL0/UPP_CHA_CLOCK/GP6[11]	H7
G3	PRU0_R30[22]/PRU1_R30[8]/UPP_CHB_WAIT/GP8[12]/PRU1_R31[24]	P3
J4	PRU0_R30[23]/MMCSD1_CMD/UPP_CHB_ENABLE/GP8[13]/PRU1_R31[25]	M3
G2	PRU0_R30[24]/MMCSD1_CLK/UPP_CHB_START/GP8[14]/PRU1_R31[26]	T2
G1	PRU0_R30[25]/MMCSD1_DAT[0]/UPP_CHB_CLOCK/GP8[15]/PRU1_R31[27]	T1
R16	PRU0_R30[30]/UHPI_HINT/PRU1_R30[11]/GP6[12]	K6
R17	PRU0_R30[31]/UHPI_HRDY/PRU1_R30[12]/GP6[13]	F2
T18	CLKOUT/UHPI_HDS2/PRU1_R30[13]/GP6[14]	J7
C9	EMA_D[0]/GP4[8]	R13
A8	EMA_D[1]/GP4[9]	T14
B8	EMA_D[2]/GP4[10]	V14
E8	EMA_D[3]/GP4[11]	U5
B5	EMA_D[4]/GP4[12]	V5
E7	EMA_D[5]/GP4[13]	R3
C6	EMA_D[6]/GP4[14]	T3
D7	EMA_D[7]/GP4[15]	R5
E10	EMA_D[8]/GP3[0]	R8
D9	EMA_D[9]/GP3[1]	T7
A7	EMA_D[10]/GP3[2]	V8
D6	EMA_D[11]/GP3[3]	P6
A6	EMA_D[12]/GP3[4]	V7
B6	EMA_D[13]/GP3[5]	U7
C7	EMA_D[14]/GP3[6]	P7
E6	EMA_D[15]/GP3[7]	T4
B18	EMA_WAIT[0]/PRU0_R30[0]/GP3[8]/PRU0_R31[0]	V16
B19	EMA_WAIT[1]/PRU0_R30[1]/GP2[1]/PRU0_R31[1]	U16
A18	EMA_CS[0]/GP2[0]	U15
A9	EMA_CAS/PRU0_R30[2]/GP2[4]/PRU0_R31[2]	U8
A16	EMA_RAS/PRU0_R30[3]/GP2[5]/PRU0_R31[3]	U13

C8	EMA_WEN_DQM[0]/GP2[3]	R7
A5	EMA_WEN_DQM[1]/GP2[2]	V6
D8	EMA_SDCKE/PRU0_R30[4]/GP2[6]/PRU0-R31[4]	T6
C14	EMA_A[0]/GP5[0]	R11
D15	EMA_A[1]/GP5[1]	T12
B14	EMA_A[2]/GP5[2]	U11
D14	EMA_A[3]/GP5[3]	T11
A14	EMA_A[4]/GP5[4]	V11
C13	EMA_A[5]/GP5[5]	R10
E13	EMA_A[6]/GP5[6]	T9
B13	EMA_A[7]/PRU1_R30[15]/GP5[7]	U10
A13	EMA_A[8]/PRU1_R30[16]/GP5[8]	V10
D12	EMA_A[9]/PRU1_R30[17]/GP5[9]	N11
C12	EMA_A[10]/PRU1_R30[18]/GP5[10]/PRU1_R31[18]	P11
B12	EMA_A[11]/PRU1_R30[19]/GP5[11]/PRU1_R31[19]	V9
D13	EMA_A[12]/PRU1_R30[20]/GP5[12]/PRU1_R31[20]	T10
D11	EMA_A[13]/PRU0_R30[21]/PRU1_R30[21]/GP5[13]/PRU1_R31[21]	N10
C15	EMA_BA[0]/GP2[8]	P12
A15	EMA_BA[1]/GP2[9]	V12
B17	EMA_CS[2]/GP3[15]	M11
A17	EMA_CS[3]/GP3[14]	V15
F9	EMA_CS[4]/GP3[13]	P8
B16	EMA_CS[5]/GP3[12]	T13
D10	EMA_A_RW/GP3[9]	T5
B15	EMA_OE/GP3[10]	V13
B9	EMA_WE/GP3[11]	R15
B7	EMA_CLK/PRU0_R30[5]/GP2[7]/PRU0_R31[5]	T8

4 Mechanical Requirements

The following sections describe some of the mechanical requirements of incorporating a MityDSP-L138F, MitySOM-1808F, or MityDSP-6748F module in a board design.

4.1 Module Connectors

The module requires as its main interface the low-profile connector socket P/N 10033853-152FSLF from FCI, which is available from Digi-Key and other vendors. Sockets which are compatible with this industry standard DDR2 memory module socket are also available from other manufacturers and vendors.

The module may also be able to use a higher-profile connector socket that is mechanically compatible, but not necessarily footprint compatible with the connector mentioned above. Please contact Critical Link for a current list of compatible connector sockets for the module.

4.2 Module Clearance

All module types use a SO-DIMM style main interface connector for electrical and mechanical attachment to the carrier board. This style of connector positions the MityDSP module in parallel with the carrier board, and as such there is limited clearance between the MityDSP module and the carrier board. Therefore it is impossible to place high-profile carrier board components underneath the MityDSP module. However, it is possible to utilize most of this space for low-profile components. Please refer to the following diagrams and tables for module-specific clearances.

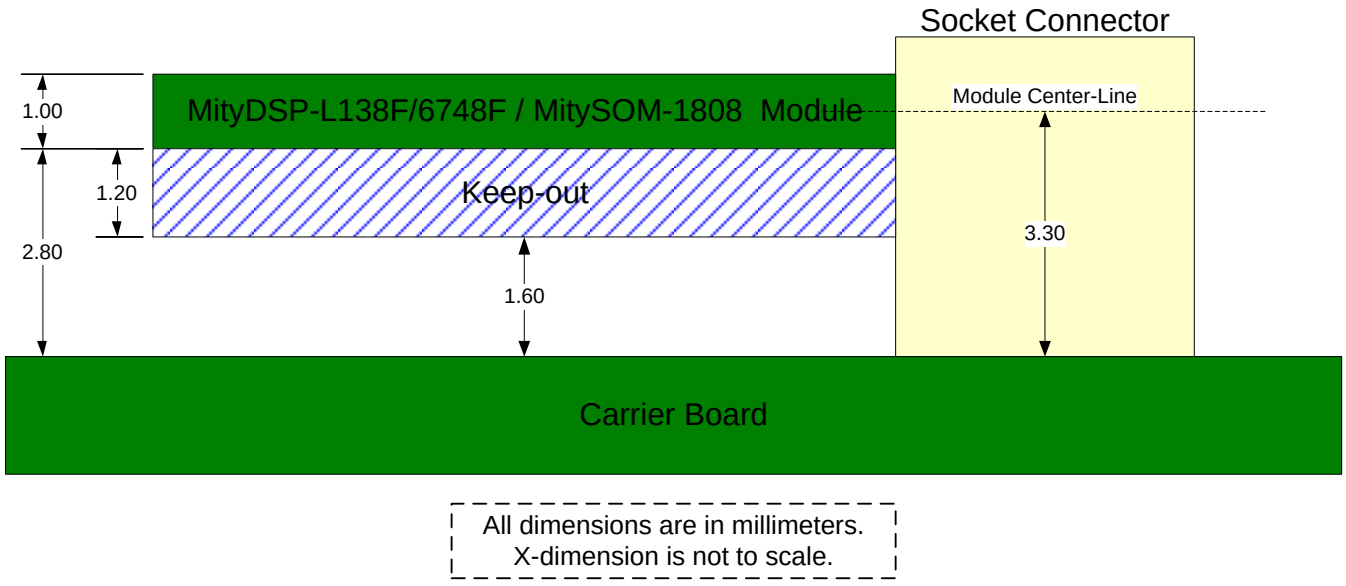

Figure 2: MityDSP-L138F, MityDSP-6748F, MitySOM-1808F Module Clearance - Side View

4.3 Mounting Methods

The modules feature an additional optional mechanical attachment method. A hard mechanical attachment by board-to-board standoffs and screw hardware may be used to mount the module. The corners of the free-floating edge of the SOMs feature mounting holes that are compatible with 4-40 size mounting hardware. The mechanical drawing in Figure 1 below illustrates the mechanical requirements of this optional attachment method.

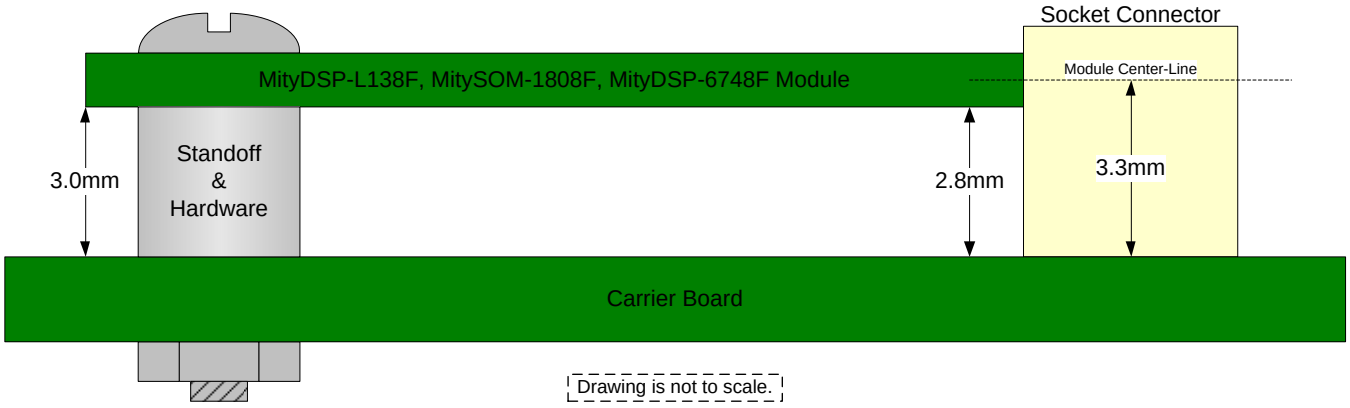

Figure 3: Metal Clip Concept Drawing

4.4 Shock & Vibration

For customers who are interested in using MityDSP modules in rugged environments, the optional mechanical attachment methods discussed in section 4.3 above enable MityDSP modules to tolerate much greater mechanical shock and vibration forces than without any additional mounting support.

4.5 Thermal Management

The MityDSP-L138F family of SOMs have no specific requirements regarding thermal management. The modules can be operated without heat sinks or air flow, and inside tight enclosures. However, if a module is intended to be used in hot industrial environments, it is advisable to do plenty of testing in the enclosure and environment that the module will be used in. In these cases, it may be necessary to either add thermal management to the enclosure, or lower the operating temperature specification of the end product.

5 Board Layout Recommendations

The following sections discuss topics for successful board layouts incorporating any module.

5.1 Placement

Placement of the module site is crucial to a successful carrier board layout. Because the module connector footprint is fine-pitch and dual-row, it is generally best to place the connector fairly centered in the overall board layout. This placement allows traces to be routed out from both sides of the connector, using mainly top-side copper tracks. The use of less signal layers, and therefore less vias, generally results in a more compact design with better signal integrity than a board using many layers and vias. Of course, ideally central placement is not always possible because of other mechanical constraints.

Mechanically, enough space must be allocated for the full extension of the module. Although it is possible for a module to hang over the edge of its carrier board, this may not be desirable if additional mechanical attachment methods are desired for ruggedness, as discussed in sections 4.3 and 4.4. Another thing to keep in mind with placement on the carrier board and in enclosures is the cam-in action of the MityDSP modules into their respective sockets. The modules are generally installed at an angle of about 25° to 30° before swinging down to locked position. Enclosure designs should accommodate this motion.

5.2 Pin-out and Routing

Because nearly half the module pins are configurable FPGA I/O, board level pin-out and routing is greatly simplified. This is done by taking advantage of the FPGA tools' sophisticated signal routing capabilities, instead of creating a tangled mess of tracks and vias in copper. MityDSP pin allocation in the schematic is generally best done in tandem with PCB layout. In this method, the components are first captured in schematic, but not yet connected to the modules configurable FPGA I/O pins, except for the dedicated functionality pins. Then in PCB layout, parts are placed according to mechanical and positional requirements with components needing connection to the MityDSP placed nearby the MityDSP's socket connector. At this point it becomes much easier to see which MityDSP pins are ideal for allocation for the various required functions. The designer can then go back and forth between schematic and layout to complete the connections between IC's and the MityDSP connector. Some PCB design tools make this process even easier with abilities to automatically re-assign nets to pins that would otherwise require many crossovers in copper features to complete. Once the signals are assigned to pins on the MityDSP, this information can be given to the FPGA designer who will capture the pin-out in a User Constraints File (UCF) for input into the FPGA's place and route tools.

Care must be taken, however, when routing the SOC high speed interfaces – specifically the USB 1.0 and 2.0 OTG ports and the SATA ports. Please refer to the specific SOC device specification for guidance related to these pins.

5.3 Access issues

Given that it is possible and often desirable to make best use of available space by placing components underneath the MityDSP module (refer to section 4.2), hardware and software engineers who will be debugging code on the platform could find themselves in a tough situation if the component they need to access is blocked by the installed MityDSP module. Because of these situations it is advisable to either not use the space under the MityDSP module for active components that might need live probing with the MityDSP in-circuit, or only place circuits there that are already tried and tested by engineers on other platforms. In the event that an obscured circuit does need to be probed, it may be necessary to solder temporary wires onto probe points. An even better solution would be to design the board with bottom-side test points, at least in the MityDSP region, if this is possible on a given design.

5.4 PCB/PCA Technology

MityDSP modules do not have any specific requirements about the PCB technology used for its carrier board. The required socket connectors are available as RoHS compliant, and may be used in both leaded and lead-free assembly processes. The only recommendation is to fabricate the carrier board thick enough to rigidly support the MityDSP socket connector. In practice, FR-4 with a common finished thickness of 0.062 inches is enough for all types of MityDSP modules.

5.5 PCB Footprints

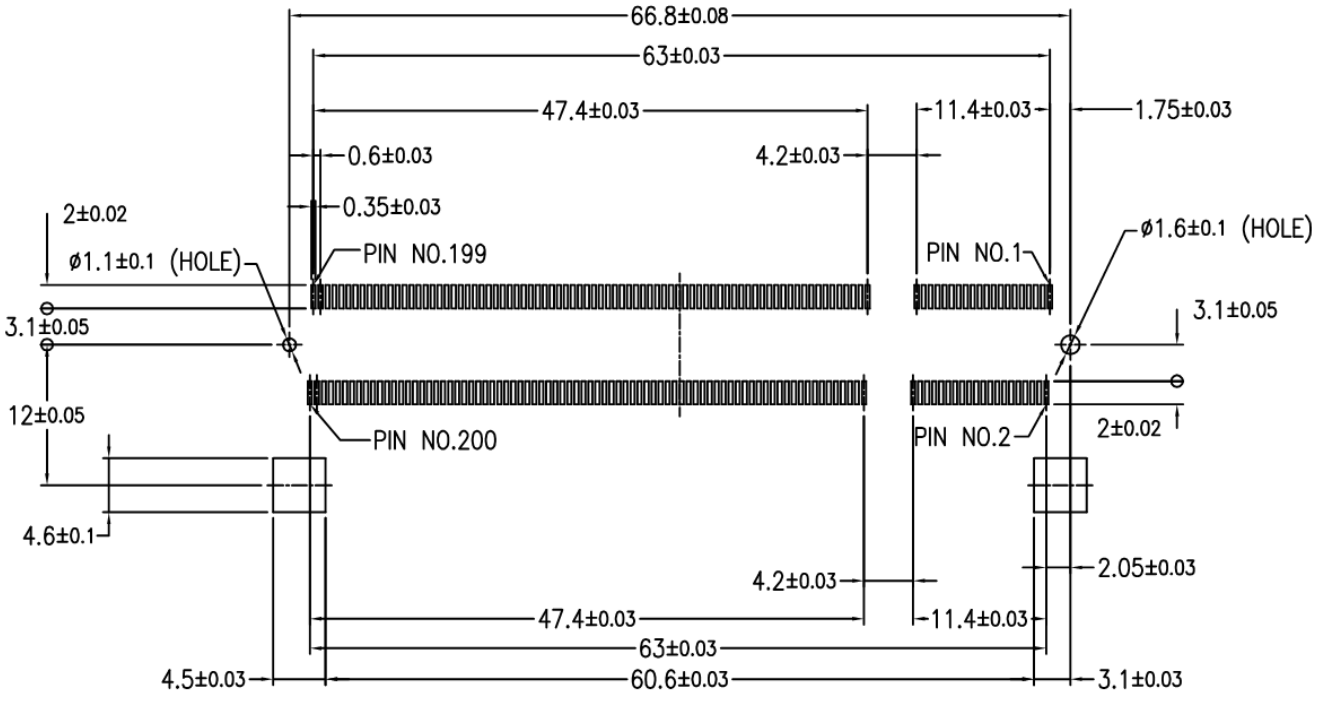

Figure 4: 10033853-152FSLF Recommended PCB Footprint

6 Revision History

Revision	Date	Description of Changes
1.0	09-Septembet-2010	Initial Revision
1.1	08-October-2010	Added connect information between FPGA and processor
1.2	11-November-2011	- Added Revision History - Added I2C address for PMIC
1.3	10-February-2012	Fixed typos for SODIMM pin numbers in table 1. Pin 180 and 170 were not properly identified in the table.
1.4	13-February-2012	Fix typo in pinout table for pins 79, 81, and 83
1.5	13-August-2012	Fix typo in pinout table for pins 79, 81, 83, 84
1.6	20-September-2012	Fix typo in pinout table for pins 120 and 186
1.7	5-March-2014	Update MitySOM product name.