

Automotive Single Supply, SPDT Analog Switch

ISL76123

The Intersil ISL76123 device is a small precision, bidirectional, single-pole/double throw (SPDT) analog switch, designed to operate from a single +2.7V to +12V supply. The device is supplied in a 6 Ld SOT-23 package. Targeted applications include automotive battery powered systems that can benefit from the device's low power consumption (5μW), low leakage currents (3nA max), and fast switching speeds ($t_{ON} = 28ns$, $t_{OFF} = 20ns$). This device will often find use in infotainment systems to "mux - in" additional functions to GPIO pins on SOCs. The device ensures the switching function is always break-before-make to help eliminate transient signal problems. Its small package size alleviates board space limitations. The part has been qualified for use in automotive applications over an operating temperature range of -40°C to +105°C.

TABLE 1. FEATURES AT A GLANCE

| | ISL76123 |
|-----------------------|-----------------|
| SW 1/SW 2 | SPDT or 2x1 MUX |
| 3.3V r_{ON} | 42Ω |
| 3.3V t_{ON}/t_{OFF} | 40ns/20ns |
| 5V r_{ON} | 23Ω |
| 5V t_{ON}/t_{OFF} | 28ns/20ns |
| 12V r_{ON} | 15Ω |
| 12V t_{ON}/t_{OFF} | 25ns/17ns |
| Package | 6 Ld SOT-23 |

Features

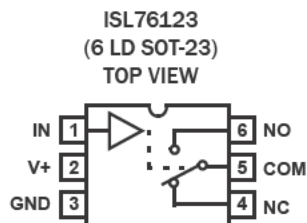
- Fully specified at 12V, 5V, and 3.3V supplies for 10% tolerances
- ON-resistance (r_{ON}) 23Ω
- r_{ON} matching between channels <1Ω
- Low charge injection 5pC (Max)
- Single supply operation +2.7V to +12V
- Low power consumption (P_D) <5μW
- Low leakage current 10nA
- Fast switching action
 - t_{ON} 28ns
 - t_{OFF} 20ns
- Guaranteed break-before-make switching
- Minimum 2000V ESD protection
- TTL, CMOS compatible
- Available in 6 Ld SOT-23 package
- Pb-free (RoHS compliant)
- AEC-Q100 qualified

Applications

- Audio and video switching
- General signal "mux - in" (where GPIO lines may be constrained)
- Various building block control applications
 - Filters
 - Signal conditioning
 - Integration reset circuits

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Pin Configuration (Note)



NOTE: Switch Shown for Logic "0" Input.

Truth Table

| LOGIC | ISL76123 | |
|-------|----------|--------|
| | PIN NC | PIN NO |
| 0 | ON | OFF |
| 1 | OFF | ON |

NOTE: Logic "0" $\leq 0.8V$. Logic "1" $\geq 2.4V$.

Pin Descriptions

| PIN NAME | PIN NUMBER | FUNCTION |
|----------|------------|-------------------------------------------|
| V+ | 2 | System Power Supply Input (+2.7V to +12V) |
| GND | 3 | Ground Connection |
| IN | 1 | Digital Control Input |
| COM | 5 | Analog Switch Common Pin |
| NO | 6 | Analog Switch Normally Open Pin |
| NC | 4 | Analog Switch Normally Closed Pin |

Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING (Note 4) | TEMP. RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|--------------------------------|--------------------------|---------------------|------------------------------|-------------|
| ISL76123AHZ-T | 123A | -40 to +105 | 6 Ld SOT-23 Tape and Reel | P6.064 |

NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL76123](#). For more information on MSL please see tech brief [TB363](#).
4. The part marking is located on the bottom of the part.

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Absolute Maximum Ratings

| | |
|------------------------------------------------------------------|-----------------------|
| V+ to GND | -0.3 to 15V |
| Input Voltages | |
| IN (Note 5) | -0.3 to ((V+) + 0.3V) |
| NO, NC (Note 5) | -0.3 to ((V+) + 0.3V) |
| Output Voltages | |
| COM (Note 5) | -0.3 to ((V+) + 0.3V) |
| Continuous Current (Any Terminal) | 30mA |
| Peak Current NO, NC, or COM (Pulsed 1ms, 10% Duty Cycle, Max) | 40mA |
| ESD Rating | |
| Human Body Model (Tested per JESD22-A114E) | 2kV |
| Machine Model (Tested per JESD22-A115-A) | 100V |
| Charged Device Model (Tested per JESD22-C101) | 1kV |
| Latch Up (Tested per JESD-78B; Class 2, Level A) | 100mA |

Thermal Information

| | | |
|------------------------------------------------|----------------------|----------------------|
| Thermal Resistance (Typical) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| 6 Ld SOT-23 Package (Notes 6, 7) | 175 | 95 |
| Maximum Junction Temperature (Plastic Package) | +150°C | |
| Maximum Storage Temperature Range | -65°C to +150°C | |

Operating Conditions

| | |
|-------------------|-----------------|
| Temperature Range | -40°C to +105°C |
|-------------------|-----------------|

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- Signals on NC, NO, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
- For θ_{JC} , the "case temp" location is taken at the package top center.

Electrical Specifications - 5V Supply Test Conditions: V+ = +4.5V to +5.5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V (Note 8), unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|--------------------------------------------------------------|---------------------------------------------------------------------------------------------------|-----------|-------------------|------|-------------------|----------|
| ANALOG SWITCH CHARACTERISTICS | | | | | | |
| Analog Signal Range, V_{ANALOG} | | Full | 0 | - | V+ | V |
| ON-Resistance, r_{ON} | V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V (Figure 5) | +25 | - | 23 | 34 | Ω |
| | | Full | - | 25 | 40 | Ω |
| r_{ON} Matching Between Channels, Δr_{ON} | V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V | +25 | - | 0.8 | 2 | Ω |
| | | Full | - | 1 | 4 | Ω |
| r_{ON} Flatness, $R_{FLAT(ON)}$ | V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1V, 2V, 3V (Note 11) | Full | - | 7 | 8 | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | V+ = 5.5V, V_{COM} = 1V, 4.5V, V_{NO} or V_{NC} = 4.5V, 1V | +25 | -3 | 0.01 | 3 | nA |
| | | Full | -5 | - | 5 | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$ | V+ = 5.5V, V_{COM} = 4.5V, 1V, V_{NO} or V_{NC} = 1V, 4.5V | +25 | -3 | - | 3 | nA |
| | | Full | -5 | - | 5 | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | V+ = 5.5V, V_{COM} = 1V, 4.5V, or V_{NO} or V_{NC} = 1V, 4.5V or Floating | +25 | -5 | - | 5 | nA |
| | | Full | -10 | - | 10 | nA |
| DYNAMIC CHARACTERISTICS | | | | | | |
| Turn-ON Time, t_{ON} | V_{NO} or V_{NC} = 3V, R_L = 1k Ω , C_L = 35pF, V_{IN} = 0V to 3V (See Figure 1) | +25 | - | 28 | - | ns |
| | | Full | - | 40 | - | ns |
| Turn-OFF Time, t_{OFF} | V_{NO} or V_{NC} = 3V, R_L = 1k Ω , C_L = 35pF, V_{IN} = 0V to 3V (See Figure 1) | +25 | - | 20 | - | ns |
| | | Full | - | 30 | - | ns |
| Break-Before-Make Time Delay, t_D | R_L = 300 Ω , C_L = 35pF, V_{NO} = V_{NC} = 3V, V_{IN} = 0V to 3V (See Figure 3) | Full | - | 10 | - | ns |
| Charge Injection, Q | C_L = 1.0nF, V_G = 0V, R_G = 0 Ω (See Figure 2) | +25 | - | 3 | - | pC |
| OFF Isolation | R_L = 50 Ω , C_L = 5pF, f = 1MHz (See Figure 4) | +25 | - | 76 | - | dB |
| Power Supply Rejection Ratio | R_L = 50 Ω , C_L = 5pF, f = 1MHz | +25 | - | 60 | - | dB |
| NO or NC OFF Capacitance, C_{OFF} | f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7) | +25 | - | 8 | - | pF |

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Electrical Specifications - 5V Supply Test Conditions: $V+ = +4.5V$ to $+5.5V$, $GND = 0V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$ (Note 8), unless otherwise specified. **Boldface limits apply over the operating temperature range, $-40^{\circ}C$ to $+105^{\circ}C$.** (Continued)

| PARAMETER | TEST CONDITIONS | TEMP ($^{\circ}C$) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|--------------------------------------|-----------------------------------------------------------------|-------------------------|----------------------|--------|----------------------|---------|
| COM OFF Capacitance, $C_{COM(OFF)}$ | $f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$ (See Figure 7) | +25 | - | 8 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | $f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$ (See Figure 7) | +25 | - | 28 | - | pF |
| POWER SUPPLY CHARACTERISTICS | | | | | | |
| Power Supply Range | | Full | 2.7 | - | 12 | V |
| Positive Supply Current, $I+$ | $V+ = 5.5V$, $V_{IN} = 0V$ or $V+$, all channels on or off | Full | -1 | 0.0001 | 1 | μA |
| DIGITAL INPUT CHARACTERISTICS | | | | | | |
| Input Voltage Low, V_{INL} | | Full | - | - | 0.8 | V |
| Input Voltage High, V_{INH} | | Full | 2.4 | - | - | V |
| Input Current, I_{INH} , I_{INL} | $V+ = 5.5V$, $V_{IN} = 0V$ or $V+$ | Full | -1 | - | 1 | μA |

Electrical Specifications - 3.3V Supply Test Conditions: $V+ = +3.0V$ to $+3.6V$, $GND = 0V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$ (Note 8), unless otherwise specified. **Boldface limits apply over the operating temperature range, $-40^{\circ}C$ to $+105^{\circ}C$.**

| PARAMETER | TEST CONDITIONS | TEMP ($^{\circ}C$) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|--------------------------------------------------------------|----------------------------------------------------------------------------------------|-------------------------|----------------------|------|----------------------|----------|
| ANALOG SWITCH CHARACTERISTICS | | | | | | |
| Analog Signal Range, V_{ANALOG} | | Full | 0 | - | V+ | V |
| ON-Resistance, r_{ON} | $V+ = 3V$, $I_{COM} = 1.0mA$, V_{NO} or $V_{NC} = 1.5V$ | +25 | - | 42 | 60 | Ω |
| | | Full | - | 45 | 70 | Ω |
| r_{ON} Matching Between Channels, Δr_{ON} | $V+ = 3.3V$, $I_{COM} = 1.0mA$, V_{NO} or $V_{NC} = 1.5V$ | +25 | - | 0.8 | 2 | Ω |
| | | Full | - | 1 | 4 | Ω |
| r_{ON} Flatness, $R_{FLAT(ON)}$ | $V+ = 3.3V$, $I_{COM} = 1.0mA$, V_{NO} or $V_{NC} = 0.5V, 1V, 1.5V$ | +25 | - | 6 | 10 | Ω |
| | | Full | - | 7 | 12 | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | $V+ = 3.6V$, $V_{COM} = 1V, 3V$, V_{NO} or $V_{NC} = 3V, 1V$ | +25 | -3 | 0.01 | 3 | nA |
| | | Full | -5 | - | 5 | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$ | $V+ = 3.6V$, $V_{COM} = 3V, 1V$, V_{NO} or $V_{NC} = 1V, 3V$ | +25 | -3 | 0.01 | 3 | nA |
| | | Full | -5 | - | 5 | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | $V+ = 3.6V$, $V_{COM} = 1V, 3V$, or V_{NO} or $V_{NC} = 1V, 3V$ or floating | +25 | -5 | - | 5 | nA |
| | | Full | -10 | - | 10 | nA |
| DYNAMIC CHARACTERISTICS | | | | | | |
| Turn-ON Time, t_{ON} | V_{NO} or $V_{NC} = 1.5V$, $R_L = 1k\Omega$, $C_L = 35pF$, $V_{IN} = 0V$ to $3V$ | +25 | - | 40 | - | ns |
| | | Full | - | 60 | - | ns |
| Turn-OFF Time, t_{OFF} | V_{NO} or $V_{NC} = 1.5V$, $R_L = 1k\Omega$, $C_L = 35pF$, $V_{IN} = 0V$ to $3V$ | +25 | - | 20 | - | ns |
| | | Full | - | 30 | - | ns |
| Break-Before-Make Time Delay, t_D | $R_L = 300\Omega$, $C_L = 35pF$, V_{NO} or $V_{NC} = 1.5V$, $V_{IN} = 0V$ to $3V$ | Full | - | 20 | - | ns |
| Charge Injection, Q | $C_L = 1.0nF$, $V_G = 0V$, $R_G = 0\Omega$ | +25 | - | 1 | - | pC |
| OFF Isolation | $R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$ | +25 | - | 76 | - | dB |
| Power Supply Rejection Ratio | $R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$ | +25 | - | 56 | - | dB |
| NO or NC OFF Capacitance, C_{OFF} | $f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$ | +25 | - | 8 | - | pF |
| COM OFF Capacitance, $C_{COM(OFF)}$ | $f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$ | +25 | - | 8 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | $f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$ (Figure 7) | +25 | - | 28 | - | pF |

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Electrical Specifications - 3.3V Supply Test Conditions: $V+ = +3.0V$ to $+3.6V$, $GND = 0V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$ (Note 8), unless otherwise specified. **Boldface limits apply over the operating temperature range, $-40^{\circ}C$ to $+105^{\circ}C$.** (Continued)

| PARAMETER | TEST CONDITIONS | TEMP ($^{\circ}C$) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|--------------------------------------|--------------------------------------------------------------|-------------------------|----------------------|-----|----------------------|---------|
| POWER SUPPLY CHARACTERISTICS | | | | | | |
| Positive Supply Current, $I+$ | $V+ = 3.6V$, $V_{IN} = 0V$ or $V+$, all channels on or off | Full | -1 | - | 1 | μA |
| DIGITAL INPUT CHARACTERISTICS | | | | | | |
| Input Voltage Low, V_{INL} | | Full | - | - | 0.8 | V |
| Input Voltage High, V_{INH} | | Full | 2.4 | - | - | V |
| Input Current, I_{INH} , I_{INL} | $V+ = 3.6V$, $V_{IN} = 0V$ or $V+$ | Full | -1 | - | 1 | μA |

Electrical Specifications - 12V Supply Test Conditions: $V+ = +10.8V$ to $+13V$, $GND = 0V$, $V_{INH} = 4V$, $V_{INL} = 0.8V$ (Note 8), unless otherwise specified. **Boldface limits apply over the operating temperature range, $-40^{\circ}C$ to $+105^{\circ}C$.**

| PARAMETER | TEST CONDITIONS | TEMP ($^{\circ}C$) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|--------------------------------------------------------------|---------------------------------------------------------------------------------------|-------------------------|----------------------|------|----------------------|----------|
| ANALOG SWITCH CHARACTERISTICS | | | | | | |
| Analog Signal Range, V_{ANALOG} | | Full | 0 | - | V+ | V |
| ON-Resistance, r_{ON} | $V+ = 10.8V$, $I_{COM} = 1.0mA$, V_{NO} or $V_{NC} = 10V$ | +25 | - | 15 | 23 | Ω |
| | | Full | - | 16 | 25 | Ω |
| r_{ON} Matching Between Channels, Δr_{ON} | $V+ = 12V$, $I_{COM} = 1.0mA$, V_{NO} or $V_{NC} = 10V$ | +25 | - | 0.8 | 2 | Ω |
| | | Full | - | 1 | 4 | Ω |
| r_{ON} Flatness, $R_{FLAT(ON)}$ | $V+ = 12V$, $I_{COM} = 1.0mA$, V_{NO} or $V_{NC} = 3V, 6V, 9V$ (Note 11) | +25 | - | 1 | 4 | Ω |
| | | Full | - | - | 6 | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | $V+ = 13V$, $V_{COM} = 1V, 12V$, V_{NO} or $V_{NC} = 12V, 1V$ | +25 | -3 | 0.01 | 3 | nA |
| | | Full | -5 | - | 5 | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$ | $V+ = 13V$, $V_{COM} = 12V, 1V$, V_{NO} or $V_{NC} = 1V, 12V$ | +25 | -3 | 0.01 | 3 | nA |
| | | Full | -5 | - | 5 | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | $V+ = 13V$, $V_{COM} = 1V, 12V$, or V_{NO} or $V_{NC} = 1V, 12V$ or floating | +25 | -5 | - | 5 | nA |
| | | Full | -12 | - | 12 | nA |
| DYNAMIC CHARACTERISTICS | | | | | | |
| Turn-ON Time, t_{ON} | V_{NO} or $V_{NC} = 10V$, $R_L = 1k\Omega$, $C_L = 35pF$, $V_{IN} = 0V$ to $4V$ | +25 | - | 25 | - | ns |
| | | Full | - | 35 | - | ns |
| Turn-OFF Time, t_{OFF} | V_{NO} or $V_{NC} = 10V$, $R_L = 1k\Omega$, $C_L = 35pF$, $V_{IN} = 0V$ to $4V$ | +25 | - | 17 | - | ns |
| | | Full | - | 26 | - | ns |
| Break-Before-Make Time Delay, t_D | $R_L = 300\Omega$, $C_L = 35pF$, V_{NO} or $V_{NC} = 10V$, $V_{IN} = 0V$ to $4V$ | Full | - | 2 | - | ns |
| Charge Injection, Q | $C_L = 1.0nF$, $V_G = 0V$, $R_G = 0\Omega$ | +25 | - | 5 | - | pC |
| OFF Isolation | $R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$ | +25 | - | 76 | - | dB |
| Crosstalk (Channel-to-Channel) | $R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$ | +25 | - | -105 | - | dB |
| Power Supply Rejection Ratio | $R_L = 50\Omega$, $C_L = 5pF$, $f = 1MHz$ | +25 | - | 63 | - | dB |
| NO or NC OFF Capacitance, C_{OFF} | $f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$ | +25 | - | 8 | - | pF |
| COM OFF Capacitance, $C_{COM(OFF)}$ | $f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$ | +25 | - | 8 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | $f = 1MHz$, V_{NO} or $V_{NC} = V_{COM} = 0V$ (Figure 7) | +25 | - | 28 | - | pF |
| POWER SUPPLY CHARACTERISTICS | | | | | | |
| Positive Supply Current, $I+$ | $V+ = 13V$, $V_{IN} = 0V$ or $V+$, all channels on or off | Full | -1 | - | 1 | μA |

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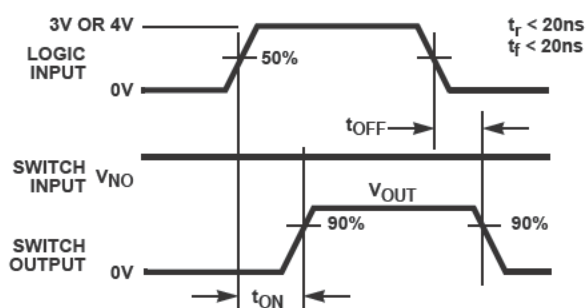
Electrical Specifications - 12V Supply Test Conditions: $V^+ = +10.8V$ to $+13V$, $GND = 0V$, $V_{INH} = 4V$, $V_{INL} = 0.8V$ (Note 8), unless otherwise specified. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+105^\circ C$.** (Continued)

| PARAMETER | TEST CONDITIONS | TEMP ($^\circ C$) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|--------------------------------------|--------------------------------------|------------------------|----------------------|-----|----------------------|---------|
| DIGITAL INPUT CHARACTERISTICS | | | | | | |
| Input Voltage Low, V_{INL} | | Full | - | - | 0.8 | V |
| Input Voltage High, V_{INH} | | Full | 4 | - | - | V |
| Input Current, I_{INH} , I_{INL} | $V^+ = 13V$, $V_{IN} = 0V$ or V^+ | Full | -1 | - | 1 | μA |

NOTES:

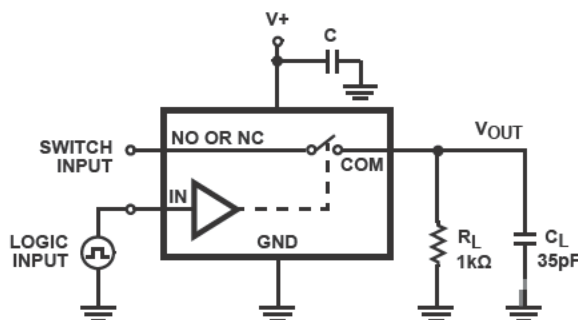
8. V_{IN} = input voltage to perform proper function.
9. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
11. Limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO \text{ OR } NC)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

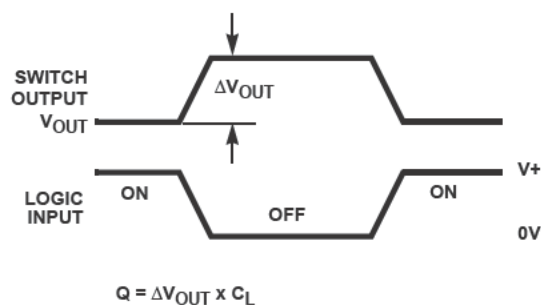


FIGURE 2A. MEASUREMENT POINTS

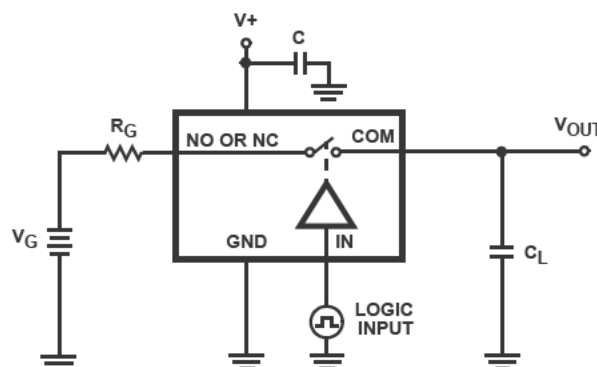


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

Test Circuits and Waveforms (Continued)

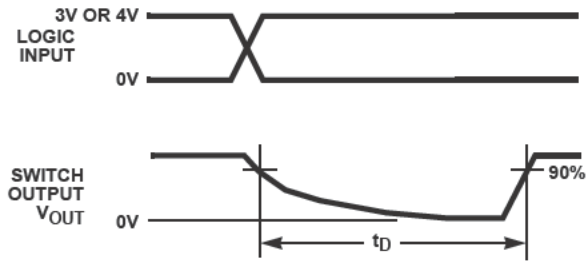
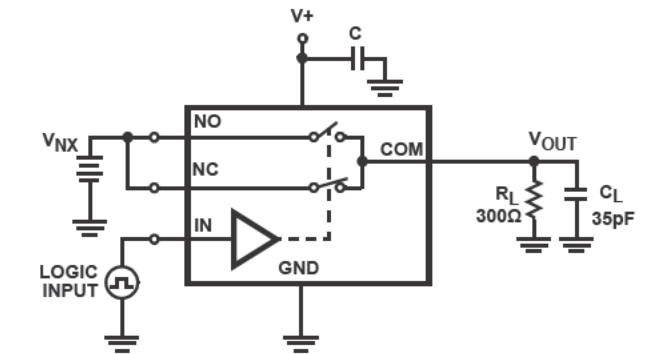


FIGURE 3A. MEASUREMENT POINTS



C_L includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME

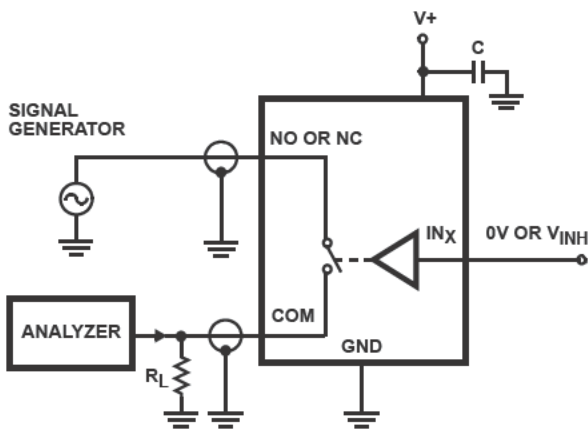


FIGURE 4. OFF ISOLATION TEST CIRCUIT

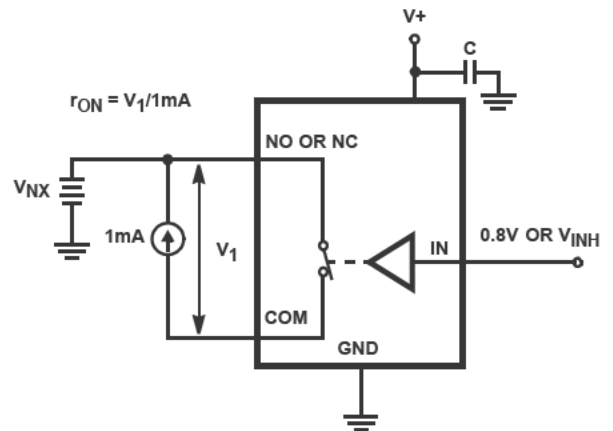


FIGURE 5. r_{ON} TEST CIRCUIT

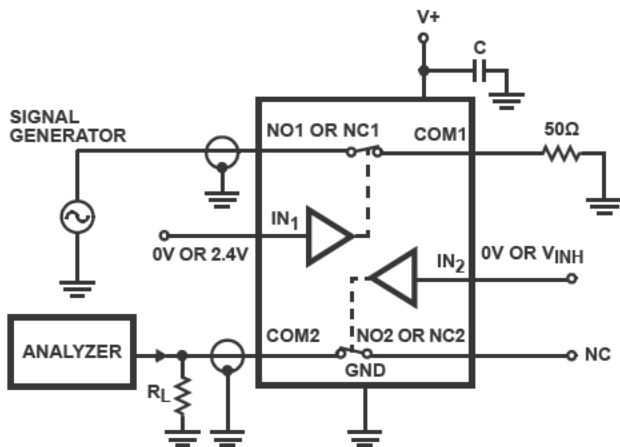


FIGURE 6. CROSSTALK TEST CIRCUIT

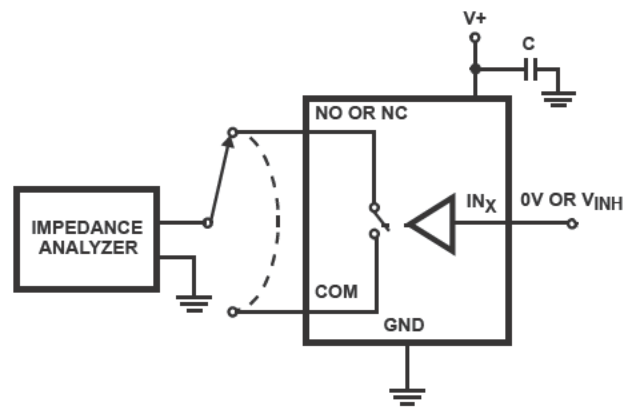


FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL76123 bidirectional, single SPDT analog switch offers precise switching capability from a single 2.7V to 12V supply with low ON-resistance (23Ω) and high speed operation ($t_{ON} = 28\text{ns}$, $t_{OFF} = 20\text{ns}$). The device is especially well suited to automotive battery powered systems thanks to the low operating supply voltage (2.7V), low power consumption (5μW), low leakage currents (3nA max), and the tiny SOT-23 packaging. High frequency applications also benefit from the wide bandwidth, and the very high off isolation rejection.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

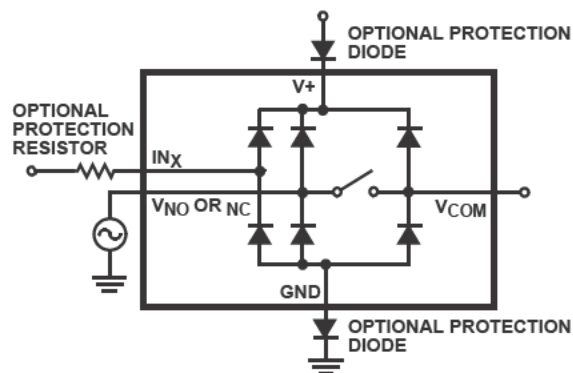


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL76123 construction is typical of most CMOS analog switches, except that they have only two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 13V maximum supply voltage, the ISL76123 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 2.7V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the “Electrical Specification” tables beginning on page 3 and “Typical Performance Curves” beginning on page 9 for details.

V+ and GND also power the internal logic and level shifter. The level shifter convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This device cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch is TTL compatible (0.8V and 2.4V) over a supply range of 3V to 11V (see Figure 15). At 12V the V_{IH} level is about 2.5V. This is still below the TTL guaranteed high output minimum level of 2.8V, but noise margin is reduced. For best results with a 12V supply, use a logic family that provides a V_{OH} greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 300MHz (see Figure 16). Figure 16 also illustrates that the frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch’s input to its output. Off isolation is the resistance to this feedthrough. Figure 17 details the high off isolation rejection provided by this part. At 10MHz, off isolation is about 50dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off isolation rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified.

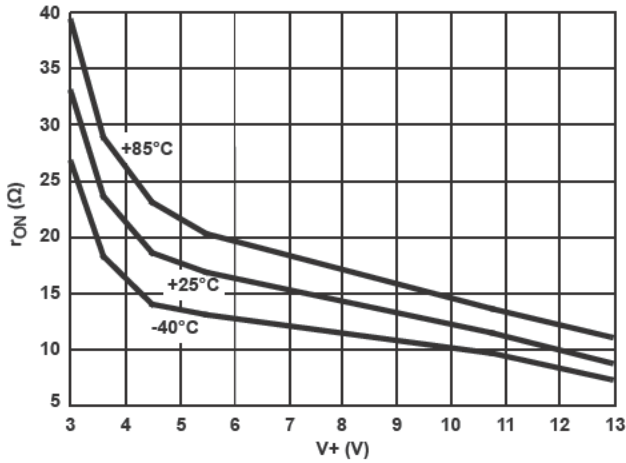


FIGURE 9. ON-RESISTANCE vs SUPPLY VOLTAGE

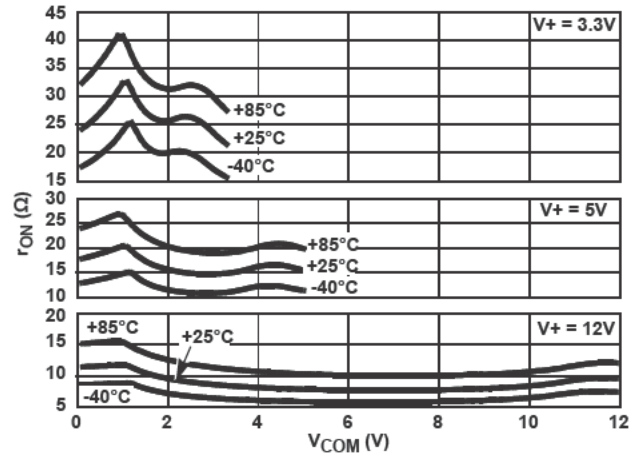


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

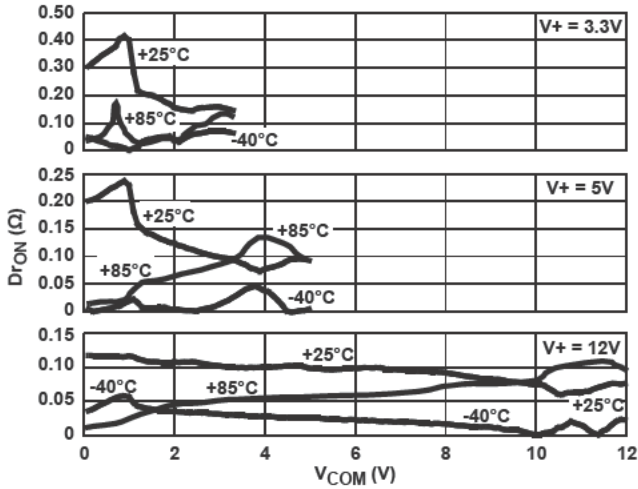


FIGURE 11. r_{ON} MATCH vs SWITCH VOLTAGE

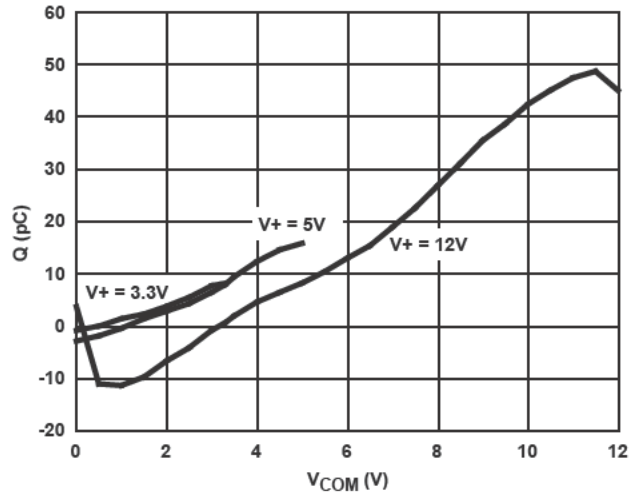


FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

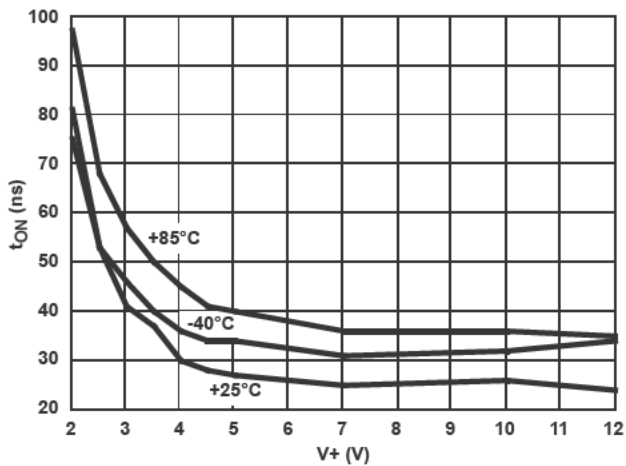


FIGURE 13. TURN-ON TIME vs SUPPLY VOLTAGE

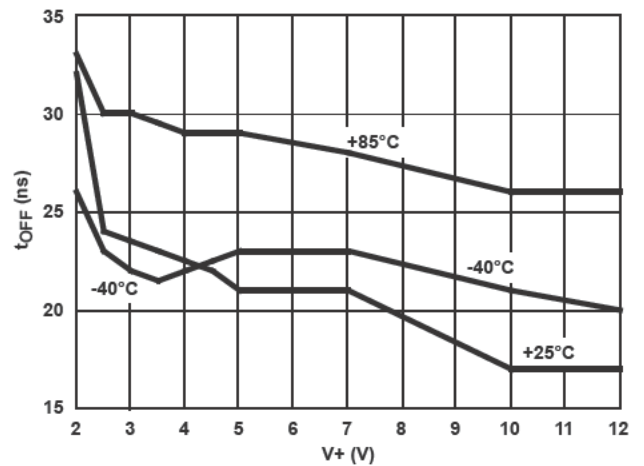


FIGURE 14. TURN-OFF TIME vs SUPPLY VOLTAGE

Typical Performance Curves $T_A = +25^\circ\text{C}$, Unless Otherwise Specified. (Continued)

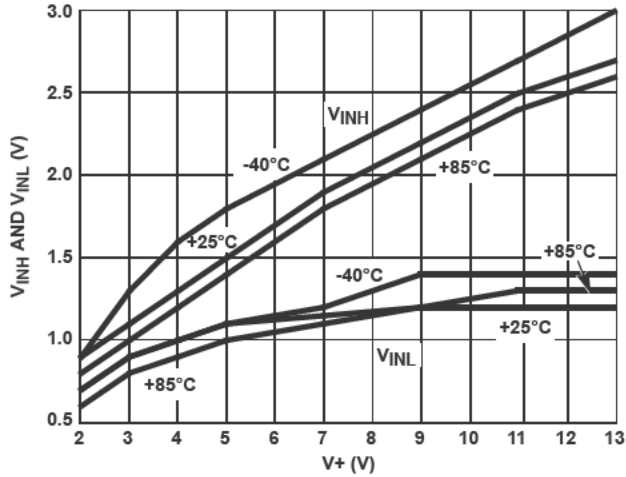


FIGURE 15. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

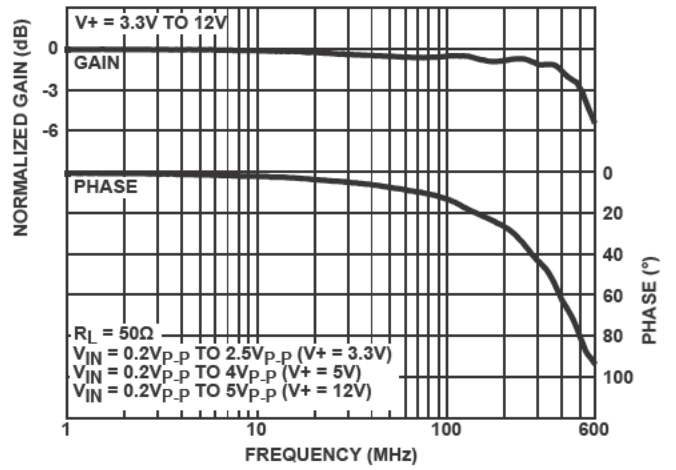


FIGURE 16. FREQUENCY RESPONSE

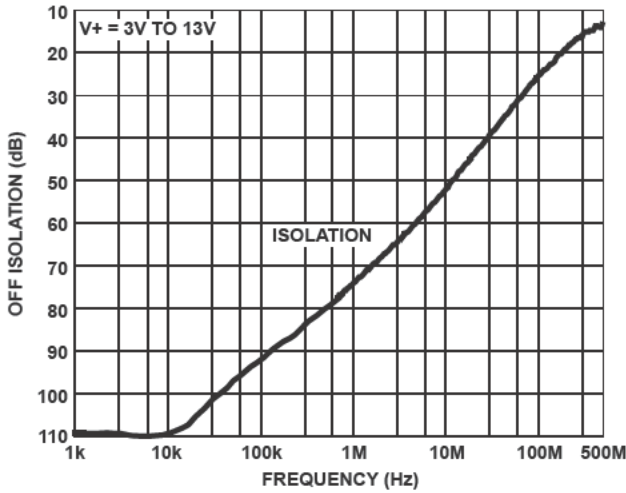


FIGURE 17. OFF ISOLATION

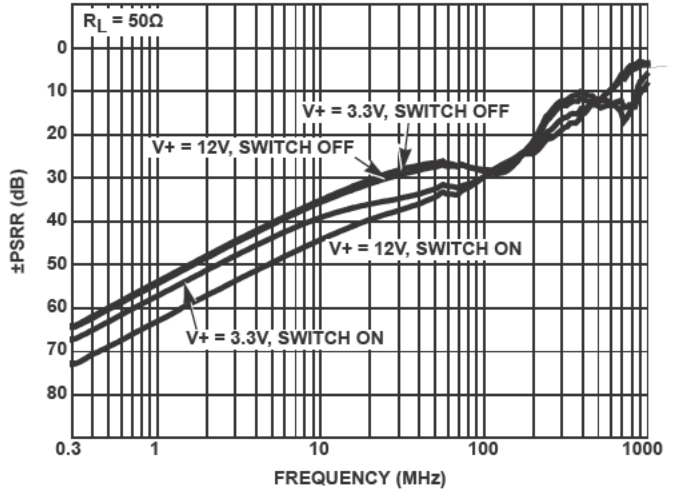


FIGURE 18. \pm PSRR vs FREQUENCY

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|--------------------|----------|------------------|
| September 28, 2012 | FN8297.1 | Initial Release. |

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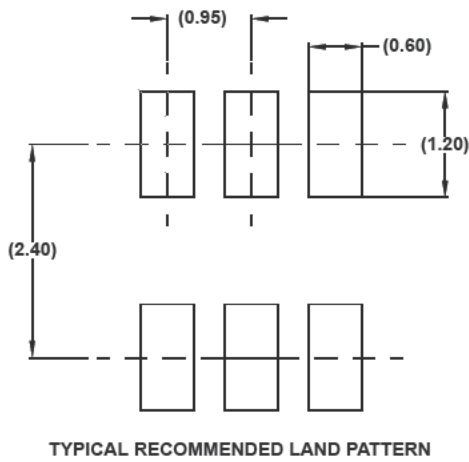
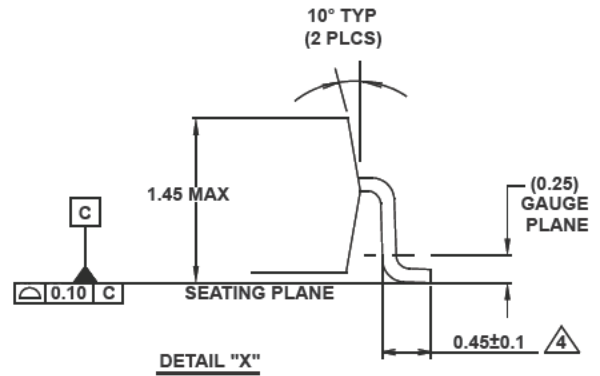
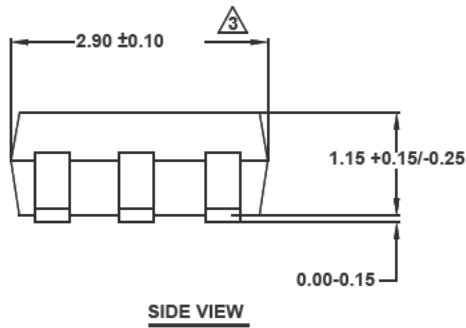
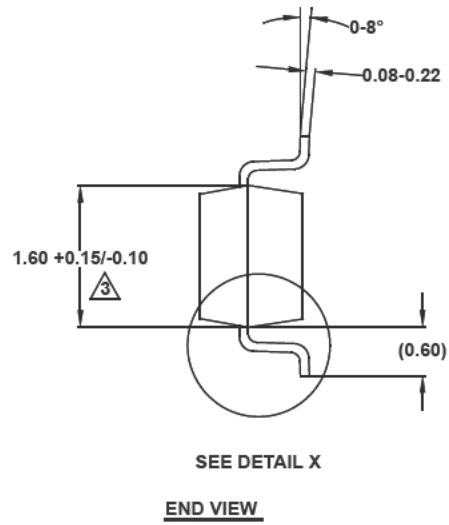
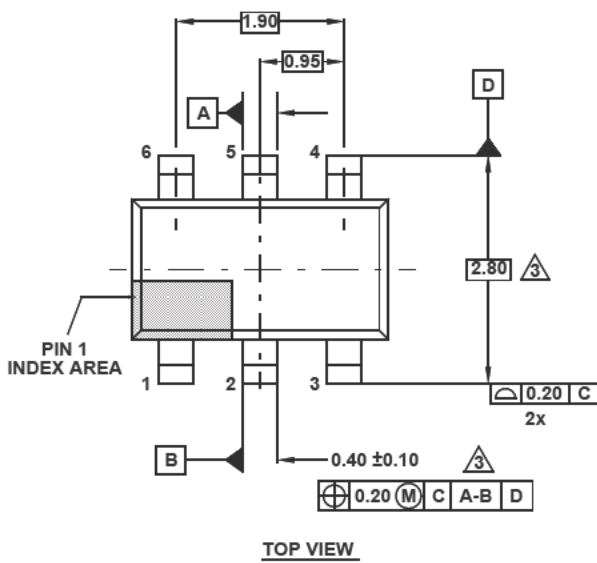
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Package Outline Drawing

P6.064

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

Rev 4, 2/10



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to gauge plane.
5. Package conforms to JEDEC MO-178AB.