ECE1200

ECE1200 Silicon Errata and Data Sheet Clarification

TABLE 1: DEVICE IDENTIFICATION

Part Number	Silicon Identifier	Functional Revision A	Functional Revision B		
ECE1200-I/LD	DeviceID_DeviceSubID(1)	0021_65h	0021_65h		
	Silicon Revision ID(2)	A0h	B0h		
	Default Base Address(3)	008Eh	008Ch		

Note 1: The DeviceID_DeviceSubID code is visible at Plug and Play Configuration Indexes 1Fh - 1Dh.

2: The Silicon Revision Number is visible as an 8-bit number at Plug and Play Configuration Index 1Ch

3: The Default Base Address differs. The address 008Eh is discontinued after Functional Rev. A and is replaced with 008Ch. Access to the ID registers is affected by this difference.

TABLE 2: DEVICE ERRATA SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A	B		
eSPI Interface Clocking	Max Frequency	1.	eSPI interface is compliant only to the 33MHz eSPI specification parameters.	x	-		
Default Base Address	Max Frequency	2.	Default Base Address not easily accessible.	x	-		
Oscillator Lock	Max Frequency	3.	Potential loss of oscillator lock during Wake from Deep Sleep.	x	-		

Note 1: Only those issues indicated with an “X” in the column apply to that functional revision.

Device Errata Issues

1. Module: eSPI Interface Clocking

DESCRIPTION

The eSPI bus is compliant only to the Intel 33MHz (maximum) eSPI timing parameters.

END USER IMPLICATIONS

The Host Chipset's PCH has Soft-Strap settings that regulate the eSPI maximum frequency for each eSPI slave device. In those settings, the maximum frequency for an ECE1200 device must be set to 33MHz or lower, rather than the setting for 50MHz. No subsequent software action may change this frequency above 33MHz either.

As stated in the data sheet, the ECE1200 device does not limit the eSPI clock speed by any local declaration, making it necessary to change this limit in the Intel PCH Soft Straps.

Bus propagation delays obey the 33MHz parameters. See the Intel eSPI Interface Base Specification, Intel Document #327432-004 for these timing parameters.

Work Around

None.

2. Module: Default Base Address

DESCRIPTION

It has been discovered that an initial I/O Base Address of 008Eh for this device makes the DATA register (at 8Fh) not easily accessible through the Host Chipset in some system configurations. Starting with Functional Revision B, this address is changed to 008Ch, placing INDEX at 8Ch and DATA at 8Dh. The data sheet release is now edited to document the much simpler initialization requirements resulting from it. The old initialization requirements are given in the Work Around section below.

Changing the HW default Base Address to 8Ch makes both the INDEX and DATA I/O locations of the device accessible in place, and usually by HW default in the Host Chipset. Moving the Base Address, if necessary, is also greatly simplified, and need not involve anything but Legacy decode ranges in the Chipset.

END USER IMPLICATIONS

Re-assignment of the Base Address was mandatory in many system configurations, and the process of accomplishing this was fairly complex, as shown below.

Work Around

The following initialization steps apply only to Functional Revision A. For Functional Revision B, see the data sheet instead.

From its reset state, the ECE1200 Functional Revision A device requires special routing considerations within the Host Chipset, and may also require re-configuration internally in order to move it into another desired Legacy or Generic I/O region.

By default, it is mapped to an unused section of the Port 80h ("Debug Port" or "RPR") region of the I/O space, at addresses 8Eh (INDEX) and 8Fh (DATA). The address 008Eh is its initial "Base Address".

FIGURE 1: INITIALIZATION SEQUENCES FOR REGISTER ACCESS

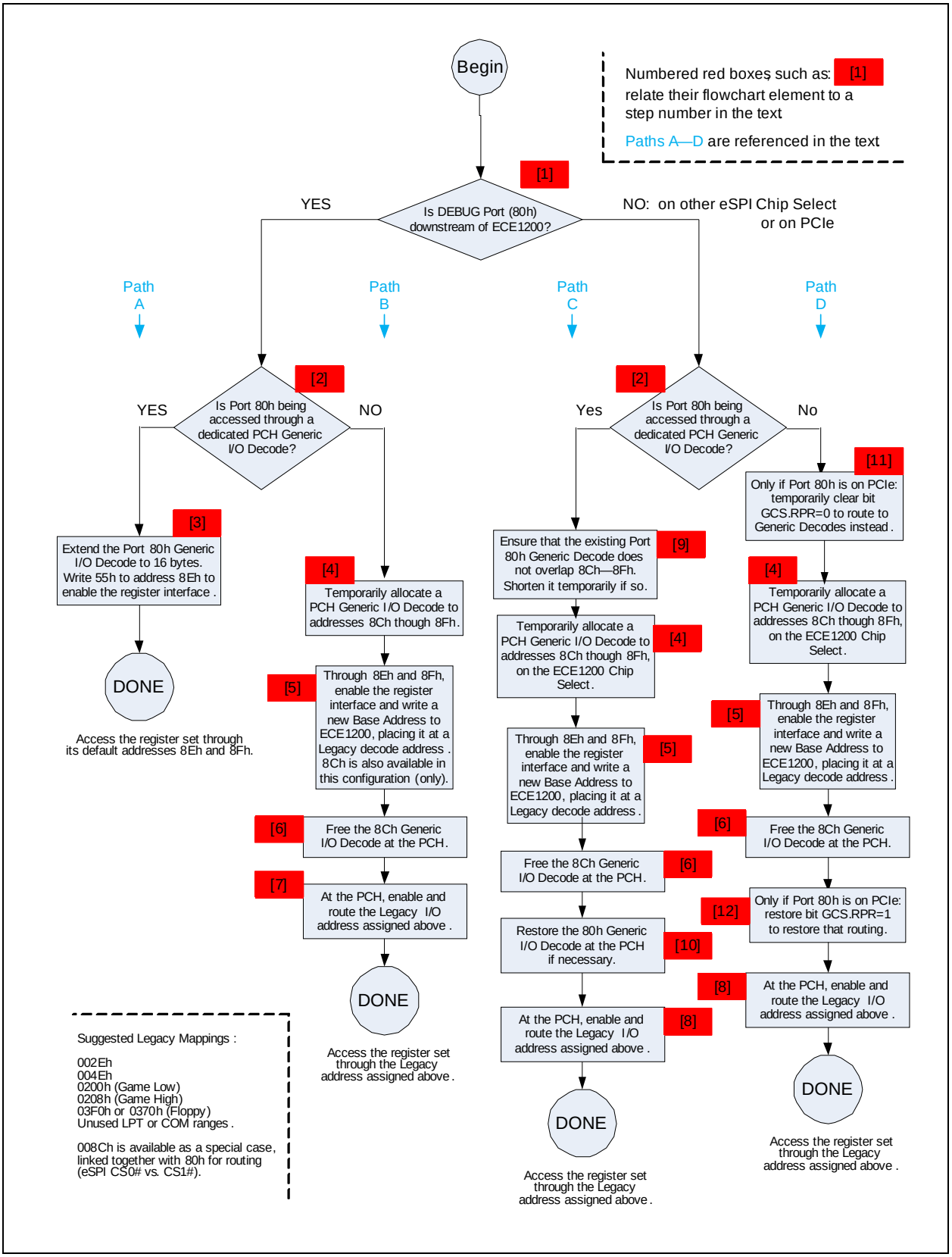

Figure 1 illustrates the sequences used in order to map the register set as desired. These are explained in more detail in the Step list below.

Referring to Figure 1, the first two decisions, Step [1] and Step [2], separate the initialization process into one of four “Paths”, Path A through Path D. These are based on the intended system mapping of the Port 80h (“Debug Port” or “RPR”) I/O region.

Step [1]: Is DEBUG Port (80h) downstream of ECE1200?

If the intention of the system is for Port 80h I/O traffic to go to the LPC bus through the ECE1200, then the simplest setup methods may be followed, in Path A or Path B.
If instead the intention is to route Port 80h traffic so that it is not seen by the ECE1200, then Path C or Path D is taken. This represents cases where Port 80h is on a different eSPI Chip Select from the ECE1200, or it is routed to the PCIe bus instead.

Step [2]: Is Port 80h being accessed through a dedicated PCH Generic I/O Decode?

With some newer techniques for accessing a wider Port 80h, it is becoming popular to assign one of the Generic I/O Decode registers within the PCH to Port 80h, so that individual bytes of a multi-byte value can be accessed as well as the byte at 80h itself.

If YES, then either Path A or Path C is taken, depending on Step [1].

If NO, then either Path B or Path D is taken. In these cases, it may not be desirable to keep a Generic I/O range dedicated to Port 80h (and by extension the ECE1200). In particular, if these are on eSPI Chip Select CS1#, then there is only one Generic I/O Decode register available instead of the four on CS0#, meaning that it may be considered too precious a resource to dedicate permanently to this.

According to the above decisions, one of the Paths in Figure 1 is taken, and this determines which of the Steps below are taken, and in which order.

Step [3]: Extend Port 80h Generic I/O Range

Appearing only in Path A: Ensure that the Generic I/O Decode Range registers allocated for Port 80h, in both the eSPI PCI Configuration space and the DMI Configuration space, are extended to 16 bytes, so that they include I/O addresses 8Eh and 8Fh as well as 80h.

Once this is done, write a byte value of 55h to location 8Eh (INDEX) to enable the register interface.

This step ends the initialization for Path A, and the ECE1200 registers may continue to be accessed using the default 8Eh/8Fh addresses.

Step [4]: Temporarily Allocate a Generic Decode Range

Appearing in Paths B, C and D, this step is taken to temporarily allocate a Generic I/O Range routing in the Host PCH to point to a place where addresses 8Eh and 8Fh can both be accessed outside the Host Chipset.

The purpose of this is to set up temporary access so that the subsequent Step [5] can move the Base Address of the ECE1200 from 8Eh/8Fh to another I/O address, which requires writing registers that are within the ECE1200.

The smallest Generic Decode region is 4 bytes, on a 4-byte boundary, so this decode would be set up as 4 bytes at 8Ch.

The PCH’s Generic I/O Decode registers are in the eSPI PCI header space:
for eSPI CS0#: ESPI_LGIR1 through ESPI_LGIR4, or
for eSPI CS1# (if it exists): PCCS1GIR1.

In addition, it will be necessary to ensure that this range is specified to be claimed by the PCH from the CPU.

Do this by setting up decodes in the following registers in the DMI Configuration space:
for eSPI CS0#: LPCLGIR1 through LPCLGIR4, or
for eSPI CS1#: there may be more decodes available.

Step [5]: Write a new Base Address

Appearing in Paths B, C and D, and immediately after Step [4] in each, this step changes the Base Address of the ECE1200 to a different Legacy location, so that a Generic I/O Decode is no longer needed.

Depending on the system, one of the more traditional Configuration ranges 4Eh/4Fh or 2Eh/2Fh may be available to be selected. In Path B (only), the location 8Ch/8Dh is often available, and more easily routed while not occupying another Legacy range. Other options such as the Game Port ranges or the Floppy Controller range may be available for use in any of these Paths.

In writing a new Base Address, the I/O address for the first location (INDEX, even) is written, and the DATA register will be the next consecutive (odd) location. This means that the least-significant bit of any new Base Address written must be zero for correct operation.

Do the following to change the ECE1200 device's 16-bit BAR Address value:

Write the value 55h to the INDEX I/O location at 8Eh to enable access.

If it is possible that this sequence is happening without a previous PLTRST# reset assertion, ensure that Logical Device 0 is selected, by doing the following:

Write 07h to the INDEX location 8Eh, designating the global Logical Device Number Register.
Write 00h to the DATA location 8Fh.

Designate a new Base Address:

Write 36h to the INDEX location 8Eh, designating the I/O BAR Address LS Register.
Write the LS byte of the new Base Address to the DATA location 8Fh.
Write 37h to the INDEX location 8Eh, designating the I/O BAR Address MS Register.
Write the MS byte of the new Base Address to the DATA location 8Fh.

Note that all four Writes must be performed, even if they do not change a value that is already in one of the registers. Until this is done, none of the 16-bit value changes internally.

From this point onward, the ECE1200 will recognize only the new Base Address, and no longer 8Eh/8Fh, for accesses to its internal registers.

Step [6]: Free the Generic Decode Range

The Generic I/O Decode Range, allocated in the PCH in Step [4], is no longer needed, and it may be restored to its earlier setting.

Step [7]: Enable and Route a Legacy Range to the new Base Address, Path B

Appearing only in Path B. Within the PCH, ensure that all Enable and Routing fields are set for the ECE1200 legacy Base Address that has been selected (2Eh/2Fh, 4Eh/4Fh, etc.).

Note that for routing to eSPI CS1# there is a PCH register at eSPI PCI Configuration offset A0h (PCCS1IORE), containing bits to redirect these legacy spaces to CS1# from CS0#.

As a special case, for using 8Ch/8Dh (Path B only), it is unnecessary to take steps to enable routing, since it is associated with Port 80h which has a hard-wired routing path by default. The only selections available for routing in this Path will already have been taken for Port 80h: selecting eSPI CS0# vs. CS1# for this "RPR" / "Debug Port" range. In existing Intel documentation, see the appropriate PCH EDS specification, bit DPCS1RE of register PCCS1IORE.

This step ends the initialization for Path B, and the ECE1200 registers may be accessed using the newly assigned Base Address.

Step [8]: Enable and Route a Legacy Range to the new Base Address, Paths C and D

Appearing in Paths C and D. Within the PCH, ensure that all Enable and Routing fields are set for the ECE1200 legacy Base Address that has been selected (2Eh/2Fh, 4Eh/4Fh, etc.). Unlike Step [7], the range 8Ch/8Dh is unavailable in these Paths because of the decision in Step [1].

Note that for routing to eSPI CS1# there is a PCH register at eSPI PCI Configuration offset A0h (PCCS1IORE), containing bits to redirect these legacy spaces to CS1# from CS0#.

Referring to Figure 1, note that there are additional steps appearing before this one: Steps [9] and [10] for Path C, and Steps [11] and [12] for Path D. These are itemized below.

This step ends the initialization for Paths C and D, and the ECE1200 registers may be accessed using the newly assigned Base Address.

Step [9]: Shorten Port 80h Decode Range

Appearing only in Path C, immediately before Step [4] (Figure 1): In this case, the PCH is configured to send Port 80h traffic to another eSPI Chip Select, and the Generic I/O range declared there might interfere with the traffic to the ECE1200. We do not want to allow two routings for the same I/O addresses 8Eh/8Fh.

To prevent this, restrict (temporarily if necessary) the Port 80h Generic Decode to addresses 80h--87h.

Step [10]: Restore Port 80h Decode Range

Appearing only in Path C, immediately before Step [8] (Figure 1): If necessary, restore the I/O range on Port 80h to its original state before Step [9]. Since the ECE1200 Base Address has been moved in Step [5] already, there is no longer a decoding conflict.

Step [11]: Temporarily Reset Routing of Port 80h to PCIe

Appearing only in Path D, immediately before Step [4] (Figure 1). This only applies if Port 80h has already been routed to the PCIe bus instead of LPC/eSPI.

Temporarily re-assign Port 80h back to LPC/eSPI by clearing the RPR bit in the PCH's GCS register to '0'.

Step [12]: Restore Routing of Port 80h to PCIe

Appearing only in Path D, immediately before Step [8] (Figure 1): Restore the RPR bit in the PCH's GCS register to its previous '1' state.

3. Module: Oscillator Lock

DESCRIPTION

In the process of waking from Deep Sleep, it is possible to lose Oscillator Lock on the internal oscillator, leading to a period of time (up to about 3 ms) during which internal clocking and the external LPC clocks stop.

END USER IMPLICATIONS

Possible loss of LPC traffic.

Work Around

Do not enable Deep Sleep mode.

Data Sheet Clarifications

TABLE 3: DATA SHEET CLARIFICATION SUMMARY

Data Sheet Number	Issue Summary
ECE1200: 00003093A	Describes Functional Revision A only.
ECE1200: 00003093B	Describes Functional Revision B and not Revision A.

APPENDIX A: DOCUMENT REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS80000835B (07-16-19)	All	Adds Base Address and Oscillator issues. Recognizes Functional Revision B.
DS80000835A (05-30-19)	Document Release	

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ISBN: 9781522447719

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