Product Advisor (PA)

Subject: Datasheet Change for the Listed Intersil TW9966AT-LC1-GR* Products
Publication Date: 11/15/2016
Effective Date: 11/15/2016

Revision Description:
Initial Release

Description of Change:
This advisory is to inform you that Intersil has made corrections to the datasheet associated with the listed Intersil TW9966AT-LC1-GR* Products. Details regarding the change are contained on the following page.

Affected Products:
TW9966AT-LC1-GR TW9966AT-LC1-GRT

Reason for Change:
The corrections align the product characteristics with the associated datasheet. The changes are primarily timing clarifications or corrections to the register description or reset values. Contact your local sales representative for a copy of the latest datasheet.

Impact on fit, form, function, quality & reliability:
The change will have no impact on the form, fit, function, quality, reliability and environmental compliance of the devices.

Product Identification:
There have been no changes to the die/silicon or product itself. There will be no change in the external marking of the packaged parts.

Qualification status: Not applicable; datasheet corrections only
Sample availability: 11/15/2016
Device material declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.

For additional information regarding this notice, please contact your regional change coordinator (below)			
Americas: PCN-US@INTERSIL.COM	Europe: PCN-EU@INTERSIL.COM	Japan: PCN-JP@INTERSIL.COM	Asia Pac: PCN-APAC@INTERSIL.COM

Datasheet Changes:

Page 5 – removed Application Schematic

Page 11
From:

Serial Host Interface Timing

PARAMETER	SYMBOL	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Bus Free Time Between STOP and START	t_{BF}	740			ns
SDAT Setup Time	t_{sSDAT}	100			ns
SDAT Hold Time (XTI 108MHz)	t_{hSDAT}	50			ns
SDAT Hold Time (XTI 54MHz)		100			ns
Setup Time for START Condition	t_{sSTA}	370			ns
Setup Time for STOP Condition	t_{sSTOP}	370			ns
Hold Time for START Condition	t_{hSTA}	74			ns
Rise Time for SCLK and SDAT	t_R			300	ns
Fall Time for SCLK and SDAT	t_F			300	ns
Capacitive Load for Each Bus Line	C_{BUS}			400	pF
LOW Period of SCLK	t_{LOW}	0.5			µs
HIGH Period of SCLK	t_{HIGH}	0.5			µs
SCLK Clock Frequency (XTI 108MHz)	f_{SCLK}			400	kHz
SCLK Clock Frequency (XTI 54MHz)				350	kHz

To:

Serial Host Interface Timing

PARAMETER	SYMBOL	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Bus Free Time Between STOP and START	t_{BF}	740			ns
SDAT Setup Time	t_{sSDAT}	100			ns
SDAT Hold Time	t_{hSDAT}	150			ns
Setup Time for START Condition	t_{sSTA}	370			ns
Setup Time for STOP Condition	t_{sSTOP}	370			ns
Hold Time for START Condition	t_{hSTA}	74			ns
Rise Time for SCLK and SDAT	t_R			300	ns
Fall Time for SCLK and SDAT	t_F			300	ns
Capacitive Load for Each Bus Line	C_{BUS}			400	pF
LOW Period of SCLK	t_{LOW}	0.5			µs
HIGH Period of SCLK	t_{HIGH}	0.5			µs
SCLK Clock Frequency	f_{SCLK}			300	kHz

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From:

ADDRESS				MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x65				VD0EB	P0	0	0	D40RD	VD40EB	VD30EB	VD20EB	VD10EB

To:

ADDRESS				MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x65				VD0EB	0	0	0	D40RD	VD40EB	VD30EB	VD20EB	VD10EB

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From:

ADDRESS				MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x73				A5NUM	AIMANU	A5NUM			0	0	0	A5DET_ENA

To:

ADDRESS				MNEMONIC	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH1	CH2	CH3	CH4									
0x73				A5NUM	0	0	0	0	0	0	0	A5DET_ENA

Pages 47 – 80:
From: Register Reset value containing a "b" or "h"

To: Removed “b” or “h” after any numbers that had them.

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From:

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X81 – ANALOG CONTROL REGISTER				
7	Reserved	R	Reserved	0
6	IREF	R/W	0 = Internal current reference 1. 1 = Internal current reference increase 30%.	0
5	VREF	R/W	0 = Internal voltage reference. 1 = Internal voltage reference shut down.	0
4	Reserved	R/W	0 = Normal operation (must be 0), 1 = AIGAINTEST	0

To:

0X81 – ANALOG CONTROL REGISTER				
7	Reserved	R	Reserved	0
6	IREF	R/W	0 = Internal current reference 1 1 = Internal current reference increase 30%	0
5	VREF	R/W	0 = Internal voltage reference 1 = Internal voltage reference shut down	0
4	Reserved	R/W	Reserved	0

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From:

0X93 – LUMA DELAY AND H FILTER CONTROL				
7	CKLM	R/W	Color Killer mode. 0 = Normal 1 = Fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-0	Reserved	RW		0h

To:

0X93 – LUMA DELAY AND H FILTER CONTROL				
7	CKLM	R/W	Color Killer mode 0 = Normal 1 = Fast (for special application)	0
6-4	YDLY	R/W	Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control.	3
3-0	HPF_RES	R/W	Reserved	0

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From:

0X9C – OVSEND				
7	HASYNC	R/W	1: The length of EAV to SAV is set up and fixed by HBLEN registers. 0: The length of SAV to EAV is set up and fixed by HACTIVE registers.	0
6-4	OFDLY	R/W	FIELD output delay. 0h: 0H line delay FIELD output. (601 mode only) 1h-6h: 1H-6H line delay FIELD output. 7h: Reserved	2

To:

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X9C – OVSEND				
7	HASYNC	R/W	1 = The length of EAV to SAV is set up and fixed by HBLEN registers. 0 = The length of SAV to EAV is set up and fixed by HACTIVE registers.	0
6-4	OFDLY	R/W	FIELD output delay. 0 = No line delay FIELD output. (601 mode only) 1-6 = 1-6 line delay FIELD output. 7 = Reserved	2

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From:

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X41 – VIDEO ENCODER STANDARD CONTROL				
7	HZ50	R/W	1 = 50Hz field rate 0 = 60Hz field rate	0
6	INTERLACE	R/W	1 = Interlaced output 0 = Noninterlaced output	1
5-4	FSCSEL	R/W	FSCSEL frequency selection 00 = NTSC-M 01 = PAL-B 10 = PAL-M 11 = PAL-N	0

To:

Register Descriptions (Continued)

BIT	FUNCTION	R/W	DESCRIPTION	RESET
0X41 – VIDEO ENCODER STANDARD CONTROL				
7	HZ50	R/W	1 = 50Hz field rate 0 = 60Hz field rate	0
6	INTERLACE	R/W	1 = Interlaced output 0 = Noninterlaced output	1
5-4	FSCSEL	R/W	FSCSEL frequency selection 0 = NTSC-M 1 = PAL-B 2 = PAL-M 3 = PAL-N	0

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Report Name: Product List
Notice Number: PA16097
Effective Date: November 11, 2016
Begin Date: November 11, 2014
End Date: November 11, 2016

Product List

TW9966AT-LC1-GR
TW9966AT-LC1-GRT