ANALOG DEVICES

EVAL-ADGM1004SDZ User Guide
UG-1462

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the ADGM1004 0 Hz/DC to 13 GHz, 2.5 kV HBM ESD, SP4T MEMS Switch with Integrated Driver

FEATURES

Single supply voltage 3.3 V
Wide frequency range
SMA connectors for RF signals
SMB connectors for switch control signals
On-board calibration transmission line for analyzer calibration

EVALUATION KIT CONTENTS

EVAL-ADGM1004SDZ evaluation board

DOCUMENTS NEEDED

ADGM1004 data sheet

EQUIPMENT NEEDED

3.3 V dc power supply
PC
EVAL-SDP-CB1Z controller board
USB cable, provided in EVAL-SDP-CB1Z board kit
Vector network analyzer

GENERAL DESCRIPTION

The EVAL-ADGM1004SDZ evaluates the ADGM1004 wideband, single-pole, four-throw (SP4T), microelectromechanical systems (MEMS) switch, and a control chip copackaged in a compact, 24-lead, 5 mm × 4 mm × 1.45 mm, lead frame chip scale package (LFCSP). The SP4T switch uses Analog Devices, Inc., MEMS switch technology, which provides optimum bandwidth performance, power handling capability, and linearity for radio frequency applications. The control chip generates the high voltage signals necessary for the MEMS switch and allows the user to control operation through a flexible, complementary metal oxide semiconductor (CMOS), low voltage transistor to transistor logic (LVTTL) compliant, parallel interface, as well as through a serial peripheral interface (SPI). It is possible to daisy-chain multiple ADGM1004 devices together, which enables the configuration of multiple devices with a minimal amount of digital lines.

For the SPI interface, the EVAL-ADGM1004SDZ connects to the USB port of a PC via a system demonstration platform (SDP) board. The EVAL-SDP-CB1Z (SDP-B) controller board is acceptable to use, and is available to order on the Analog Devices website at www.analog.com/SDP-B.

The EVAL-ADGM1004SDZ is fitted with connectors for RF and control signals, as well as links that allow the user to control the operation of the switch and evaluate the performance of the ADGM1004.

For full specifications on the ADGM1004, consult the ADGM1004 data sheet, which must be used in conjunction with this user guide when using the EVAL-ADGM1004SDZ.

TABLE OF CONTENTS

Features 1
Evaluation Kit Contents 1
Documents Needed 1
Equipment Needed 1
General Description 1
Revision History 2
Evaluation Board Connection Diagram 3
Evaluation Board Hardware 4
Power Supply 4
RF Connectors 4
Switch Control Connectors 4
Evaluation Board Software for SPI Interface 6
Installing the Software 6
Initial Setup 6
Block Diagram and Description 7
Memory Map 8
Measuring Switch Performance 9
Network Analyzer Calibration Procedure 11
Handling Guidelines 12
Evaluation Board Schematics and Artwork 13
Ordering Information 18
Bill of Materials 18

REVISION HISTORY

11/2019—Revision 0: Initial Version

EVALUATION BOARD CONNECTION DIAGRAM

Figure 1 shows the evaluation board connect diagram.

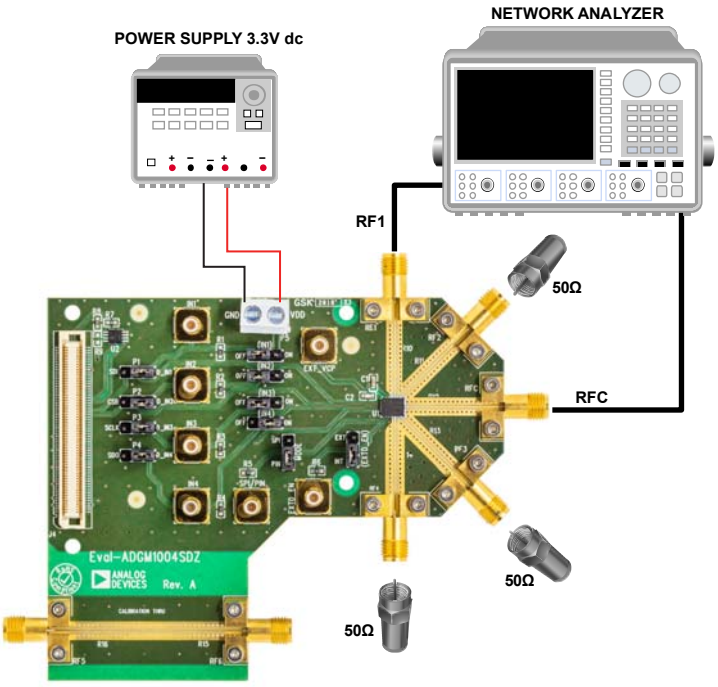

Figure 1.

EVALUATION BOARD HARDWARE

The EVAL-ADGM1004SDZ evaluation kit contains a fully fitted printed circuit board (PCB).

The EVAL-ADGM1004SDZ allows the RF signals to connect to the MEMS switch. Control the switch operation either by using the on-board links or by applying the correct control signals to the appropriate connectors.

The EVAL-ADGM1004SDZ provides an additional transmission line to facilitate the calibration of the network analyzer, which minimizes the effects of the PCB tracks that connect the RF signals to the MEMS switch. The calibration process is described in the Network Analyzer Calibration Procedure section.

POWER SUPPLY

To operate the EVAL-ADGM1004SDZ, provide an external power supply connected to the P5 power block. The supply voltage is 3.3 V, and must be positive with respect to the ground of the PCB. The ground of the PCB is marked as GND on the silkscreen (see Figure 18).

RF CONNECTORS

The RF1 to RF4, and RFC Subminiature Version A (SMA) edge connectors on the EVAL-ADGM1004SDZ connect to each switch on the ADGM1004 for performance evaluation purposes. The RF5 and RF6 connectors connect to a transmission line to estimate the loss associated with the PCB (see the Measuring Switch Performance section). Table 1 describes the RF connectors on the ADGM1004.

Table 1. ADGM1004 RF Connectors

Connector	Description
RFC	Common RF port of the ADGM1004
RF1	Port RF1 of the ADGM1004
RF2	Port RF2 of the ADGM1004
RF3	Port RF3 of the ADGM1004
RF4	Port RF4 of the ADGM1004
RF5, RF6	CALIBRATION THRU calibration transmission lines used for calibration

SWITCH CONTROL CONNECTORS

The internal control IC co-packaged with the MEMS switch generates the voltage required to drive the switch. The control IC generates a reference clock signal at 10 MHz. In normal operation, set the EXTD_EN link to the INT position to allow the built in, 10 MHz oscillator to enable the internal driver IC voltage boost circuitry. Setting the EXTD_EN link to the EXT position disables the internal 10 MHz oscillator and driver boost circuitry. Disabling the internal oscillator eliminates the associated 10 MHz noise feedthrough from the switch. With the internal oscillator disabled, the VCP pin must be driven with 80 V dc from an external voltage supply. An external 80 V dc must be applied at the EXT_VCP SMB connector located on the EVAL-ADGM1004SDZ. With the oscillator disabled, the switch can be controlled by parallel logic interface (as shown in Table 4) or via the SPI. With the internal oscillator disabled, the ADGM1004 only consumes a 50 μA maximum supply current.

R10 to R16 are the place holder locations for the 10 MΩ shunt resistors, which can be placed on all RFx pins (RF1 to RF4, and RFC) to avoid floating nodes. For more details, see the ADGM1004 data sheet.

The ADGM1004 comes with a standard LVTTL parallel interface consisting of four input pins (Pin IN1 to Pin IN4) which are controlled by the IN1 to IN4 links. See Table 4 for more details on the logic control when using the parallel interface.

The ADGM1004 also has an SPI interface, which the P1 to P4 links control. Set the MODE link to the SPI position to enable the SPI interface. Set the MODE link to the PIN position to enable parallel interface (see Table 2).

Table 2. MODE Link Position

Position	Reference Clock Setting
PIN (Default)	Enables parallel interface
SPI	Enables SPI interface, disables parallel interface

Table 3. EXTD_EN Link Position

Position	Reference Clock Setting
INT (Default)	Enables built in 10 MHz oscillator
EXT	Disables the internal oscillator

RFx to RFC Switch Control

The IN1 to IN4 input pins control the switch state and operation mode of the ADGM1004 in parallel interface mode. The EVAL-ADGM1004SDZ allows the user to control these pins by using the IN1 to IN4 and P1 to P4 links (see Table 4), or by applying external signals to the IN1 to IN4 SMB connectors when in parallel interface mode. To apply external digital signals to the IN1 to IN4 links via the SMA connectors, headers must be removed to leave the IN1 to IN4 links floating.

Table 4. P1 to P4 and IN1 to IN4 Link Settings for Parallel Logic Interface

Controlled RF Switch	RF Switch Status	Link Name	Link Position
RF1 to RFC	On	P1	D_IN1
		IN1	On
	Off	P1	D_IN1 (default)
		IN1	Off (default)
RF2 to RFC	On	P2	D_IN2
		IN2	On
	Off	P2	D_IN2 (default)
		IN2	Off (default)
RF3 to RFC	On	P3	D_IN3
		IN3	On
	Off	P3	D_IN3 (default)
		IN3	Off (default)
RF4 to RFC	On	P4	D_IN4
		IN4	On
	Off	P4	D_IN4 (default)
		IN4	Off (default)

EVALUATION BOARD SOFTWARE FOR SPI INTERFACE

INSTALLING THE SOFTWARE

The EVAL-ADGM1004SDZ uses the Analog Devices Analysis, Control, Evaluation (ACE) software. The ACE software is a desktop software application that allows the evaluation and control of multiple evaluation systems.

The ACE software installer installs the necessary SDP drivers and .NET Framework 4 by default. Install the ACE software before connecting the SDP-B board to the EVAL-ADGM1004SDZ. Find the ACE software and access to full instructions on how to install and use the software on the Analog Devices website at www.analog.com/ace.

When the installation is finished, the ACE software starts and the EVAL-ADGM1004SDZ plugins appear.

INITIAL SETUP

To set up the EVAL-ADGM1004SDZ, take the following steps:

1. Change the position of the P1, P2, P3, and P4 links to SDI, $\overline{CS}$, SCLK, and SDO, respectively.
2. Change the MODE link position from PIN to SPI and keep the EXTD_EN link position set to INT.
3. Connect the EVAL-ADGM1004SDZ to the SDP-B board, and connect the SDP-B board to the PC via the USB cable.
4. Power up the EVAL-ADGM1004SDZ as described in the Power Supply section.
5. Run the ACE software. The EVAL-ADGM1004SDZ plugins appear in the **Attached Hardware** section of the **Start** tab (see Figure 2).
6. Double click the **EVAL-ADGM1004SDZ** plugin to open the **EVAL-ADGM1004SDZ** view in Figure 3.
7. Double click the ADGM1004 chip to access the chip block diagram (see Figure 4). This diagram provides a basic representation of the EVAL-ADGM1004SDZ functionality. The main functions are labeled in Figure 4.

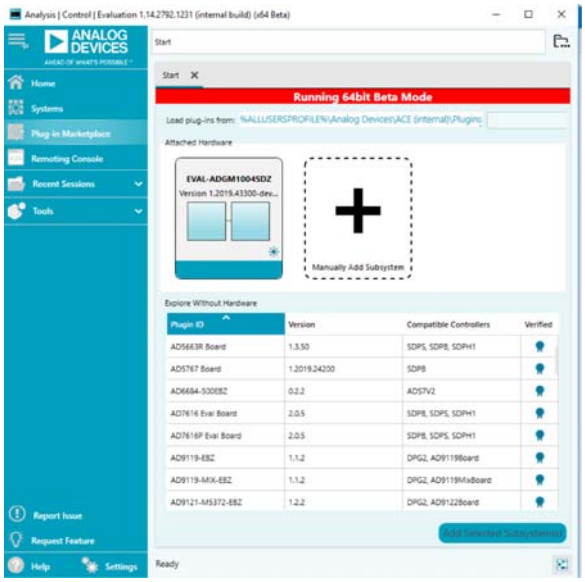

Figure 2. EVAL-ADGM1004SDZ Plugin Startup Window

Table 5. SPI Interface Link Descriptions

Link	Position	Description
P1	SDI	Serial data input (SDI) pin
P2	CSB	Chip select ($\overline{CS}$) pin
P3	SCLK	Clock input (SCLK) pin
P4	SDO	Serial data output (SDO) pin

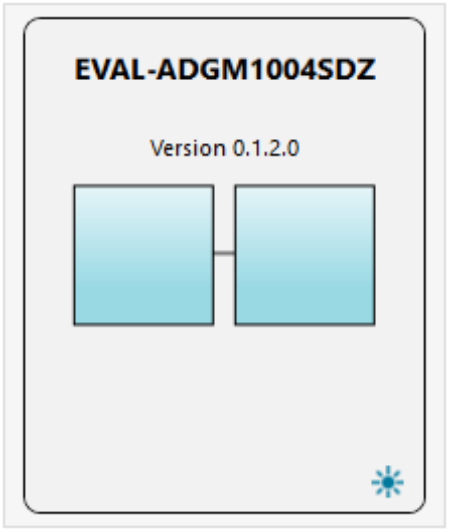

Figure 3. Evaluation Board View of the EVAL-ADGM1004SDZ Plugin

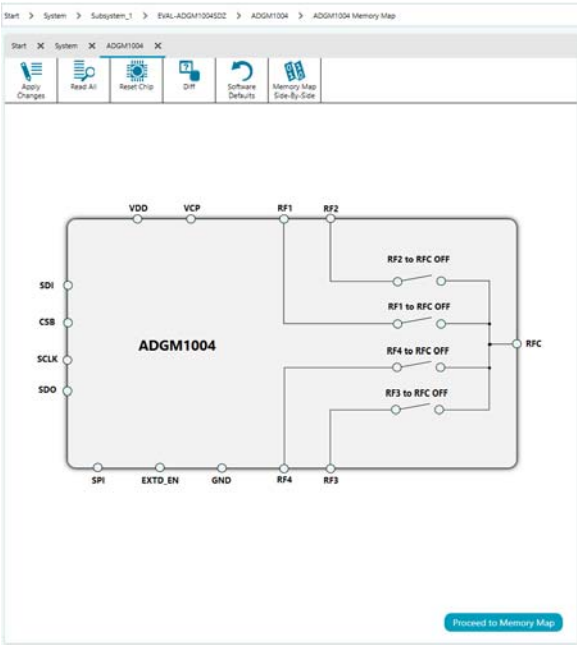

Figure 4. Chip Block Diagram View of the EVAL-ADGM1004SDZ Plugin

BLOCK DIAGRAM AND DESCRIPTION

The organization of the ACE software is similar to the functional block diagram shown in the ADGM1004 data sheet. In this way, it is easy to correlate the functions on the EVAL-ADGM1004SDZ with the corresponding descriptions in the data sheet. The ADGM1004 data sheet provides a full description of each block and register, as well as the respective settings.

Some blocks and the corresponding functions pertain to the EVAL-ADGM1004SDZ, and are described in Table 6. The full screen block diagram shown in Figure 5 displays the functionality of each block.

All changes to the blocks correspond to the block diagram in the ACE software. For example, when the internal register bit is enabled, it displays as enabled on the block diagram. Any bits or registers that are bolded are modified values that have not been transferred to the EVAL-ADGM1004SDZ. Click **Apply Changes** to transfer the data to the EVAL-ADGM1004SDZ.

Table 6. Block Diagram Functions

Label	Function
A	Click the switch symbol to open and close the RF1 to RFC switch.
B	Click the switch symbol to open and close the RF2 to RFC switch.
C	Click the switch symbol to open and close the RF3 to RFC switch.
D	Click the switch symbol to open and close the RF4 to RFC switch.
E	Click **Apply Changes** to apply all modified values to the EVAL-ADGM1004SDZ.

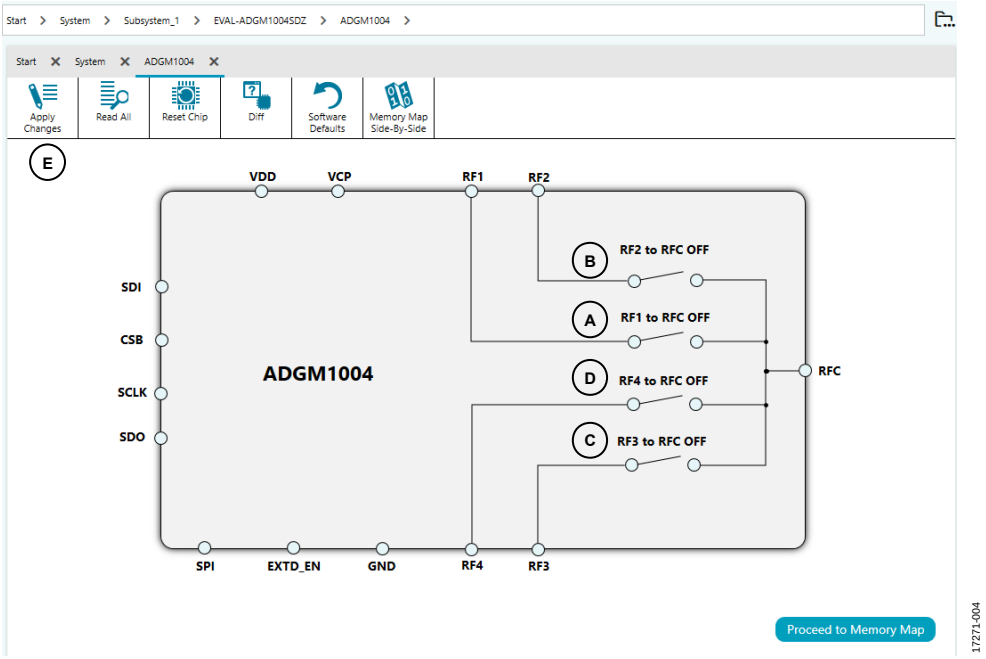

Figure 5. Labeled EVAL-ADGM1004SDZ Block Diagram

MEMORY MAP

All registers are fully accessible from the **ADGM1004 Memory Map** tab, and can be edited at a bit level (see Figure 6). The bits in dark gray are read only bits and cannot be accessed from the ACE software. All other bits are toggled. The **Apply Changes** button transfers data to the device. All changes made in this tab correspond to the block diagram.

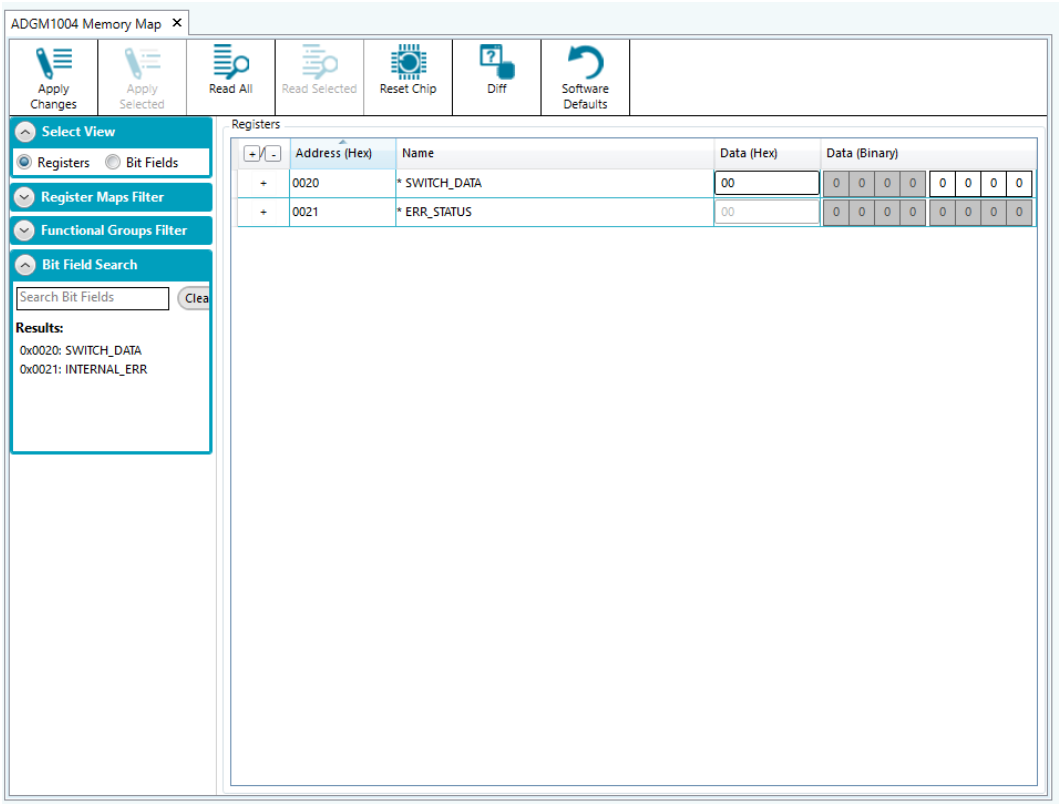

Figure 6. ADGM1004 Memory Map

MEASURING SWITCH PERFORMANCE

Figure 1 shows the EVAL-ADGM1004SDZ connection diagram. Apply a VDD supply (V_{DD}) to the EVAL-ADGM1004SDZ to measure the performance of the switch. The links are set according to the switch under test (see Table 4). After selecting the desired channel and the state of the channel, use a network analyzer to collect the switch performance data. Terminate the RFx edge connectors of unused switch channels to 50 Ω loads to achieve the full performance of the channel under test.

The EVAL-ADGM1004SDZ comes with the CALIBRATION THRU calibration transmission line on the PCB. This calibration transmission line removes the insertion loss and phase offset of the PCB transmission lines connecting to the switch from the measurement. Figure 7 shows the calibration transmission line, and Figure 8 shows the calibration transmission line insertion loss and return loss up to 16 GHz. The calibration transmission line is exactly the same length as the distance from any one RFx connector to the RFx pin of the device, plus the distance from the RFC connector to the RFC pin of the device (see Label A and Label B in Figure 9).

Figure 7. EVAL-ADGM1004SDZ Calibration Transmission Line for PCB Insertion Loss and Phase Offset Correction

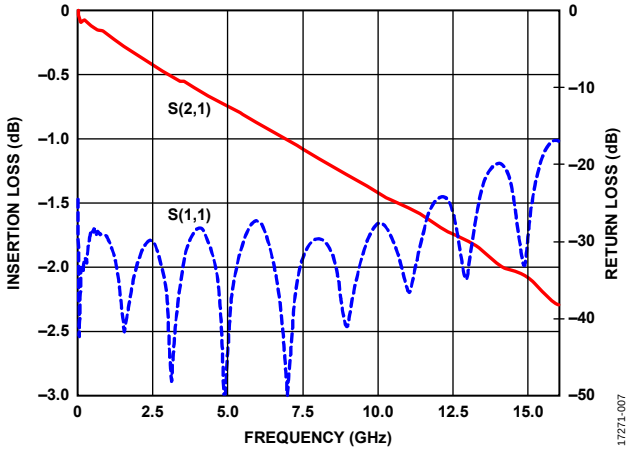

Figure 8. Calibration Transmission Line Insertion Loss (S(2,1)) and Return Loss (S(1,1))

Figure 9 shows the calibration transmission line length. All RF traces connecting to the ADGM1004 are of equal length.

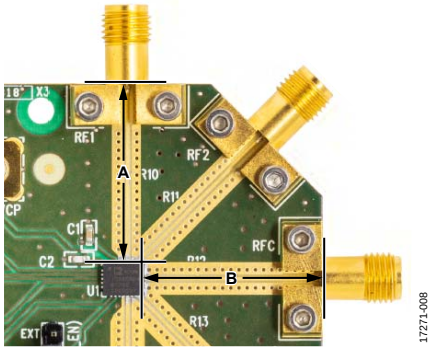

Figure 9. Length of A + B Equal to Length of Calibration Transmission Line

To de-embed the PCB calibration transmission line insertion loss from the entire switch insertion loss board measurement (the RF1 to RFC path), divide the S(2,1) of measured data by the |S(2,1)| of the calibration transmission line. To perform this de-embedding using the network analyzer at the time of the measurement or after the measurement, use individual measurement data files. Refer to the Network Analyzer Calibration Procedure section for more information.

Use the network analyzer port extension function to de-embed the phase offset introduced by the PCB calibration transmission lines. The port extension method uses time delay offset values for phase correction. To perform this de-embedding, enter the time delays into the port extension menu on the network analyzer corresponding to the phase offset introduced from an RF edge connector to the RFx pin of the ADGM1004. Figure 9 shows an example of these phase offsets on a typical switch measurement, labeled as A and B. Both A and B are identical in length, and can be calculated by measuring the time delay of the calibration transmission line and dividing it by 2.

Figure 10 shows the ADGM1004 switch insertion loss (network analyzer two-port S(2,1) measurement) measurement results that are de-embedded with respect to the PCB calibration transmission line losses. The blue trace is the RF2 to RFC switch channel, and the red trace is the RF1 to RFC switch channel. The dashed traces are the respective return loss traces. The performance of the RF2 switch is identical to the RF3 switch, and the performance of the RF1 switch is identical to the RF4 switch.

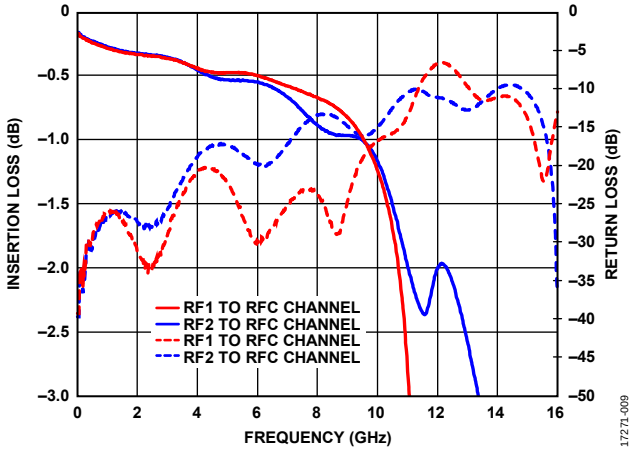

Figure 10. PCB De-Embedded ADGM1004 Insertion Loss and Return Loss Performance

Figure 11 shows the ADGM1004 switch off isolation performance measurement results for two channels. The blue trace is the RF2 to RFC switch channel, and the red trace is the RF1 to RFC switch channel. The performance of the RF2 switch is identical to the RF3 switch, and the performance of the RF1 switch is identical to the RF4 switch.

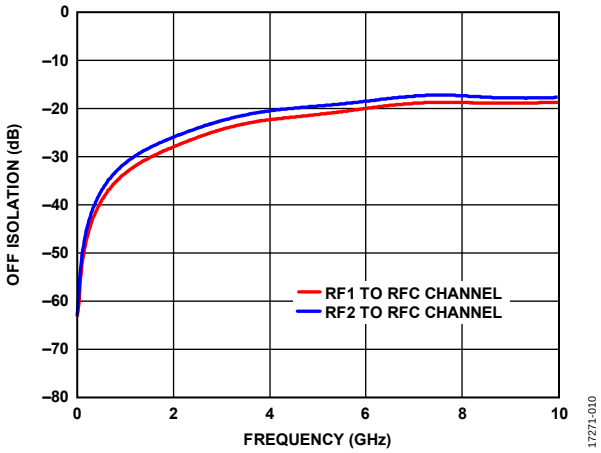

Figure 11. ADGM1004 Off Isolation Performance

NETWORK ANALYZER CALIBRATION PROCEDURE

The maximum value of the network analyzer frequency sweep for the EVAL-ADGM1004SDZ PCB can be up to 16 GHz. Assuming the user has a set of manual calibration standards or an electric calibration type unit to perform a short load open through (SLOT) calibration of the network analyzer, use the following procedure in conjunction with the EVAL-ADGM1004SDZ to perform two-port measurements of the ADGM1004:

1. Perform a full, two-port standard SLOT calibration of the network analyzer.
2. Connect the CALIBRATION THRU calibration transmission line (Connector RF5 and Connector RF6) to the analyzer and measure the insertion loss (S(2,1)).
3. Save the measured data to the network analyzer memory for later use.
4. Configure the EVAL-ADGM1004SDZ links, and power up the EVAL-ADGM1004SDZ with a 3.3 V dc power supply.
5. Connect the network analyzer to the desired MEMS switch RF connectors and apply the external control signals as needed.
6. Measure the complete insertion loss of the EVAL-ADGM1004SDZ. Include the insertion loss of the MEMS switch and test fixture (PCB calibration transmission lines and RF connectors).
7. De-embed the PCB losses from the complete EVAL-ADGM1004SDZ measurement using the data saved from Step 3 and the measured data from Step 6. Because the extraction method is dependent on the network analyzer, consult the network analyzer user manual before performing the extraction. Typically, the divide function divides the complete S(2,1) measurement data by the CALIBRATION THRU calibration transmission line S(2,1) data stored in memory.
8. Use the network analyzer port extension function to de-embed the phase offset introduced by the PCB calibration transmission lines. The port extension method uses time delay offset values to correct for phase. To switch the pin path equal to the electrical length of the calibration transmission line divided by two, enter the time delay values into the port extension menu on the network analyzer for each RF edged connector.

HANDLING GUIDELINES

Adhere to the following handling guidelines when using the EVAL-ADGM1004SDZ:

- Always treat the ADGM1004 as a static sensitive device and observe normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps, and using other electrostatic discharge (ESD) control devices.
- Take care when connecting signals. Hold the EVAL-ADGM1004SDZ from the edges to avoid any damage to the device under test (DUT).
- Avoid connecting live signal sources to the EVAL-ADGM1004SDZ. Ensure that outputs are switched off (preferably grounded) before connecting to the DUT. Ensure that all instrumentation shares a common chassis ground.
- Avoid running measurement instruments such as digital multimeters (DMMs) in autorange modes. Some instruments generate large transient compliance voltages when switching ranges.
- Use the highest practical range (lowest resolution) setting for resistance measurements to minimize compliance voltages.
- Physically handle the EVAL-ADGM1004SDZ with care.

EVALUATION BOARD SCHEMATICS AND ARTWORK

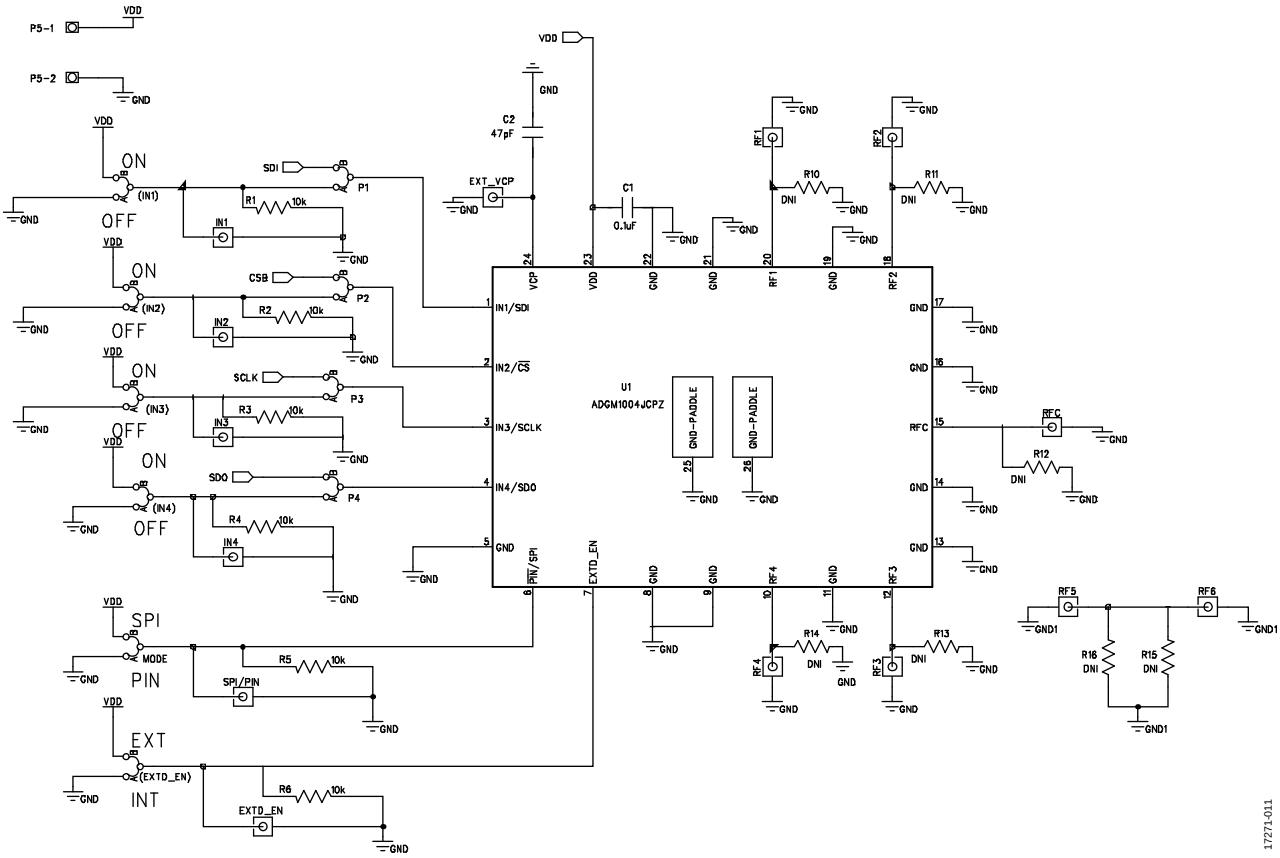

Figure 12. EVAL-ADGM1004SDZ Schematic

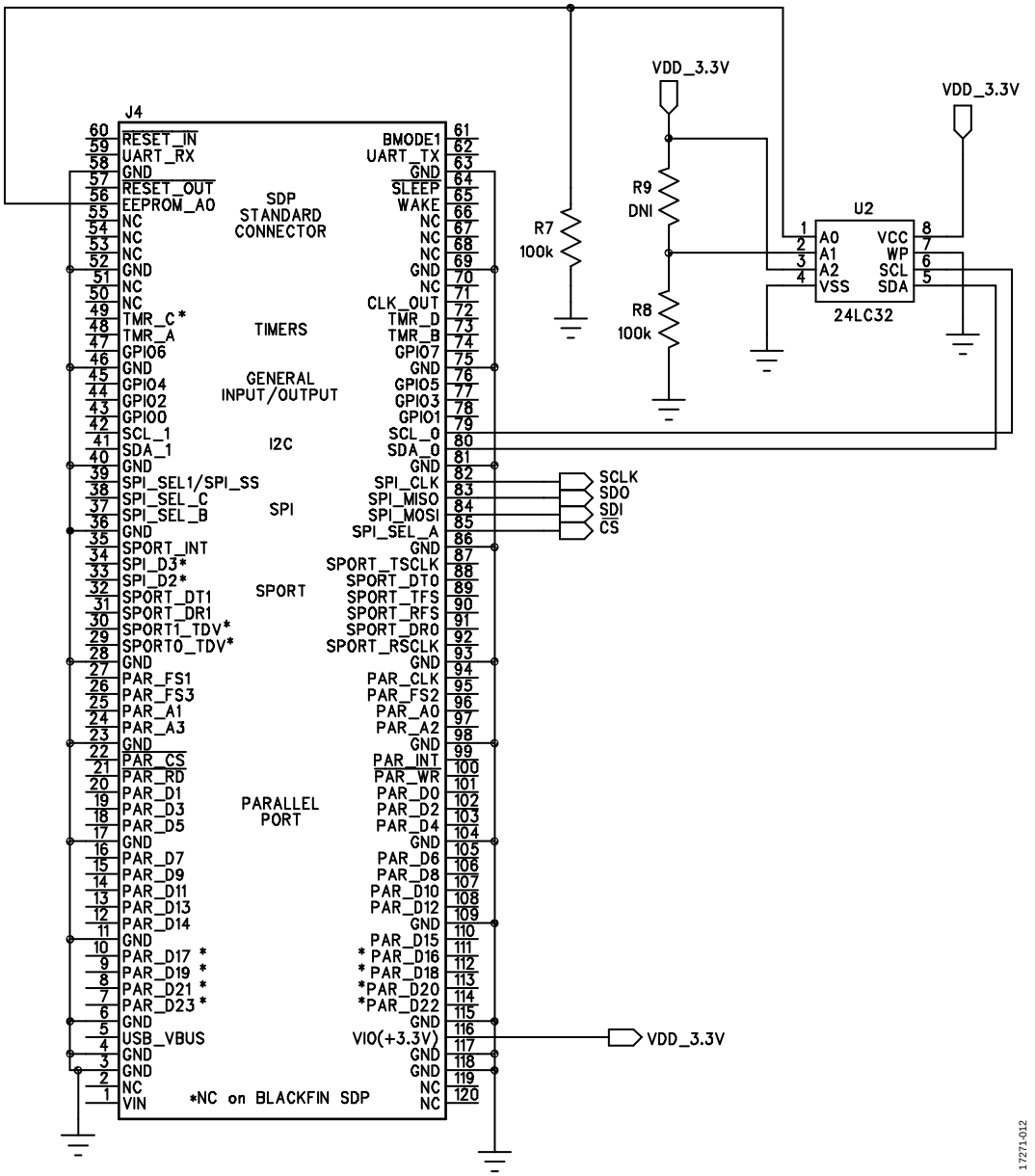

Figure 13. EVAL-ADGM1004SDZ Schematic with SDP-B Board

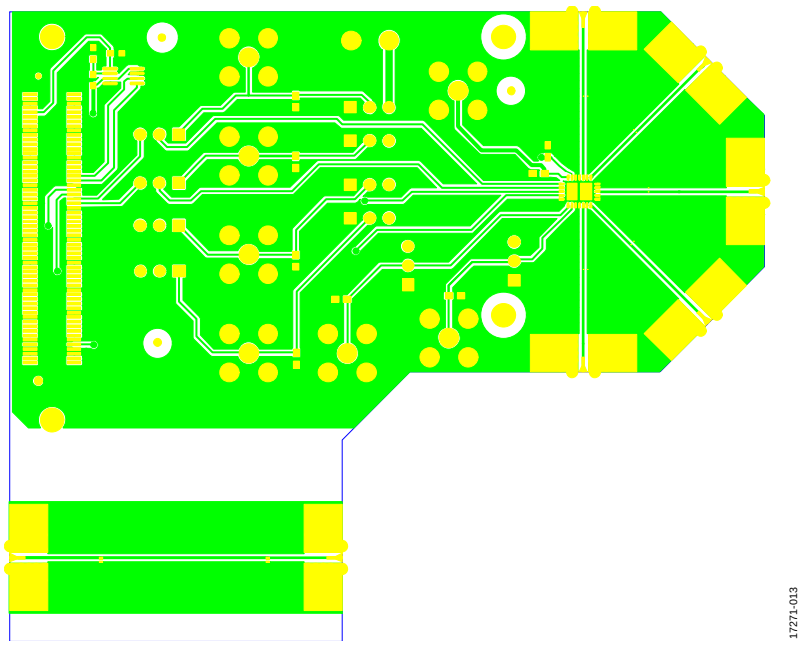

Figure 14. EVAL-ADGM1004SDZ Component Side, PCB Drawing (Layer 1)

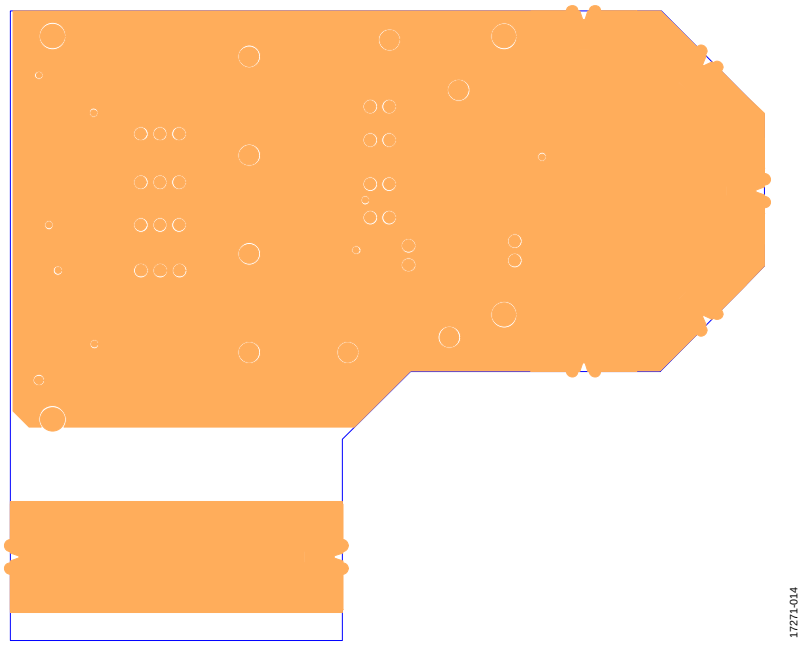

Figure 15. EVAL-ADGM1004SDZ Component Side, Ground Plane PCB Drawing (Layer 2)

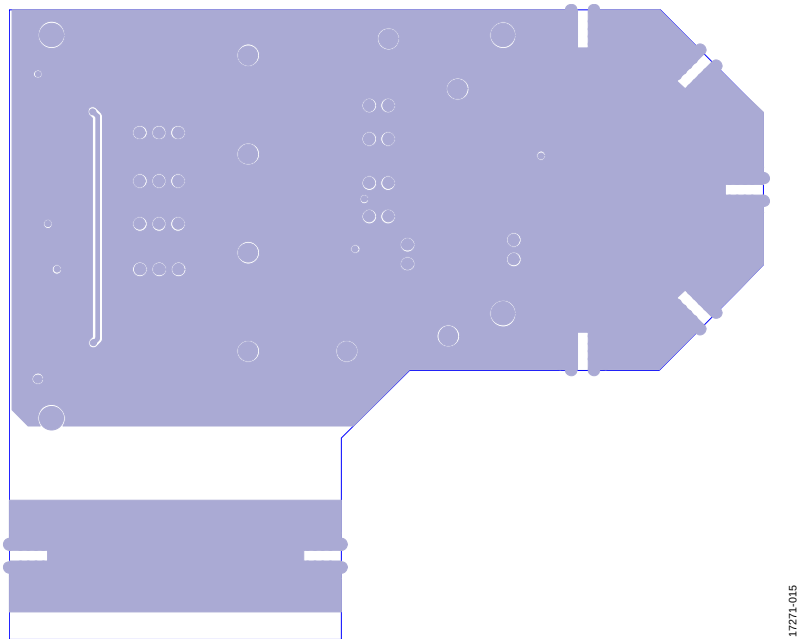

Figure 16. EVAL-ADGM1004SDZ Component Side, Ground Plane PCB Drawing (Layer 3)

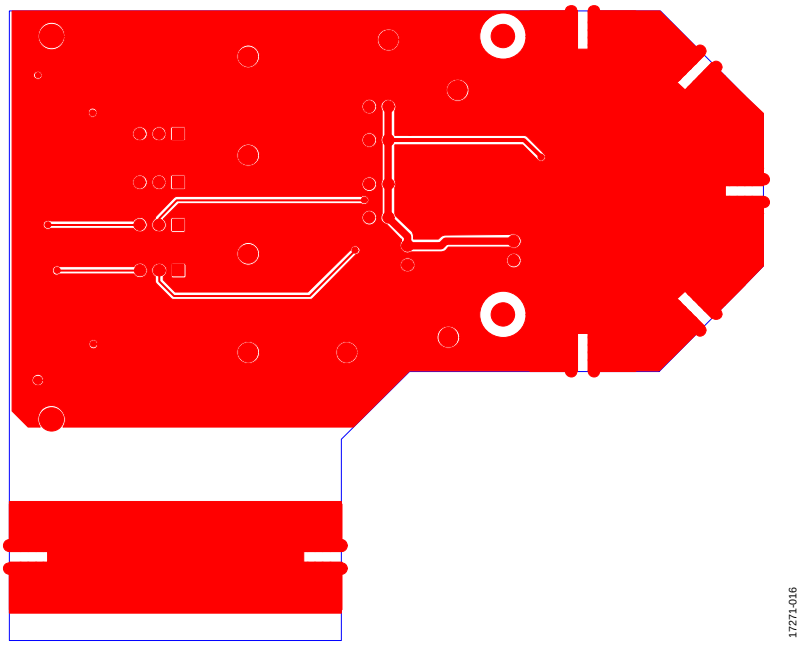

Figure 17. EVAL-ADGM1004SDZ Component Side, Bottom Side PCB Drawing (Layer 4)

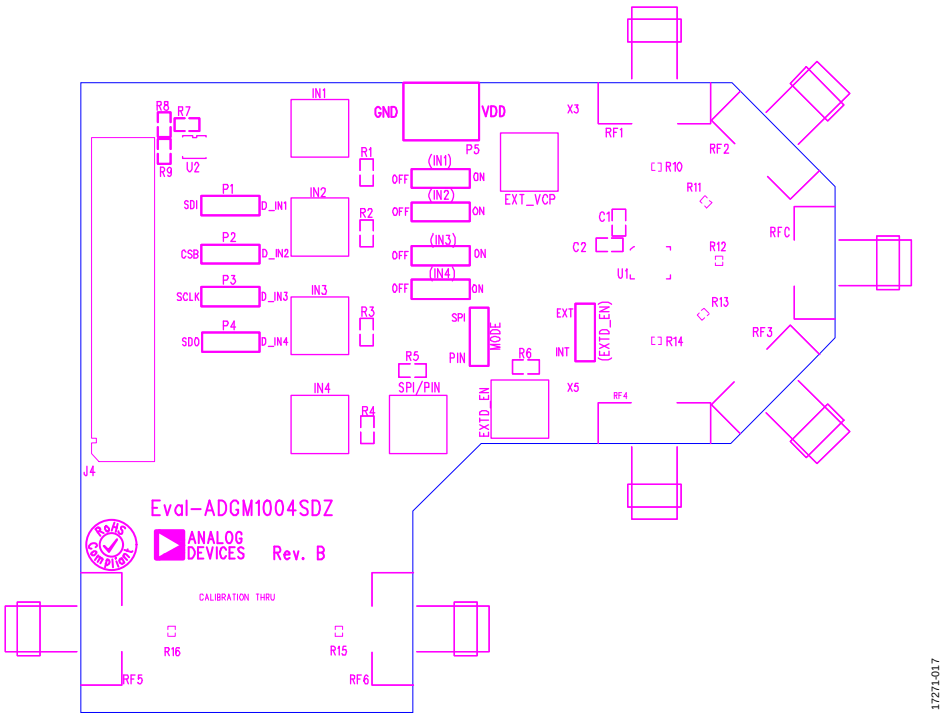

Figure 18. EVAL-ADGM1004SDZ Component Side, Silkscreen PCB Drawing (Top)

METAL 1	FINISHED COPPER PLATING: 1.5oz (2.1 THOU/53µm)
	ROGERS RO4003C: 8 THOU LAMINATE, ER 3.38 STARTING COPPER WEIGHT 0.5oz/0.5oz
METAL 2	COPPER WEIGHT: 1oz (1.4 THOU/35µM)

~37.2 THOU FR4

METAL 3	COPPER WEIGHT: 1oz (1.4 THOU/35 µm)
	ROGERS RO4003C: 8THOU LAMINATE, ER 3.38 STARTING COPPER WEIGHT 0.5oz/0.5oz
METAL 4	FINISHED COPPER PLATING: 1.5oz (2.1 THOU/53µm)

CPWG RF TRACE WIDTH: 15 THOU
CPWG RF TRACE TO GROUND GAP:12.2 THOU
FINAL OVERALL PCB THICKNESS:62 THOU
FINAL COPPER PLATING THICKNESS
ON TOP AND BOTTOM LAYERS: 1.5oz

17271-019

Figure 19. EVAL-ADGM1004SDZ PCB Stackup with Coplanar Waveguide and Ground (CPWG) Dimensions

ORDERING INFORMATION

BILL OF MATERIALS

Table 7. Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Part Number
6	IN1 to IN4, EXTD_EN, EXT_VCP	50 Ω, SMB connectors through holes	Amphenol	SMB1251B1-3GT30G-50
10	(IN1) to (IN4), (EXTD_EN), MODE, P1 to P4	3-pin headers	Harwin	M20-9990345
10	(IN1) to (IN4), (EXTD_EN), MODE, P1 to P4	Shorting links	Harwin	M7566-05
2	P5	2-pin, terminal blocks (5 mm pitch)	Lumberg	KRM 02
1	C1	0.1 µF, 0603 package, 16 V, X7R, surface mount diode (SMD) ceramic capacitor	Multicomp Pro	MCB0603R104KCT
1	C2	47 pF, 0603 package, 100 V, C0G/NP0 capacitor	AVX Corporation	06031A470JAT2A
1	J4	FX8-120S-SV(21), 120-way connector, 0.6 mm pitch	Hirose(HRS)	FX8-120S-SV(21)
6	R1 to R6	10 kΩ, (0603 package) SMD resistors	Multicomp	MC0063W0603110K
2	R7, R8	100 kΩ, (0603 package) SMD resistors	Multicomp Pro	MC0063W06031100K
1	R9	Do not install	Not applicable	Not Applicable
7	R10 to R16	10 MΩ, (0201 package) SMD resistors, do not install	Not applicable	Not Applicable
7	RF1 to RF6, RFC	50 Ω, side launch SMA connectors	Rosenberger	32K243-40ML5
1	U1	ADGM1004, 0 Hz/dc to 13 GHz, SP4T, MEMS switch with integrated driver	Analog Devices	ADGM1004
1	U2	24LC32A-I/MS, 32K I²C serial electronically erasable programmable read-only memory (EEPROM)	Microchip	24LC32A-I/MS
3	Not Applicable[1]	Wideband, 50 Ω termination SMA loads	Pasternack	PE6081

[1] Screwed on at measurement time (see Figure 1).

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ANALOG DEVICES

www.analog.com