XC6602 Series

ETR03045-007a

1A, 0.5V Low Input Voltage, High Speed LDO Regulator

■GENERAL DESCRIPTION

The XC6602 series is a low voltage input (0.5V) operation and provides high accuracy ±15mV/±20mV and can supply large current efficiently due to its ultra low on-resistance even at low output voltages.

The series is ideally suited to the applications which require high current in low input/output voltages and consists of a Nch driver transistor, a voltage reference, an error amplifier, a current limiter, a fold-back circuit, a thermal shutdown (TSD) circuit, an under voltage lock out (UVLO) circuit, a soft-start circuit and a phase compensation circuit.

Output voltage is selectable in 0.1V increments within a range of 0.5V to 1.8V using laser trimming technology and ceramic capacitors can be used for the output stabilization capacitor (C_L). The inrush current (I_{RUSH}) from V_{IN} to V_{OUT} for charging C_L at start-up can be reduced and makes the V_{IN} stable. The soft-start time is optimized internally.

The CE function enables the output to be turned off and the series to be put in stand-by mode resulting in greatly reduced power consumption. At the time of entering the stand-by mode, the series enables the electric charge at the output capacitor (C_L) to be discharged via the internal switch. As a result the V_{OUT} pin quickly returns to the V_{SS} level.

The CE pull-down function keeps the IC to be in stand-by mode even if the CE pin is left open.

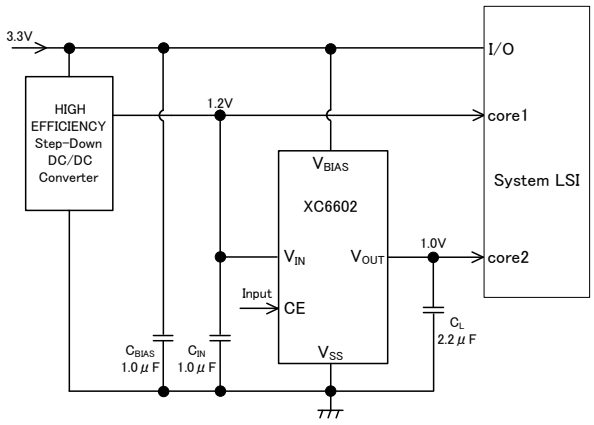
■APPLICATIONS

- Smart phones / Mobile phones
- Digital still cameras / Camcorders
- Note PC / Tablet PC
- E-book Readers / Electronic dictionaries
- Wireless LAN

■FEATURES

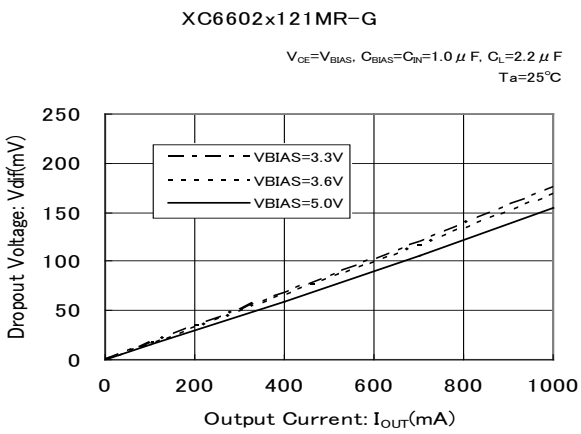
Maximum Output Current	:	1A (1.3A Limit)
ON Resistance	:	0.15Ω@V_{BIAS}=3.6V,V_{OUT}=1.2V
Bias Voltage Range	:	2.5V ~ 6.0V
Input Voltage Range	:	0.5V ~ 3.0V
Output Voltage Range	:	0.5V ~ 1.8V (0.1V increments)
Output Voltage Accuracy	:	±0.015V@V_{OUT}＜1.2V ±0.020@V_{OUT}≧1.2V
Ripple Rejection	:	60dB@f=1kHz (V_{BIAS_PSRR}) 75dB@f=1kHz(V_{IN_PSRR})
Low Power Consumption	:	100μA (V_{BIAS}), 6.5μA(V_{IN})@V_{OUT}=1.2V
Stand-by Current	:	0.01μA (V_{BIAS}), 0.01μA (V_{IN})
Under-voltage Lockout	:	1.8V (V_{BIAS}), 0.4V (V_{IN})
Thermal Shutdown	:	150℃@detect, 125℃@release
Protection Circuit	:	Fold-back Current Limit, TSD, UVLO
Function	:	Built-in Soft-start CE Pull-Down (Active High) C_L Auto Discharge
Operating Ambient Temperature	:	-40℃~ 85℃
Output Capacitor	:	Ceramic Capacitor Compatible (2.2μF)
Packages	:	USP-6C, SOT-26W, SOT-89-5,WLP-5-02
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

■ TYPICAL APPLICATION CIRCUIT



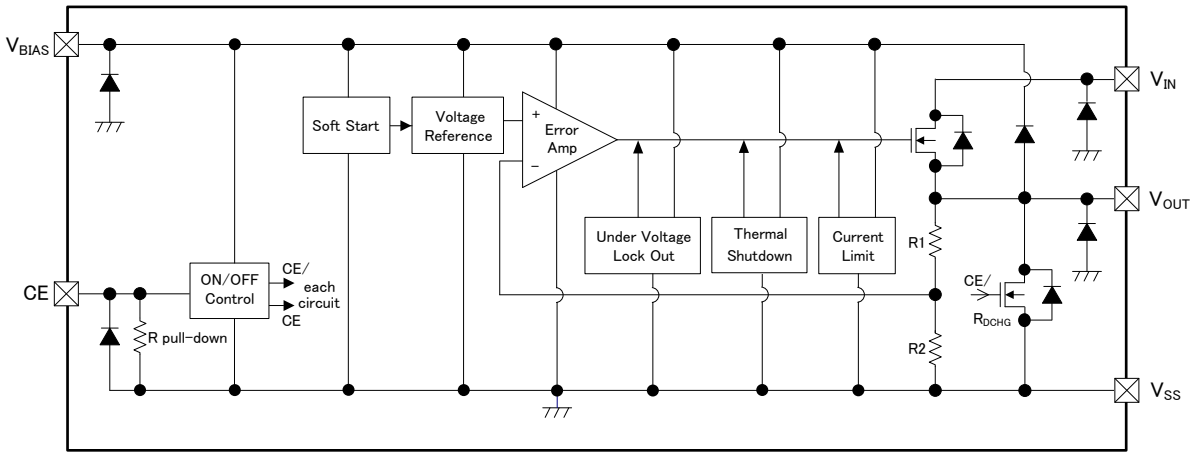
■TYPICAL PERFORMANCE CHARACTERISTICS

●Dropout Voltage vs. Output Current

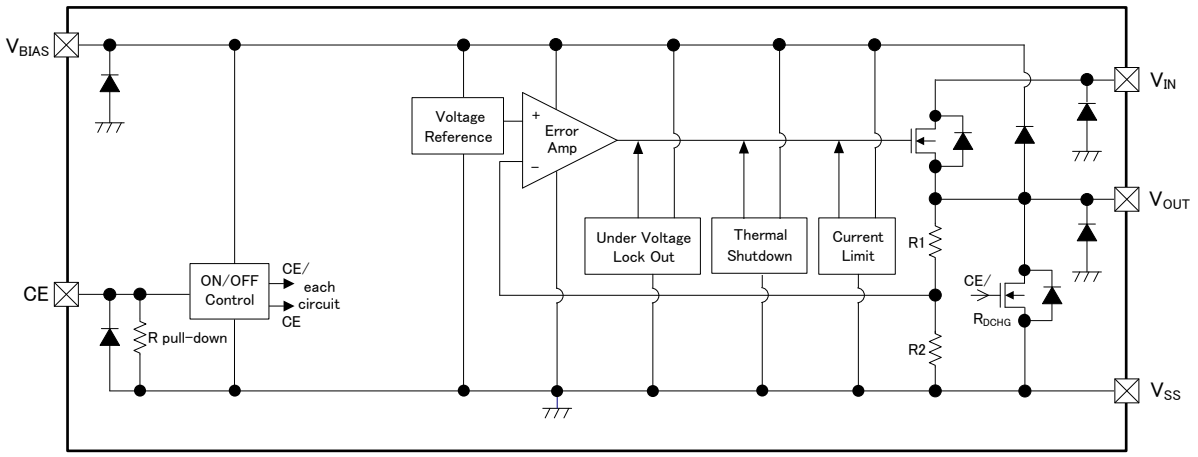


■BLOCK DIAGRAMS

・Type A



・Type B



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

■PRODUCT CLASSIFICATION

1）Ordering Information

XC6602①②③④⑤⑥–⑦(*1) With soft-start circuit built-in, can be selected from with or without functions

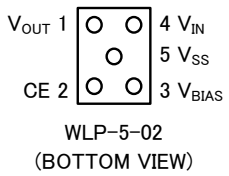
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	A	Soft-start included
		B	Soft-start excluded
②③	Output Voltage	05~18	e.g. 1.2V → ②=1、③=2
④	Output Voltage Accuracy	1	±0.015V (V_{OUT}＜1.2V), ±0.020V (V_{OUT}≧1.2V)
⑤⑥–⑦(*1)	Packages (Order Unit)	ER-G	USP-6C (3,000pcs/Reel)
		MR-G	SOT-26W (3,000pcs/Reel)
		PR-G	SOT-89-5 (1,000pcs/Reel)
		0R-G	WLP-5-02 (3,000pcs/Reel)

(*1) The “-G” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

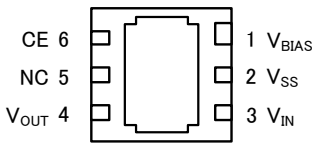
2) Selection Guide

TYPE	SOFT-START	CURRENT LIMITTER	THERMAL SHUTDOWN	UVLO	CE PULL-DOWN RESISTOR	C_L AUTO-DISCHARGE
A	Yes	Yes	Yes	Yes	Yes	Yes
B	No	Yes	Yes	Yes	Yes	Yes

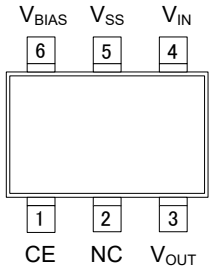
■PIN CONFIGURATION



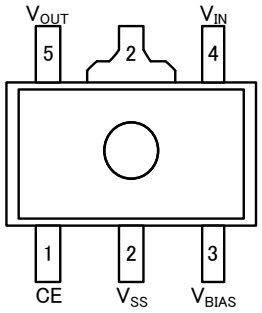
WLP-5-02
(BOTTOM VIEW)



USP-6C
(BOTTOM VIEW)



SOT-26W
(TOP VIEW)



SOT-89-5
(TOP VIEW)

*The dissipation pad for the USP-6C package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the V_{SS} (No. 2) pin.

■PIN ASSIGNMENT

PIN NUMBER				PIN NAME	FUNCTIONS
USP-6C	SOT-26W	SOT-89-5	WLP-5-02		
1	6	3	3	V_{BIAS}	Power Supply Input
2	5	2	5	V_{SS}	Ground
3	4	4	4	V_{IN}	Driver Transistor Input
4	3	5	1	V_{OUT}	Output
5	2	-	-	NC	No Connection
6	1	1	2	CE	ON/OFF Control

■FUNCTION CHART

XC6602 Series, Type A/B

PIN NAME	SIGNAL	STATUS
CE	L	Stand-by
	H	Active
	OPEN	Stand-by

■ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
Bias Voltage		V_{BIAS}	V_{SS} - 0.3 ~ V_{SS} + 6.5	V
Input Voltage		V_{IN}	V_{SS} - 0.3 ~ V_{SS} + 6.5	V
Output Voltage		V_{OUT}	V_{SS} - 0.3 ~ V_{BIAS} + 0.3 ≦ V_{SS} + 6.5	V
			V_{SS} - 0.3 ~ V_{IN} + 0.3 ≦ V_{SS} + 6.5	V
CE Input Voltage		V_{CE}	V_{SS} - 0.3 ~ V_{SS} + 6.5	V
Power Dissipation (Ta=25℃)	USP-6C	Pd	120	mW
			1000 (40mm x 40mm Standard board)(*1)	
			1250 (JESD51-7 board)(*1)	
	SOT-26W		250	
			600 (40mm x 40mm Standard board)(*1)	
			830 (JESD51-7 board)(*1)	
	SOT-89-5		500	
			1300 (40mm x 40mm Standard board)(*1)	
			1750 (JESD51-7 board)(*1)	
	WLP-5-02		750 (40mm x 40mm Standard board)(*1)	
Operating Ambient Temperature		Topr	-40 ~ 85	℃
Storage Temperature		Tstg	-55 ~ 125	℃

(*1) The power dissipation figure shown is PCB mounted and is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

■ELECTRICAL CHARACTERISTICS

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	CIRCUIT
Bias Voltage	V_{BIAS}			2.5	-	6.0	V	①
Input Voltage	V_{IN}			0.5	-	3.0	V	①
Output Voltage	$V_{OUT(E)}$(*2)	I_{OUT}=100mA	$V_{OUT(T)}$＜1.2V	-0.015	$V_{OUT(T)}$(*3)	+0.015	V	①
			$V_{OUT(T)}$≧1.2V	-0.020		+0.020		
Maximum Output Current(*4)	I_{OUTMAX}	$V_{OUT(T)}$≦1.2V, V_{BIAS}=V_{CE}=2.5V		1.0	-	-	A	①
		$V_{OUT(T)}$＞1.2V,V_{BIAS}=V_{CE}=$V_{OUT(T)}$+1.3V						
Load Regulation (WLP-5-02)	ΔV_{OUT}	1mA≦I_{OUT}≦1A		-	13	26	mV	①
Load Regulation (USP-6C,SOT-26W,SOT-89-5)	ΔV_{OUT}	1mA≦I_{OUT}≦1A		-	37	68	mV	①
Dropout Voltage	Vdif (*5)	I_{OUT}=1A		-	E-1(*8)		mV	①
Supply Current 1(*9)	I_{BIAS}	I_{OUT}=0A		76	100	143	μA	②
Supply Current 2	I_{IN}	I_{OUT}=0A	$V_{OUT(T)}$＜1.2V	0.1	-	8.7	μA	②
			$V_{OUT(T)}$≧1.2V	3.9	-	14.2		
Stand-by Current 1	I_{BIAS_STB}	V_{BIAS}=6.0V,V_{IN}=3.0V,V_{CE}=V_{SS}		-	0.01	0.10	μA	②
Stand-by Current 2	I_{IN_STB}	V_{BIAS}=6.0V,V_{IN}=3.0V,V_{CE}=V_{SS}		-	0.01	0.15	μA	②
Bias Line Regulation	ΔV_{OUT}/ (ΔV_{BIAS}・V_{OUT})	$V_{OUT(T)}$≦1.2V,V_{CE}=V_{BIAS} 2.5V≦V_{BIAS}≦6.0V		-	0.01	0.10	%/V	①
		$V_{OUT(T)}$＞1.2V,V_{CE}=V_{BIAS} $V_{OUT(T)}$+1.3V≦V_{BIAS}≦6.0V						
Input Line Regulation	ΔV_{OUT}/ (ΔV_{IN}・V_{OUT})	$V_{OUT(T)}$+0.1V≦V_{IN}≦3.0V		-	0.01	0.10	%/V	①
Bias UVLO Voltage	V_{BIAS_UVLOD}			V_{SS}	-	1.28	V	①
Bias UVLO Release Voltage	V_{BIAS_UVLOR}			2.5	-	6.0	V	①
Input UVLO Voltage	V_{IN_UVLOD}			V_{SS}	-	0.23	V	①
Input UVLO Release Voltage	V_{IN_UVLOR}			0.5	-	3.0	V	①
Output Voltage Temperature Characteristics	ΔV_{OUT}/ (ΔTopr・V_{OUT})	I_{OUT}=100mA -40℃≦Topr≦85℃		-	±30	-	ppm/℃	①
Bias Ripple Rejection Ratio	V_{BIAS_PSRR}	V_{BIAS}=V_{CE}=3.6V_{DC}+0.2V_{p-pAC} I_{OUT}=100mA,f=1kHz,C_{BIAS}=OPEN		-	60	-	dB	③
Input Ripple Rejection Ratio	V_{IN_PSRR}	V_{IN}=$V_{OUT(T)}$+0.3V_{DC}+0.2V_{p-pAC} I_{OUT}=100mA,f=1kHz,C_{IN}=OPEN		-	75	-	dB	③
Limit Current(*4)	I_{LIM}	V_{OUT}=$V_{OUT(E)}$×0.95		1.0	1.3	-	A	①
Short Current	I_{SHORT}	V_{OUT}=V_{SS}		-	90	-	mA	①
Thermal Shutdown Detect Temperature	T_{TSD}	Junction Temperature		-	150	-	℃	①
Thermal Shutdown Release Temperature	T_{TSR}	Junction Temperature		-	125	-	℃	①
Thermal Shutdown Hysteresis Width	T_{TSD} - T_{TSR}	Junction Temperature		-	25	-	℃	①
C_LAuto-Discharge Resistance	R_{DCHG}	V_{CE}=V_{SS},V_{OUT}=$V_{OUT(T)}$		130	190	255	Ω	①
CE "H" Level Voltage	V_{CEH}			0.65	-	6.00	V	④
CE "L" Level Voltage	V_{CEL}			V_{SS}	-	0.41	V	④
CE "H" Level Current	I_{CEH}	V_{BIAS}=V_{CE}=6.0V		3.2	6.0	10.6	μA	④
CE "L" Level Current	I_{CEL}	V_{BIAS}=6.0V,V_{CE}=V_{SS}		-0.1	-	0.1	μA	④
Soft-Start Time (Type A) (*10)	t_{SS}	V_{CE}=0V→3.6V,tr=5μs		225	430	600	μs	⑤
Output Rise Time (Type B) (*10)	t_{ON}	V_{CE}=0V→3.6V,tr=5μs		-	-	110	μs	⑤
Inrush Current (Type A)	I_{RUSH}	C_L=2.2μF	$V_{OUT(T)}$≦1.2V	-	-	70	mA	⑤
			$V_{OUT(T)}$＞1.2V	-	-	85	mA	⑤
		C_L=10μF	$V_{OUT(T)}$≦1.2V	-	-	155	mA	⑤
			$V_{OUT(T)}$＞1.2V	-	-	215	mA	⑤

* 1: Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}=C_{IN}=1.0μF, C_L=2.2μF
* 2: $V_{OUT(E)}$ = Effective output voltage
* 3: $V_{OUT(T)}$ = Nominal output voltage
* 4: Mount conditions affect heat dissipation. Maximum output current is not guaranteed when TSD starts to operate earlier.
* 5: Vdif = {V_{IN1}(*6)-V_{OUT1}(*7)}.
* 6: V_{IN1} is an input voltage when V_{OUT1} appears at the output during decreasing input voltage gradually.
* 7: V_{OUT1} is a voltage equal to 98% of the output voltage where V_{BIAS}=V_{CE}=3.6 and V_{IN}=$V_{OUT(T)}$+0.3V at I_{OUT}=1A is input to the V_{IN} pin.
* 8: Please refer to the table E-1 named DROPOUT VOLTAGE CHART
* 9: Supply current 1 may be fluctuated because that some bias current flows into the output.
* 10: A time between the CE input goes over the CE H threshold and the output reaches $V_{OUT(E)}$x0.9V.

■ELECTRICAL CHARACTERISTICS (Continued)

●OUTPUT VOLTAGE CHART (WLP-5-02)

NOMINAL OUTPUT VOLTAGE	E-1														
	DROPOUT VOLTAGE (mV)														
	V_{BIAS}=3.0V			V_{BIAS}=3.3V			V_{BIAS}=3.6V			V_{BIAS}=4.2V			V_{BIAS}=5.0V		
	V_{GS}	Vdif(mV)		V_{GS}	Vdif(mV)		V_{GS}	Vdif(mV)		V_{GS}	Vdif(mV)		V_{GS}	Vdif(mV)	
$V_{OUT(T)}$	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.
0.5	2.5	79	134	2.8	76	129	3.1	76	129	3.7	73	124	4.5	72	122
0.6	2.4	82	139	2.7			3.0			3.6			4.4		
0.7	2.3			2.6			2.9			3.5			4.3		
0.8	2.2	85	144	2.5	79	134	2.8			3.4			4.2		
0.9	2.1	88	149	2.4	82	139	2.7			3.3			4.1		
1.0	2.0	91	154	2.3			2.6			3.2	76	129	4.0		
1.1	1.9	94	159	2.2	85	144	2.5	79	134	3.1			3.9		
1.2	1.8	100	169	2.1	88	149	2.4	82	139	3.0			3.8	73	124
1.3	1.7	109	184	1.9	91	154	2.3			2.9			3.7		
1.4	1.6	118	199	1.9	94	159	2.2	85	144	2.8			3.6		
1.5	1.5	130	219	1.8	100	169	2.1	88	149	2.7			3.5		
1.6	1.4	144	244	1.7	109	184	2.0	91	154	2.6			3.4		
1.7	1.3	171	289	1.6	118	199	1.9	94	159	2.5	79	134	3.3		
1.8	1.2	201	339	1.5	130	219	1.8	100	169	2.4	82	139	3.2	76	129

* Dropout voltage is defined as the V_{GS}(=V_{BIAS}–$V_{OUT(E)}$) of the driver transistor.

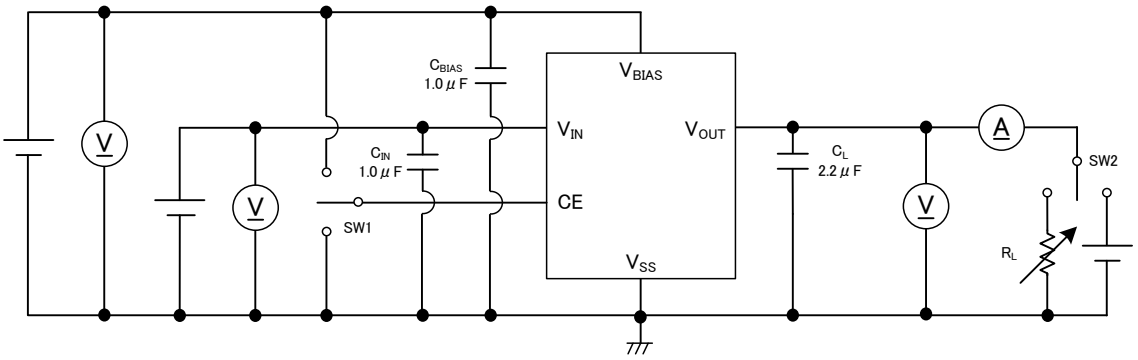
●OUTPUT VOLTAGE CHART (USP-6C,SOT-26W,SOT-89-5)

NOMINAL OUTPUT VOLTAGE	E-1														
	DROPOUT VOLTAGE (mV)														
	V_{BIAS}=3.0V			V_{BIAS}=3.3V			V_{BIAS}=3.6V			V_{BIAS}=4.2V			V_{BIAS}=5.0V		
	V_{GS}	Vdif (mV)		V_{GS}	Vdif (mV)		V_{GS}	Vdif (mV)		V_{GS}	Vdif (mV)		V_{GS}	Vdif (mV)	
$V_{OUT(T)}$	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.	(V)	TYP.	MAX.
0.5	2.5	152	218	2.8	146	213	3.1	146	213	3.7	140	208	4.5	137	206
0.6	2.4	155	223	2.7			3.0			3.6			4.4		
0.7	2.3			2.6			2.9			3.5			4.3		
0.8	2.2	158	228	2.5	152	218	2.8			3.4			4.2		
0.9	2.1	162	233	2.4	155	223	2.7			3.3			4.1		
1.0	2.0	165	238	2.3			2.6			3.2	146	213	4.0		
1.1	1.9	167	243	2.2	158	228	2.5	152	218	3.1			3.9		
1.2	1.8	169	253	2.1	162	233	2.4	155	223	3.0			3.8	140	208
1.3	1.7	179	268	2.0	165	238	2.3			2.9			3.7		
1.4	1.6	189	283	1.9	167	243	2.2	158	228	2.8			3.6		
1.5	1.5	202	303	1.8	169	253	2.1	162	233	2.7			3.5		
1.6	1.4	213	328	1.7	179	268	2.0	165	238	2.6			3.4		
1.7	1.3	225	373	1.6	189	283	1.9	167	243	2.5	152	218	3.3		
1.8	1.2	255	423	1.5	202	303	1.8	169	253	2.4	155	223	3.2	146	213

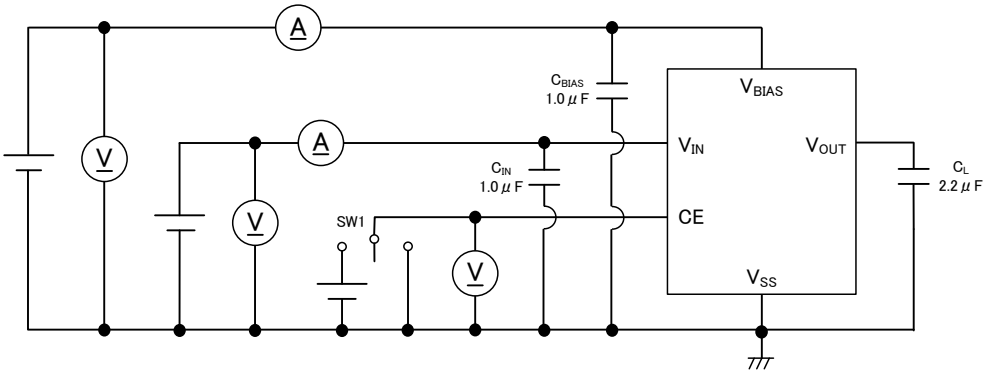
* Dropout voltage is defined as the V_{GS}(=V_{BIAS}–$V_{OUT(E)}$) of the driver transistor.

■TEST CIRCUITS

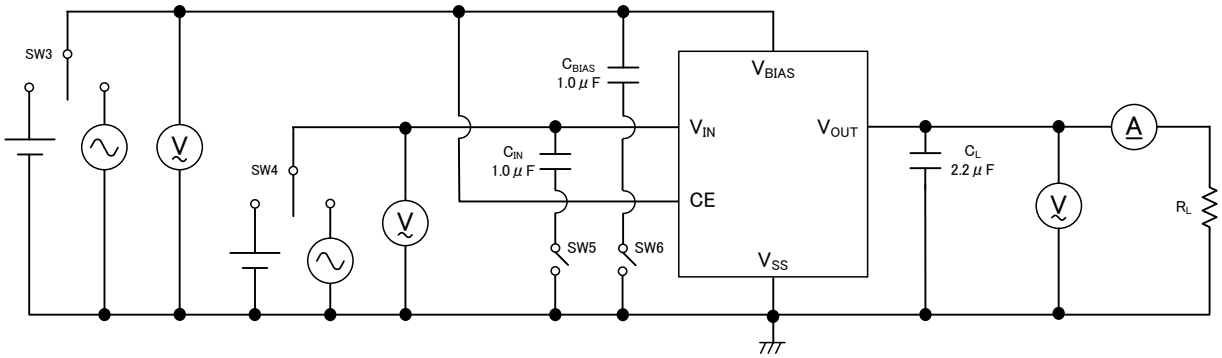
●Circuit ①



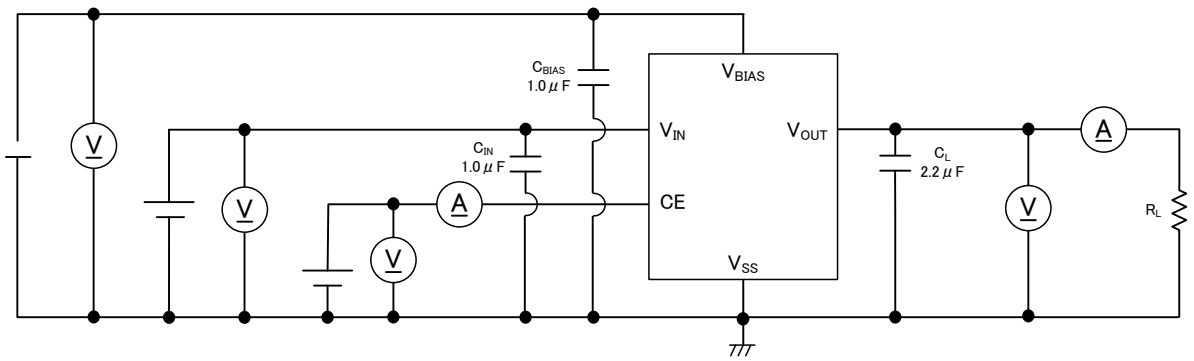
●Circuit ②



●Circuit ③

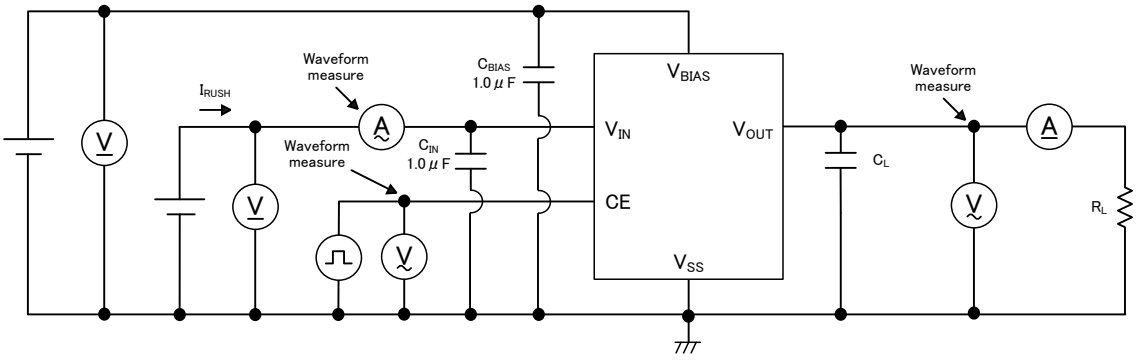


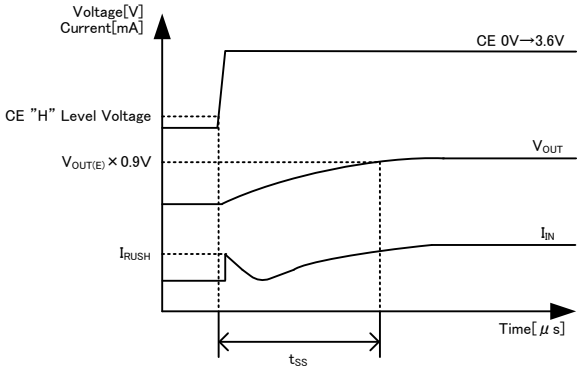
●Circuit ④



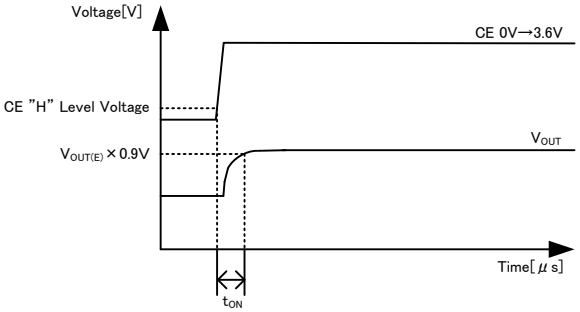
■TEST CIRCUITS (Continued)

●Circuit ⑤ (Timing Chart)





XC6602 Series, Type A



XC6602 Series, Type B

■OPERATIONAL EXPLANATION

The voltage divided by resistors R1 and R2 is compared with the internal reference voltage by the error amplifier. The V_{OUT} pin is then driven by the subsequent output signal. The output voltage at the V_{OUT} pin is controlled and stabilized by a system of negative feedback.

V_{BIAS} pin is power supply pin for output voltage control circuit, protection circuit and CE circuit. Also, the V_{BIAS} pin supplies some current as output current. V_{IN} pin is connected to a driver transistor and provides output current.

In order to obtain high efficient output current through low on-resistance, please take enough V_{GS} (=V_{BIAS} – $V_{OUT(E)}$) of the driver transistor.

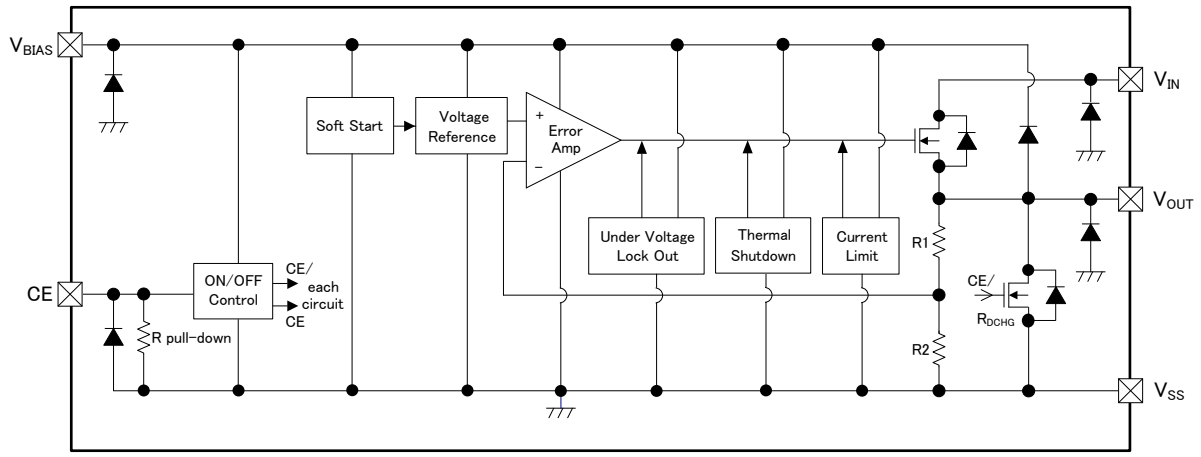


Figure1: XC6602 Series, Type A

<Soft-Start Function>

With the XC6602 (Type A), the inrush current (I_{RUSH}) from V_{IN} to V_{OUT} for charging C_L at start-up can be reduced and makes the V_{IN} stable.

As for the XC6602, the soft-start time in the type A is optimized internally. On the other hand, the type B of the XC6602 does not have the soft-start time function.

<Current Limiter, Short-Circuit Protection>

The XC6602 series includes a combination of a fixed current limiter circuit and a foldback short-circuit protection. When the output current reaches the current limit, the output voltage drops and this operation makes the output current foldback to be decreased.

<Thermal Shutdown Circuit (TSD) >

When the junction temperature of the built-in driver transistor reaches the temperature limit, the thermal shutdown circuit operates and the driver transistor will be set to OFF. The IC resumes its operation when the thermal shutdown function is released and the IC's operation is automatically restored because the junction temperature drops to the level of the thermal shutdown release temperature.

<Under Voltage Lock Out (UVLO) >

When the V_{BIAS} pin and V_{IN} pin voltage drops, the output driver transistor is set to OFF by UVLO function to prevent false output caused by unstable operation of the internal circuitry. When the V_{BIAS} pin voltage and the V_{IN} pin voltage rises at release voltage, the UVLO function is released. The driver transistor is turned ON and start to operate voltage regulation.

■OPERATIONAL EXPLANATION (Continued)

<CE Pin>

The XC6602 internal circuitry can be shutdown via the signal to the CE pin. In shutdown mode with CE low level voltage, the V_{OUT} pin will be pulled down to the V_{SS} level via C_L discharge resistance (R_{DCHG}) placed in parallel to R1 and R2.

The CE pin has pull-down circuitry so that CE input current flows during IC operation. If the CE pin voltage is taken from V_{BIAS} pin or V_{SS} pin then logic is fixed and the IC will operate normally. However, supply current may increase as a result of through current in the IC's internal circuitry when medium voltage is input.

<CL High Speed Auto-Discharge>

XC6602 series can quickly discharge the electric charge at the output capacitor (C_L) via the internal transistor located between the V_{OUT} pin and the V_{SS} pin when a low signal to the CE pin which enables a whole IC circuit put into OFF state. When the IC is disabled, electric charge at the output capacitor (C_L) is quickly discharged so that it could avoids malfunction. Discharge time of the output capacitor (C_L) is set by the C_L auto-discharge resistance (R_{DCHG}) and the output capacitor (C_L). By setting time constant of a C_L auto-discharge resistance value (R_{DCHG}) and an output capacitor value (C_L) as τ ($\tau = C_L \times R_{DCHG}$), the output voltage after discharge via the internal transistor is calculated by the following formula. Please also note R_{DCHG} is depended on V_{BIAS}. When V_{BIAS} is larger, R_{DCHG} is smaller.

$$V = V_{OUT(E)} \times e^{-t/\tau} \quad or \quad t = \tau \ln (V_{OUT(E)} / V)$$

(V: Output voltage after discharge, $V_{OUT(E)}$: Initial Output voltage, t: Discharge time,
τ : C_L auto-discharge resistance $R_{DCHG} \times C_L$ Output capacitance

<Low ESR Capacitor>

With the XC6602 series, a stable output voltage is achievable even if used with low ESR capacitors, as a phase compensation circuit is built-in. The output capacitor (C_L) should be connected as close to V_{OUT} pin and V_{SS} pin to obtain stable phase compensation. Values required for the phase compensation are as the table below.

For a stable power input, please connect an bias capacitor (C_{BIAS}) between the V_{BIAS} pin and the V_{SS} pin. Also, please connect an input capacitor (C_{IN}) between the V_{IN} pin and the V_{SS} pin. In order to ensure the stable phase compensation while avoiding run-out of values, please use the capacitor (C_{BIAS}, C_{IN}, C_L) which does not depend on bias or temperature too much. The table below shows recommended values of C_{BIAS}, C_{IN}, C_L.

CHART 1 : Recommended Values of C_{BIAS}, C_{IN}, C_L (MIN.)

OUTPUT VOLTAGE RANGE $V_{OUT(T)}$	BIAS CAPACITOR C_{BIAS}	INPUT CAPACITOR C_{IN}	OUTPUT CAPACITOR C_L
0.5V ~ 1.8V	1.0μF	1.0μF	2.2μF

■NOTES ON USE

1. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please keep the resistance low for the V_{BIAS}, V_{IN} and V_{SS} wiring in particular.

3. Please wire the C_{BIAS}, C_{IN} and C_L as close to the IC as possible.

4. Capacitances of these capacitors (C_{BIAS}, C_{IN}, C_L) are decreased by the influences of bias voltage and ambient temperature. Care shall be taken for capacitor selection to ensure stability of phase compensation from the point of ESR influence.

5. When it is used in a quite small input / output dropout voltage, output may go into unstable operation. Please test it thoroughly before using it in production.

6. Torex places an importance on improving our products and their reliability.
   We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems

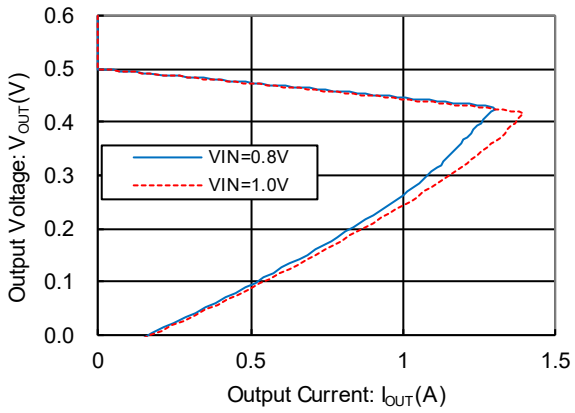
7. Note on mounting (WLP-5-02)
   (1) Mount pad design should be optimized for user's conditions.
   (2) Sn-AG-Cu is used for the package terminals. If eutectic solder is used, mounting reliability is decreased. Please do not use eutectic solder paste.
   (3) When underfill agent is used to increase interfacial bonding strength, please take enough evaluation for selection. Some underfill materials and applied conditions may decrease bonding reliability.
   (4) The IC has exposed surface of silicon material in the top marking face and sides so that it is weak against mechanical damages. Please take care of handling to avoid cracks and breaks.
   (5) The IC has exposed surface of silicon material in the top marking face and sides. Please use the IC with keeping the circuit open (avoiding short-circuit from the out).
   (6) Semi-transparent resin is coated on the circuit face of the package. Please be noted that the usage under strong lights may affects device performance.

■ TYPICAL PERFORMANCE CHARACTERISTICS

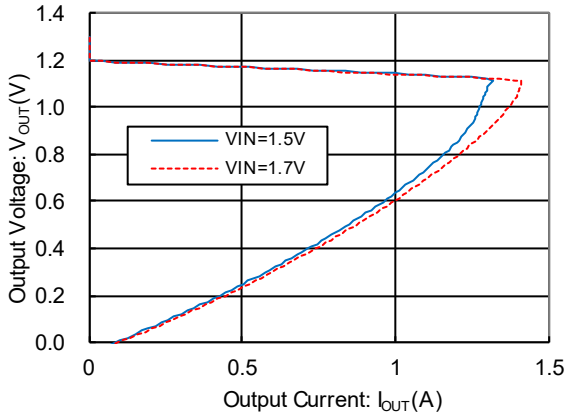
* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(1) Output Voltage vs. Output Current

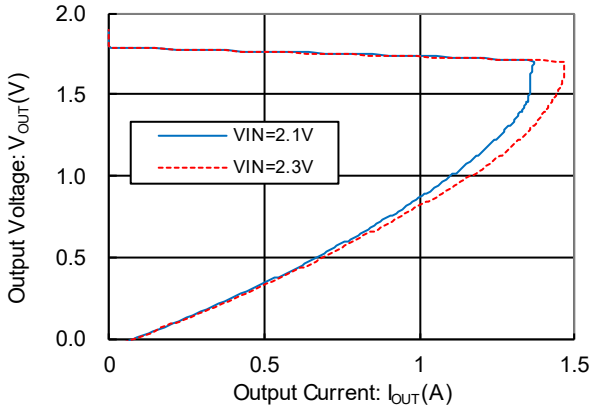
XC6602x051MR-G



XC6602x121MR-G

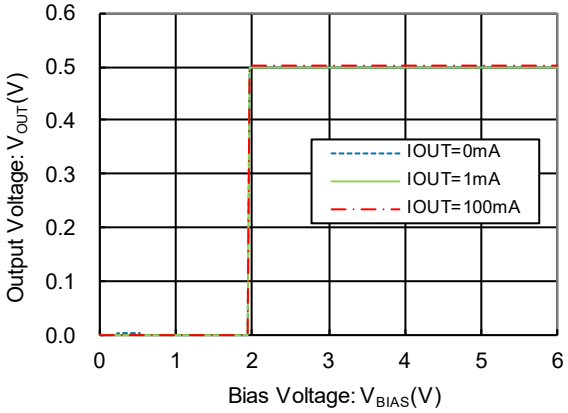


XC6602x181MR-G

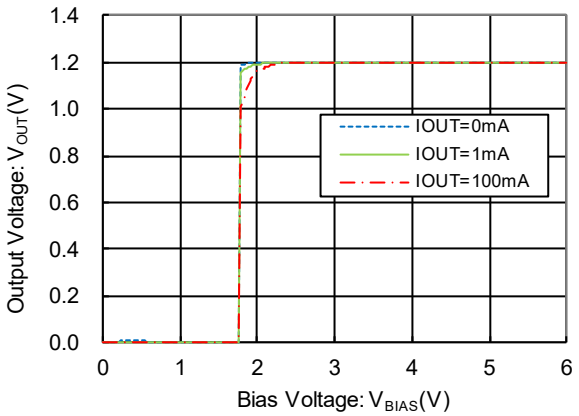


(2) Output Voltage vs. Bias Voltage

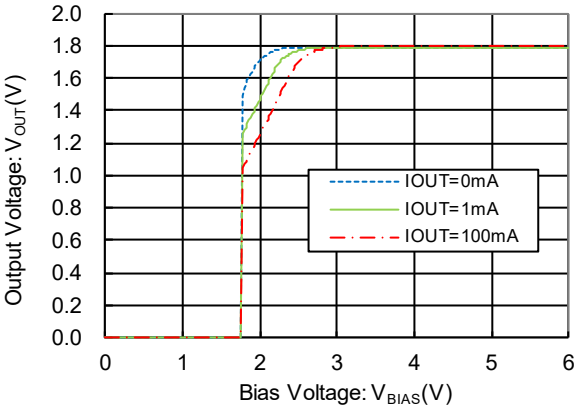
XC6602x051xR-G



XC6602x121xR-G



XC6602x181xR-G



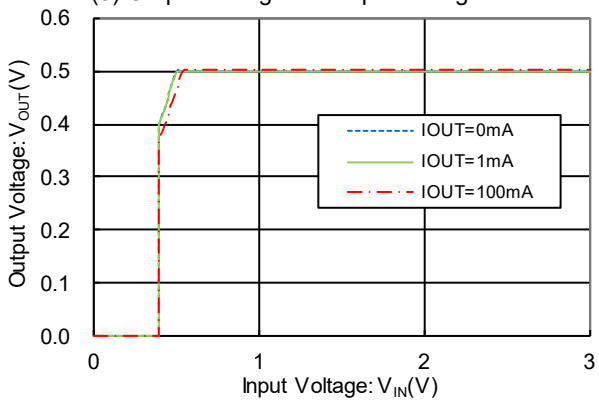
* Mount conditions affect heat dissipation. Thermal shutdown may start to operate before reaching the current limit.

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

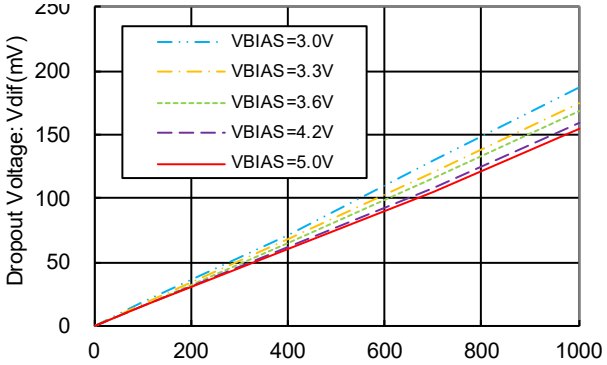
XC6602x051xR-G

(3) Output Voltage zvs. Input Voltage

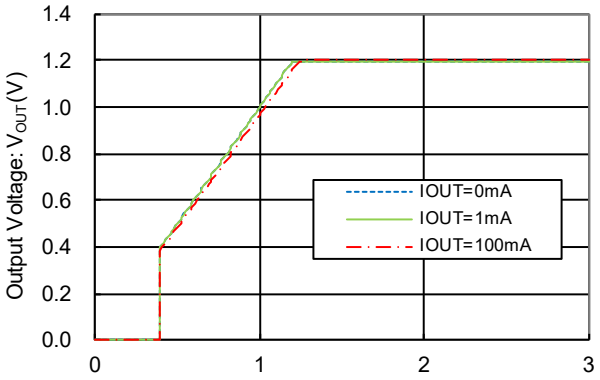


XC6602x121MR-G

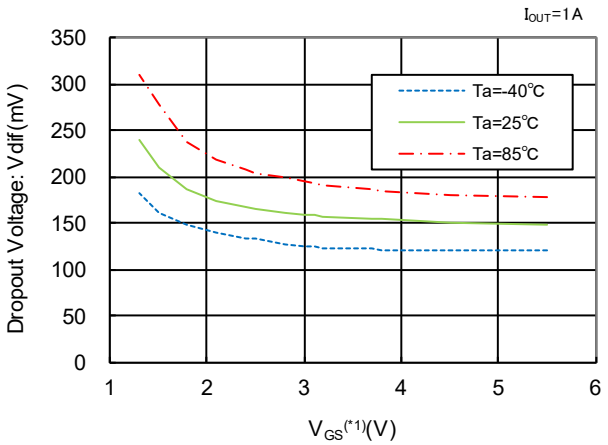
(4) Dropout Voltage vs. Output Current



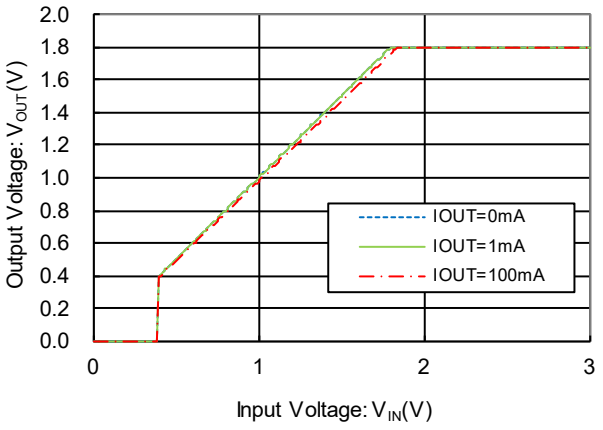
XC6602x121xR-G



XC6602xxx1MR-G



XC6602x181xR-G



(*1) V_{GS} is a Gate –Source voltage of the driver transistor that is defined as the value of V_{BIAS} - $V_{OUT(E)}$.
A value of the dropout voltage is determined by the value of the V_{GS}.

■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

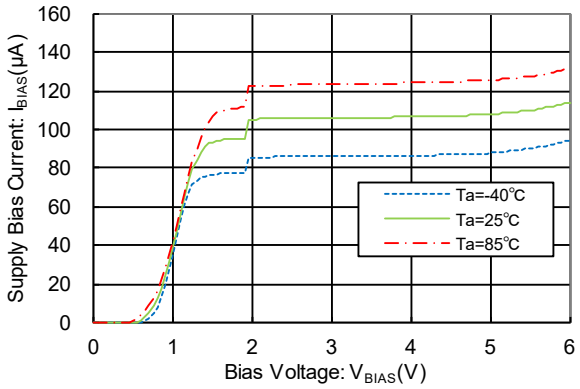
* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(5) Supply Bias Current vs. Bias Voltage

(6) Supply Input Current vs. Input Voltage

XC6602x051xR-G

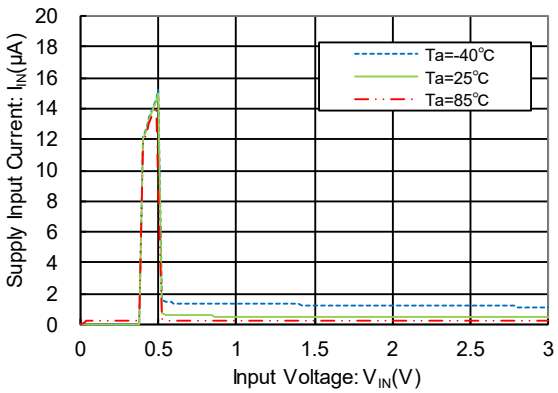
C_{IN}=C_{BIAS}=C_L=OPEN



XC6602x051xR-G

C_{IN}=C_{BIAS}=C_L=OPEN

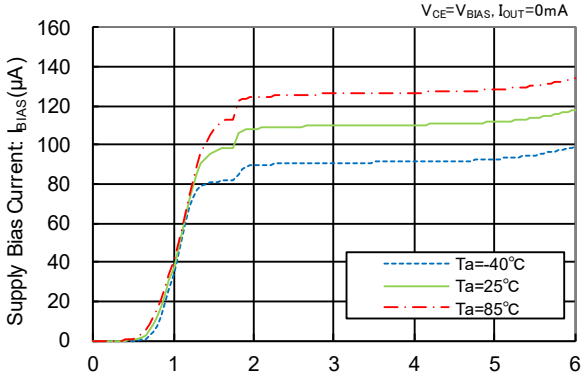
I_{OUT}=0mA



XC6602x121xR-G

C_{IN}=C_{BIAS}=C_L=OPEN

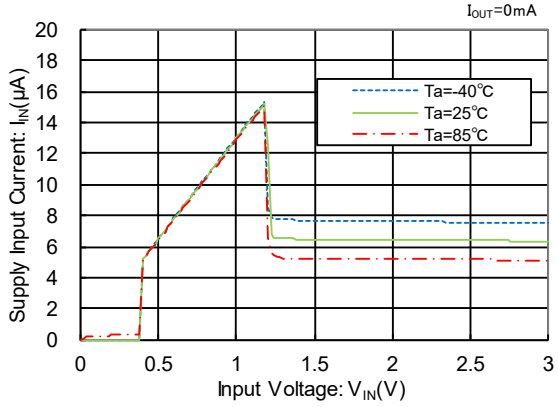
V_{CE}=V_{BIAS}, I_{OUT}=0mA



XC6602x121xR-G

C_{IN}=C_{BIAS}=C_L=OPEN

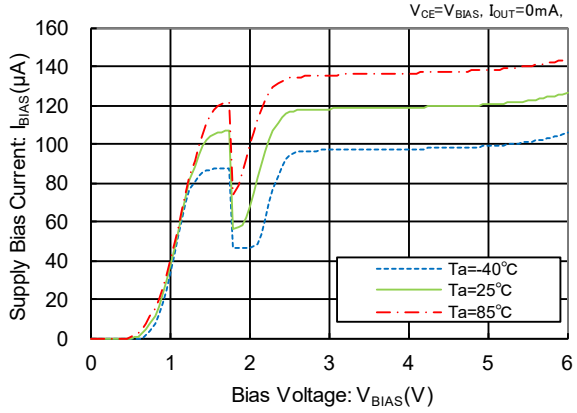
I_{OUT}=0mA



XC6602x181xR-G

C_{IN}=C_{BIAS}=C_L=OPEN

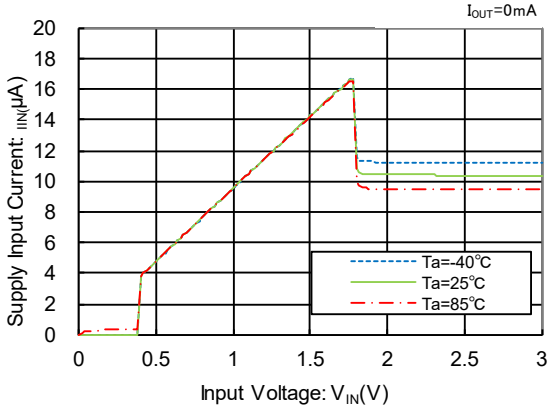
V_{CE}=V_{BIAS}, I_{OUT}=0mA,



XC6602x181xR-G

C_{IN}=C_{BIAS}=C_L=OPEN

I_{OUT}=0mA

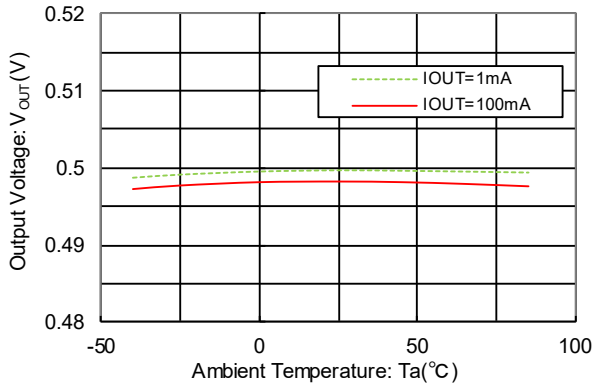


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

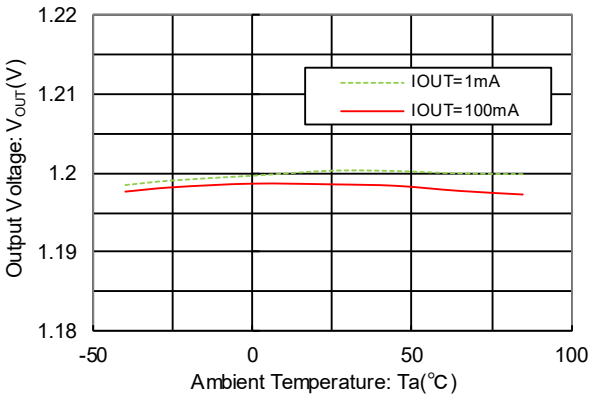
* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(7) Output Voltage vs. Ambient Temperature

XC6602x051xR-G



XC6602x121xR-G



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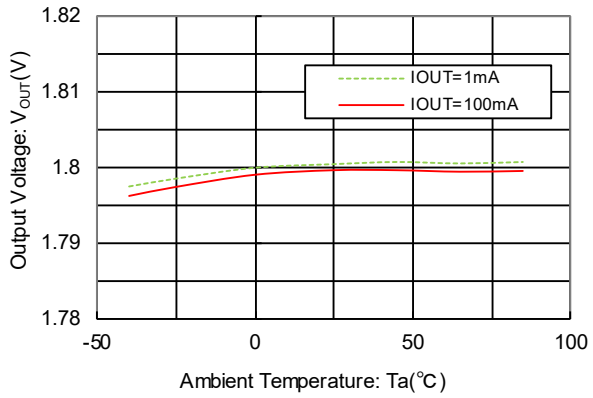
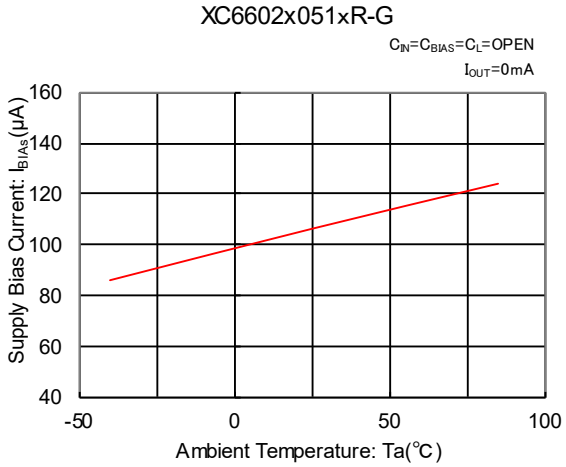
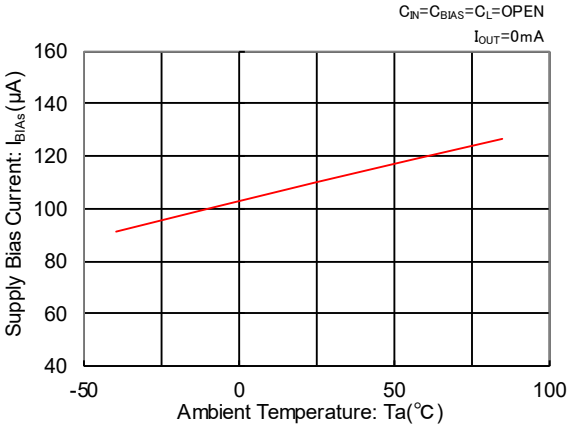


(8) Supply Bias Current vs. Ambient Temperature

XC6602x051xR-G



XC6602x121xR-G



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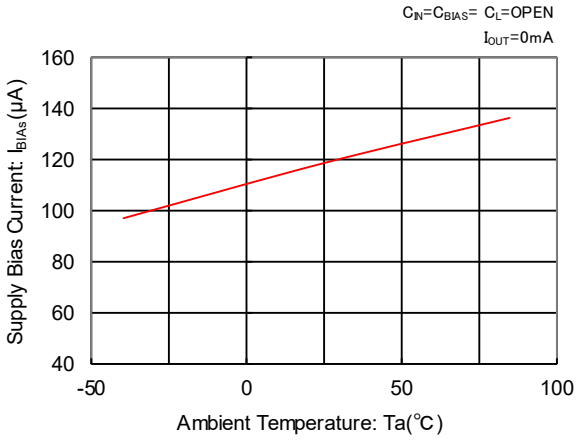
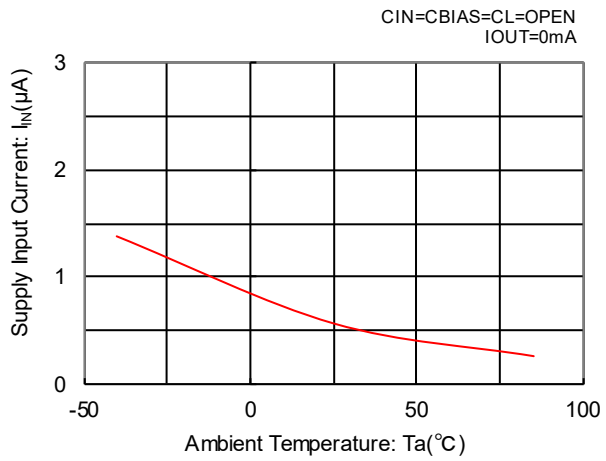


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

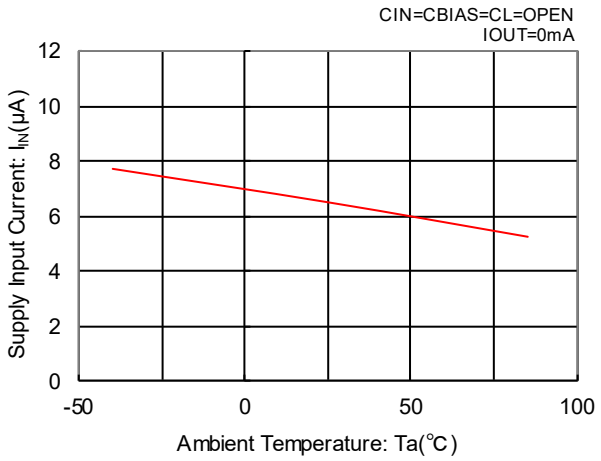
* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(9) Supply Input Current vs. Ambient Temperature

XC6602x051xR-G



XC6602x121xR-G



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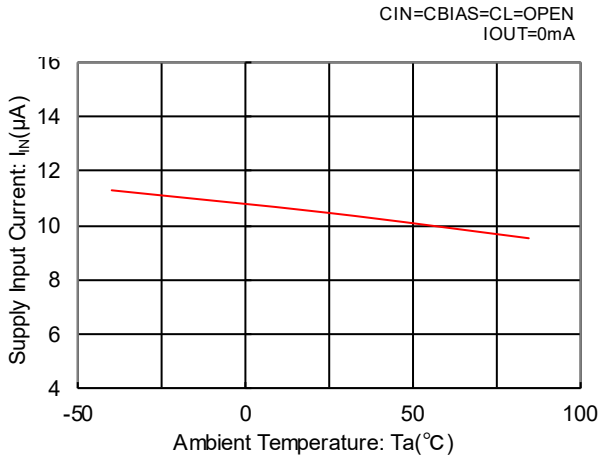
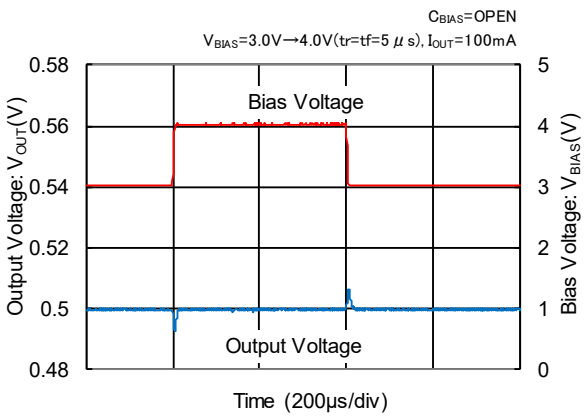


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

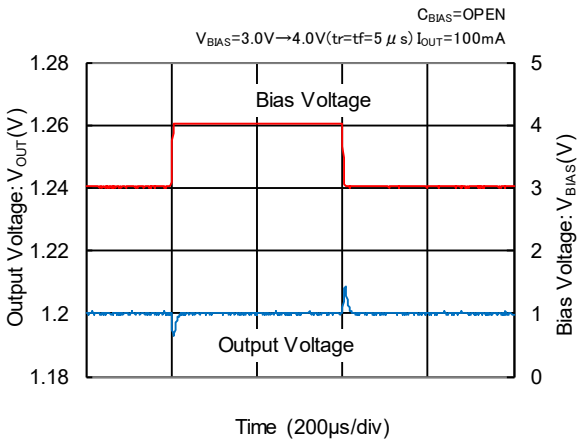
* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(10) Bias Transient Response

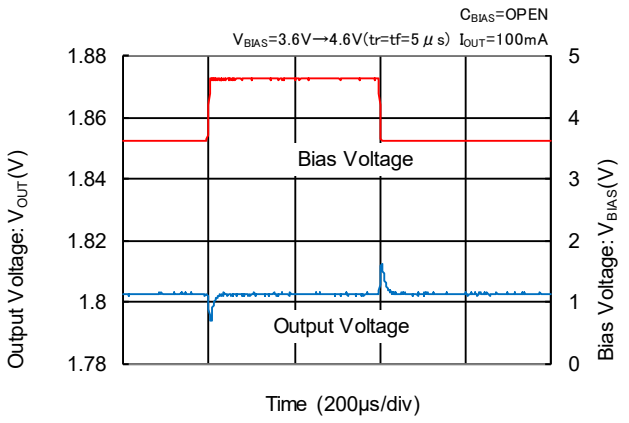
XC6602x051xR-G



XC6602x121xR-G

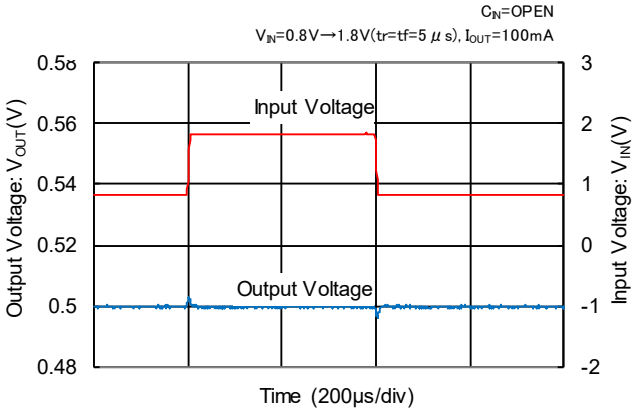


XC6602x181xR-G

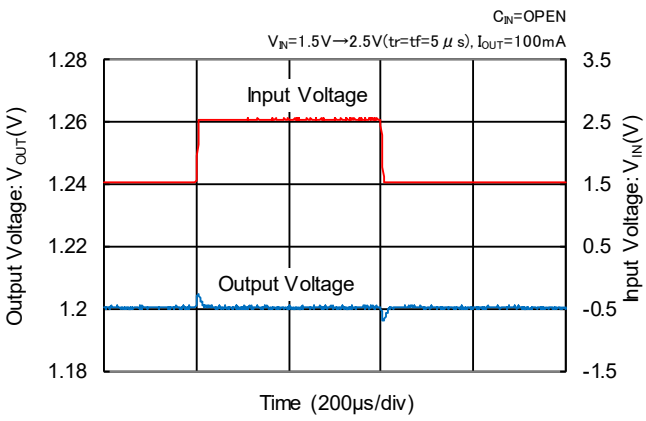


(11) Input Transient Response

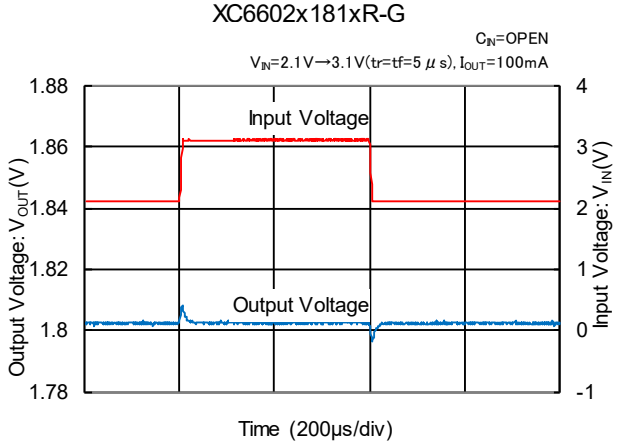
XC6602x051xR-G



XC6602x121xR-G



XC6602x181xR-G

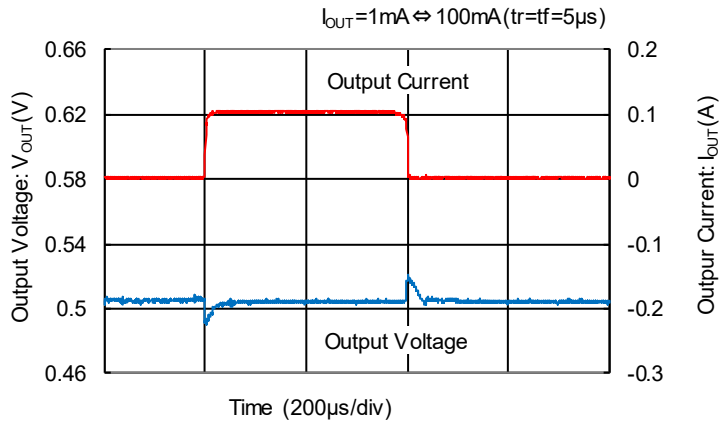


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(12) Load Transient Response

XC6602x051xR-G



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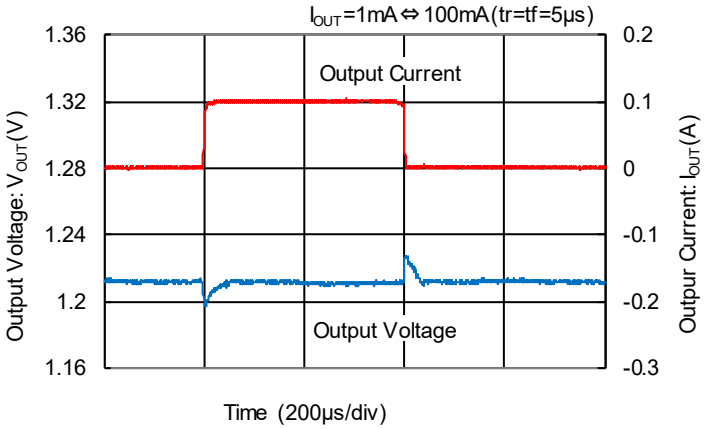

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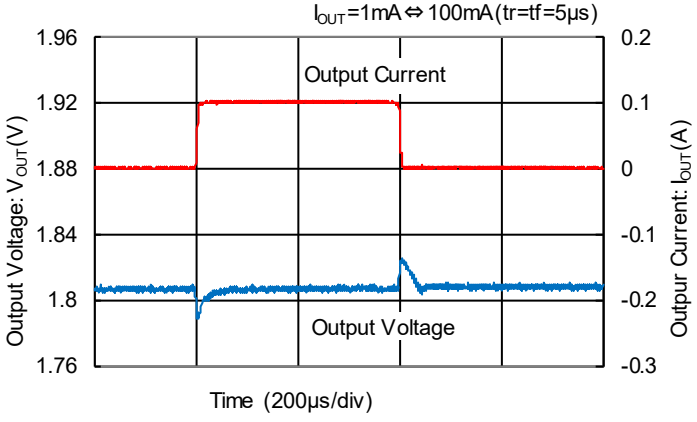
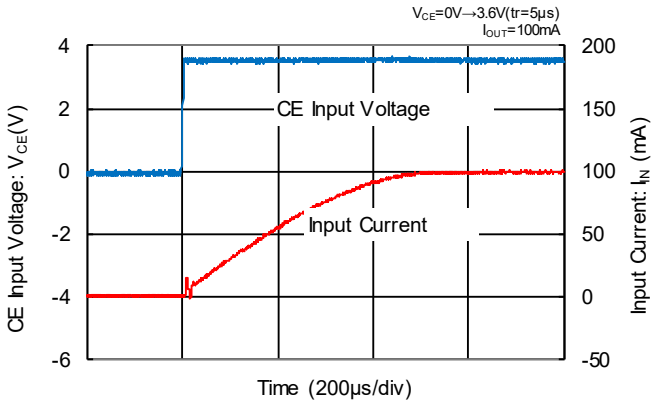


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(13) CE Input Voltage Response

XC6602A051xR-G



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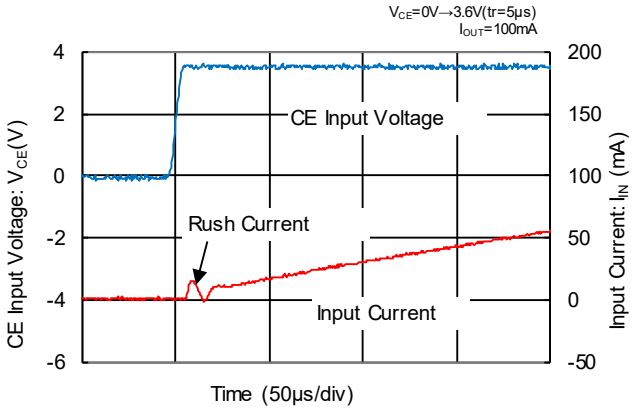

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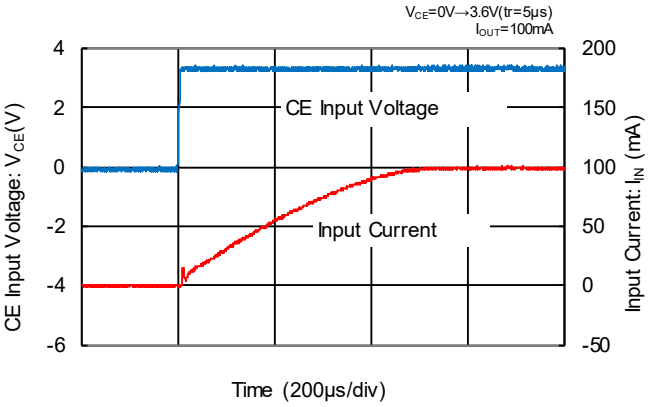

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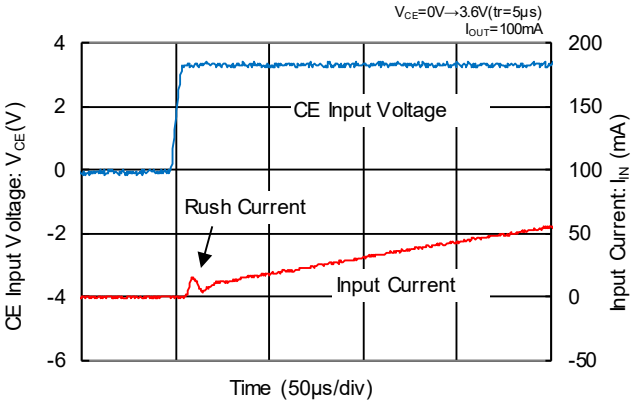

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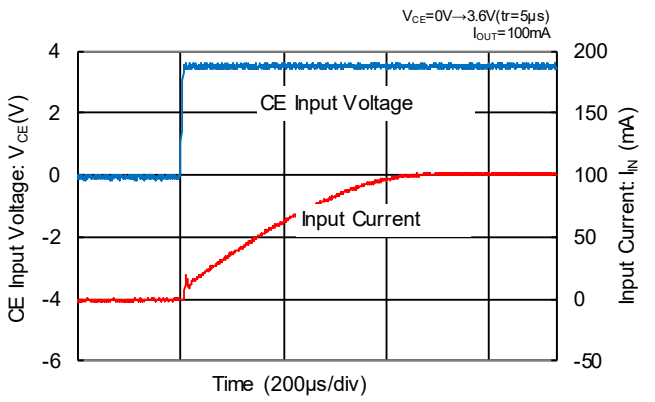

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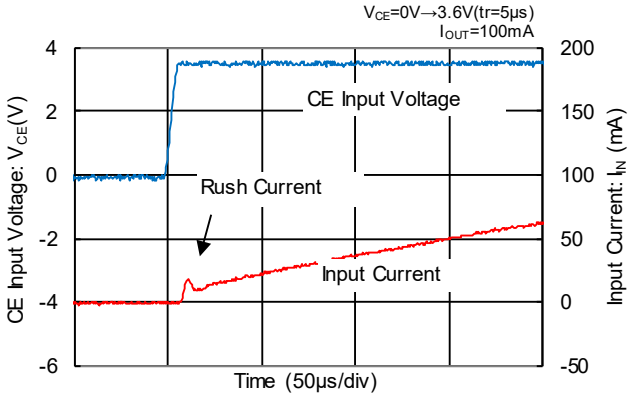
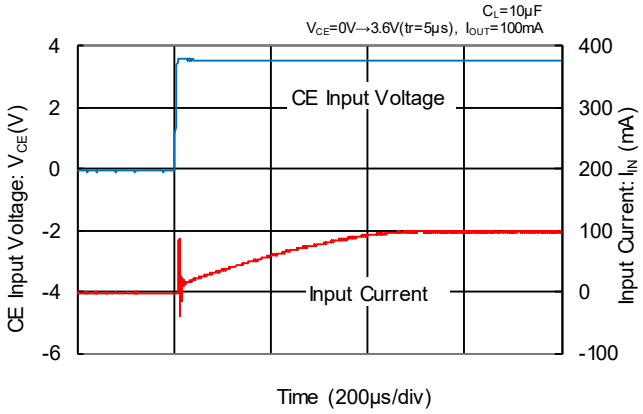


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(13)CE Input Voltage Response (Continued)

XC6602A051xR-G



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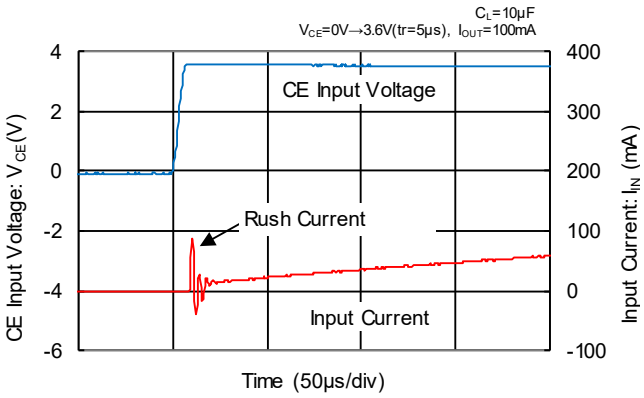

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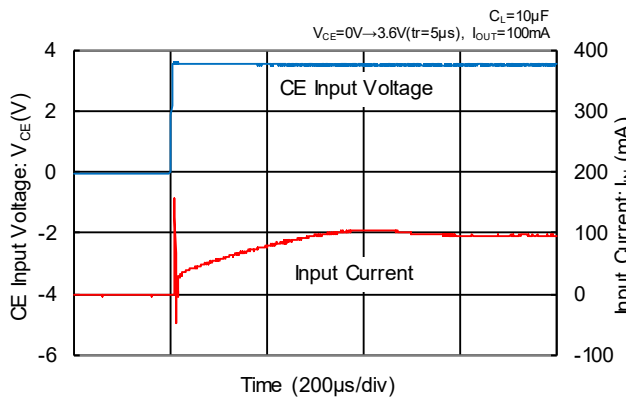

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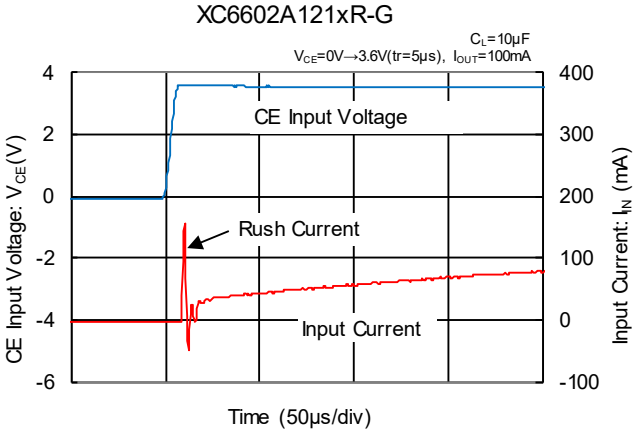

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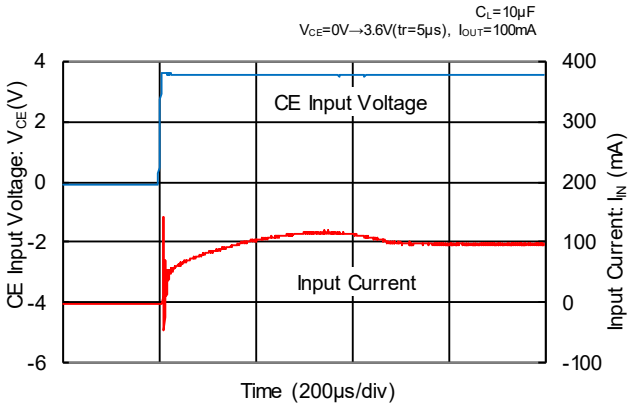

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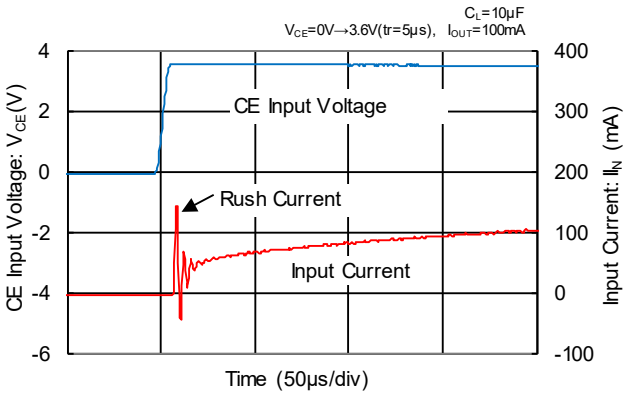
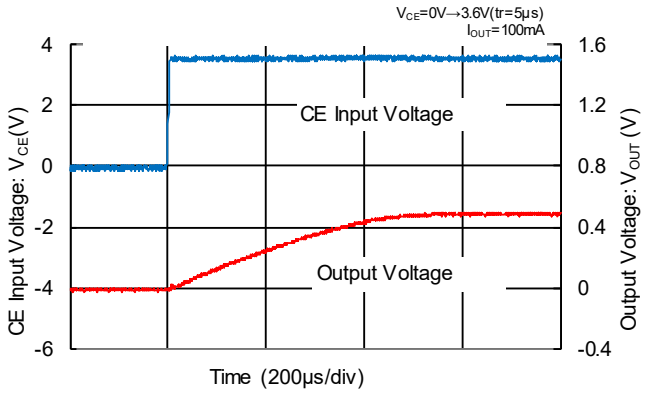


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(14) CE Rising Response Time

XC6602A051xR-G



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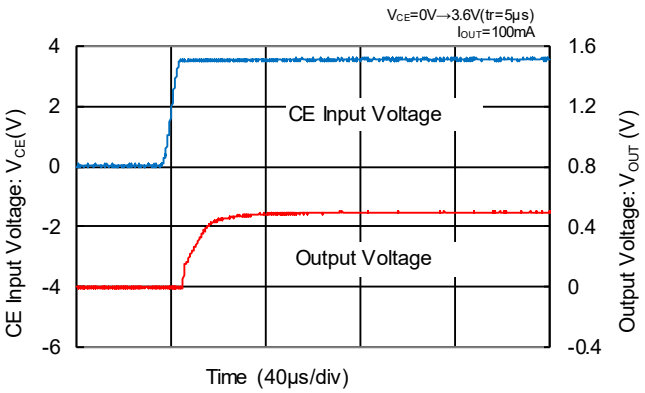
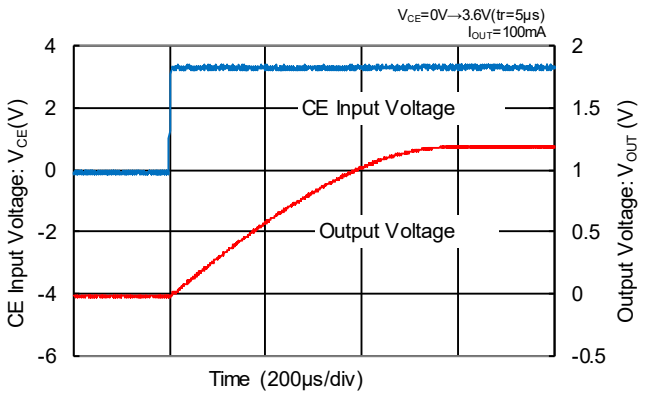


XC6602A121xR-G



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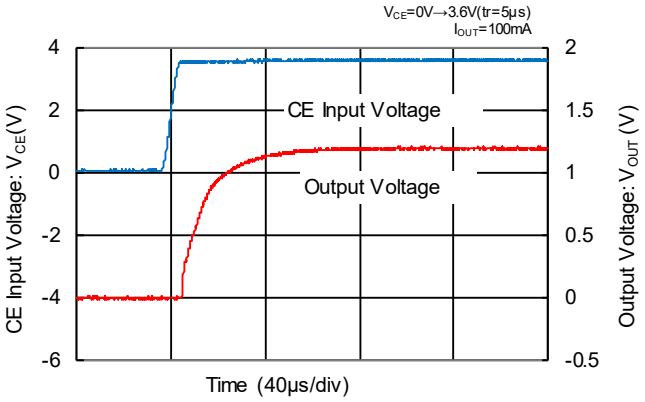

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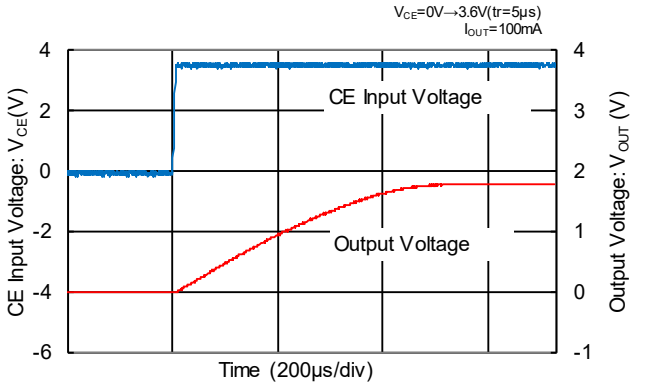

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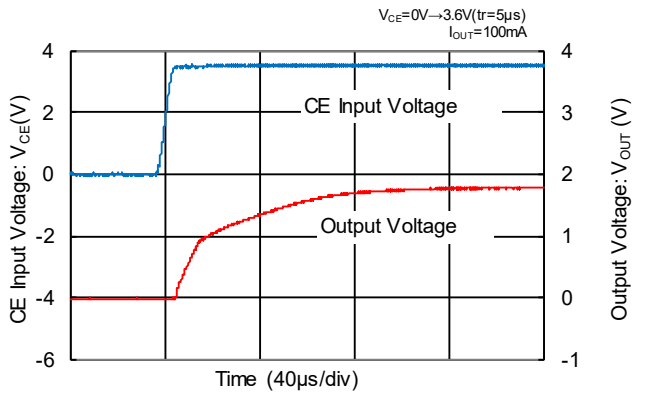
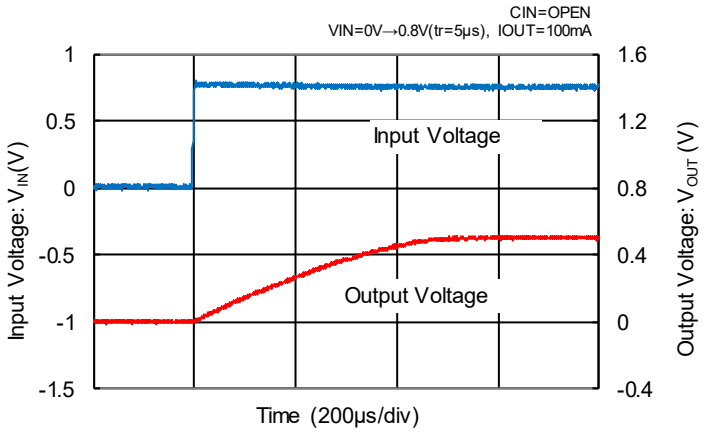


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

(15) V_{IN} Rising Response Time

XC6602A051xR-G



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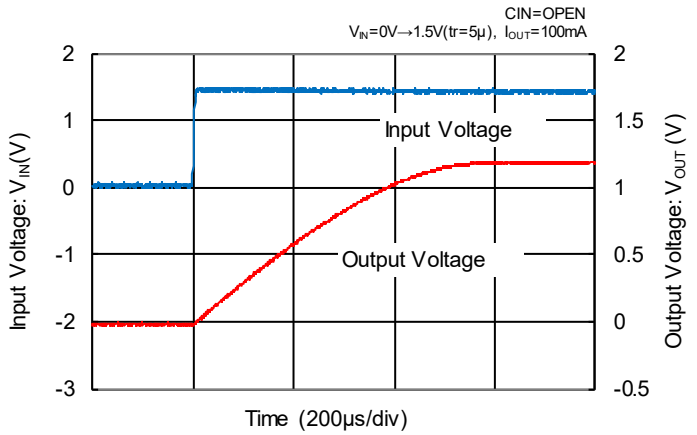

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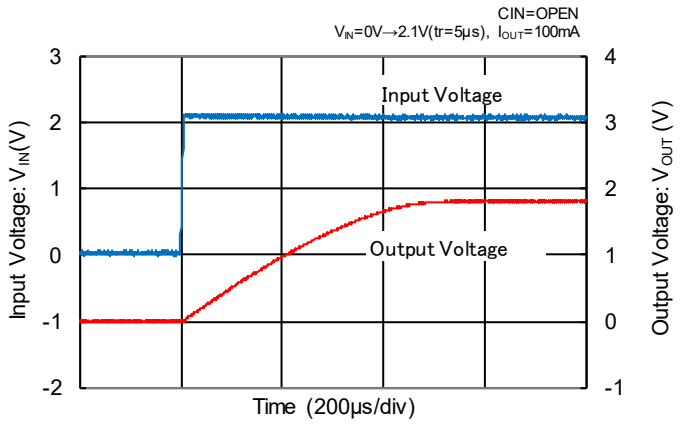
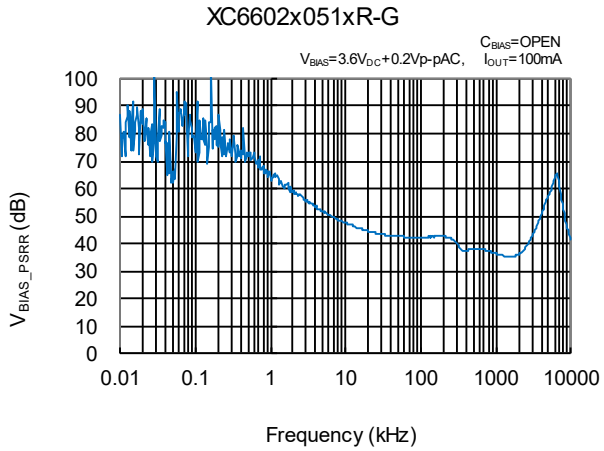
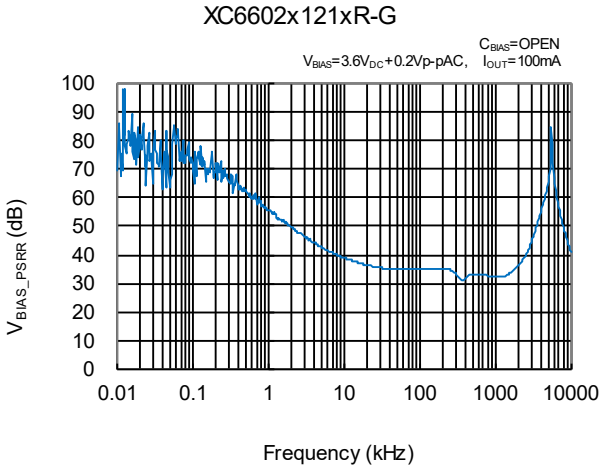


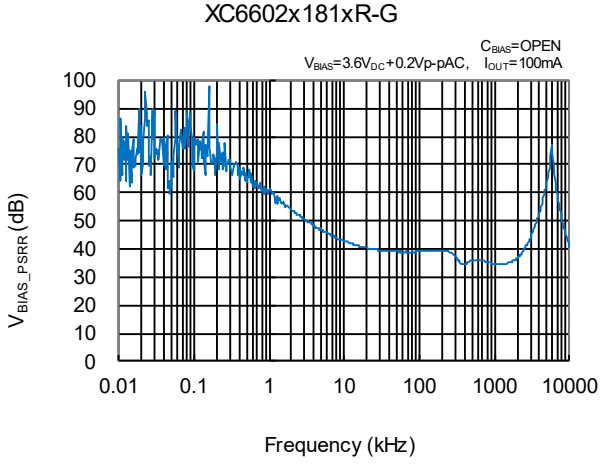
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

* Unless otherwise stated, V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=1mA, C_{BIAS}= C_{IN}=1.0μF, C_L=2.2μF, Ta=25℃

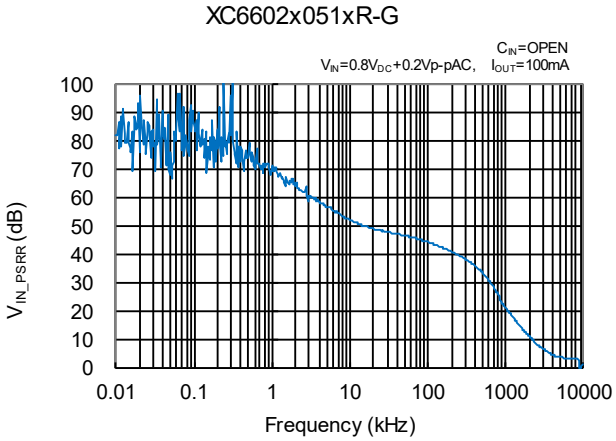
(16) Bias Voltage Ripple Rejection

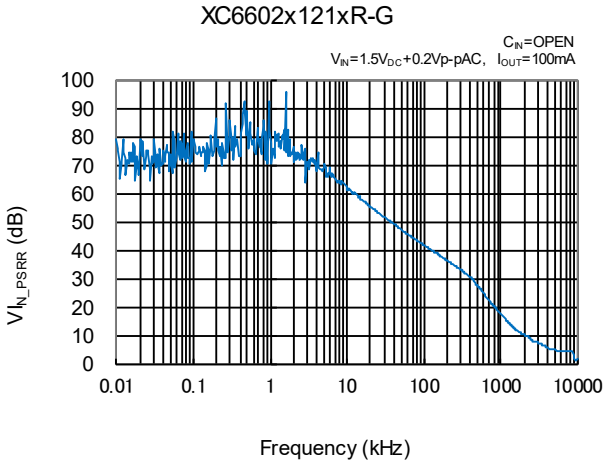


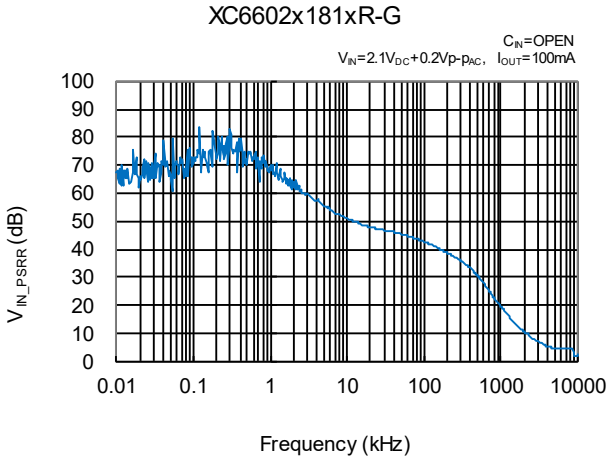




(17) Input Voltage Ripple Rejection







■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

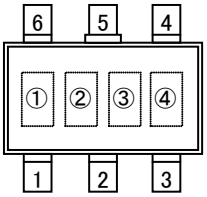
PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
SOT-26W	SOT-26W PKG	SOT-26W Power Dissipation
SOT-89-5	SOT-89-5 PKG	SOT-89-5 Power Dissipation
USP-6C	USP-6C PKG	USP-6C Power Dissipation
WLP-5-02	WLP-5-02 PKG	WLP-5-02 Power Dissipation

■MARKING RULE

① represents product series

MARK	PRODUCT SERIES
P	XC6602A****-G
R	XC6602B****-G

SOT-26W



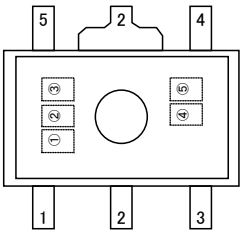
② represents voltage range

MARK	OUTPUT VOLTAGE (V)	MARK	OUTPUT VOLTAGE (V)
A	0.5	N	1.5
B	0.6	P	1.6
C	0.7	R	1.7
D	0.8	S	1.8
E	0.9	T	-
F	1.0	U	-
H	1.1	V	-
K	1.2	X	-
L	1.3	Y	-
M	1.4	Z	-

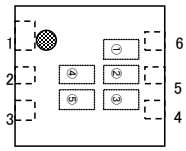
③④ represents production lot number
01 to 09, 0A to 0Z, 11 to 9Z, A1 to A9, AA to Z9, B1 to ZZ in order.
(G, I, J, O, Q, W excluded)
*No character inversion used.

■MARKING RULE (Continued)

SOT-89-5



USP-6C



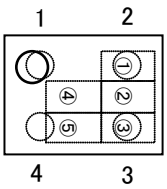
① represents product series

MARK	PRODUCT SERIES
7	XC6602******-G

② represents regulator type

MARK	PRODUCT SERIES
A	XC6602A****-G
B	XC6602B****-G

WLP-5-02



③ represents voltage range

MARK	OUTPUT VOLTAGE (V)	MARK	OUTPUT VOLTAGE (V)	MARK	OUTPUT VOLTAGE (V)
0	0.5	A	1.5	N	-
1	0.6	B	1.6	P	-
2	0.7	C	1.7	R	-
3	0.8	D	1.8	S	-
4	0.9	E	-	T	-
5	1.0	F	-	U	-
6	1.1	H	-	V	-
7	1.2	K	-	X	-
8	1.3	L	-	Y	-
9	1.4	M	-	Z	-

④⑤ represents production lot number
01 to 09, 0A to 0Z, 11 to 9Z, A1 to A9, AA to AZ, B1 to ZZ in order.
(G, I, J, O, Q, W excluded)

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9.

TOREX SEMICONDUCTOR LTD.