MX555ABB300M000

Ultra-Low Jitter 300MHz LVDS XO

ClockWorks® FUSION

General Description

The MX555ABB300M000 is an ultra-low phase jitter XO with LVDS output optimized for high line rate applications.

Features

- 300MHz LVDS
- Typical phase noise:
  - 100fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 5mm x 3.2mm LGA package

Absolute Maximum Ratings[1]

Supply Voltage (VIN)....................................+4.6V
Lead Temperature (soldering, 10s)............................260°C
Case Temperature..115°C
Storage Temperature (T_S)............................-65°C to +125°C
ESD Machine Model..200V
ESD Rating (HBM)..2kV

Operating Ratings[2]

Supply Voltage (VIN).......................+2.375V to +3.63V
Ambient Temperature (TA)....................-40°C to +85°C
Junction Thermal Resistance
    LGA (T_{JC}) Still Air.....................................58°C/W

Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 100 Ohms between Q and /Q.[3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current			90	100	mA
F0	Center Frequency			300		MHz
	Frequency Stability	Note 4			±50	ppm
Øj	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		140 100		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		100		400	ps
	Duty Cycle		45		55	%
VOH	Output High Voltage VOH max = VCM max + 1/2 VOD max	LVDS output levels	1.248	1.375	1.602	V
VOL	Output Low Voltage VOL min = VCM min - 1/2 VOD max	LVDS output levels	0.898	1.025	1.252	V
VOD	Output Differential Voltage		247	350	454	mV
VCM	Common Mode Output Voltage		1.125	1.2	1.375	V

Notes:

1. Exceeding the absolute maximum ratings may damage the device.

2. The device is not guaranteed to function outside its operating ratings.

3. Guaranteed after thermal equilibrium.

4. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX555ABB300M000	MX555A	BB3000	Tube	6-Pin 5mm x 3.2mm LGA
MX555ABB300M000-TR	MX555A	BB3000	Tape and Reel	6-Pin 5mm x 3.2mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration
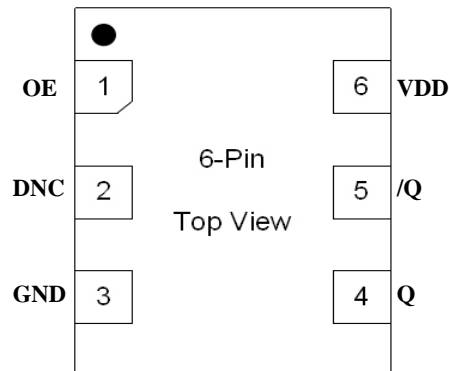
Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVCMOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up (Internal)
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVDS	Clock Output Frequency = 300MHz
6	VDD	PWR		Power Supply

Environmental Specifications

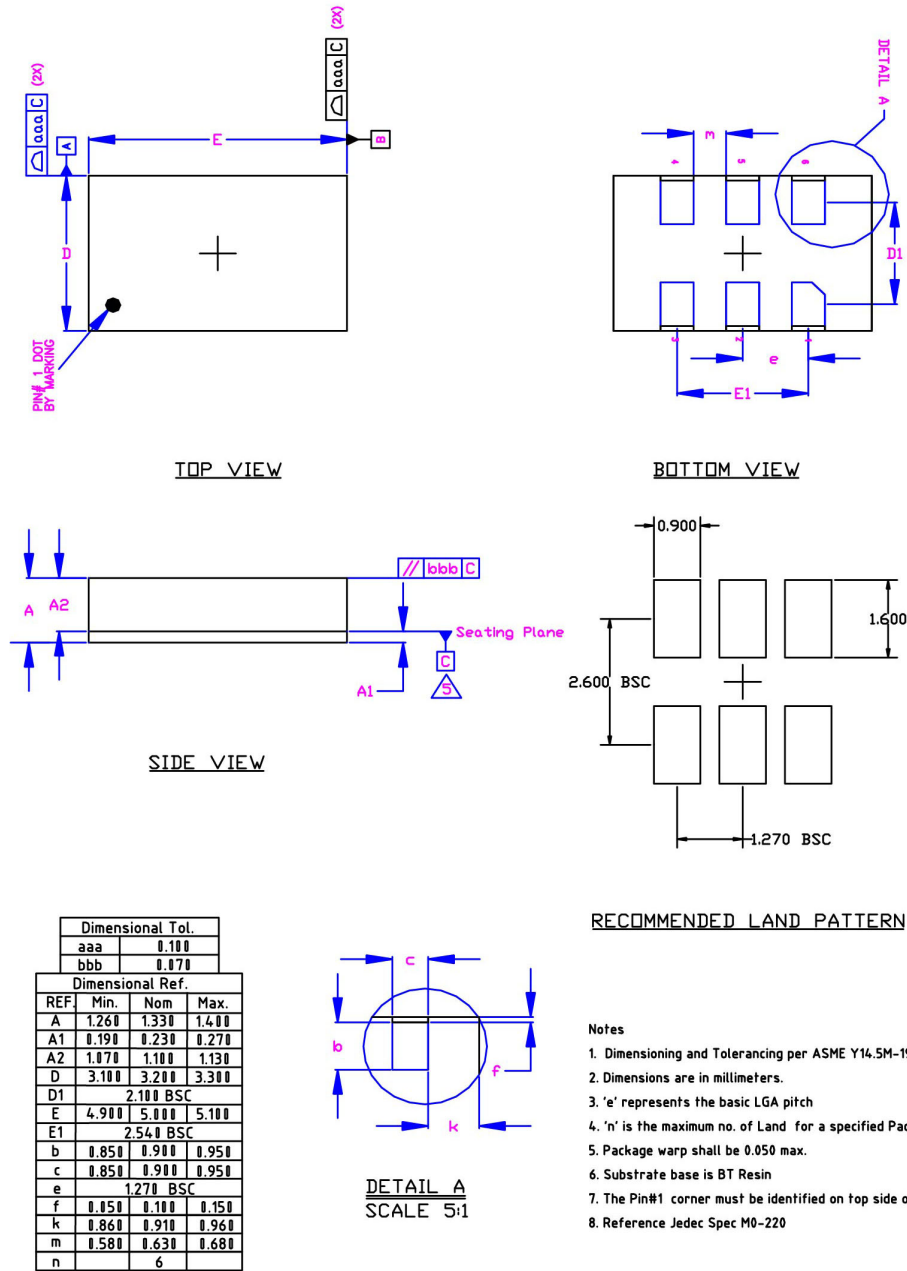|	
Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Mechanical Shock	MIL-STD-883, Method 2002, Condition C
Mechanical Vibration	MIL-STD-883, Method 2007, Condition A
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free devices (except 2 cycles max)
Hazardous Substance	Pb-Free / RoHS / Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1=2x10-8 atm cc/s
MSL Level	Crystal - MSL-1, Package MSL-3
Solvent Resistance	MIL-STD-202, Method 215
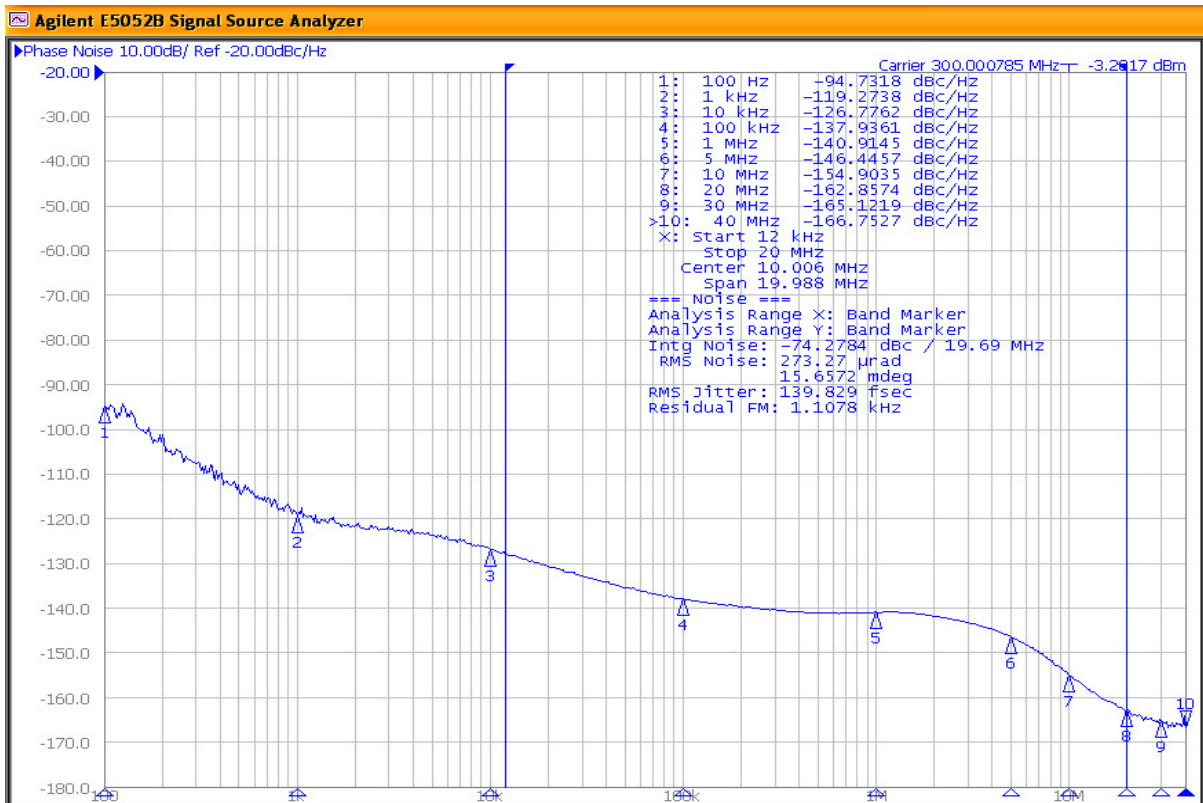
Figure 1. LVDS Output 300MHz 12kHz-20MHz 140fs

Package Information and Recommended Land Pattern for 6-Pin LGA³

TOP VIEW

BOTTOM VIEW

SIDE VIEW

	0.900		
2.600 BSC	1.600	
1.270 BSC	

RECOMMENDED LAND PATTERN

Dimensional Tol.	
aaa	0.100
bbb	0.070

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.260	1.330	1.400
A1	0.190	0.230	0.270
A2	1.070	1.100	1.130
D	3.100	3.200	3.300
D1	2.100 BSC		
E	4.900	5.000	5.100
E1	2.540 BSC		
b	0.850	0.900	0.950
c	0.850	0.900	0.950
e	1.270 BSC		
f	0.050	0.100	0.150
k	0.860	0.910	0.960
m	0.580	0.630	0.680
n	6		

DETAIL A
SCALE 5:1

Notes

1. Dimensioning and Tolerancing per ASME Y14.5M-1994.

2. Dimensions are in millimeters.

3. 'e' represents the basic LGA pitch

4. 'n' is the maximum no. of Land for a specified Package.

5. Package warp shall be 0.050 max.

6. Substrate base is BT Resin

7. The Pin#1 corner must be identified on top side only.

8. Reference Jedec Spec M0-220

6-Pin LGA (5x3.2mm)

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

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