Single, 3 V, CMOS, LVDS Differential Line Receiver

Data Sheet

ADN4662

FEATURES

- ±15 kV ESD protection on input pins
- 400 Mbps (200 MHz) switching rates
- Flow-through pinout simplifies PCB layout
- 2.5 ns maximum propagation delay
- 3.3 V power supply
- High impedance outputs on power-down
- Low power design: typically 18 mW (quiescent)
- Interoperable with existing 5 V LVDS drivers
- Accepts small swing (310 mV typical) differential signal levels
- Supports open, short, and terminated input fail-safe
- 0 V to −100 mV threshold region
- Conforms to TIA/EIA-644 LVDS standard
- Industrial operating temperature range: −40°C to +85°C
- Available in surface-mount (SOIC) package

APPLICATIONS

- Point-to-point data transmission
- Multidrop buses
- Clock distribution networks
- Backplane receivers

FUNCTIONAL BLOCK DIAGRAM

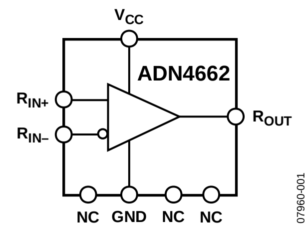

Figure 1.

GENERAL DESCRIPTION

The ADN4662 is a single, CMOS, low voltage differential signaling (LVDS) line receiver offering data rates of over 400 Mbps (200 MHz), and ultralow power consumption. It features a flow-through pinout for easy PCB layout and separation of input and output signals.

The device accepts low voltage (310 mV typical) differential input signals and converts them to a single-ended 3 V TTL/CMOS logic level.

The ADN4662 and its companion driver, the ADN4661, offer a new solution to high speed, point-to-point data transmission, and a low power alternative to emitter-coupled logic (ECL) or positive emitter-coupled logic (PECL).

Rev. A Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

10/13—Rev. 0 to Rev. A

Change to Features Section ... 1

1/09—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.0 V to 3.6 V; C_L = 15 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter[1]	Symbol	Min	Typ[2]	Max	Unit	Conditions/Comments
LVDS INPUT						
High Threshold at R_{IN+}, R_{IN-}[3]	V_{TH}			+100	mV	V_{CM} = 1.2 V, 0.05 V, 2.95 V
Low Threshold at R_{IN+}, R_{IN-}[3]	V_{TL}	−100			mV	V_{CM} = 1.2 V, 0.05 V, 2.95 V
Input Current at R_{IN+}, R_{IN-}	I_{IN}	−10	±1	+10	µA	V_{IN} = 2.8 V, V_{CC} = 3.6 V or 0 V
		−10	±1	+10	µA	V_{IN} = 0 V, V_{CC} = 3.6 V or 0 V
		−20	±1	+20	µA	V_{IN} = 3.6 V, V_{CC} = 0 V
OUTPUT						
Output High Voltage	V_{OH}	2.7	3.1		V	I_{OH} = −0.4 mA, V_{ID} = +200 mV
		2.7	3.1		V	I_{OH} = −0.4 mA, input terminated
		2.7	3.1		V	I_{OH} = −0.4 mA, input shorted
Output Low Voltage	V_{OL}		0.3	0.5	V	I_{OL} = 2 mA, V_{ID} = −200 mV
Output Short-Circuit Current[4]	I_{OS}	−15	−47	−100	mA	Enabled, V_{OUT} = 0 V
Input Clamp Voltage	V_{CL}	−1.5	−0.8		V	I_{CL} = −18 mA
POWER SUPPLY						
No Load Supply Current	I_{CC}		5.4	9	mA	Inputs open
ESD PROTECTION						
R_{IN+}, R_{IN-} Pins			±15		kV	Human body model
All Pins Except R_{IN+}, R_{IN-}			±4		kV	Human body model

[1] Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground, unless otherwise specified.
[2] All typicals are given for: V_{CC} = +3.3 V, T_A = 25°C.
[3] V_{CC} is always higher than R_{IN+} and R_{IN-} voltage. R_{IN-} and R_{IN+} are allowed to have a voltage range of −0.2 V to V_{CC} − V_{ID}/2. However, to be compliant with ac specifications, the common voltage range is 0.1 V to 2.3 V.
[4] Output short-circuit current (I_{OS}) is specified as magnitude only; the minus sign indicates direction only. Only one output should be shorted at a time. Do not exceed maximum junction temperature specification.

AC CHARACTERISTICS

V_{DD} = 3.0 V to 3.6 V; C_L[1] = 15 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ[2]	Max	Unit	Conditions/Comments[3]
Differential Propagation Delay High to Low	t_{PHLD}	1.0	2.15	2.5	ns	C_L = 15 pF, V_{ID} = 200 mV (see Figure 2 and Figure 3)
Differential Propagation Delay Low to High	t_{PLHD}	1.0	2.03	2.5	ns	C_L = 15 pF, V_{ID} = 200 mV (see Figure 2 and Figure 3)
Differential Pulse Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$[4]	t_{SKD1}	0	80	400	ps	C_L = 15 pF, V_{ID} = 200 mV (see Figure 2 and Figure 3)
Differential Part-to-Part Skew[5]	t_{SKD3}			1.0	ns	C_L = 15 pF, V_{ID} = 200 mV (see Figure 2 and Figure 3)
Differential Part-to-Part Skew[6]	t_{SKD4}			1.5	ns	C_L = 15 pF, V_{ID} = 200 mV (see Figure 2 and Figure 3)
Rise Time	t_{TLH}		510	800	ps	C_L = 15 pF, V_{ID} = 200 mV (see Figure 2 and Figure 3)
Fall Time	t_{THL}		445	800	ps	C_L = 15 pF, V_{ID} = 200 mV (see Figure 2 and Figure 3)
Maximum Operating Frequency[7]	f_{MAX}	200	250		MHz	All channels switching

[1] C_L includes probe and jig capacitance.
[2] All typicals are given for V_{CC} = 3.3 V, T_A = 25°C.
[3] Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, t_{TLH} and t_{THL} (0% to 100%) ≤ 3 ns for R_{IN+}/R_{IN-}.
[4] t_{SKD1} is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
[5] t_{SKD3}, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
[6] t_{SKD4}, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |maximum − minimum| differential propagation delay.
[7] f_{MAX} generator input conditions: f = 200 MHz, t_{TLH} = t_{THL} < 1 ns (0% to 100%), 50% duty cycle, differential (1.05 V to 1.35 V peak-to-peak). Output criteria: 60%/40% duty cycle, V_{OL} (maximum 0.4 V), V_{OH} (minimum 2.7 V), load = 15 pF (stray plus probes).

Test Circuits and Timing Diagrams

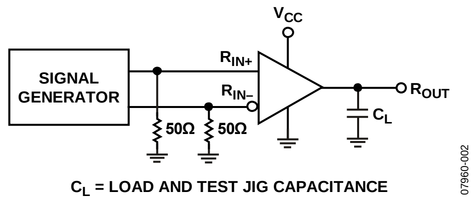

Figure 2. Test Circuit for Receiver Propagation Delay and Transition Time

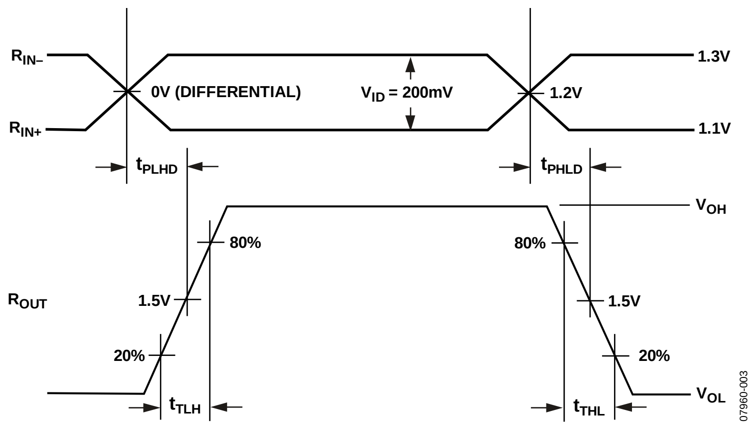

Figure 3. Receiver Propagation Delay and Transition Time Waveforms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC} to GND	−0.3 V to +4 V
Input Voltage (R_{IN+}, R_{IN-}) to GND	−0.3 V to V_{CC} + 3.9 V
Output Voltage (R_{OUT}) to GND	−0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	
Industrial Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
SOIC Package	
θ_{JA} Thermal Impedance	149.5°C/W
Reflow Soldering Peak Temperature	
Pb-Free	260°C ± 5°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

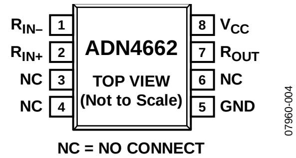

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{IN-}	Receiver Channel 1 Inverting Input. When this input is more negative than R_{IN+}, R_{OUT} is high. When this input is more positive than R_{IN+}, R_{OUT} is low.
2	R_{IN+}	Receiver Channel 1 Noninverting Input. When this input is more positive than R_{IN-}, R_{OUT} is high. When this input is more negative than R_{IN-}, R_{OUT} is low.
3	NC	No Connect.
4	NC	No Connect.
5	GND	Ground reference point for all circuitry on the part.
6	NC	No Connect.
7	R_{OUT}	Receiver Output (3 V TTL/CMOS). If the differential input voltage between R_{IN+} and R_{IN-} is positive, this output is high. If the differential input voltage is negative, this output is low.
8	V_{CC}	Power Supply Input. This part can be operated from 3.0 V to 3.6 V.

TYPICAL PERFORMANCE CHARACTERISTICS

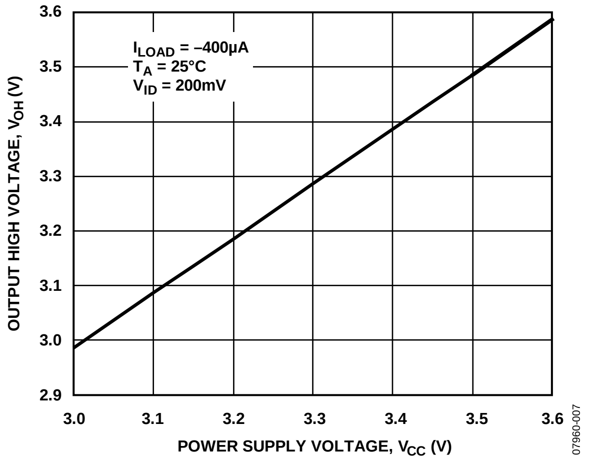

Figure 5. Output High Voltage vs. Power Supply Voltage

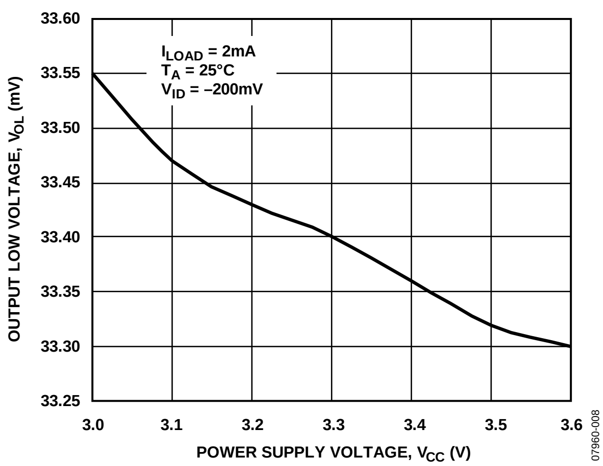

Figure 6. Output Low Voltage vs. Power Supply Voltage

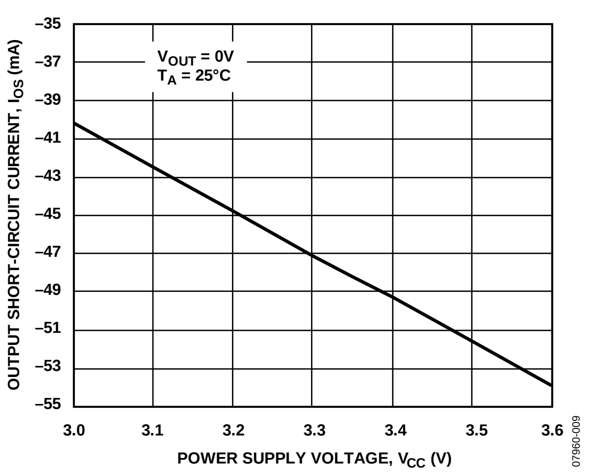

Figure 7. Output Short-Circuit Current vs. Power Supply Voltage

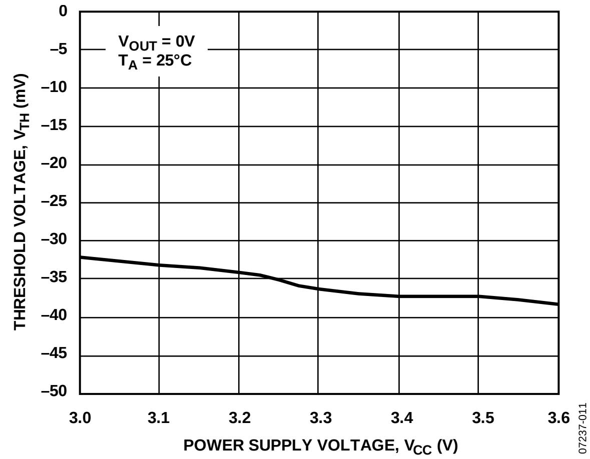

Figure 8. Threshold Voltage vs. Power Supply Voltage

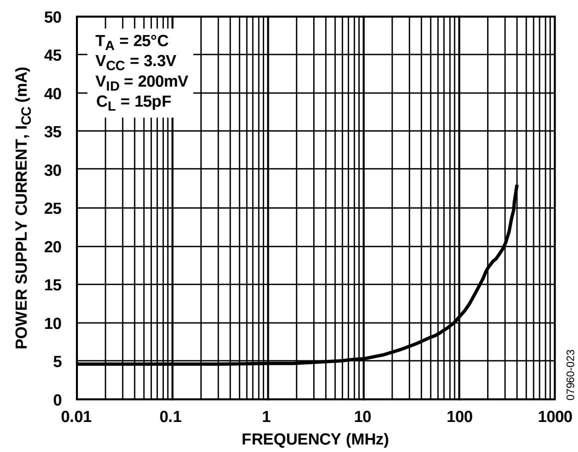

Figure 9. Power Supply Current vs. Frequency

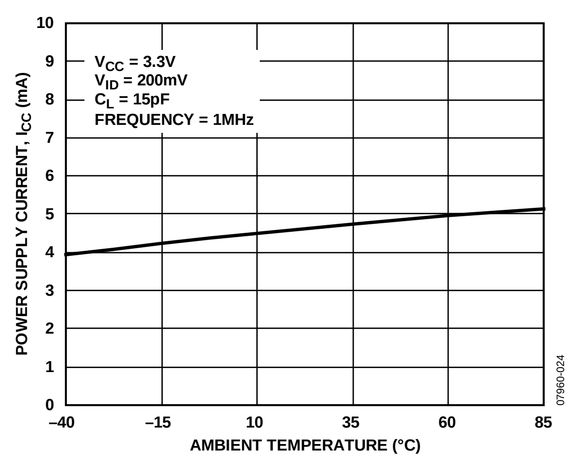

Figure 10. Power Supply Current vs. Ambient Temperature

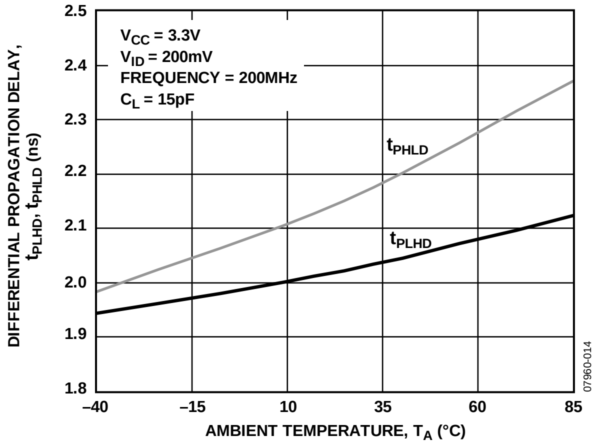

Figure 11. Differential Propagation Delay vs. Ambient Temperature

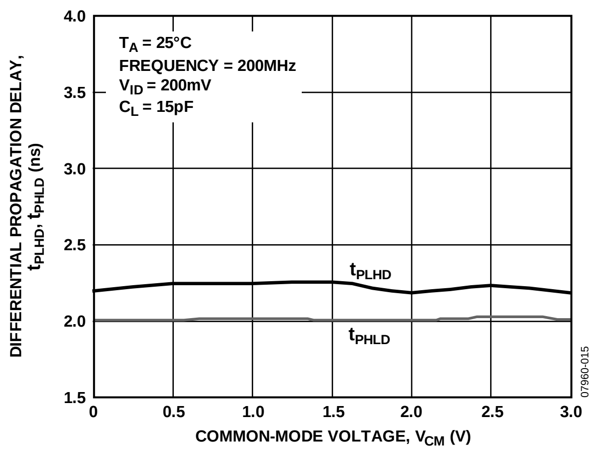

Figure 12. Differential Propagation Delay vs. Common-Mode Voltage

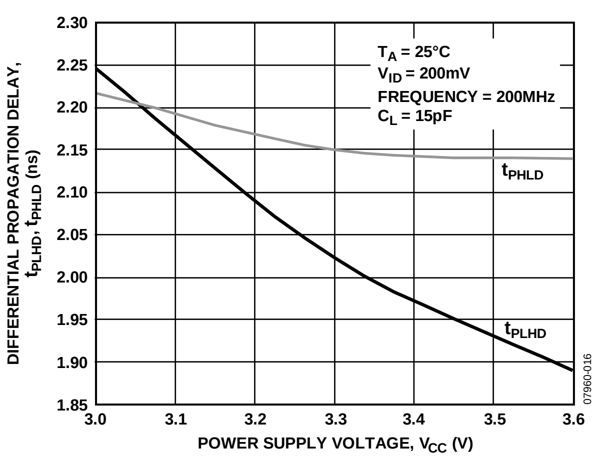

Figure 13. Differential Propagation Delay vs. Power Supply Voltage

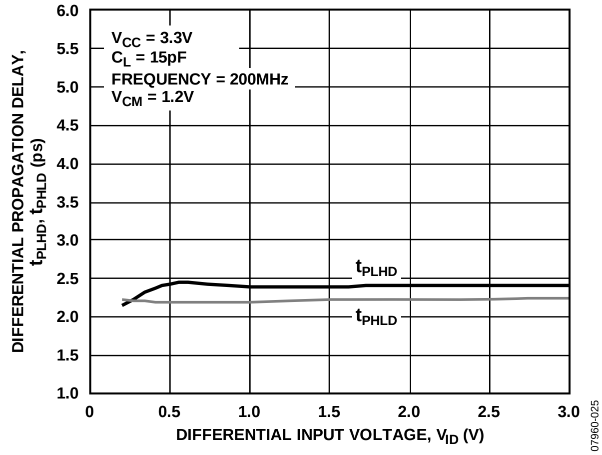

Figure 14. Differential Propagation Delay vs. Differential Input Voltage

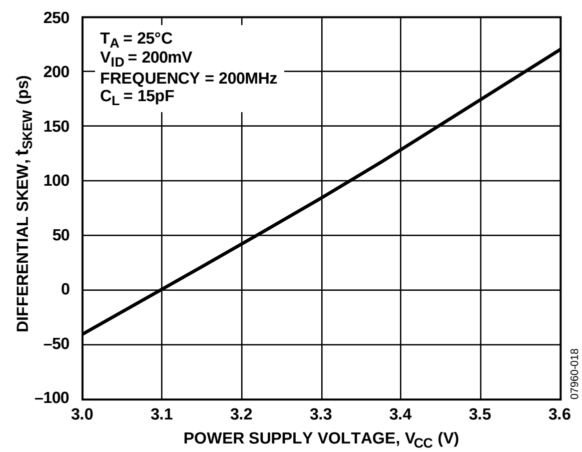

Figure 15. Differential Skew vs. Power Supply Voltage

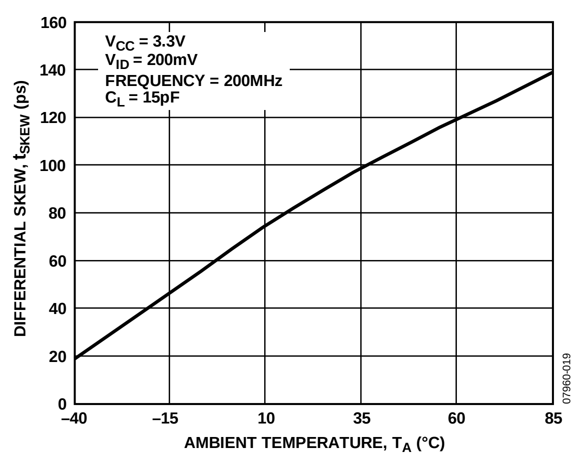

Figure 16. Differential Skew vs. Ambient Temperature

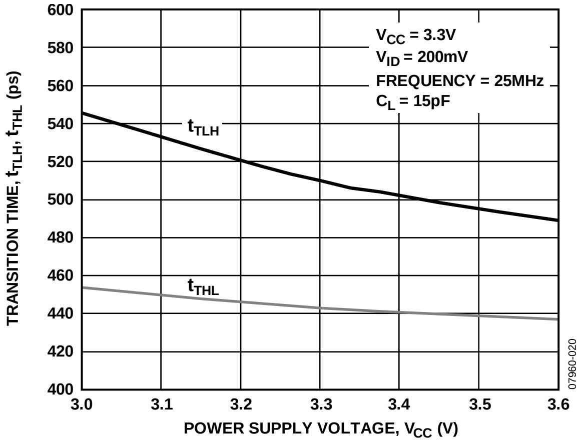

Figure 17. Transition Time vs. Power Supply Voltage

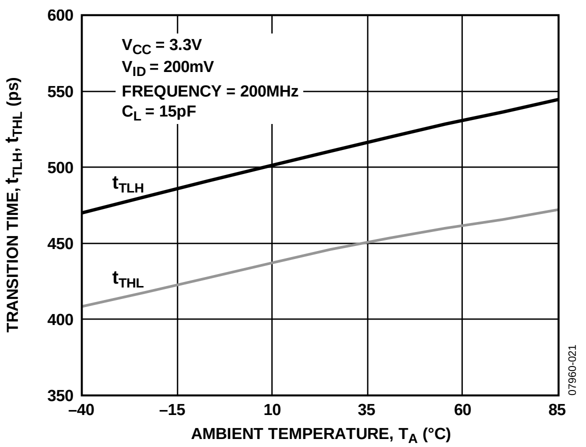

Figure 18. Transition Time vs. Ambient Temperature

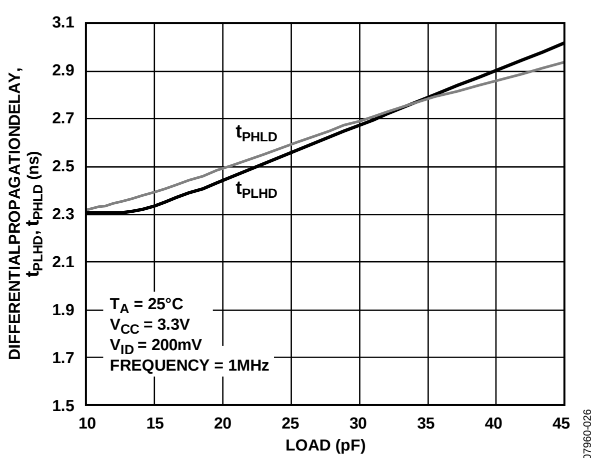

Figure 19. Differential Propagation Delay vs. Load at 1 MHz

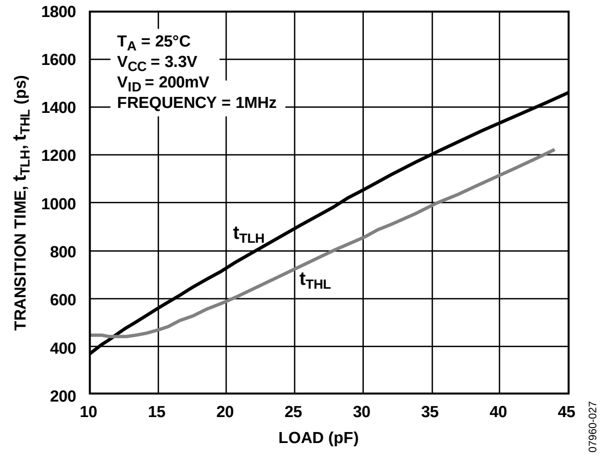

Figure 20. Transition Time vs. Load

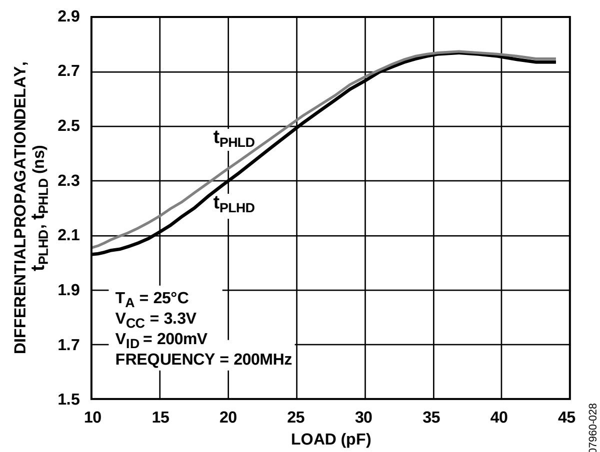

Figure 21. Differential Propagation Delay vs. Load at 200 MHz

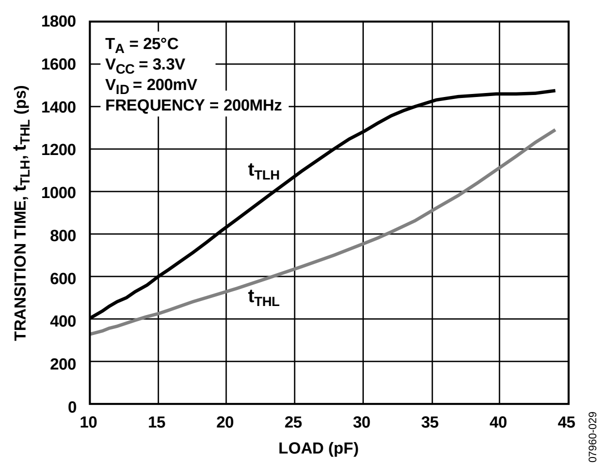

Figure 22. Transition Time vs. Load at 200 MHz

THEORY OF OPERATION

The ADN4662 is a single line receiver for low voltage differential signaling. It takes a differential input signal of 310 mV typically and converts it into a single-ended 3 V TTL/CMOS logic signal.

A differential current input signal, received via a transmission medium, such as a twisted pair cable, develops a voltage across a terminating resistor, R_T. This resistor is chosen to match the characteristic impedance of the medium, typically around 100 Ω. The differential voltage is detected by the receiver and converted back into a single-ended logic signal.

When the noninverting receiver input, R_{IN+}, is positive with respect to the inverting input R_{IN-} (current flows through R_T from R_{IN+} to R_{IN-}), then R_{OUT} is high. When the noninverting receiver input R_{IN+} is negative with respect to the inverting input R_{IN-} (current flows through R_T from R_{IN-} to R_{IN+}), then R_{OUT} is low.

The ADN4662 differential line receiver is capable of receiving signals of 100 mV over a ±1 V common-mode range centered around 1.2 V. This relates to the typical driver offset voltage value of 1.2 V. The signal originating from the driver is centered around 1.2 V and may shift ±1 V around this center point. This ±1 V shifting may be caused by a difference in the ground potential of the driver and receiver, the common-mode effect of coupled noise, or both.

Using the ADN4663 as a driver, the received differential current is between 2.5 mA and 4.5 mA (typically 3.1 mA), developing between 250 mV and 450 mV across a 100 Ω termination resistor. The received voltage is centered around the receiver offset of 1.2 V. In other words, the noninverting receiver input is typically (1.2 V + [310 mV/2]) = 1.355 V, and the inverting receiver input (1.2 V − [310 mV/2]) = 1.045 V for Logic 1. For Logic 0, the inverting and noninverting input voltages are reversed. Note that because the differential voltage reverses polarity, the peak-to-peak voltage swing across R_T is twice the differential voltage.

Current mode signalling offers considerable advantages over voltage mode signalling, such as RS-422. The operating current remains fairly constant with increased switching frequency, whereas with voltage mode drivers the current increases exponentially in most cases. This is caused by the overlap as internal gates switch between high and low, which causes currents to flow from V_{CC} to ground. A current mode device simply reverses a constant current between its two outputs, with no significant overlap currents.

This is similar to emitter-coupled logic (ECL) and positive emitter-coupled logic (PECL), but without the high quiescent current of ECL and PECL.

APPLICATIONS INFORMATION

Figure 23 shows a typical application for point-to-point data transmission using the ADN4663 as the driver.

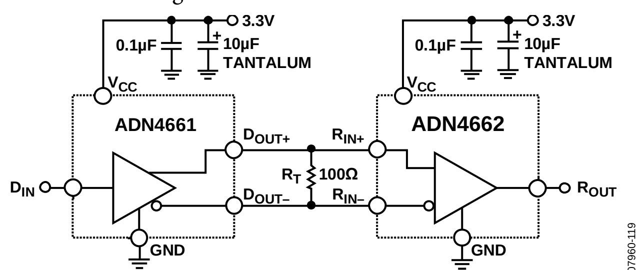

Figure 23. Typical Application Circuit

OUTLINE DIMENSIONS

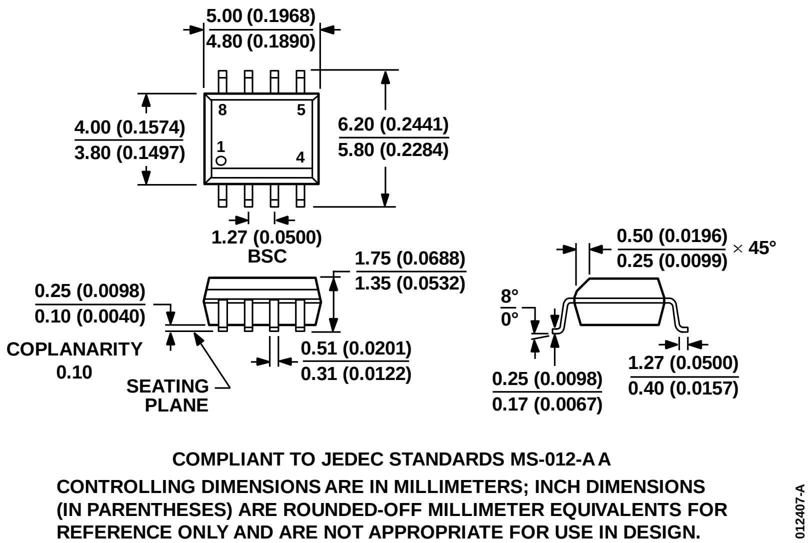

Figure 24. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADN4662BRZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
ADN4662BRZ-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Compliant Part.