



CY91F583AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK
CY91F584AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK
CY91F585AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK

CY91580M/S Series, FR81S 32-bit Microcontroller Datasheet

This series is a Cypress 32-bit microcontroller for automobile motor control. They use the FR81S CPU that is compatible with the FR family.

Features

FR81S CPU Core

- 32-bit RISC, load/store architecture, pipeline 5-stage structure
- Maximum operating frequency: 128MHz (Source oscillation= 4.0MHz, 32 multiplied (PLL clock multiplication system))
- General-purpose register: 32 bits × 16 sets
- 16-bit fixed length instructions (basic instructions), 1 instruction per cycle
- Instructions appropriate to embedded applications
 - Memory-to-memory transfer instructions
 - Bit manipulation instructions
 - Barrel shift instructions
- High-level language support instructions
 - Function entry/exit instructions
 - Register content multi-load and store instructions
- Bit search instructions
Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot
Overhead decrement during branch process
- Register interlock function
Easy assembler writing
- Built-in multiplier and instruction level support
 - Signed 32-bit multiplication: 5 cycles
 - Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS saving)
6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR family
- Built-in memory protection function (MPU)
 - Eight protection areas can be specified commonly for instructions and data.
 - Control access privilege in both privilege mode and user mode
- Built-in FPU (floating-point operation)
 - IEEE754 compliant
 - Floating-point register: 32 bits × 16 sets

Peripheral functions

- Clock generation (SSCG function is available)
 - Main oscillation (4 MHz to 20 MHz)
 - PLL multiplication rate: 1 to 32 times
- CR oscillation
 - Oscillation frequency: 100kHz, with frequency accuracy ± 50% (pre-trimming)
 - Trimming is enabled
 - To be used as a count clock of hardware watchdog
 - Oscillation stop feature during standby is not available
CY91F583AMJ/F584AMJ/F585AMJ/F583AMK/F584AMK/F585AMK
CY91F583ASJ/F584ASJ/F585ASJ/F583ASK/F584ASK/F585ASK
 - Oscillation stop feature during standby is available
CY91F583AMG/F584AMG/F585AMG/F583AMH/F584AMH/F585AMH
CY91F583ASG/F584ASG/F585ASG/F583ASH/F584ASH/F585ASH
- Built-in program flash memory capacity
CY91F583: 256+64 Kbytes
CY91F584: 384+64 Kbytes
CY91F585: 512+64 Kbytes
- Built-in data flash (WorkFlash) 64 Kbytes
- Built-in RAM capacity
 - Main RAM
CY91F583: 32 Kbytes
CY91F584: 48 Kbytes
CY91F585: 48 Kbytes
 - Backup RAM 8 Kbytes
- General-purpose port:
CY91F583AM/F584AM/F585AM 76 ports
Including eight I²C pseudo open drain corresponding ports
CY91F583AS/F584AS/F585AS 44ports
Including two I²C pseudo open drain corresponding ports

- DMA controller
 - Up to 8 channels can be started simultaneously.
 - 2 transfer factors (Internal peripheral request and software)
- External interrupt input

CY91F583AM/F584AM/F585AM: 8 channels
 CY91F583AS/F584AS/F585AS: 7 channels
 Level ("H" / "L") or edge detection (rising or falling) enabled
- Multi-function serial communication (built-in transmission/reception FIFO memory)

CY91F583AM/F584AM/F585AM: 4 channels
 CY91F583AS/F584AS/F585AS: 2 channels

 - UART (Asynchronous serial interface)
 - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
 - Parity or no parity is selectable.
 - Built-in dedicated baud rate generator
 - An external clock can be used as the transfer clock
 - Parity, frame, and overrun error detection functions provided
 - DMA transfer supported
 - CSIO (Synchronous serial interface)
 - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
 - SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
 - Built-in dedicated baud rate generator (Master operation)
 - An external clock can be entered. (Slave operation)
 - Overrun error detection function is provided.
 - Built-in chip selection function
 - DMA transfer supported
 - LIN interface (v2.1)
 - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
 - LIN protocol revision 2.1 supported.
 - Master and slave systems supported
 - Framing error and overrun error detection
 - LIN sync break generation and detection; LIN sync delimiter generation
 - Built-in dedicated baud rate generator
 - An external clock can be adjusted by the reload counter.
 - DMA transfer supported
 - I²C
 - CY91F583AM/F584AM/F585AM: Supported for 3 channels: ch.0, ch.2, and ch.3
 CY91F583AS/F584AS/F585AS: Supported for 1 channel: ch.0
 - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
 - Standard mode (Max. 100 kbps) / high-speed mode (Max. 400 kbps) supported
- DMA transfer supported (for transmission only)
- CAN controller (CAN)

CY91F583AM/F584AM/F585AM: 2 channels
 CY91F583AS/F584AS/F585AS: 1 channel

 - Transfer speed: Up to 1Mbps
 - 64-transmission/reception message buffering
- FlexRay controller

CY91F583AMG/F584AMG/F585AMG/F583AMJ/F584AMJ/F585AMJ/
 F583ASG/F584ASG/F585ASG/F583ASJ/F584ASJ/F585ASJ:
 1 unit (ch.A/ch.B)

 - FlexRay Specifications Version 2.1 supported
 - Up to 128 message buffers
 - 8K bytes of message RAM
 - Variable length of message buffers
 - Each message buffer can be allocated as a part of reception buffer, transmission buffer or reception FIFO memory
 - Host access to the message buffer via input and output buffers
 - Filtering for slot counter, cycle counter and channels
 - Maskable interrupts are supported
- PPG: 16 bits × 6 channels
- Reload timer: 16 bits × 4 channels
- A/D converter (successive approximation type)
 - 12-bit resolution

CY91F583AM/F584AM/F585AM: 3 units (23 channels)
 CY91F583AS/F584AS/F585AS: 3 units (17 channels)
 - Conversion time: 1 μs
- Free-run timer

16 bits × 6 channels (1 channel can be selected for input capture, and 1 channel for output compare.)
- Input capture: 16 bits × 4 channels (linked to the free-run timer)
- Output compare: 16 bits × 7 channels (linked to the free-run timer)
- Waveform generator: 2 units (7 channels)
- 10-bit D/A converter: 1 channel
- Calibration: The hardware watchdog for CR oscillation drive
 The CR oscillation frequency can be trimmed.
- Clock Supervisor
 - Anomaly supervisory feature (by damaged quartz, etc.) of external main oscillation (4MHz)
 - When anomaly is detected, clock is switched to CR.
- Up/ down counter: 2 channels
 - 8/16-bit Up/ down counter
- Base timer: 2 channels
 - 16-bit timer
 - Any of four PWM/PPG/PWC/reload timer functions can be selected and used.
 - As for the functions of PWC and reload timer, 2 channels of cascade mode can be used as 32-bit timer.

- CRC generation
- Watchdog timer
 - Hardware watchdog
 - Software watchdog
- NMI
- Interrupt controller
- Interrupt request batch read
Multiple interrupts from peripherals can be read by a series of registers.
- I/O relocation (CY91F583AM/F584AM/F585AM)
Change of pin position of peripheral functions
- Low-power consumption mode
 - Sleep/Stop/Watch
 - Stop (Power shutdown)/Watch (Power shutdown)
- Power-on reset
- Low-voltage detection reset (external low-voltage detection)
- Low-voltage detection reset (internal low-voltage detection)
- Package

CY91F583AM/F584AM/F585AM:	LQFP-100
CY91F583AS/F584AS/F585AS:	LQFP-64
- CMOS 90 nm technology
- Power supplies
 - Single 5V power supply
 - The voltage step-down circuit brings the 5.0V down to generate 1.2V internally
 - I/O 5.0V

Contents

1. Product Lineup	5	11.1 Absolute Maximum Ratings	111
2. Pin Assignment	11	11.2 Recommended Operating Conditions	113
3. Pin Description	13	11.3 DC Characteristics	114
4. I/O Circuit Type	24	11.4 AC Characteristics	121
5. Handling Precautions	30	11.5 A/D Converter	147
5.1 Precautions for Product Design	30	11.6 D/A Converter	150
5.2 Precautions for Package Mounting.....	31	11.7 Flash memory	150
5.3 Precautions for Use Environment.....	32	12. Example Characteristics	151
6. Handling Devices	33	13. Ordering Information	155
7. Block Diagram	35	14. Package Dimensions	156
8. Memory Map	37	15. Major Changes	158
9. I/O Map	38	Document History	160
10. Interrupt Vector Table	106	Sales, Solutions, and Legal Information	161
11. Electrical Characteristics	111		

1. Product Lineup

CY91580AM Series Product Lineup Comparison

■ Memory size

Items	CY91F583AMG CY91F583AMH CY91F583AMJ CY91F583AMK	CY91F584AMG CY91F584AMH CY91F584AMJ CY91F584AMK	CY91F585AMG CY91F585AMH CY91F585AMJ CY91F585AMK
Flash memory capacity (program)	256+64 Kbytes	384+64 Kbytes	512+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	32 Kbytes	48 Kbytes	48 Kbytes
RAM capacity (backup)	8 Kbytes		

■ Function

Items	CY91F583AMG CY91F584AMG CY91F585AMG	CY91F583AMH CY91F584AMH CY91F585AMH	CY91F583AMJ CY91F584AMJ CY91F585AMJ	CY91F583AMK CY91F584AMK CY91F585AMK
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during standby	Provided	Provided	Not provided	Not provided
External bus interface	Not provided			
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	4 channels			
Output compare	7 channels			
Waveform generator	2 units (7 channels)			
16-bit reload timer	4 channels			
PPG	6 channels			
External interrupt	8 channels			
A/D converter	3 units (23 channels)			
R/D converter	Not provided			
D/A converter	Provided			
Up/ down counter	2 channels			
Multi-function serial interface	4 channels			
CAN	64msb × 2 channels (ch.0/ch.1)			
FlexRay	128msb × 1 unit (ch.A / ch.B)	Not provided	128msb × 1 unit (ch.A / ch.B)	Not provided
Software watchdog	Provided			
Hardware watchdog	Provided			
CRC generation	2 channels			
Low-voltage detection reset (internal low-voltage detection)	Provided			

Items	CY91F583AMG CY91F584AMG CY91F585AMG	CY91F583AMH CY91F584AMH CY91F585AMH	CY91F583AMJ CY91F584AMJ CY91F585AMJ	CY91F583AMK CY91F584AMK CY91F585AMK
Low-voltage detection reset (external low-voltage detection)	Provided			
Device package	LQFP-100			
Debug interface	Built-in OCD (On Chip Debug Unit)			

CY91580AS Series Product Lineup Comparison
■ Memory size

Items	CY91F583ASG CY91F583ASH CY91F583ASJ CY91F583ASK	CY91F584ASG CY91F584ASH CY91F584ASJ CY91F584ASK	CY91F585ASG CY91F585ASH CY91F585ASJ CY91F585ASK
Flash memory capacity (program)	256+64 Kbytes	384+64 Kbytes	512+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	32 Kbytes	48 Kbytes	48 Kbytes
RAM capacity (backup)	8 Kbytes		

■ Function

Items	CY91F583ASG CY91F584ASG CY91F585ASG	CY91F583ASH CY91F584ASH CY91F585ASH	CY91F583ASJ CY91F584ASJ CY91F585ASJ	CY91F583ASK CY91F584ASK CY91F585ASK
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during standby	Provided	Provided	Not provided	Not provided
External bus interface	Not provided			
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	4 channels			
Output compare	7 channels			
Waveform generator	2 units (7 channels)			
16-bit reload timer	4 channels			
PPG	6 channels			
External interrupt	7 channels			
A/D converter	3 units (17 channels)			
R/D converter	Not provided			
D/A converter	Provided			
Up/ down counter	2 channels			
Multi-function serial interface	2 channels			
CAN	64msb × 1 channel (ch.0)			
FlexRay	128msb × 1unit (ch.A / ch.B)	Not provided	128msb × 1unit (ch.A / ch.B)	Not provided
Software watchdog	Provided			
Hardware watchdog	Provided			
CRC generation	2 channels			
Low-voltage detection reset (internal low-voltage detection)	Provided			

Items	CY91F583ASG CY91F584ASG CY91F585ASG	CY91F583ASH CY91F584ASH CY91F585ASH	CY91F583ASJ CY91F584ASJ CY91F585ASJ	CY91F583ASK CY91F584ASK CY91F585ASK
Low-voltage detection reset (external low-voltage detection)	Provided			
Device package	LQFP-64			
Debug interface	Built-in OCD (On Chip Debug Unit)			

CY91580L Series Product Lineup Comparison

■ Memory size

Items	CY91F585LA CY91F585LB CY91F585LC CY91F585LD	CY91F586LA CY91F586LB CY91F586LC CY91F586LD	CY91F587LA CY91F587LB CY91F587LC CY91F587LD
Flash memory capacity (program)	512+64 Kbytes	768+64 Kbytes	1024+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	48 Kbytes	64 Kbytes	96 Kbytes
RAM capacity (backup)	8 Kbytes		

■ Function

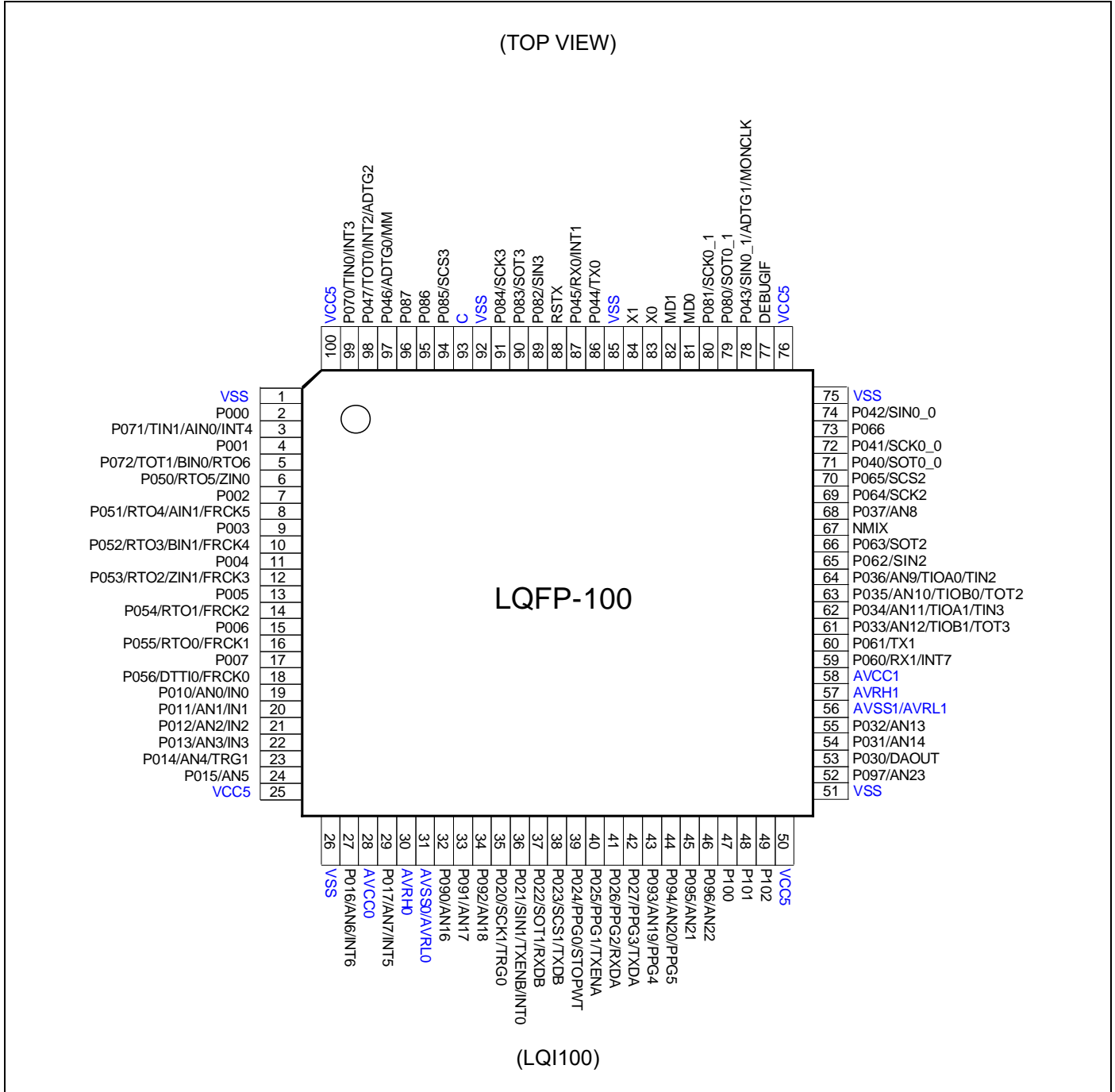
Items	CY91F585LA CY91F586LA CY91F587LA	CY91F585LB CY91F586LB CY91F587LB	CY91F585LC CY91F586LC CY91F587LC	CY91F585LD CY91F586LD CY91F587LD
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during standby	Provided	Provided	Not provided	Not provided
External bus interface	Not provided	Address: 22 bits Data: 16 bits	Not provided	Address: 22 bits Data: 16 bits
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	8 channels			
Output compare	12 channels			
Waveform generator	2 units (12 channels)			
16-bit reload timer	4 channels			
PPG	24 channels			
External interrupt	8 channels			
A/D converter	3 units (24 channels)			
R/D converter	Provided	Not provided	Provided	Not provided
D/A converter	Not provided	Provided	Not provided	Provided
Up/ down counter	2 channels			
Multi-function serial interface	5 channels			
CAN	64 msb × 3 channels (ch.0/ch.1/ch.2)			
FlexRay	128 msb × 1 unit (ch.A / ch.B)			
Software watchdog	Provided			
Hardware watchdog	Provided			
CRC generation	1 channel			
Low-voltage detection reset (internal low-voltage detection)	Provided			
Low-voltage detection reset (external low-voltage detection)	Provided			

Items	CY91F585LA CY91F586LA CY91F587LA	CY91F585LB CY91F586LB CY91F587LB	CY91F585LC CY91F586LC CY91F587LC	CY91F585LD CY91F586LD CY91F587LD
Device package	LQFP-144			
Debug interface	Built-in OCD (On Chip Debug Unit)			

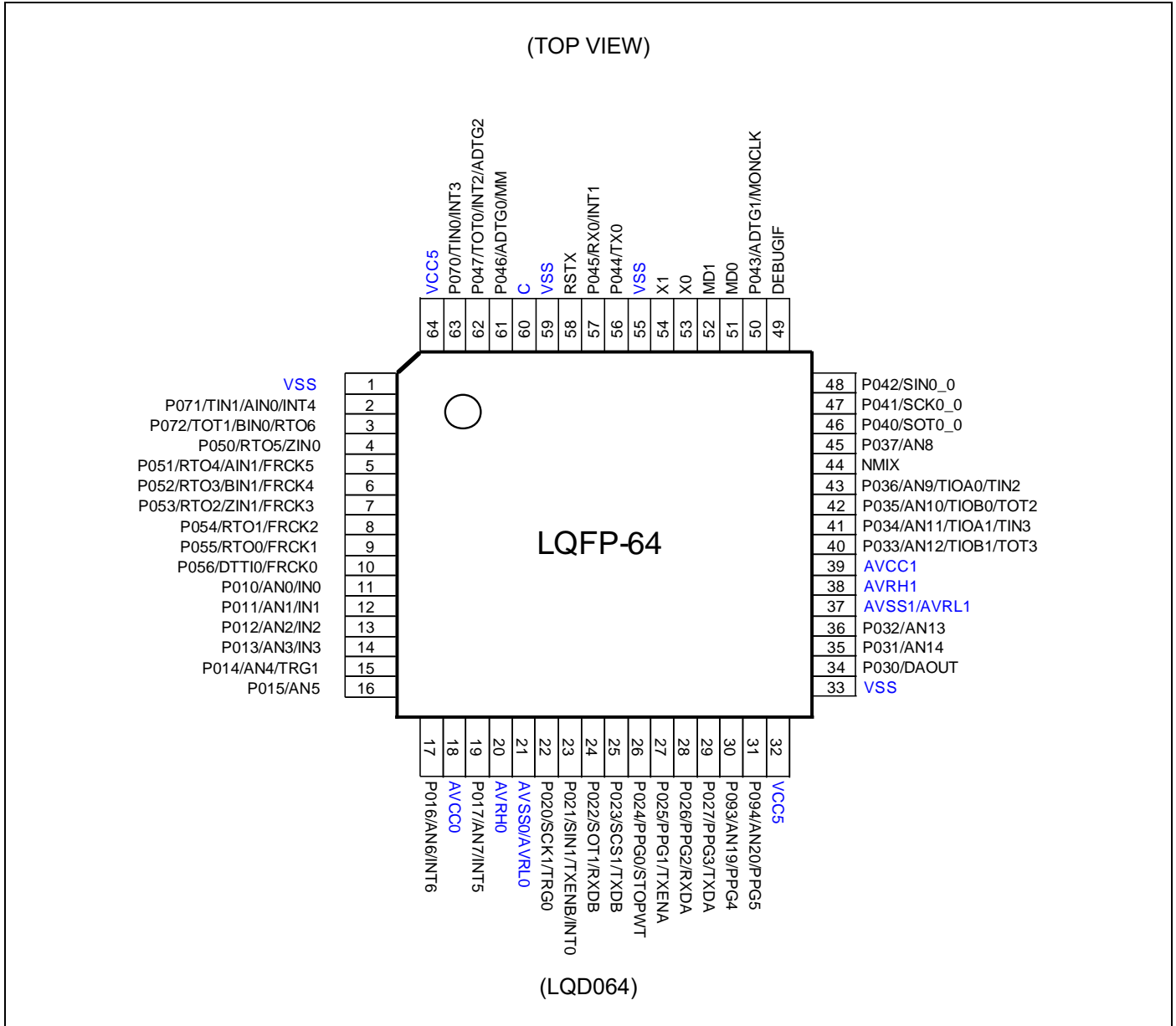
Note: For details on the CY91580L series, see the "CY91580L Series HARDWARE MANUAL".

2. Pin Assignment

LQFP-100 Pin Assignment CY91F583AM/F584AM/F585AM



LQFP-64 Pin Assignment CY91F583AS/F584AS/F585AS



3. Pin Description

CY91F583AM/F584AM/F585AM

Pin No.	Pin name	I/O circuit type*	Function
83	X0	A	Main clock oscillation input pin
84	X1		Main clock oscillation output pin
67	NMIX	B	Interrupt input pin without mask
88	RSTX	B	External reset input pin
81	MD0	C	Mode pin 0 (with high-voltage control)
82	MD1	C	Mode pin 1 (with high-voltage control)
2	P000	D	General-purpose I/O port
4	P001	D	General-purpose I/O port
7	P002	D	General-purpose I/O port
9	P003	D	General-purpose I/O port
11	P004	D	General-purpose I/O port
13	P005	D	General-purpose I/O port
15	P006	D	General-purpose I/O port
17	P007	D	General-purpose I/O port
19	P010	F	General-purpose I/O port
	IN0		16-bit input capture ch.0 external pulse input pin
	AN0		ADC analog 0 input pin
20	P011	F	General-purpose I/O port
	IN1		16-bit input capture ch.1 external pulse input pin
	AN1		ADC analog 1 input pin
21	P012	F	General-purpose I/O port
	IN2		16-bit input capture ch.2 external pulse input pin
	AN2		ADC analog 2 input pin
22	P013	F	General-purpose I/O port
	IN3		16-bit input capture ch.3 external pulse input pin
	AN3		ADC analog 3 input pin
23	P014	F	General-purpose I/O port
	TRG1		PPG ch.4, ch.5 external trigger
	AN4		ADC analog 4 input pin
24	P015	F	General-purpose I/O port
	AN5		ADC analog 5 input pin
27	P016	G	General-purpose I/O port
	AN6		ADC analog 6 input pin
	INT6		INT6 external interrupt input pin

Pin No.	Pin name	I/O circuit type*	Function
29	P017	G	General-purpose I/O port
	AN7		ADC analog 7 input pin
	INT5		INT5 external interrupt input pin
35	P020	D	General-purpose I/O port
	SCK1		Multi-function serial ch.1 clock I/O pin
	TRG0		PPG ch.0 to ch.3 external trigger
36	P021	L	General-purpose I/O port
	SIN1		Multi-function serial ch.1 serial data input pin
	TXENB		FlexRay ch.B operation enable output pin
	INT0		INT0 external interrupt input pin
37	P022	K	General-purpose I/O port
	SOT1		Multi-function serial ch.1 serial data output pin
	RXDB		FlexRay ch.B data input pin
38	P023	K	General-purpose I/O port
	SCS1		Multi-function serial ch.1 serial chip select I/O pin
	TXDB		FlexRay ch.A operation enable output pin
39	P024	D	General-purpose I/O port
	PPG0		PPG ch.0 output pin
	STOPWT		FlexRay Stopwatch input pin
40	P025	K	General-purpose I/O port
	PPG1		PPG ch.1 output pin
	TXENA		FlexRay ch.A operation enable output pin
41	P026	K	General-purpose I/O port
	PPG2		PPG ch.2 output pin
	RXDA		FlexRay ch.A data input pin
42	P027	K	General-purpose I/O port
	PPG3		PPG ch.3 output pin
	TXDA		FlexRay ch.A data output pin
53	P030	M	General-purpose I/O port
	DAOUT		DAC analog output pin
54	P031	F	General-purpose I/O port
	AN14		ADC analog 14 input pin

Pin No.	Pin name	I/O circuit type*	Function
55	P032	F	General-purpose I/O port
	AN13		ADC analog 13 input pin
61	P033	F	General-purpose I/O port
	TIOB1		Base timer ch.1 TIOB input pin
	TOT3		Reload timer ch.3 output pin
	AN12		ADC analog 12 input pin
62	P034	F	General-purpose I/O port
	TIOA1		Base timer ch.1 TIOA I/O pin
	TIN3		Reload timer ch.3 event input pin
	AN11		ADC analog 11 input pin
63	P035	F	General-purpose I/O port
	TIOB0		Base timer ch.0 TIOB input pin
	TOT2		Reload timer ch.2 output pin
	AN10		ADC analog 10 input pin
64	P036	F	General-purpose I/O port
	TIOA0		Base timer ch.0 TIOA output pin
	TIN2		Reload timer ch.2 event input pin
	AN9		ADC analog 9 input pin
68	P037	F	General-purpose I/O port
	AN8		ADC analog 8 input pin
71	P040	H	General-purpose I/O port
	SOT0_0		Multi-function serial ch.0 serial data output pin (0)/ I ² C ch.0 serial data I/O pin (SDA)
72	P041	H	General-purpose I/O port
	SCK0_0		Multi-function serial ch.0 clock I/O pin (0)/ I ² C ch.0 clock I/O pin (SCL)
74	P042	D	General-purpose I/O port
	SIN0_0		Multi-function serial ch.0 serial data input pin (0)
78	P043	D	General-purpose I/O port
	SIN0_1		Multi-function serial ch.0 serial data input pin (1)
	ADTG1		A/D converter ch.8 to ch.14 external trigger input pin
	MONCLK		Clock monitor output pin
86	P044	D	General-purpose I/O port
	TX0		CAN transmission data 0 output pin

Pin No.	Pin name	I/O circuit type*	Function
87	P045	E	General-purpose I/O port
	RX0		CAN reception data 0 input pin
	INT1		INT1 external interrupt input pin
97	P046	D	General-purpose I/O port
	ADTG0		A/D converter ch.0 to ch.7 external trigger input pin
	MM		Clock supervisor main clock stop detection output pin
98	P047	E	General-purpose I/O port
	TOT0		Reload timer ch.0 output pin
	INT2		INT2 external interrupt input pin
	ADTG2		A/D converter ch.16-ch.23 external trigger input pin
6	P050	D	General-purpose I/O port
	RTO5		Waveform generator ch.5 output pin
	ZIN0		Up/down counter ch.0 ZIN input pin
8	P051	D	General-purpose I/O port
	RTO4		Waveform generator ch.4 output pin
	AIN1		Up/down counter ch.1 AIN input pin
	FRCK5		Free-run timer ch.5 external clock input pin
10	P052	D	General-purpose I/O port
	RTO3		Waveform generator ch.3 output pin
	BIN1		Up/down counter ch.1 BIN input pin
	FRCK4		Free-run timer ch.4 external clock input pin
12	P053	D	General-purpose I/O port
	RTO2		Waveform generator ch.2 output pin
	ZIN1		Up/down counter ch.1 ZIN input pin
	FRCK3		Free-run timer ch.3 external clock input pin
14	P054	D	General-purpose I/O port
	RTO1		Waveform generator ch.1 output pin
	FRCK2		Free-run timer ch.2 external clock input pin
16	P055	D	General-purpose I/O port
	RTO0		Waveform generator ch.0 output pin
	FRCK1		Free-run timer ch.1 external clock input pin
18	P056	D	General-purpose I/O port
	DTTI0		Waveform generator output stop signal input pin 0
	FRCK0		Free-run timer ch.0 external clock input pin
59	P060	E	General-purpose I/O port
	RX1		CAN reception data 1 input pin
	INT7		INT7 external interrupt input pin
60	P061	D	General-purpose I/O port
	TX1		CAN transmission data 1 output pin

Pin No.	Pin name	I/O circuit type*	Function
65	P062	D	General-purpose I/O port
	SIN2		Multi-function serial ch.2 serial data input pin
66	P063	H	General-purpose I/O port
	SOT2		Multi-function serial ch.2 serial data output pin/ I ² C ch.2 serial data I/O pin (SDA)
69	P064	H	General-purpose I/O port
	SCK2		Multi-function serial ch.2 clock I/O pin/ I ² C ch.2 clock I/O pin (SCL)
70	P065	D	General-purpose I/O port
	SCS2		Multi-function serial ch.2 serial chip select I/O pin
73	P066	D	General-purpose I/O port
99	P070	E	General-purpose I/O port
	TIN0		Reload timer ch.0 event input pin
	INT3		INT3 external interrupt input pin
3	P071	E	General-purpose I/O port
	TIN1		Reload timer ch.1 event input pin
	AIN0		Up/down counter ch.0 AIN input pin
	INT4		INT4 external interrupt input pin
5	P072	D	General-purpose I/O port
	TOT1		Reload timer ch.1 output pin
	BIN0		Up/down counter ch.0 BIN input pin
	RTO6		Waveform generator ch.6 output pin
79	P080	H	General-purpose I/O port
	SOT0_1		Multi-function serial ch.0 serial data output pin (1)/ I ² C ch.0 serial data I/O pin (1) (SDA)
80	P081	H	General-purpose I/O port
	SCK0_1		Multi-function serial ch.0 clock I/O pin (1)/ I ² C ch.0 clock I/O pin (1) (SCL)
89	P082	D	General-purpose I/O port
	SIN3		Multi-function serial ch.3 serial data input pin
90	P083	H	General-purpose I/O port
	SOT3		Multi-function serial ch.3 serial data output pin/ I ² C ch.3 serial data I/O pin (SDA)
91	P084	H	General-purpose I/O port
	SCK3		Multi-function serial ch.3 clock I/O pin/ I ² C ch.3 clock I/O pin (SCL)
94	P085	D	General-purpose I/O port
	SCS3		Multi-function serial ch.3 serial chip select I/O pin
95	P086	D	General-purpose I/O port
96	P087	D	General-purpose I/O port

Pin No.	Pin name	I/O circuit type*	Function
32	P090	F	General-purpose I/O port
	AN16		ADC analog 16 input pin
33	P091	F	General-purpose I/O port
	AN17		ADC analog 17 input pin
34	P092	F	General-purpose I/O port
	AN18		ADC analog 18 input pin
43	P093	F	General-purpose I/O port
	PPG4		PPG ch.4 output pin
	AN19		ADC analog 19 input pin
44	P094	F	General-purpose I/O port
	PPG5		PPG ch.5 output pin
	AN20		ADC analog 20 input pin
45	P095	F	General-purpose I/O port
	AN21		ADC analog 21 input pin
46	P096	F	General-purpose I/O port
	AN22		ADC analog 22 input pin
52	P097	F	General-purpose I/O port
	AN23		ADC analog 23 input pin
47	P100	D	General-purpose I/O port
48	P101	D	General-purpose I/O port
49	P102	D	General-purpose I/O port
77	DEBUGIF	I	DEBUG I/F pin
28	AVCC0	-	A/D converter analog power supply
58	AVCC1	-	A/D converter analog power supply
30	AVRH0	-	A/D converter upper limit reference voltage
57	AVRH1	-	A/D converter upper limit reference voltage
31	AVSS0	-	A/D converter GND
	AVRL0		A/D converter lower limit reference voltage
56	AVSS1	-	A/D converter GND
	AVRL1		A/D converter lower limit reference voltage
93	C	-	External capacity connection output pin
25, 50, 76, 100	VCC5	-	+5.0V power supply
1, 26, 51, 75, 85, 92	VSS	-	GND

* For I/O circuit types, see 4 I/O Circuit Type

CY91F583AS/F584AS/F585AS

Pin No.	Pin name	I/O circuit type*	Function
53	X0	A	Main clock oscillation input pin
54	X1		Main clock oscillation output pin
44	NMIX	B	Interrupt input pin without mask
58	RSTX	B	External reset input pin
51	MD0	C	Mode pin 0 (with high-voltage control)
52	MD1	C	Mode pin 1 (with high-voltage control)
11	P010	F	General-purpose I/O port
	IN0		16-bit input capture ch.0 external pulse input pin
	AN0		ADC analog 0 input pin
12	P011	F	General-purpose I/O port
	IN1		16-bit input capture ch.1 external pulse input pin
	AN1		ADC analog 1 input pin
13	P012	F	General-purpose I/O port
	IN2		16-bit input capture ch.2 external pulse input pin
	AN2		ADC analog 2 input pin
14	P013	F	General-purpose I/O port
	IN3		16-bit input capture ch.3 external pulse input pin
	AN3		ADC analog 3 input pin
15	P014	F	General-purpose I/O port
	TRG1		PPG ch.4, ch.5 external trigger
	AN4		ADC analog 4 input pin
16	P015	F	General-purpose I/O port
	AN5		ADC analog 5 input pin
17	P016	G	General-purpose I/O port
	AN6		ADC analog 6 input pin
	INT6		INT6 external interrupt input pin
19	P017	G	General-purpose I/O port
	AN7		ADC analog 7 input pin
	INT5		INT5 external interrupt input pin
22	P020	D	General-purpose I/O port
	SCK1		Multi-function serial ch.1 clock I/O pin
	TRG0		PPG ch.0 to ch.3 external trigger
23	P021	L	General-purpose I/O port
	SIN1		Multi-function serial ch.1 serial data input pin
	TXENB		FlexRay ch.B operation enable output pin
	INT0		INT0 external interrupt input pin

Pin No.	Pin name	I/O circuit type*	Function
24	P022	K	General-purpose I/O port
	SOT1		Multi-function serial ch.1 serial data output pin
	RXDB		FlexRay ch.B data input pin
25	P023	K	General-purpose I/O port
	SCS1		Multi-function serial ch.1 serial chip select I/O pin
	TXDB		FlexRay ch.B data output pin
26	P024	D	General-purpose I/O port
	PPG0		PPG ch.0 output pin
	STOPWT		FlexRay Stopwatch input pin
27	P025	K	General-purpose I/O port
	PPG1		PPG ch.1 output pin
	TXENA		FlexRay ch.A operation enable output pin
28	P026	K	General-purpose I/O port
	PPG2		PPG ch.2 output pin
	RXDA		FlexRay ch.A data input pin
29	P027	K	General-purpose I/O port
	PPG3		PPG ch.3 output pin
	TXDA		FlexRay ch.A data output pin
34	P030	M	General-purpose I/O port
	DAOUT		DAC analog output pin
35	P031	F	General-purpose I/O port
	AN14		ADC analog 14 input pin
36	P032	F	General-purpose I/O port
	AN13		ADC analog 13 input pin
40	P033	F	General-purpose I/O port
	TIOB1		Base timer ch.1 TIOB input pin
	TOT3		Reload timer ch.3 output pin
	AN12		ADC analog 12 input pin
41	P034	F	General-purpose I/O port
	TIOA1		Base timer ch.1 TIOA I/O pin
	TIN3		Reload timer ch.3 event input pin
	AN11		ADC analog 11 input pin
42	P035	F	General-purpose I/O port
	TIOB0		Base timer ch.0 TIOB input pin
	TOT2		Reload timer ch.2 output pin
	AN10		ADC analog 10 input pin

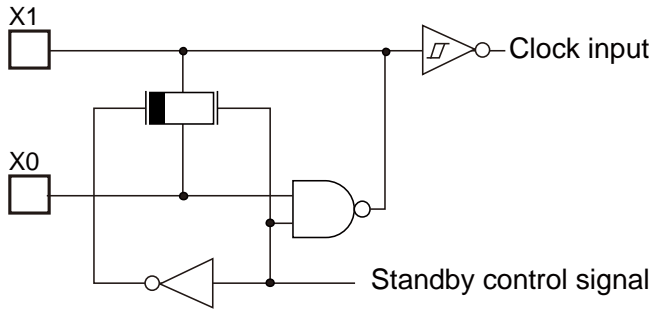
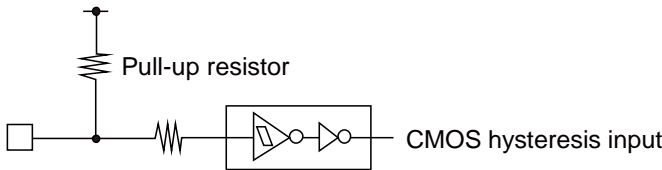
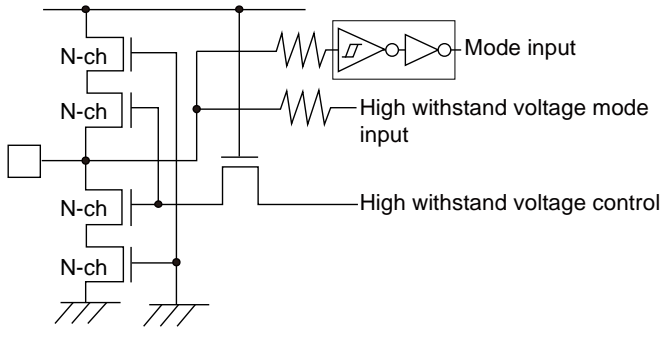
Pin No.	Pin name	I/O circuit type*	Function
43	P036	F	General-purpose I/O port
	TIOA0		Base timer ch.0 TIOA output pin
	TIN2		Reload timer ch.2 event input pin
	AN9		ADC analog 9 input pin
45	P037	F	General-purpose I/O port
	AN8		ADC analog 8 input pin
46	P040	H	General-purpose I/O port
	SOT0_0		Multi-function serial ch.0 serial data output pin(0)/ I ² C ch.0 serial data I/O pin (0) (SDA)
47	P041	H	General-purpose I/O port
	SCK0_0		Multi-function serial ch.0 clock I/O pin (0)/ I ² C ch.0 clock I/O pin (0) (SCL)
48	P042	D	General-purpose I/O port
	SIN0_0		Multi-function serial ch.0 serial data input pin (0)
50	P043	D	General-purpose I/O port
	ADTG1		A/D converter ch.8 to ch.14 external trigger input pin
	MONCLK		Clock monitor output pin
56	P044	D	General-purpose I/O port
	TX0		CAN transmission data 0 output pin
57	P045	E	General-purpose I/O port
	RX0		CAN reception data 0 input pin
	INT1		INT1 external interrupt input pin
61	P046	D	General-purpose I/O port
	ADTG0		A/D converter ch.0 to ch.7 external trigger input pin
	MM		Clock supervisor main clock stop detection output pin
62	P047	E	General-purpose I/O port
	TOT0		Reload timer ch.0 output pin
	INT2		INT2 external interrupt input pin
	ADTG2		A/D converter ch.19 to ch.20 external trigger input pin
4	P050	D	General-purpose I/O port
	RTO5		Waveform generator ch.5 output pin
	ZIN0		Up/down counter ch.0 ZIN input pin
5	P051	D	General-purpose I/O port
	RTO4		Waveform generator ch.4 output pin
	AIN1		Up/down counter ch.1 AIN input pin
	FRCK5		Free-run timer ch.5 external clock input pin

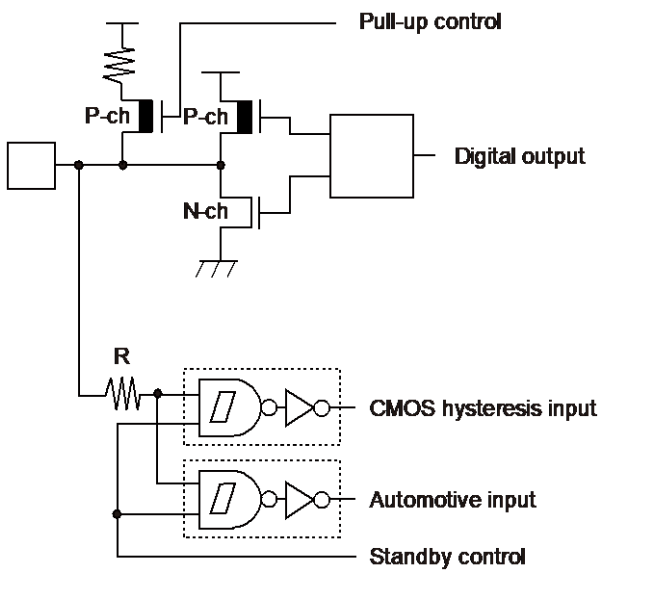
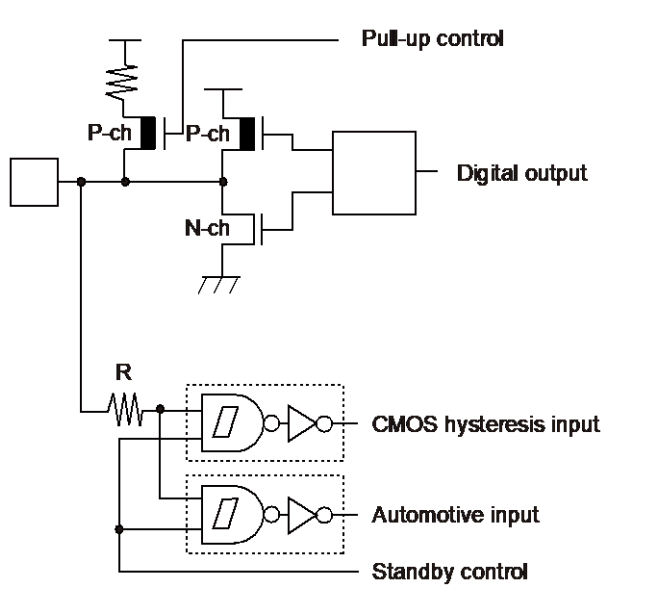
Pin No.	Pin name	I/O circuit type*	Function
6	P052	D	General-purpose I/O port
	RTO3		Waveform generator ch.3 output pin
	BIN1		Up/down counter ch.1 BIN input pin
	FRCK4		Free-run timer ch.4 external clock input pin
7	P053	D	General-purpose I/O port
	RTO2		Waveform generator ch.2 output pin
	ZIN1		Up/down counter ch.1 ZIN input pin
	FRCK3		Free-run timer ch.3 external clock input pin
8	P054	D	General-purpose I/O port
	RTO1		Waveform generator ch.1 output pin
	FRCK2		Free-run timer ch.2 external clock input pin
9	P055	D	General-purpose I/O port
	RTO0		Waveform generator ch.0 output pin
	FRCK1		Free-run timer ch.1 external clock input pin
10	P056	D	General-purpose I/O port
	DTTI0		Waveform generator output stop signal input pin 0
	FRCK0		Free-run timer ch.0 external clock input pin
63	P070	E	General-purpose I/O port
	TIN0		Reload timer ch.0 event input pin
	INT3		INT3 external interrupt input pin
2	P071	E	General-purpose I/O port
	TIN1		Reload timer ch.1 event input pin
	AIN0		Up/down counter ch.0 AIN input pin
	INT4		INT4 external interrupt input pin
3	P072	D	General-purpose I/O port
	TOT1		Reload timer ch.1 output pin
	BIN0		Up/down counter ch.0 BIN input pin
	RTO6		Waveform generator ch.6 output pin
30	P093	F	General-purpose I/O port
	PPG4		PPG ch.4 output pin
	AN19		ADC analog 19 input pin
31	P094	F	General-purpose I/O port
	PPG5		PPG ch.5 output pin
	AN20		ADC analog 20 input pin
49	DEBUGIF	I	DEBUG I/F pin
18	AVCC0	-	A/D converter analog power supply
39	AVCC1	-	A/D converter analog power supply
20	AVRH0	-	A/D converter upper limit reference voltage
38	AVRH1	-	A/D converter upper limit reference voltage

Pin No.	Pin name	I/O circuit type*	Function
21	AVSS0	-	A/D converter GND
	AVRL0		A/D converter lower limit reference voltage
37	AVSS1	-	A/D converter GND
	AVRL1		A/D converter lower limit reference voltage
60	C	-	External capacity connection output pin
32, 64	VCC5	-	+5.0V power supply
1, 33, 55, 59	VSS	-	GND

* For I/O circuit types, see 4 I/O Circuit Type

4. I/O Circuit Type

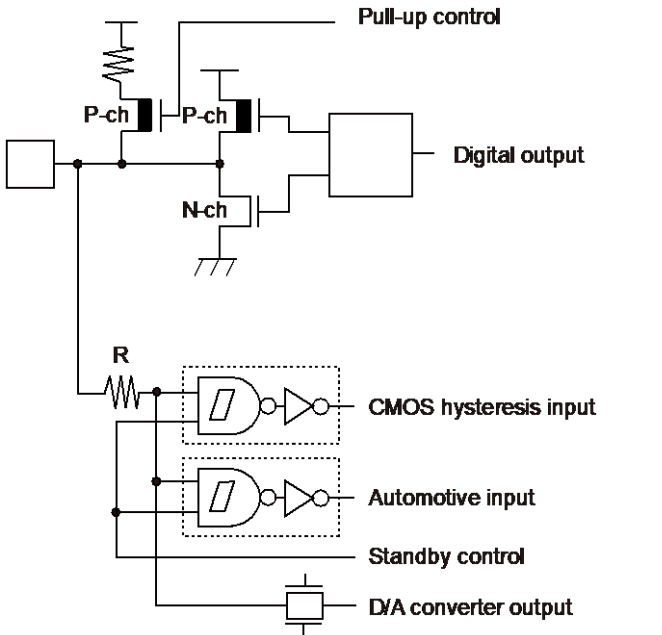
Type	Circuit	Remarks
A		<p>Oscillation feedback resistor: Approx. 1 MΩ</p>
B		<ul style="list-style-type: none"> ■ CMOS hysteresis input ■ With 50 kΩ pull-up resistor
C		<ul style="list-style-type: none"> ■ Schmitt input ■ With high withstand voltage control

Type	Circuit	Remarks
D	 <p>The diagram for Type D shows a CMOS output stage. A pull-up resistor is connected to the output node through a P-channel MOSFET controlled by 'Pull-up control'. The output node is also connected to an N-channel MOSFET controlled by 'Standby control'. The output node is connected to a 'Digital output' terminal. The input node is connected to a resistor 'R' and is also connected to the inputs of two CMOS hysteresis input and automotive input blocks, which are controlled by 'Standby control'.</p>	<ul style="list-style-type: none"> ■ General-purpose I/O port ■ CMOS level output $I_{OH}=-2/-5\text{mA}$, $I_{OL}=2/5\text{mA}$ ■ With 50kΩ pull-up resistor control ■ CMOS hysteresis input (0.7V_{cc}/0.3V_{cc}) ■ Automotive input (0.8V_{cc}/0.5V_{cc})
E	 <p>The diagram for Type E is similar to Type D, showing a CMOS output stage with pull-up control, digital output, CMOS hysteresis input, automotive input, and standby control. The circuit components and connections are identical to those shown in Type D.</p>	<ul style="list-style-type: none"> ■ General-purpose I/O port ■ CMOS level output $I_{OH}=-2/-5\text{mA}$, $I_{OL}=2/5\text{mA}$ ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7V_{cc}/0.3V_{cc}) During standby, the input value retains the previous value. ■ Automotive input (0.8V_{cc}/0.5V_{cc}) During standby, the input value retains the previous value.

Type	Circuit	Remarks
F	<p>The diagram for Type F shows a pull-up control circuit. It features a pull-up resistor connected to a P-channel MOSFET (P-ch) and a pull-down N-channel MOSFET (N-ch). The gates of these transistors are controlled by a 'Pull-up control' signal. The output of the N-ch MOSFET is labeled 'Digital output'. A resistor 'R' is connected to the input node. This node is also connected to a 'CMOS hysteresis input' (represented by a hysteresis symbol), an 'Automotive input' (represented by a triangle symbol), and a 'Standby control' signal. An 'Analog input' is also shown at the bottom of the circuit.</p>	<ul style="list-style-type: none"> ■ With analog input, general-purpose I/O port ■ CMOS level output $I_{OH}=-2/-5mA$, $I_{OL}=2/5mA$ ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7V_{cc}/0.3V_{cc}) ■ Automotive input (0.8V_{cc}/0.5V_{cc})
G	<p>The diagram for Type G is identical to the one for Type F, showing the same pull-up control circuit with P-ch and N-ch transistors, digital output, resistor R, CMOS hysteresis input, Automotive input, Standby control, and Analog input.</p>	<ul style="list-style-type: none"> ■ With analog input, general-purpose I/O port ■ CMOS level output $I_{OH}=-2/-5mA$, $I_{OL}=2/5mA$ ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7V_{cc}/0.3V_{cc}) During standby, the input value retains the previous value. ■ Automotive input (0.8V_{cc}/0.5V_{cc}) During standby, the input value retains the previous value.

Type	Circuit	Remarks
H	<p>The diagram for Type H shows a CMOS output stage. It features a pull-up resistor connected to a 'Pull-up control' input. The output node is connected to a 'Digital output' and also to a network of inputs: a resistor 'R' leading to a 'CMOS hysteresis input' (represented by a hysteresis symbol), an 'Automotive input' (represented by a hysteresis symbol), and a 'Standby control' input. The output stage consists of a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch) connected in a push-pull configuration.</p>	<ul style="list-style-type: none"> ■ With I²C, general-purpose I/O port ■ CMOS level output I_{OH}=-3mA, I_{OL}=3mA (at I²C output) I_{OH}=-2/-5mA, I_{OL}=2/5mA (other than above) ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7V_{cc}/0.3V_{cc}) ■ Automotive input (0.8V_{cc}/0.5V_{cc})
I	<p>The diagram for Type I shows an open drain I/O configuration. It features a pull-up resistor connected to a 'Digital output' node. The output node is also connected to a 'TTL schmitt input' (represented by a hysteresis symbol). The output stage consists of an N-channel MOSFET (N-ch) connected to ground.</p>	<p>Open drain I/O</p>

Type	Circuit	Remarks
K	<p>The diagram for Type K shows a pull-up control circuit with a resistor and two P-ch MOSFETs. The digital output is connected to a CMOS inverter. The FlexRay input is connected to a resistor R and a CMOS inverter. The Automotive input is connected to a resistor R and a CMOS inverter. The Standby control is connected to a CMOS inverter. The Analog output is connected to a CMOS inverter.</p>	<ul style="list-style-type: none"> ■ With analog output, general-purpose I/O port ■ CMOS level output $I_{OH}=-2/-4mA$, $I_{OL}=2/4mA$ ■ With 50 kΩ pull-up resistor control ■ FlexRay input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)
L	<p>The diagram for Type L is identical to Type K, showing a pull-up control circuit with a resistor and two P-ch MOSFETs. The digital output is connected to a CMOS inverter. The FlexRay input is connected to a resistor R and a CMOS inverter. The Automotive input is connected to a resistor R and a CMOS inverter. The Standby control is connected to a CMOS inverter. The Analog output is connected to a CMOS inverter.</p>	<ul style="list-style-type: none"> ■ With analog output, general-purpose I/O port ■ CMOS level output $I_{OH}=-2/-4mA$, $I_{OL}=2/4mA$ ■ With 50 kΩ pull-up resistor control ■ FlexRay input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. ■ Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.

Type	Circuit	Remarks
M		<ul style="list-style-type: none"> ■ With D/A converter output, general-purpose I/O port ■ CMOS level output $I_{OH} = -2/-5\text{mA}$, $I_{OL} = 2/5\text{mA}$ ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7V_{cc}/0.3V_{cc}) ■ Automotive input (0.8V_{cc}/0.5V_{cc})

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPJ junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

The latch-up prevention and pin processing are explained below.

■ For latch-up prevention

If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC and VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supplies (AVCC0, AVCC1, AVRH0, AVRH1) and analog input must not exceed the digital power supply (VCC5) when the power supply to the analog system is turned on or off.

In the correct power-on sequence, turn on the digital power supply voltage (VCC5) and analog power supply voltages (AVCC0, AVCC1, AVRH0, AVRH1) simultaneously. Alternatively, turn on the digital power supply voltage (VCC5) first, and then turn on the analog power supplies (AVCC0, AVCC1, AVRH0, AVRH1).

■ Treatment of unused pins

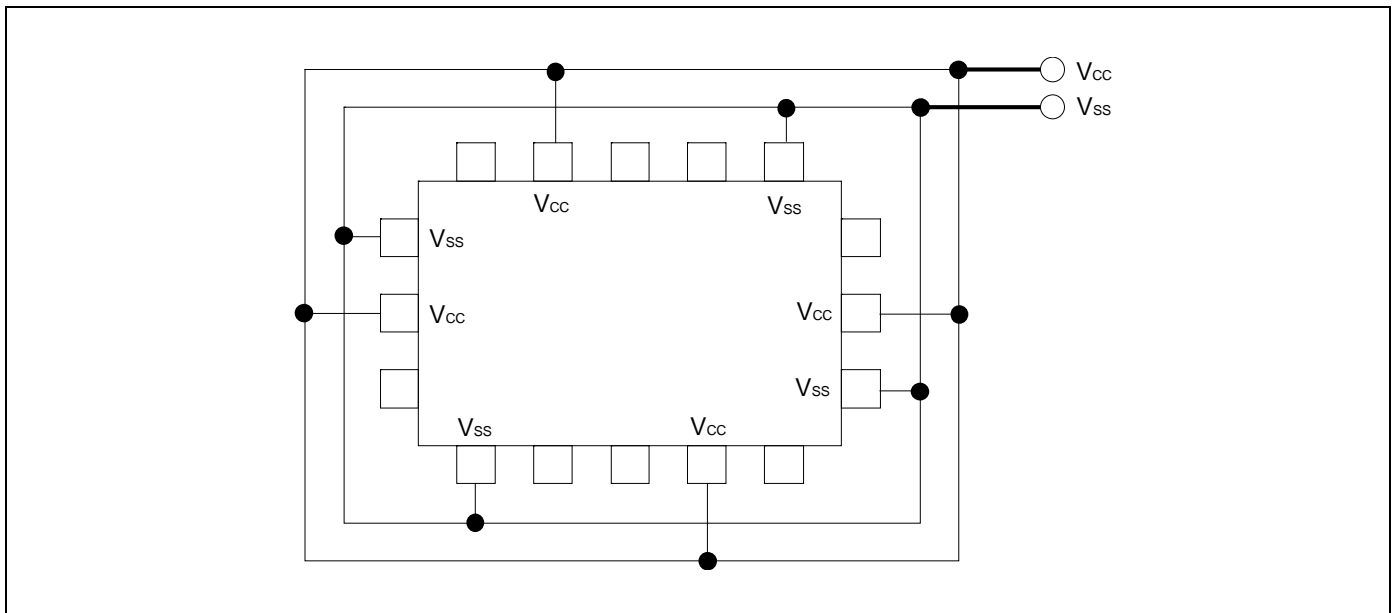
If unused input pins are left open, they may cause a permanent damage to the device due to device malfunction or latch-up. Connect a 2kΩ or higher resistor to each of unused input pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

■ Power supply pins

The device is designed to ensure that if the device contains multiple VCC or VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in following figure, all VSS power supply pins must be treated in the similar way. If multiple VCC or VSS systems are connected, the device cannot operate correctly even within the guaranteed operating range.

■ Power Supply Input Pins



The power supply pins should be connected to VCC and VSS of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC and VSS pins.

■ Crystal oscillation circuit

An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

■ Mode pin (MD[1:0])

Connect the MD[1:0] mode pin to the VCC or VSS pin directly.

To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

■ During power-on

To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on.

■ Notes during PLL clock operation

When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self oscillator circuit built in the PLL. This operation is not guaranteed.

■ Treatment of A/D converter power supply pins

Connect the pins to have AVCC0 = AVCC1 = AVRHO = AVRH1 = VCC,

AVSS0/AVRL0 = AVSS1/AVRL1 = VSS even if the A/D converter is not used.

■ Note on using external clock

The external clock is unsupported.

External direct clock input cannot use.

■ Power-on sequence of A/D converter power supply analog inputs

Be sure to turn on the digital power supply (VCC5) first, and then turn on the A/D converter power supplies (AVCC0, AVCC1, AVRHO, AVRH1, AVRL0, AVRL1) and analog inputs (AN0 to AN14, AN16 to AN23). Also, turn off the A/D converter power supplies (AVCC0, AVCC1, AVRHO, AVRH1, AVRL0, AVRL1) and analog inputs (AN0 to AN14, AN16 to AN23) first, and then turn off the digital power supply (VCC5). When the AVRHO and AVRH1 pin voltages are turned on or off, they must not exceed AVCC0 and AVCC1. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVCC0 or AVCC1. (However, the analog power supply voltage and digital power supply voltage can be turned on or off simultaneously.)

■ Treatment of C pin

This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

■ Function Switching of a Multiplexed Port

To switch between the port function and the multiplexed pin function, use the PFR (port function register). For details, see "I/O PORTS" in Hardware Manual.

■ Low-power Consumption Mode

To set Sleep mode / Watch mode / Stop mode (power-off) / Stop mode (power-off), see the section "Launching Sleep mode / Watch mode / Stop mode" or "Launching Watch mode (power-off) / Stop mode (power-off)" of "POWER CONSUMPTION CONTROL" in Hardware Manual, and follow the procedures.

Do not perform the following when using a monitor debugger.

- Do not set a break point for the low-power consumption transition program.
- Do not execute an operation step for the low-power consumption transition program.

■ Notes When Writing Data in a Register Having the Status Flag

When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, take care not to clear its status flag erroneously.

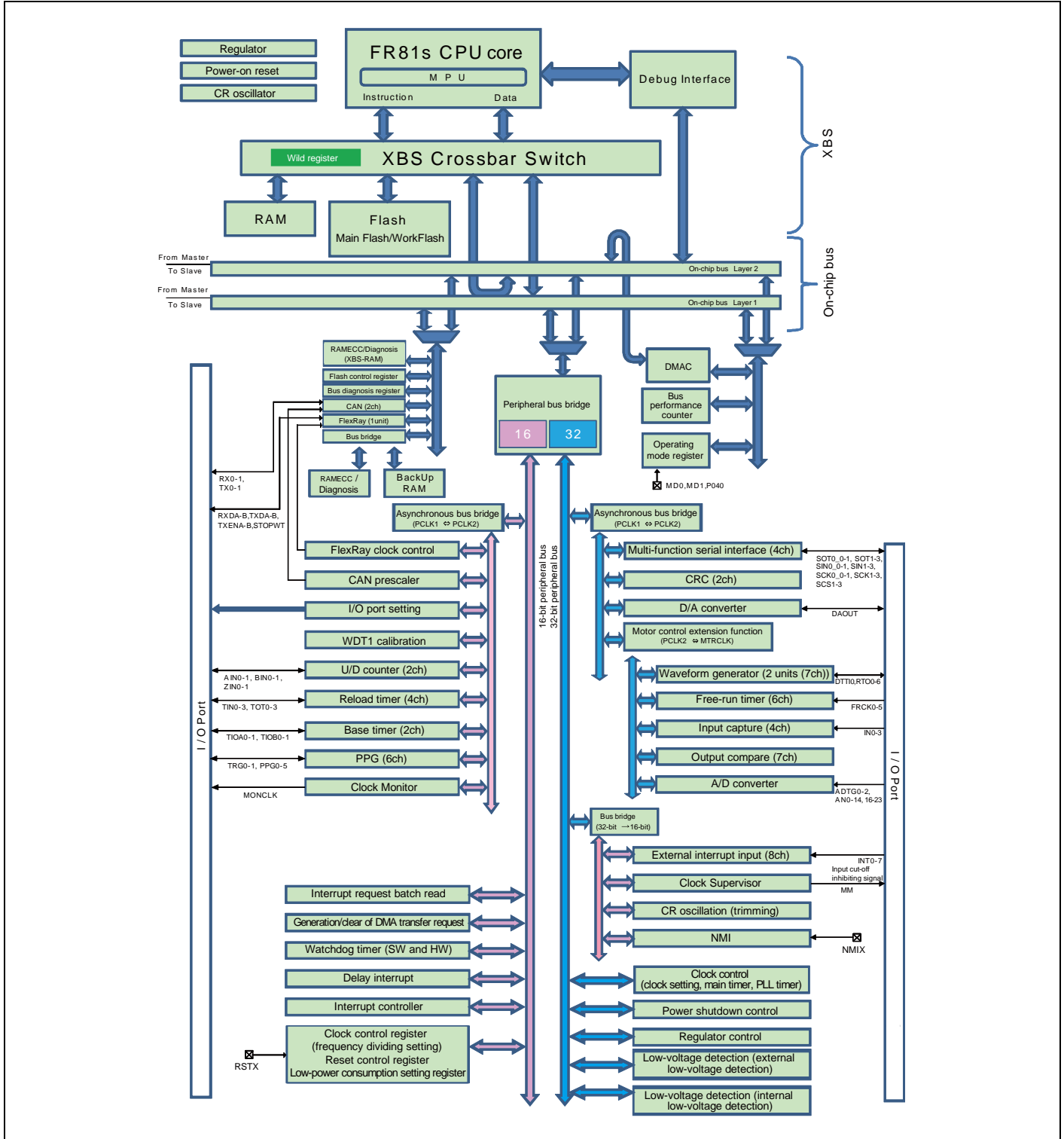
The program must be written not to clear the flag to the status bit, and to set the control bits to have the desired value.

Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) The Byte, Half-word, or Word access must be used to write data in the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

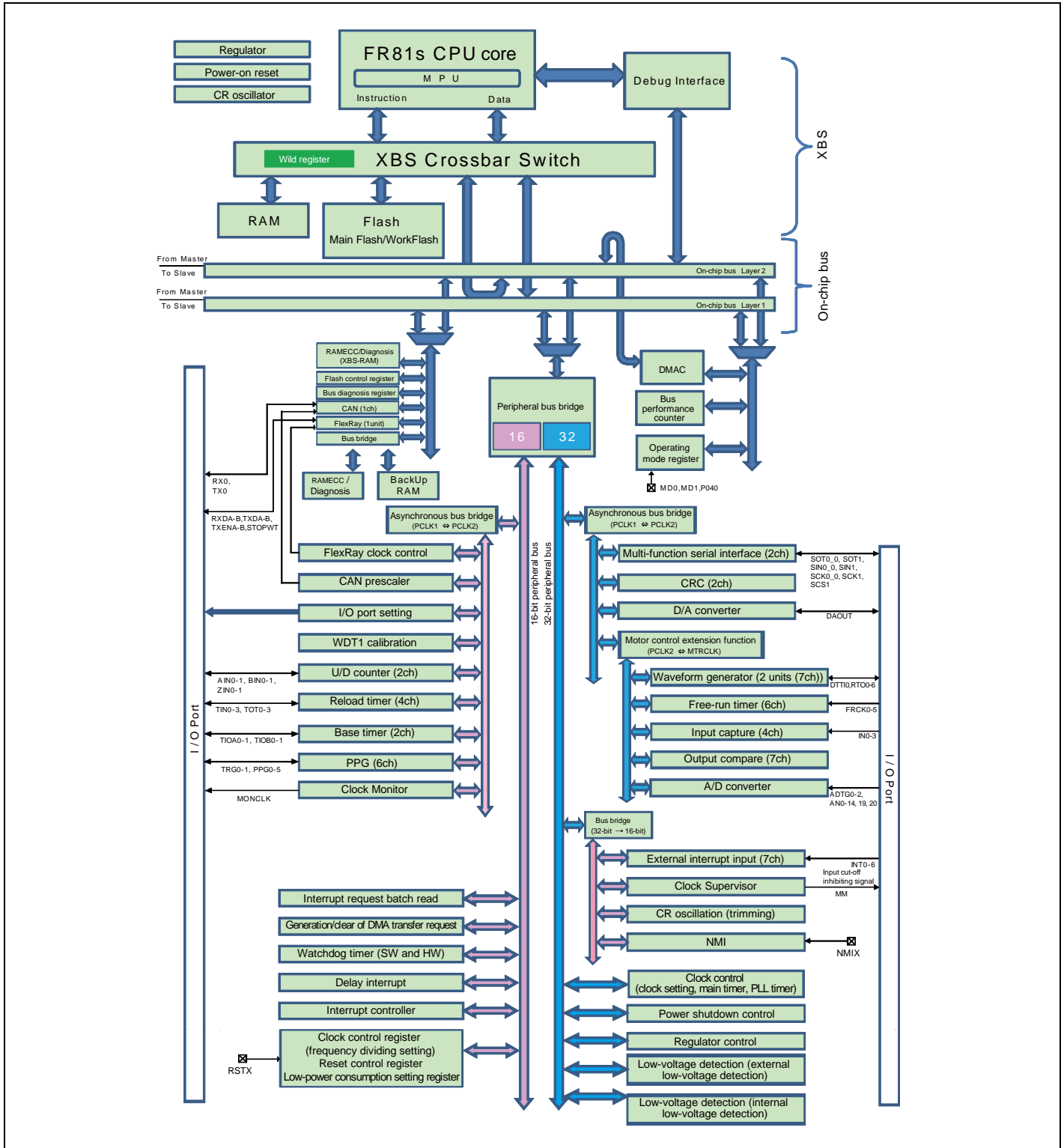
Note: These points can be ignored because the bit instructions already take the points into consideration for registers that support read-modify-write (RMW) operations. These points must be considered when using the bit instructions for registers that do not support RMW operations.

7. Block Diagram

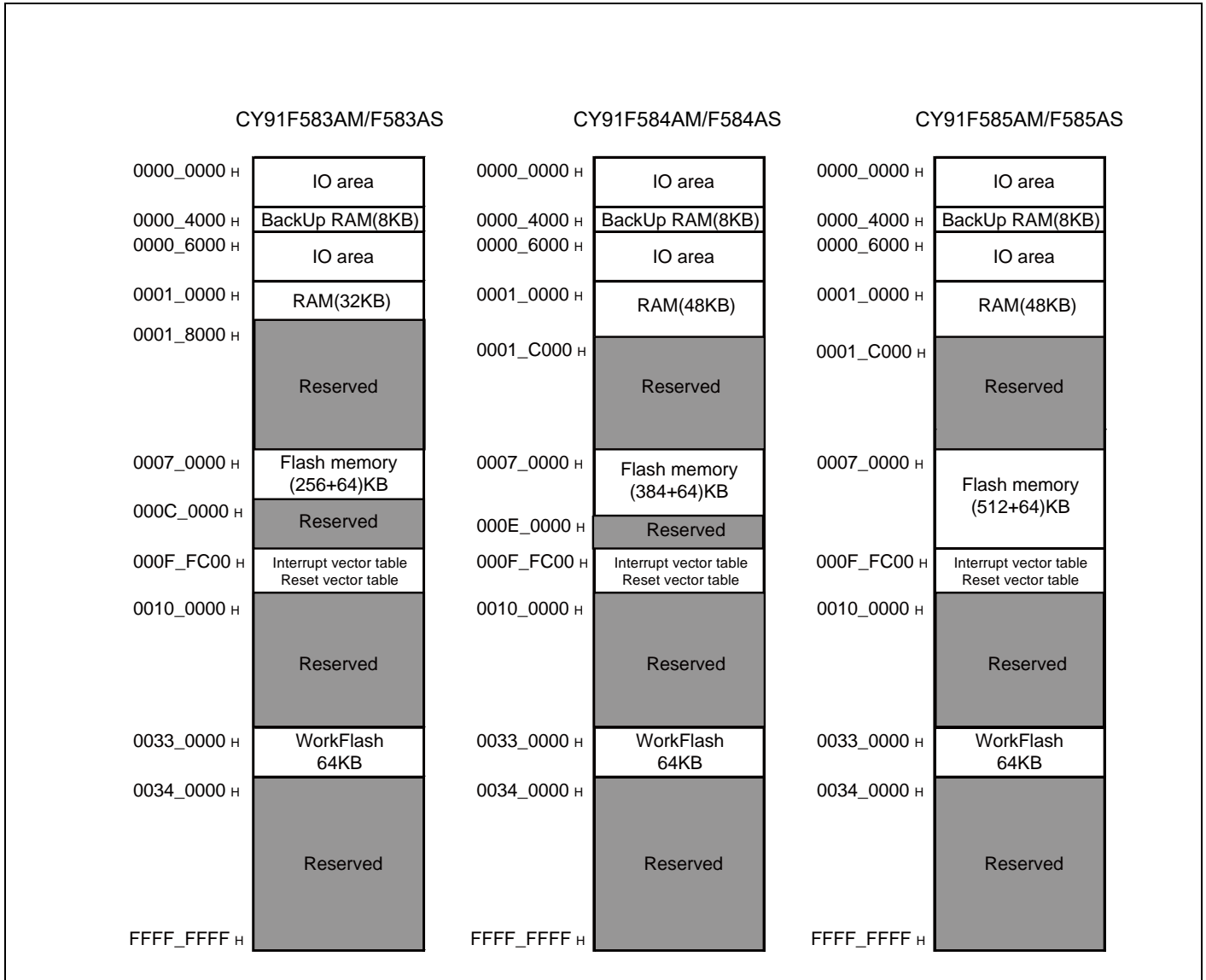
■ CY91F583AM/F584AM/F585AM



■ CY91F583AS/F584AS/F585AS



8. Memory Map



9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map

Read/Write attribute (R: Read W: Write)

Address	Address offset value/Register name				Block
	+ 0	+ 1	+ 2	+ 3	
000090 _H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] B,H,W 00000000 00000000		Base timer 1
000094 _H	-	BT1STC [R/W] B 00000000	-	-	
000098 _H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
00009C _H	BTSEL [R/W] B ----0000	-	BTSSSR [W] B, H -----11		
0000A0 _H	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D converter
0000A4 _H	ADCS1 [R/W] B,H,W 00000000	ADCS0 [R/W] B,H,W 00000000	ADCR1 [R] B,H,W ----XX	ADCR0 [R] B,H,W XXXXXXXX	
0000A8 _H	ADCT1 [R/W] B,H,W 00010000	ADCT0 [R/W] B,H,W 00101100	ADSCH [R/W] B,H,W --0000	ADECH [R/W] B,H,W --0000	

Data access attribute
 B: Byte
 H: Half-word
 W: Word
(Note)
 The access by the data access attribute not described is disabled.

Initial register value after reset

The initial register values after reset are indicated as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- "*": Initial value "0" or "1" according to the setting

Note:

It is prohibited to access addresses not described here.

■ CY91F583AM/F584AM/F585AM

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000000 _H	PDR00[R/W] B,H,W XXXXXXXXXX	PDR01[R/W] B,H,W XXXXXXXXXX	PDR02[R/W] B,H,W XXXXXXXXXX	PDR03[R/W] B,H,W XXXXXXXXXX	Port data register
000004 _H	PDR04[R/W] B,H,W XXXXXXXXXX	PDR05[R/W] B,H,W -XXXXXXXXX	PDR06[R/W] B,H,W -XXXXXXXXX	PDR07[R/W] B,H,W ----XXX	
000008 _H	PDR08[R/W] B,H,W XXXXXXXXXX	PDR09[R/W] B,H,W XXXXXXXXXX	PDR10[R/W] B,H,W ----XXX	-	
00000C _H	-	-	-	-	
000010 _H 000038 _H	-	-	-	-	Reserved
00003C _H	WDTCR0[R/W] B,H,W -0--0000	WDT CPR0[W] B,H,W 00000000	WDT CR1[R] B,H,W ----0010	WDT CPR1[W] B,H,W 00000000	Watchdog timer [S]
000040 _H	-	-	-	-	Reserved
000044 _H	DICR[R/W] B -----0	-	-	-	Delay interrupt
000048 _H 00005C _H	-	-	-	-	Reserved
000060 _H	TMRLRA0[R/W] H XXXXXXXXXX XXXXXXXX		TMR0[R] H XXXXXXXXXX XXXXXXXX		Reload timer 0
000064 _H	TMRLRB0[R/W] H XXXXXXXXXX XXXXXXXX		TMCSR0[R/W] B,H,W 00000000 0-000000		
000068 _H 00007C _H	-	-	-	-	Reserved
000080 _H	BT0TMR[R] H 00000000 00000000		BT0TMCR[R/W] H -0000000 00000000		Base timer 0
000084 _H	BT0TMCR2[R/W] B -----0	BT0STC[R/W] B -0-0-0-0	-	-	
000088 _H	BT0PCSR/BT0PRL[R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
00008C _H	-	-	-	-	
000090 _H	BT1TMR[R] H 00000000 00000000		BT1TMCR[R/W] H -0000000 00000000		Base timer 1
000094 _H	BT1TMCR2[R/W] B -----0	BT1STC[R/W] B -0-0-0-0	-	-	
000098 _H	BT1PCSR/BT1PRL[R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF[R/W] H 00000000 00000000		
00009C _H	BTSEL01[R/W] B ----0000	-	BTSSSR[W] B,H -----11		Base timer 0,1
0000A0 _H 0000FC _H	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000100 _H	TMRLRA1[R/W] H XXXXXXXX XXXXXXXX		TMR1[R] H XXXXXXXX XXXXXXXX		Reload timer 1
000104 _H	TMRLRB1[R/W] H XXXXXXXX XXXXXXXX		TMCSR1[R/W] B,H,W 00000000 0-000000		
000108 _H	TMRLRA2[R/W] H XXXXXXXX XXXXXXXX		TMR2[R] H XXXXXXXX XXXXXXXX		Reload timer 2
00010C _H	TMRLRB2[R/W] H XXXXXXXX XXXXXXXX		TMCSR2[R/W] B,H,W 00000000 0-000000		
000110 _H	TMRLRA3[R/W] H XXXXXXXX XXXXXXXX		TMR3[R] H XXXXXXXX XXXXXXXX		Reload timer 3
000114 _H	TMRLRB3[R/W] H XXXXXXXX XXXXXXXX		TMCSR3[R/W] B,H,W 00000000 0-000000		
000118 _H 00011C _H	-	-	-	-	Reserved
000120 _H	IRPR0H[R] B,H,W 00-----	IRPR0L[R] B,H,W 00-----	IRPR1H[R] B,H,W 00-----	IRPR1L[R] B,H,W -----	Interrupt request batch read register
000124 _H	IRPR2H[R] B,H,W -----	IRPR2L[R] B,H,W *5 0000----	IRPR3H[R] B,H,W 00-----	IRPR3L[R] B,H,W 00-----	
000128 _H	IRPR4H[R] B,H,W 00-----	IRPR4L[R] B,H,W 000000--	IRPR5H[R] B,H,W 00-----	IRPR5L[R] B,H,W 00-----	
00012C _H	IRPR6H[R] B,H,W 0000----	IRPR6L[R] B,H,W 00-----	IRPR7H[R] B,H,W 00-----	IRPR7L[R] B,H,W -----	
000130 _H	IRPR8H[R] B,H,W -----	IRPR8L[R] B,H,W 00-----	IRPR9H[R] B,H,W 00-----	IRPR9L[R] B,H,W 00-----	
000134 _H	IRPR10H[R] B,H,W 00-----	IRPR10L[R] B,H,W 00-----	IRPR11H[R] B,H,W 00-----	IRPR11L[R] B,H,W 0000000-	
000138 _H	IRPR12H[R] B,H,W 0000000-	IRPR12L[R] B,H,W 00000000	IRPR13H[R] B,H,W 0000000-	IRPR13L[R] B,H,W 00000000	
00013C _H	IRPR14H[R] B,H,W 00-----	IRPR14L[R] B,H,W 00-----	IRPR15H[R] B,H,W 00000000	IRPR15L[R] B,H,W 0000----	
000140 _H	IRPR16H[R] B,H,W 00-----	IRPR16L[R] B,H,W 00-----	IRPR17H[R] B,H,W 00-----	IRPR17L[R] B,H,W -----	
000144 _H	IRPR18H[R] B,H,W -----	IRPR18L[R] B,H,W 000000--	-	-	
000148 _H 0001FC _H	-	-	-	-	Reserved
000200 _H	PCN0[R/W] B,H,W 00000000 000000-0		PCSR0[W] H,W XXXXXXXX XXXXXXXX		PPG0
000204 _H	PDUT0[W] H,W XXXXXXXX XXXXXXXX		PTMR0[R] H,W 11111111 11111111		
000208 _H	PCN1[R/W] B,H,W 00000000 000000-0		PCSR1[W] H,W XXXXXXXX XXXXXXXX		PPG1

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00020C _H	PDUT1[W] H,W XXXXXXXX XXXXXXXX		PTMR1[R] H,W 11111111 11111111		PPG2
000210 _H	PCN2[R/W] B,H,W 00000000 000000-0		PCSR2[W] H,W XXXXXXXX XXXXXXXX		
000214 _H	PDUT2[W] H,W XXXXXXXX XXXXXXXX		PTMR2[R] H,W 11111111 11111111		PPG3
000218 _H	PCN3[R/W] B,H,W 00000000 000000-0		PCSR3[W] H,W XXXXXXXX XXXXXXXX		
00021C _H	PDUT3[W] H,W XXXXXXXX XXXXXXXX		PTMR3[R] H,W 11111111 11111111		PPG4
000220 _H	PCN4[R/W] B,H,W 00000000 000000-0		PCSR4[W] H,W XXXXXXXX XXXXXXXX		
000224 _H	PDUT4[W] H,W XXXXXXXX XXXXXXXX		PTMR4[R] H,W 11111111 11111111		PPG5
000228 _H	PCN5[R/W] B,H,W 00000000 000000-0		PCSR5[W] H,W XXXXXXXX XXXXXXXX		
00022C _H	PDUT5[W] H,W XXXXXXXX XXXXXXXX		PTMR5[R] H,W 11111111 11111111		Reserved
000230 _H 0002BC _H	-		-		
0002C0 _H	GTRS0[R/W] B,H,W -0000000 -0000000		GTRS1[R/W] B,H,W -0000000 -0000000		PPG Control
0002C4 _H	GTRS2[R/W] B,H,W -0000000 -0000000		-		
0002C8 _H	-		-		
0002CC _H	-		-		
0002D0 _H	-		-		
0002D4 _H	-		-		
0002D8 _H	GTREN0[R/W] H,W ----- --000000		-		Reserved
0002DC _H	-		-		
0002E0 _H	-	GATEC0[R/W] B,H,W -----00	-	GATEC2[R/W] B,H,W -----00	PPG GATE Control
0002E4 _H	-	GATEC4[R/W] B,H,W -----00	-	-	
0002E8 _H	-	-	-	-	Reserved
0002EC _H	-	-	-	-	
0002F0 _H	RCRH0[W] H,W 00000000	RCRL0[W] B,H,W 00000000	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	U/D counter 0
0002F4 _H	CCR0[R/W] B,H 00000000 -0001000		-	CSR0[R] B 00000000	
0002F8 _H	RCRH1[W] H,W 00000000	RCRL1[W] B,H,W 00000000	UDCRH1[R] H,W 00000000	UDCRL1[R] B,H,W 00000000	U/D counter 1
0002FC _H	CCR1[R/W] B,H 00000000 -0001000		-	CSR1[R] B 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000300 _H	-				Reserved
000304 _H	-	-	-	-	Reserved
000308 _H	-				Reserved
00030C _H	-	-	-	-	
000310 _H	-	-	MPUCR[R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314 _H	-	-	-	-	
000318 _H	-				
00031C _H	-	-	-		
000320 _H	DPVAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324 _H	-	-	DPVSR[R/W] H ----- 00000-0		
000328 _H	DEAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00032C _H	-	-	DESR[R/W] H ----- 00000-0		
000330 _H	PABR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334 _H	-	-	PACR0[R/W] H 000000-0 00000--0		
000338 _H	PABR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00033C _H	-	-	PACR1[R/W] H 000000-0 00000--0		
000340 _H	PABR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344 _H	-	-	PACR2[R/W] H 000000-0 00000--0		
000348 _H	PABR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00034C _H	-	-	PACR3[R/W] H 000000-0 00000--0		
000350 _H	PABR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000354 _H	-	-	PACR4[R/W] H 000000-0 00000--0		
000358 _H	PABR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00035C _H	-	-	PACR5[R/W] H 000000-0 00000--0		
000360 _H	PABR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364 _H	-	-	PACR6[R/W] H 000000-0 00000--0		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000368 _H	PABR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only the CPU can access this area)
00036C _H	-	-	PACR7[R/W] H 000000-0 00000--0		
000370 _H	-				Reserved [S]
000374 _H	-				
000378 _H	-				
00037C _H	-	-	-		
000380 _H	-				
000384 _H	-	-	-		
000388 _H	-				
00038C _H	-	-	-		
000390 _H	-				
000394 _H	-	-	-		
000398 _H	-				Reserved [S]
00039C _H	-	-	-		
0003A0 _H	-				
0003A4 _H	-	-	-		
0003A8 _H	-				
0003AC _H	-	-	-		
0003B0 _H 0003CC _H	-	-	-	-	Reserved [S]
0003D0 _H	-				Reserved [S]
0003D4 _H	-				
0003D8 _H	-				
0003DC _H	-				
0003E0 _H 0003FC _H	-	-	-	-	Reserved [S]
000400 _H	ICSEL0[R/W] B,H,W ----000	ICSEL1[R/W] B,H,W -----0	ICSEL2[R/W] B,H,W -----0	ICSEL3[R/W] B,H,W -----0	Generation and clear of DMA transfer request
000404 _H	ICSEL4[R/W] B,H,W -----0	ICSEL5[R/W] B,H,W -----0	ICSEL6[R/W] B,H,W -----0	ICSEL7[R/W] B,H,W ----000	
000408 _H	ICSEL8[R/W] B,H,W -----0	ICSEL9[R/W] B,H,W -----0	ICSEL10[R/W] B,H,W -----00	ICSEL11[R/W] B,H,W -----0	
00040C _H	ICSEL12[R/W] B,H,W -----0	ICSEL13[R/W] B,H,W -----0	ICSEL14[R/W] B,H,W -----0	ICSEL15[R/W] B,H,W -----0	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000410 _H	ICSEL16[R/W] B,H,W -----0	ICSEL17[R/W] B,H,W -----0	ICSEL18[R/W] B,H,W -----0	ICSEL19[R/W] B,H,W -----0	Generation and clear of DMA transfer request
000414 _H	ICSEL20[R/W] B,H,W -----0	ICSEL21[R/W] B,H,W ----000	ICSEL22[R/W] B,H,W ----000	ICSEL23[R/W] B,H,W ----000	
000418 _H	ICSEL24[R/W] B,H,W ----000	ICSEL25[R/W] B,H,W ----000	ICSEL26[R/W] B,H,W -----0	ICSEL27[R/W] B,H,W -----0	
00041C _H	-	-	-	-	
000420 _H	-	-	-	-	
000424 _H 00043C _H	-	-	-	-	Reserved
000440 _H	ICR00[R/W] B,H,W ---11111	ICR01[R/W] B,H,W ---11111	ICR02[R/W] B,H,W ---11111	ICR03[R/W] B,H,W ---11111	Interrupt controller [S]
000444 _H	ICR04[R/W] B,H,W ---11111	ICR05[R/W] B,H,W ---11111	ICR06[R/W] B,H,W ---11111	ICR07[R/W] B,H,W ---11111	
000448 _H	ICR08[R/W] B,H,W ---11111	ICR09[R/W] B,H,W ---11111	ICR10[R/W] B,H,W ---11111	ICR11[R/W] B,H,W ---11111	
00044C _H	ICR12[R/W] B,H,W ---11111	ICR13[R/W] B,H,W ---11111	ICR14[R/W] B,H,W ---11111	ICR15[R/W] B,H,W ---11111	
000450 _H	ICR16[R/W] B,H,W ---11111	ICR17[R/W] B,H,W ---11111	ICR18[R/W] B,H,W ---11111	ICR19[R/W] B,H,W ---11111	
000454 _H	ICR20[R/W] B,H,W ---11111	ICR21[R/W] B,H,W ---11111	ICR22[R/W] B,H,W ---11111	ICR23[R/W] B,H,W ---11111	
000458 _H	ICR24[R/W] B,H,W ---11111	ICR25[R/W] B,H,W ---11111	ICR26[R/W] B,H,W ---11111	ICR27[R/W] B,H,W ---11111	
00045C _H	ICR28[R/W] B,H,W ---11111	ICR29[R/W] B,H,W ---11111	ICR30[R/W] B,H,W ---11111	ICR31[R/W] B,H,W ---11111	
000460 _H	ICR32[R/W] B,H,W ---11111	ICR33[R/W] B,H,W ---11111	ICR34[R/W] B,H,W ---11111	ICR35[R/W] B,H,W ---11111	
000464 _H	ICR36[R/W] B,H,W ---11111	ICR37[R/W] B,H,W ---11111	ICR38[R/W] B,H,W ---11111	ICR39[R/W] B,H,W ---11111	
000468 _H	ICR40[R/W] B,H,W ---11111	ICR41[R/W] B,H,W ---11111	ICR42[R/W] B,H,W ---11111	ICR43[R/W] B,H,W ---11111	
00046C _H	ICR44[R/W] B,H,W ---11111	ICR45[R/W] B,H,W ---11111	ICR46[R/W] B,H,W ---11111	ICR47[R/W] B,H,W ---11111	
000470 _H 00047C _H	-	-	-	-	
000480 _H	RSTRR[R] B,H,W XXXX--XX	RSTCR[R/W] B,H,W 111----0	STBCR[R/W] B,H,W 000---11*	-	Reset control [S] Power consumption control [S] * Writing to STBCR by DMA is disabled.
000484 _H	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000488 _H	DIVR0[R/W] B,H,W 000-----	-	DIVR2[R/W] B,H,W 0011----	-	Clock control [S]
00048C _H	-	-	-	-	Reserved [S]
000490 _H	IORR0[R/W] B,H,W -0000000	IORR1[R/W] B,H,W -0000000	IORR2[R/W] B,H,W -0000000	IORR3[R/W] B,H,W -0000000	DMA transfer request from a peripheral [S]
000494 _H	IORR4[R/W] B,H,W -0000000	IORR5[R/W] B,H,W -0000000	IORR6[R/W] B,H,W -0000000	IORR7[R/W] B,H,W -0000000	
000498 _H	-	-	-	-	
00049C _H	-	-	-	-	
0004A0 _H	-	-	-	-	Reserved
0004A4 _H	CANPRE[R/W] B,H,W ---00000	-	-	-	CAN prescaler
0004A8 _H 0004AC _H	-	-	-	-	Reserved
0004B0 _H	-	-	-	-	Reserved
0004B4 _H 0004C0 _H	-	-	-	-	Reserved
0004C4 _H	CUCR1[R/W] B,H,W ----- --0--00		CUTD1[R/W] B,H,W 11000011 01010000		WDT1 calibration
0004C8 _H	CUTR1[R] B,H,W ----- 00000000 00000000 00000000				
0004CC _H 0004DC _H	-	-	-	-	Reserved
0004E0 _H	-	-	CSCFG[R/W] B,H,W ---0----	CMCFG[R/W] B,H,W 00000000	Clock monitor
0004E4 _H	-	-	-	-	
0004E8 _H	PLL2DIVM[R/W] B,H,W ----0000	PLL2DIVN[R/W] B,H,W -0000000	PLL2DIVG[R/W] B,H,W ----0000	PLL2MULG[R/W] B,H,W 00000000	FlexRay clock control *5
0004EC _H	PLL2CTRL[R/W] B,H,W ----0000	PLL2DIVK[R/W] B,H,W -----0	CLKR2[R/W] B,H,W 000--000	-	
0004F0 _H 0004FC _H	-	-	-	-	Reserved
000500 _H	-	-	-	-	Reserved
000504 _H	-	-	-	-	Reserved
000508 _H 00050C _H	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000510 _H	CSELR[R/W] B,H,W -0----00	CMONR[R] B,H,W -01---00	MTMCR[R/W] B,H,W 00001111	-	Clock control [S]
000514 _H	PLLCR[R/W] B,H,W 00-00000 11110000	-	CSTBR[R/W] B,H,W ----0000	PTMCR[R/W] B,H,W 00-----	
000518 _H	-	-	CPUAR[R/W] B,H,W 0---XXXX	-	Reset [S]
00051C _H	-	-	-	-	Reserved [S]
000520 _H	CCPSELR[R/W] B,H,W -----0	-	-	CCPSDIVR[R/W] B,H,W -000-000	Clock control 2
000524 _H	-	CCPLLFBR[R/W] B,H,W -0000000	CCSSFBR0[R/W] B,H,W --000000	CCSSFBR1[R/W] B,H,W ---00000	
000528 _H	-	CCSSCCR0[R/W] B,H,W ----0000	CCSSCCR1[R/W] B,H,W 000-----	-	
00052C _H	-	CCCGRCR0[R/W] B,H,W 00----00	CCCGRCR1[R/W] B,H,W 00000000	CCCGRCR2[R/W] B,H,W 00000000	
000530 _H	-	-	CCPMUCR0[R/W] B,H,W 0-----00	CCPMUCR1[R/W] B,H,W 0--00000	
000534 _H	-	-	-	-	
000538 _H	-	-	-	-	
00053C _H	-	-	-	-	
000540 _H 00054C _H	-	-	-	-	Reserved
000550 _H	EIRR0[R/W] B,H,W XXXXXXXX	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000	-	External interrupt (INT0 to 7)
000554 _H 000568 _H	-	-	-	-	Reserved
00056C _H	-	CSVCR[R/W] B -0--1--0	-	-	CSV
000570 _H	CRTR[R/W] B,H,W 01111111	-	-	-	WDT1 calibration (trimming)
000574 _H 00057C _H	-	-	-	-	Reserved
000580 _H	REGSEL[R/W] B,H,W 01--110-	-	-	-	Regulator control
000584 _H	LVD5R[R/W] B,H,W -----1	LVD5F[R/W] B,H,W 001100-1	LVD[R/W] B,H,W 01000--0	-	Low-voltage detection

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000588 _H 00058C _H	-	-	-	-	Reserved
000590 _H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00---	PWRTMCTL[R/W] B,H,W -----011	-	PMU
000594 _H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00----	-	
000598 _H	-	-	-	-	
00059C _H	-	-	-	-	
0005A0 _H 0005FC _H	-	-	-	-	Reserved
000600 _H 00060C _H	-	-	-	-	Reserved [S]
000610 _H 00063C _H	-	-	-	-	Reserved [S]
000640 _H 00064C _H	-	-	-	-	Reserved [S]
000650 _H 00067C _H	-	-	-	-	Reserved [S]
000680 _H 00068C _H	-	-	-	-	Reserved [S]
000690 _H 0006BC _H	-	-	-	-	Reserved [S]
0006C0 _H 0006CC _H	-	-	-	-	Reserved [S]
0006D0 _H 0006F0 _H	-	-	-	-	Reserved
0006F4 _H	-				Reserved
0006F8 _H 0006FC _H	-	-	-	-	Reserved
000700 _H	-				Reserved
000704 _H 00070C _H	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000710 _H	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	-	Bus performance counter
000714 _H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718 _H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
00071C _H	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				
000720 _H 0007F8 _H	-	-	-	-	Reserved
0007FC _H	BMODR[R] B,H,W XXXXXXXX	-	-	-	Operation mode
000800 _H 00083C _H	-	-	-	-	Reserved [S]
000840 _H	FCTLR[R/W] H -0--1000 0--0----		-	FSTR[R/W] B ----001	Flash memory register [S]
000844 _H	-	-	-	-	Reserved [S]
000848 _H 000854 _H	-	-	-	-	Reserved [S]
000858 _H	-	-	WREN[R/W] H 00000000 00000000		Wild register [S]
00085C _H 00087C _H	-	-	-	-	Reserved [S]
000880 _H	WRAR0[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884 _H	WRDR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888 _H	WRAR01[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
00088C _H	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890 _H	WRAR02[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
000894 _H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898 _H	WRAR03[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
00089C _H	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008A0 _H	WRAR04[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0008A4 _H	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild register [S]
0008A8 _H	WRAR05[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008AC _H	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B0 _H	WRAR06[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008B4 _H	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B8 _H	WRAR07[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008BC _H	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C0 _H	WRAR08[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008C4 _H	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C8 _H	WRAR09[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008CC _H	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D0 _H	WRAR10[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008D4 _H	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D8 _H	WRAR11[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008DC _H	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E0 _H	WRAR12[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008E4 _H	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E8 _H	WRAR13[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008EC _H	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F0 _H	WRAR14[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008F4 _H	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F8 _H	WRAR15[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008FC _H	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000900 _H 000BF8 _H	-	-	-	-	Reserved
000BFC _H	-		UER[W] B,H,W -----X		OCDU
000C00 _H	DCCR0[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
000C04 _H	DCSR0[R/W] H 0-----000		DTCR0[R/W] H 00000000 00000000		
000C08 _H	DSAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C0C _H	DDAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C10 _H	DCCR1[R/W] W 0----000 --00--00 00000000 0-000000				
000C14 _H	DCSR1[R/W] H 0-----000		DTCR1[R/W] H 00000000 00000000		
000C18 _H	DSAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C1C _H	DDAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C20 _H	DCCR2[R/W] W 0----000 --00--00 00000000 0-000000				
000C24 _H	DCSR2[R/W] H 0-----000		DTCR2[R/W] H 00000000 00000000		
000C28 _H	DSAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C2C _H	DDAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C30 _H	DCCR3[R/W] W 0----000 --00--00 00000000 0-000000				
000C34 _H	DCSR3[R/W] H 0-----000		DTCR3[R/W] H 00000000 00000000		
000C38 _H	DSAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C3C _H	DDAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C40 _H	DCCR4[R/W] W 0----000 --00--00 00000000 0-000000				
000C44 _H	DCSR4[R/W] H 0-----000		DTCR4[R/W] H 00000000 00000000		
000C48 _H	DSAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C4C _H	DDAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000C50 _H	DCCR5[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
000C54 _H	DCSR5[R/W] H 0----- 000		DTCR5[R/W] H 00000000 00000000		
000C58 _H	DSAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C5C _H	DDAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C60 _H	DCCR6[R/W] W 0----000 --00--00 00000000 0-000000				
000C64 _H	DCSR6[R/W] H 0----- 000		DTCR6[R/W] H 00000000 00000000		
000C68 _H	DSAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C6C _H	DDAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C70 _H	DCCR7[R/W] W 0----000 --00--00 00000000 0-000000				
000C74 _H	DCSR7[R/W] H 0----- 000		DTCR7[R/W] H 00000000 00000000		
000C78 _H	DSAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C7C _H	DDAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C80 _H 000DF0 _H	-	-	-	-	
000DF4 _H	-	-	DNMIR[R/W] B 0-----0	DILVR[R/W] B ---11111	
000DF8 _H	DMACR[R/W] W 0----- 0-----				
000DFC _H	-	-	-	-	
000E00 _H	DDR00[R/W] B,H 00000000	DDR01[R/W] B,H 00000000	DDR02[R/W] B,H 00000000	DDR03[R/W] B,H 00000000	Data direction register
000E04 _H	DDR04[R/W] B,H 00000000	DDR05[R/W] B,H -0000000	DDR06[R/W] B,H -0000000	DDR07[R/W] B,H ----000	
000E08 _H	DDR08[R/W] B,H 00000000	DDR09[R/W] B,H 00000000	DDR10[R/W] B,H ----000	-	
000E0C _H	-	-	-	-	
000E10 _H 000E1C _H	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000E20 _H	PFR00[R/W] B,H 00000000	PFR01[R/W] B,H 00000000	PFR02[R/W] B,H 00000000	PFR03[R/W] B,H 00000000	Port function register
000E24 _H	PFR04[R/W] B,H 00000000	PFR05[R/W] B,H -0000000	PFR06[R/W] B,H -0000000	PFR07[R/W] B,H ----000	
000E28 _H	PFR08[R/W] B,H 00000000	PFR09[R/W] B,H 00000000	PFR10[R/W] B,H ----000	-	
000E2C _H	-	-	-	-	
000E30 _H 000E3C _H	-	-	-	-	Reserved
000E40 _H	PDDR00[R] B,H,W XXXXXXXX	PDDR01[R] B,H,W XXXXXXXX	PDDR02[R] B,H,W XXXXXXXX	PDDR03[R] B,H,W XXXXXXXX	Input data direct read register
000E44 _H	PDDR04[R] B,H,W XXXXXXXX	PDDR05[R] B,H,W -XXXXXXXX	PDDR06[R] B,H,W -XXXXXXXX	PDDR07[R] B,H,W ----XXX	
000E48 _H	PDDR08[R] B,H,W XXXXXXXX	PDDR09[R] B,H,W XXXXXXXX	PDDR10[R] B,H,W ----XXX	-	
000E4C _H	-	-	-	-	
000E50 _H 000E5C _H	-	-	-	-	Reserved
000E60 _H	EPFR00[R/W] B,H -----00	EPFR01[R/W] B,H ---00000	EPFR02[R/W] B,H --000000	EPFR03[R/W] B,H --000000	Extended port function register
000E64 _H	-	-	EPFR06[R/W] B,H -----00	EPFR07[R/W] B,H ----0000	
000E68 _H	EPFR08[R/W] B,H *5 ----0000	EPFR09[R/W] B,H -----0	EPFR10[R/W] B,H -0000000	-	
000E6C _H	-	-	EPFR14[R/W] B,H --0-0-0-	-	
000E70 _H	-	-	-	-	
000E74 _H	-	-	-	-	
000E78 _H	-	-	-	-	
000E7C _H	-	-	-	-	
000E80 _H	-	-	-	-	
000E84 _H 000EBC _H	-	-	-	-	
000EC0 _H	PPER00[R/W] B,H 00000000	PPER01[R/W] B,H 00000000	PPER02[R/W] B,H 00000000	PPER03[R/W] B,H 00000000	Port pull-up/down enable register
000EC4 _H	PPER04[R/W] B,H 00000000	PPER05[R/W] B,H -0000000	PPER06[R/W] B,H -0000000	PPER07[R/W] B,H ----000	
000EC8 _H	PPER08[R/W] B,H 00000000	PPER09[R/W] B,H 00000000	PPER10[R/W] B,H ----000	-	
000ECC _H	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000ED0 _H 000EDC _H	-	-	-	-	Reserved
000EE0 _H	PILR00[R/W] B,H 11111111	PILR01[R/W] B,H 11111111	PILR02[R/W] B,H 11111111	PILR03[R/W] B,H 11111111	Port input level selection register
000EE4 _H	PILR04[R/W] B,H 11111111	PILR05[R/W] B,H -1111111	PILR06[R/W] B,H -1111111	PILR07[R/W] B,H ----111	
000EE8 _H	PILR08[R/W] B,H 11111111	PILR09[R/W] B,H 11111111	PILR10[R/W] B,H ----111	-	
000EEC _H	-	-	-	-	
000EF0 _H 000EFC _H	-	-	-	-	Reserved
000F00 _H 000F1C _H	-	-	-	-	Reserved
000F20 _H	PODR00[R/W] B,H 00000000	PODR01[R/W] B,H 00000000	PODR02[R/W] B,H 00000000	PODR03[R/W] B,H 00000000	Port output drive register
000F24 _H	PODR04[R/W] B,H 00000000	PODR05[R/W] B,H -0000000	PODR06[R/W] B,H -0000000	PODR07[R/W] B,H ----000	
000F28 _H	PODR08[R/W] B,H 00000000	PODR09[R/W] B,H 00000000	PODR10[R/W] B,H ----000	-	
000F2C _H	-	-	-	-	
000F30 _H 000F3C _H	-	-	-	-	Reserved
000F40 _H	PORTEN[R/W] B,H,W -----00	-	-	-	Port input enable register
000F44 _H	KEYCDR[R/W] H 00000000 00000000		-	-	Port key code
000F48 _H	ADERH[R/W] B,H ----- 11111111		ADERL[R/W] B,H -1111111 11111111		Analog input enable register
000F4C _H	DAER[R/W] B,H -----0	-	-	-	Analog output enable register
000F50 _H 000FFC _H	-	-	-	-	Reserved
001000 _H	SACR[R/W] B,H,W -----0	PICD[R/W] B,H,W ----0011	-	-	Synchronous/asyn chronous switch control
001004 _H 0010BC _H	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0010C0 _H	-	-	-	CRCCR[R/W] B,H,W -0000000	CRC arithmetic operation 0
0010C4 _H	CRCINIT[R/W] B,H,W 11111111 11111111 11111111 11111111				
0010C8 _H	CRCIN[R/W] B,H,W 00000000 00000000 00000000 00000000				
0010CC _H	CRCCR[R] B,H,W 11111111 11111111 11111111 11111111				
0010D0 _H	-	-	-	CRCCR1[R/W] B,H,W -0000000	CRC arithmetic operation 1
0010D4 _H	CRCINIT1[R/W] B,H,W 11111111 11111111 11111111 11111111				
0010D8 _H	CRCIN1[R/W] B,H,W 00000000 00000000 00000000 00000000				
0010DC _H	CRCCR1[R] B,H,W 11111111 11111111 11111111 11111111				
0010E0 _H 0010FC _H	-	-	-	-	Reserved
001100 _H	TCGS[R/W] B,H,W -----00	-	-	TCGSE[R/W] B,H,W --000000	Free-run timer simultaneous activation
001104 _H	CPCLRB0/CPCLR0[R/W] H,W 11111111 11111111		TCDT0[R/W] H,W 00000000 00000000		Free-run timer 0
001108 _H	TCCS0[R/W] B,H,W 00000000 01000000 ----0000 -----				
00110C _H	CPCLRB1/CPCLR1[R/W] H,W 11111111 11111111		TCDT1[R/W] H,W 00000000 00000000		Free-run timer 1
001110 _H	TCCS1[R/W] B,H,W 00000000 01000000 ----0000 -----				
001114 _H	CPCLRB2/CPCLR2[R/W] H,W 11111111 11111111		TCDT2[R/W] H,W 00000000 00000000		Free-run timer 2
001118 _H	TCCS2[R/W] B,H,W 00000000 01000000 ----0000 -----				
00111C _H	CPCLRB3/CPCLR3[R/W] H,W 11111111 11111111		TCDT3[R/W] H,W 00000000 00000000		Free-run timer 3
001120 _H	TCCS3[R/W] B,H,W 00000000 01000000 ----0000 -----				
001124 _H	CPCLRB4/CPCLR4[R/W] H,W 11111111 11111111		TCDT4[R/W] H,W 00000000 00000000		Free-run timer 4
001128 _H	TCCS4[R/W] B,H,W 00000000 01000000 ----0000 -----				
00112C _H	CPCLRB5/CPCLR5[R/W] H,W 11111111 11111111		TCDT5[R/W] H,W 00000000 00000000		Free-run timer 5
001130 _H	TCCS5[R/W] B,H,W 00000000 01000000 ----0000 -----				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001134 _H	FRS0[R/W] B,H,W ----- -000-000 -000-000 -000-000				Free-run timer selection
001138 _H	FRS1[R/W] B,H,W ----- -000-000 -000-000				
00113C _H	FRS2[R/W] B,H,W ----- -000-000 -000-000 -000-000				
001140 _H	-				
001144 _H	FRS4[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001148 _H	FRS5[R/W] B,H,W ----000 -000-000 -000-000 -000-000				
00114C _H	FRS6[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001150 _H	-				
001154 _H	OCCPB0/OCCP0[R/W] H,W 00000000 00000000		OCCPB1/OCCP1[R/W] H,W 00000000 00000000		Output compare 0/1
001158 _H	OCS01[R/W] B,H,W -110--00 00001100		-	OCMOD01[R/W] B,H,W -----00	
00115C _H	OCCPB2/OCCP2[R/W] H,W 00000000 00000000		OCCPB3/OCCP3[R/W] H,W 00000000 00000000		Output compare 2/3
001160 _H	OCS23[R/W] B,H,W -110--00 00001100		-	OCMOD23[R/W] B,H,W -----00	
001164 _H	OCCPB4/OCCP4[R/W] H,W 00000000 00000000		OCCPB5/OCCP5[R/W] H,W 00000000 00000000		Output compare 4/5
001168 _H	OCS45[R/W] B,H,W -110--00 00001100		-	OCMOD45[R/W] B,H,W -----00	
00116C _H	OCCPB6/OCCP6[R/W] H,W 00000000 00000000		OCCPB7/OCCP7[R/W] H,W 00000000 00000000		Output compare 6/7
001170 _H	OCS67[R/W] B,H,W -110--00 00001100		-	OCMOD67[R/W] B,H,W -----00	
001174 _H	OCCPB8/OCCP8[R/W] H,W 00000000 00000000		OCCPB9/OCCP9[R/W] H,W 00000000 00000000		Output compare 8/9
001178 _H	OCS89[R/W] B,H,W -110--00 00001100		-	OCMOD89[R/W] B,H,W -----00	
00117C _H	OCCPB10/OCCP10[R/W] H,W 00000000 00000000		OCCPB11/OCCP11[R/W] H,W 00000000 00000000		Output compare 10/11
001180 _H	OCS1011[R/W] B,H,W -110--00 00001100		-	OCMOD1011 [R/W] B,H,W -----00	
001184 _H	IPCP0[R] H,W 00000000 00000000		IPCP1[R] H,W 00000000 00000000		Input capture 0/1
001188 _H	ICS01[R/W] B,H,W -----00 00000000		-	LSYNS[R/W] B,H,W ----0000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00118C _H	IPCP2[R] H,W 00000000 00000000		IPCP3[R] H,W 00000000 00000000		Input capture 2/3
001190 _H	ICS23[R/W] B,H,W -----00 00000000		-	-	
001194 _H	-				Reserved
001198 _H	-				
00119C _H	-				Reserved
0011A0 _H	-				
0011A4 _H	DTSR[R/W] B,H,W -----10	-	-	-	DTTI selection
0011A8 _H	TMRR0[R/W] H,W 00000000 00000001		TMRR1[R/W] H,W 00000000 00000001		Waveform generator 0/1/2
0011AC _H	TMRR2[R/W] H,W 00000000 00000001		-	-	
0011B0 _H	DTSCR0[R/W] B,H,W 00000000	DTSCR1[R/W] B,H,W 00000000	DTSCR2[R/W] B,H,W 00000000	-	
0011B4 _H	-	DTIR0[R/W] B,H,W 000000--	-	DTMNS0[R/W] B,H,W 00---000	
0011B8 _H	-	SIGCR10[R/W] B,H,W 00000000	-	SIGCR20[R/W] B,H,W 000000-1	
0011BC _H	PICS0[R/W] B,H,W 000000-- -----				
0011C0 _H	TMRR3[R/W] H,W 00000000 00000001		TMRR4[R/W] H,W 00000000 00000001		Waveform generator 3/4/5
0011C4 _H	TMRR5[R/W] H,W 00000000 00000001		-	-	
0011C8 _H	DTSCR3[R/W] B,H,W 00000000	DTSCR4[R/W] B,H,W 00000000	DTSCR5[R/W] B,H,W 00000000	-	
0011CC _H	-	DTIR1[R/W] B,H,W 000000--	-	DTMNS1[R/W] B,H,W 00---000	Waveform generator 3/4/5
0011D0 _H	-	SIGCR11[R/W] B,H,W 00000000	-	SIGCR21[R/W] B,H,W -----1	
0011D4 _H	-				
0011D8 _H	-				
0011DC _H	ADTSS[R/W] B,H,W -----0	-	-	-	12-bit A/D converter
0011E0 _H	ADTSE[R/W] B,H,W ----- 00000000 -0000000 00000000				
0011E4 _H	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		
0011E8 _H	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		
0011EC _H	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		
0011F0 _H	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0011F4 _H	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		12-bit A/D converter
0011F8 _H	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		
0011FC _H	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		
001200 _H	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		-		
001204 _H	ADCOMP16/ADCOMPB16[R/W] H,W 00000000 00000000		ADCOMP17/ADCOMPB17[R/W] H,W 00000000 00000000		
001208 _H	ADCOMP18/ADCOMPB18[R/W] H,W 00000000 00000000		ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000		
00120C _H	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000		ADCOMP21/ADCOMPB21[R/W] H,W 00000000 00000000		
001210 _H	ADCOMP22/ADCOMPB22[R/W] H,W 00000000 00000000		ADCOMP23/ADCOMPB23[R/W] H,W 00000000 00000000		
001214 _H	-	-	-	-	
001218 _H	-	-	-	-	
00121C _H	-	-	-	-	
001220 _H	-	-	-	-	
001224 _H	ADTCS0[R/W] B,H,W 00000000 0010-000		ADTCS1[R/W] B,H,W 00000000 0010-000		
001228 _H	ADTCS2[R/W] B,H,W 00000000 0010-000		ADTCS3[R/W] B,H,W 00000000 0010-000		
00122C _H	ADTCS4[R/W] B,H,W 00000000 0010-000		ADTCS5[R/W] B,H,W 00000000 0010-000		
001230 _H	ADTCS6[R/W] B,H,W 00000000 0010-000		ADTCS7[R/W] B,H,W 00000000 0010-000		
001234 _H	ADTCS8[R/W] B,H,W 00000000 0010-000		ADTCS9[R/W] B,H,W 00000000 0010-000		
001238 _H	ADTCS10[R/W] B,H,W 00000000 0010-000		ADTCS11[R/W] B,H,W 00000000 0010-000		
00123C _H	ADTCS12[R/W] B,H,W 00000000 0010-000		ADTCS13[R/W] B,H,W 00000000 0010-000		
001240 _H	ADTCS14[R/W] B,H,W 00000000 0010-000		-		
001244 _H	ADTCS16[R/W] B,H,W 00000000 00100000		ADTCS17[R/W] B,H,W 00000000 00100000		
001248 _H	ADTCS18[R/W] B,H,W 00000000 00100000		ADTCS19[R/W] B,H,W 00000000 00100000		
00124C _H	ADTCS20[R/W] B,H,W 00000000 00100000		ADTCS21[R/W] B,H,W 00000000 00100000		
001250 _H	ADTCS22[R/W] B,H,W 00000000 00100000		ADTCS23[R/W] B,H,W 00000000 00100000		
001254 _H	-	-	-	-	
001258 _H	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00125C _H	-	-	-	-	12-bit A/D converter
001260 _H	-	-	-	-	
001264 _H	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001268 _H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		
00126C _H	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001270 _H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
001274 _H	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
001278 _H	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
00127C _H	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
001280 _H	ADTCD14[R] B,H,W 10--0000 00000000		-		
001284 _H	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
001288 _H	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		
00128C _H	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		
001290 _H	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
001294 _H	-	-	-	-	
001298 _H	-	-	-	-	
00129C _H	-	-	-	-	
0012A0 _H	-	-	-	-	
0012A4 _H	ADCS0[R/W] B,H,W 0-----		ADCH0[R] B,H,W ----000	ADMD0[R/W] B,H,W ----0000	
0012A8 _H	ADCS1[R/W] B,H,W 0-----		ADCH1[R] B,H,W ----000	ADMD1[R/W] B,H,W ----0000	
0012AC _H	ADCS2[R/W] B,H,W 0-----		ADCH2[R] B,H,W ----000	ADMD2[R/W] B,H,W ----0000	
0012B0 _H	MTRCSR[R/W] B,H,W -----0	-	-	-	Motor control extension function
0012B4 _H	RTOSEL0[R/W] B,H,W --000000	RTOSEL1[R/W] B,H,W -----0	-	-	
0012B8 _H	-	-	-	-	Reserved
0012FC _H	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001300 _H	-	-	-	-	Reserved
001304 _H	-	-	-	-	
001308 _H	-	-	-	-	
00130C _H	-	-	-	-	
001310 _H	-	-	-	-	
001314 _H	-	-	-	-	
001318 _H	-	-	-	-	
00131C _H	-	-	-	-	
001320 _H	-	-	-	-	
001324 _H	-	-	-	-	
001328 _H 00132C _H	-	-	-	-	Reserved
001330 _H	-	-	-	-	Reserved
001334 _H 0013FC _H	-	-	-	-	
001400 _H	DACR[R/W] B,H,W -----0	-	DADR[R/W] H,W -----XX XXXXXXXX	-	DAC
001404 _H 0014FC _H	-	-	-	-	Reserved
001500 _H	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000000-0	SSR0[R/W] B,H,W 0--00011	ESCR0/(IBSR0) [R/W] B,H,W 00000000	Multi Function Serial I/F 0
001504 _H	-/(RDR10/(TDR10))[R/W] B,H,W ----- *3		RDR00/(TDR00)[R/W] B,H,W -----0 00000000 *1		*1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001508 _H	SACSR0[R/W] B,H,W 0----000 00000000		STMRO[R] B,H,W 00000000 00000000		
00150C _H	STMCR0[R/W] B,H,W 00000000 00000000		-/(SFUR0) [R/W] B,H,W ----- *4		
001510 _H	-	-	-/(SFLR10) [R/W] B,H,W ----- *4	-/(SFLR00) [R/W] B,H,W ----- *4	
001514 _H	-	-	-	-	*4: Reserved because LIN2.1 mode is not set immediately after reset
001518 _H	-	-	-	-	
00151C _H	BGR0[R/W] H,W 00000000 00000000		-/(ISMK0)[R/W] B,H,W ----- *2	-/(ISBA0)[R/W] B,H,W ----- *2	
001520 _H	FCR10[R/W] B,H,W 00-00100	FCR00[R/W] B,H,W -0000000	FBYTE20[R/W] B,H,W 00000000	FBYTE10[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001524 _H	SCR1[R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000000-0	SSR1[R/W] B,H,W 0--00011	ESCR1[R/W] B,H,W 00000000	Multi Function Serial I/F 1 *1: Byte access is possible only for access to lower 8 bits. *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001528 _H	-/(RDR11/(TDR11))[R/W] B,H,W ----- *3		RDR01/(TDR01)[R/W] B,H,W -----0 00000000 *1		
00152C _H	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		
001530 _H	STMCR1[R/W] B,H,W 00000000 00000000		-/(SCSCR1/SFUR1) [R/W] B,H,W ----- *3 *4		
001534 _H	-/(SCSTR31) [R/W] B,H,W ----- *3	-/(SCSTR21) [R/W] B,H,W ----- *3	-/(SCSTR11/ SFLR11) [R/W] B,H,W ----- *3 *4	-/(SCSTR01/ SFLR01) [R/W] B,H,W ----- *3 *4	
001538 _H	-	-	-	-	
00153C _H	-	-	-	TBYTE01[R/W] B,H,W 00000000	
001540 _H	BGR1[R/W] H,W 00000000 00000000		-	-	
001544 _H	FCR11[R/W] B,H,W 00-00100	FCR01[R/W] B,H,W -0000000	FBYTE21[R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	
001548 _H	SCR2/(IBCR2) [R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000000-0	SSR2[R/W] B,H,W 0--00011	ESCR2/(IBSR2) [R/W] B,H,W 00000000	
00154C _H	-/(RDR12/(TDR12))[R/W] B,H,W ----- *3		RDR02/(TDR02)[R/W] B,H,W -----0 00000000 *1		
001550 _H	SACSR2[R/W] B,H,W 0----000 00000000		STMR2[R] B,H,W 00000000 00000000		
001554 _H	STMCR2[R/W] B,H,W 00000000 00000000		-/(SCSCR2/SFUR2) [R/W] B,H,W ----- *3 *4		
001558 _H	-/(SCSTR32) [R/W] B,H,W ----- *3	-/(SCSTR22) [R/W] B,H,W ----- *3	-/(SCSTR12/ SFLR12) [R/W] B,H,W ----- *3 *4	-/(SCSTR02/ SFLR02) [R/W] B,H,W ----- *3 *4	
00155C _H	-	-	-	-	
001560 _H	-	-	-	TBYTE02[R/W] B,H,W 00000000	
001564 _H	BGR2[R/W] H,W 00000000 00000000		-/(ISMK2)[R/W] B,H,W ----- *2	-/(ISBA2)[R/W] B,H,W ----- *2	
001568 _H	FCR12[R/W] B,H,W 00-00100	FCR02[R/W] B,H,W -0000000	FBYTE22[R/W] B,H,W 00000000	FBYTE12[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00156C _H	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3[R/W] B,H,W 000000-0	SSR3[R/W] B,H,W 0--00011	ESCR3/(IBSR3) [R/W] B,H,W 00000000	Multi Function Serial I/F 3 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001570 _H	-/(RDR13/(TDR13))[R/W] B,H,W ----- *3		RDR03/(TDR03)[R/W] B,H,W -----0 00000000 *1		
001574 _H	SACSR3[R/W] B,H,W 0---000 00000000		STMR3[R] B,H,W 00000000 00000000		
001578 _H	STMCR3[R/W] B,H,W 00000000 00000000		-/(SCSCR3/SFUR3) [R/W] B,H,W ----- *3 *4		
00157C _H	-/(SCSTR33) [R/W] B,H,W ----- *3	-/(SCSTR23) [R/W] B,H,W ----- *3	-/(SCSTR13/ SFLR13) [R/W] B,H,W ----- *3 *4	-/(SCSTR03/ SFLR03) [R/W] B,H,W ----- *3 *4	
001580 _H	-	-	-	-	
001584 _H	-	-	-	TBYTE03[R/W] B,H,W 00000000	
001588 _H	BGR3[R/W] H,W 00000000 00000000		-/(ISMK3)[R/W] B,H,W ----- *2	-/(ISBA3)[R/W] B,H,W ----- *2	
00158C _H	FCR13[R/W] B,H,W 00-00100	FCR03[R/W] B,H,W -0000000	FBYTE23[R/W] B,H,W 00000000	FBYTE13[R/W] B,H,W 00000000	
001590 _H 001FFC _H	-	-	-	-	
002000 _H	CTRLR0[R/W] B,H,W ----- 000-0001		STATR0[R/W] B,H,W ----- 00000000		CAN 0 64msb
002004 _H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0[R/W] B,H,W -0100011 00000001		
002008 _H	INTR0[R] B,H,W 00000000 00000000		TESTR0[R/W] B,H,W ----- X00000--		
00200C _H	BRPER0[R/W] B,H,W ----- ----0000		-		
002010 _H	IF1CREQ0[R/W] B,H,W 0----- 00000001		IF1CMSK0[R/W] B,H,W ----- 00000000		
002014 _H	IF1MSK20[R/W] B,H,W 11-11111 11111111		IF1MSK10[R/W] B,H,W 11111111 11111111		
002018 _H	IF1ARB20[R/W] B,H,W 00000000 00000000		IF1ARB10[R/W] B,H,W 00000000 00000000		
00201C _H	IF1MCTR0[R/W] B,H,W 00000000 0---0000		-		
002020 _H	IF1DTA10[R/W] B,H,W 00000000 00000000		IF1DTA20[R/W] B,H,W 00000000 00000000		
002024 _H	IF1DTB10[R/W] B,H,W 00000000 00000000		IF1DTB20[R/W] B,H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002028 _H , 00202C _H	-				CAN 0 64msb
002030 _H , 002034 _H	Reserved (IF1 data mirror)				
002038 _H , 00203C _H	-				
002040 _H	IF2CREQ0[R/W] B,H,W 0----- 00000001		IF2CMSK0[R/W] B,H,W ----- 00000000		
002044 _H	IF2MSK20[R/W] B,H,W 11-11111 11111111		IF2MSK10[R/W] B,H,W 11111111 11111111		
002048 _H	IF2ARB20[R/W] B,H,W 00000000 00000000		IF2ARB10[R/W] B,H,W 00000000 00000000		
00204C _H	IF2MCTR0[R/W] B,H,W 00000000 0---0000		-		
002050 _H	IF2DTA10[R/W] B,H,W 00000000 00000000		IF2DTA20[R/W] B,H,W 00000000 00000000		
002054 _H	IF2DTB10[R/W] B,H,W 00000000 00000000		IF2DTB20[R/W] B,H,W 00000000 00000000		
002058 _H , 00205C _H	-				
002060 _H , 002064 _H	Reserved (IF2 data mirror)				
002068 _H , 00207C _H	-				
002080 _H	TREQR20[R] B,H,W 00000000 00000000		TREQR10[R] B,H,W 00000000 00000000		
002084 _H	TREQR40[R] B,H,W 00000000 00000000		TREQR30[R] B,H,W 00000000 00000000		
002088 _H	-				
00208C _H	-				
002090 _H	NEWDT20[R] B,H,W 00000000 00000000		NEWDT10[R] B,H,W 00000000 00000000		
002094 _H	NEWDT40[R] B,H,W 00000000 00000000		NEWDT30[R] B,H,W 00000000 00000000		
002098 _H	-				
00209C _H	-				
0020A0 _H	INTPND20[R] B,H,W 00000000 00000000		INTPND10[R] B,H,W 00000000 00000000		
0020A4 _H	INTPND40[R] B,H,W 00000000 00000000		INTPND30[R] B,H,W 00000000 00000000		
0020A8 _H	-				
0020AC _H	-				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0020B0 _H	MSGVAL20[R] B,H,W 00000000 00000000		MSGVAL10[R] B,H,W 00000000 00000000		CAN 0 64msb
0020B4 _H	MSGVAL40[R] B,H,W 00000000 00000000		MSGVAL30[R] B,H,W 00000000 00000000		
0020B8 _H	-		-		
0020BC _H	-		-		
0020C0 _H 0020FC _H	-		-		
002100 _H	CTRLR1[R/W] B,H,W ----- 000-0001		STATR1[R/W] B,H,W ----- 00000000		CAN 1 64msb
002104 _H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1[R/W] B,H,W -0100011 00000001		
002108 _H	INTR1[R] B,H,W 00000000 00000000		TESTR1[R/W] B,H,W ----- X00000--		
00210C _H	BRPER1[R/W] B,H,W ----- ----0000		-		
002110 _H	IF1CREQ1[R/W] B,H,W 0----- 00000001		IF1CMSK1[R/W] B,H,W ----- 00000000		
002114 _H	IF1MSK21[R/W] B,H,W 11-11111 11111111		IF1MSK11[R/W] B,H,W 11111111 11111111		
002118 _H	IF1ARB21[R/W] B,H,W 00000000 00000000		IF1ARB11[R/W] B,H,W 00000000 00000000		
00211C _H	IF1MCTR1[R/W] B,H,W 00000000 0---0000		-		
002120 _H	IF1DTA11[R/W] B,H,W 00000000 00000000		IF1DTA21[R/W] B,H,W 00000000 00000000		
002124 _H	IF1DTB11[R/W] B,H,W 00000000 00000000		IF1DTB21[R/W] B,H,W 00000000 00000000		
002128 _H , 00212C _H	-		-		
002130 _H , 002134 _H	Reserved (IF1 data mirror)				
002138 _H , 00213C _H	-		-		
002140 _H	IF2CREQ1[R/W] B,H,W 0----- 00000001		IF2CMSK1[R/W] B,H,W ----- 00000000		
002144 _H	IF2MSK21[R/W] B,H,W 11-11111 11111111		IF2MSK11[R/W] B,H,W 11111111 11111111		
002148 _H	IF2ARB21[R/W] B,H,W 00000000 00000000		IF2ARB11[R/W] B,H,W 00000000 00000000		
00214C _H	IF2MCTR1[R/W] B,H,W 00000000 0---0000		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002150 _H	IF2DTA11[R/W] B,H,W 00000000 00000000		IF2DTA21[R/W] B,H,W 00000000 00000000		CAN 1 64msb
002154 _H	IF2DTB11[R/W] B,H,W 00000000 00000000		IF2DTB21[R/W] B,H,W 00000000 00000000		
002158 _H , 00215C _H	-		-		
002160 _H , 002164 _H	Reserved (IF2 data mirror)				
002168 _H 00217C _H	-		-		
002180 _H	TREQR21[R] B,H,W 00000000 00000000		TREQR11[R] B,H,W 00000000 00000000		
002184 _H	TREQR41[R] B,H,W 00000000 00000000		TREQR31[R] B,H,W 00000000 00000000		
002188 _H	-		-		
00218C _H	-		-		
002190 _H	NEWDT21[R] B,H,W 00000000 00000000		NEWDT11[R] B,H,W 00000000 00000000		
002194 _H	NEWDT41[R] B,H,W 00000000 00000000		NEWDT31[R] B,H,W 00000000 00000000		
002198 _H	-		-		
00219C _H	-		-		
0021A0 _H	INTPND21[R] B,H,W 00000000 00000000		INTPND11[R] B,H,W 00000000 00000000		
0021A4 _H	INTPND41[R] B,H,W 00000000 00000000		INTPND31[R] B,H,W 00000000 00000000		
0021A8 _H	-		-		
0021AC _H	-		-		
0021B0 _H	MSGVAL21[R] B,H,W 00000000 00000000		MSGVAL11[R] B,H,W 00000000 00000000		
0021B4 _H	MSGVAL41[R] B,H,W 00000000 00000000		MSGVAL31[R] B,H,W 00000000 00000000		
0021B8 _H	-		-		
0021BC _H	-		-		
0021C0 _H 0021FC _H	-		-		
002200 _H 0022FC _H	-		-		Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002300 _H	DFCTLR[R/W] B,H,W -0-----	-	-	DFSTR[R/W] B,H,W ----001	WorkFlash
002304 _H	-	-	-	-	
002308 _H	FLIFCTLR[R/W] B,H,W ---0--00	-	FLIFFER1[R/W] B,H,W -----	FLIFFER2[R/W] B,H,W -----	Reserved
00230C _H 002FFC _H	-	-	-	-	
003000 _H	SEEARX[R] B,H,W --000000 00000000	-	DEEARX[R] B,H,W --000000 00000000	-	XBS RAM ECC control register
003004 _H	EECSR[R/W] B,H,W ----00-0	-	EFEARX[R/W] B,H,W --000000 00000000	-	
003008 _H	-	EFECRX[R/W] B,H,W -----0 00000000 00000000	-	-	XBS RAM diagnosis register
00300C _H	TEAR0X[R] B,H,W 000----- --000000 00000000	-	-	-	
003010 _H	TEAR1X[R] B,H,W 000----- --000000 00000000	-	-	-	XBS RAM diagnosis register
003014 _H	TEAR2X[R] B,H,W 000----- --000000 00000000	-	-	-	
003018 _H	TAEARX[R/W] B,H,W --101111 11111111	-	TASARX[R/W] B,H,W --000000 00000000	-	XBS RAM diagnosis register
00301C _H	TFECRX[R/W] B,H,W ----0000	TICRX[R/W] B,H,W ----0000	TTCRX[R/W] B,H,W -----00 00001100	-	
003020 _H	TSRCRX[R/W] B,H,W 0-----	-	-	TKCCRX[R/W] B,H,W 00----00	Backup RAM ECC control register
003024 _H	SEEARA[R] B,H,W --000000 00000000	-	DEEARA[R] B,H,W --000000 00000000	-	
003028 _H	EECSRA[R/W] B,H,W ----00-0	-	EFEARA[R/W] B,H,W --000000 00000000	-	Backup RAM ECC control register
00302C _H	-	EFECRA[R/W] B,H,W -----0 00000000 00000000	-	-	
003030 _H	TEAR0A[R] B,H,W 000----- ----000 00000000	-	-	-	Backup RAM diagnosis register
003034 _H	TEAR1A[R] B,H,W 000----- ----000 00000000	-	-	-	
003038 _H	TEAR2A[R] B,H,W 000----- ----000 00000000	-	-	-	Backup RAM diagnosis register
00303C _H	TAEARA[R/W] B,H,W ----111 11111111	-	TASARA[R/W] B,H,W ----000 00000000	-	
003040 _H	TFECRA[R/W] B,H,W ----0000	TICRA[R/W] B,H,W ----0000	TTCRA[R/W] B,H,W -----00 00001100	-	Backup RAM diagnosis register
003044 _H	TSRCRA[R/W] B,H,W 0-----	-	-	TKCCRA[R/W] B,H,W 00----00	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
003048 _H 0030FC _H	-	-	-	-	Reserved
003100 _H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		Bus diagnosis
003104 _H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108 _H	BUSADR0[R] W 00000000 00000000 00000000 00000000				
00310C _H	BUSADR1[R] W 00000000 00000000 00000000 00000000				
003110 _H	BUSADR2[R] W 00000000 00000000 00000000 00000000				
003114 _H	-		BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118 _H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--0000 00000000		
00311C _H	-				
003120 _H	BUSADR3[R] W 00000000 00000000 00000000 00000000				
003124 _H	BUSADR4[R] W 00000000 00000000 00000000 00000000				Bus diagnosis
003128 _H 003FFC _H	-	-	-	-	Reserved
004000 _H 005FFC _H	Backup RAM				Backup RAM area
006000 _H 00CFFC _H	-	-	-	-	Reserved
00D000 _H	CIF0[R] W 00000100 11111111 01011011 11111111				FlexRay CIF *5
00D004 _H	CIF1[R/W] W 00000000 -----0 -0000000 -----				
00D008 _H 00D00C _H	-	-	-	-	Reserved
00D010 _H	-				FlexRay GIF *5
00D014 _H	-				
00D018 _H	-	-	-	-	
00D01C _H	LCK[R/W] W ----- 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D020 _H	EIR[R/W] W ----000 ----000 ----0000 00000000				FlexRay INT ⁵
00D024 _H	SIR[R/W] W -----00 -----00 00000000 00000000				
00D028 _H	EILS[R/W] W ----000 ----000 ----0000 00000000				
00D02C _H	SILS[R/W] W -----11 -----11 11111111 11111111				
00D030 _H	EIES[R/W] W ----000 ----000 ----0000 00000000				
00D034 _H	EIER[R/W] W ----000 ----000 ----0000 00000000				
00D038 _H	SIES[R/W] W -----00 -----00 00000000 00000000				
00D03C _H	SIER[R/W] W -----00 -----00 00000000 00000000				
00D040 _H	ILE[R/W] W -----000000000000000000000000				
00D044 _H	T0C[R/W] W --000000 00000000 -0000000 -00000000				
00D048 _H	T1C[R/W] W --000000 00000010 -----00000000				
00D04C _H	STPW1[R/W] W --000000 00000000 --000000 -00000000				
00D050 _H	STPW2[R] W ----000 00000000 ----000 00000000				
00D054 _H 00D07C _H	-	-	-	-	
00D080 _H	SUCC1[R/W] W ----1100 01000000 00010-00 1---0000				FlexRay SUC ⁵
00D084 _H	SUCC2[R/W] W ----0001 ---00000 00000101 00000100				
00D088 _H	SUCC3[R/W] W -----00000000000000000000000000010001				
00D08C _H	NEMC[R/W] W -----00000000000000000000000000000000				FlexRay NEM ⁵
00D090 _H	PRTC1[R/W] W 000010-0 01001100 0000-110 00110011				FlexRay PRT ⁵
00D094 _H	PRTC2[R/W] W --001111 00101101 --001010 --001110				
00D098 _H	MHDC[R/W] W ---00000 00000000 -----00000000				FlexRay MHD ⁵
00D09C _H	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D0A0 _H	GTUC1[R/W] W ----- ----0000 00000010 10000000				FlexRay GTU ¹⁵
00D0A4 _H	GTUC2[R/W] W ----- ----0010 --000000 00001010				
00D0A8 _H	GTUC3[R/W] W -0000010 -0000010 00000000 00000000				
00D0AC _H	GTUC4[R/W] W --000000 00001000 --000000 00000111				
00D0B0 _H	GTUC5[R/W] W 00001110 ---00000 00000000 00000000				
00D0B4 _H	GTUC6[R/W] W ----000 00000010 ----000 00000000				
00D0B8 _H	GTUC7[R/W] W -----00 00000010 -----00 00000100				
00D0BC _H	GTUC8[R/W] W --00000 00000000 ----- --000010				
00D0C0 _H	GTUC9[R/W] W ----- -----00 ---00001 --000001				
00D0C4 _H	GTUC10[R/W] W ----000 00000010 --000000 00000101				
00D0C8 _H	GTUC11[R/W] W ----000 ----000 -----00 -----00				
00D0CC _H 00D0FC _H	-				Reserved
00D100 _H	CCSV[R] W --000000 00010000 -100--00 00000000				FlexRay
00D104 _H	CCEV[R] W ----- ----- ---00000 00--0000				SUC ¹⁵
00D108 _H 00D10C _H	-				Reserved
00D110 _H	SCV[R] W ----000 00000000 ----000 00000000				FlexRay GTU ¹⁵
00D114 _H	MTCCV[R] W ----- --000000 --000000 00000000				
00D118 _H	RCV[R] W ----- ----- ----0000 00000000				
00D11C _H	OCV[R] W ----- -----000 00000000 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D120 _H	SFS[R] W ----- ----0000 00000000 00000000				FlexRay GTU ¹⁵
00D124 _H	SWNIT[R] W ----- ----0000 00000000				
00D128 _H	ACS[R/W] W ----- ----00000 ---00000				
00D12C _H	-				
00D130 _H	ESID1[R] W ----- 00----00 00000000				
00D134 _H	ESID2[R] W ----- 00----00 00000000				
00D138 _H	ESID3[R] W ----- 00----00 00000000				
00D13C _H	ESID4[R] W ----- 00----00 00000000				
00D140 _H	ESID5[R] W ----- 00----00 00000000				
00D144 _H	ESID6[R] W ----- 00----00 00000000				
00D148 _H	ESID7[R] W ----- 00----00 00000000				
00D14C _H	ESID8[R] W ----- 00----00 00000000				
00D150 _H	ESID9[R] W ----- 00----00 00000000				
00D154 _H	ESID10[R] W ----- 00----00 00000000				
00D158 _H	ESID11[R] W ----- 00----00 00000000				
00D15C _H	ESID12[R] W ----- 00----00 00000000				
00D160 _H	ESID13[R] W ----- 00----00 00000000				
00D164 _H	ESID14[R] W ----- 00----00 00000000				
00D168 _H	ESID15[R] W ----- 00----00 00000000				
00D16C _H	-				
00D170 _H	OSID1[R] W ----- 00----00 00000000				
00D174 _H	OSID2[R] W ----- 00----00 00000000				
00D178 _H	OSID3[R] W ----- 00----00 00000000				
00D17C _H	OSID4[R] W ----- 00----00 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D180 _H	OSID5[R] W ----- 00---00 00000000				FlexRay GTU ⁵
00D184 _H	OSID6[R] W ----- 00---00 00000000				
00D188 _H	OSID7[R] W ----- 00---00 00000000				
00D18C _H	OSID8[R] W ----- 00---00 00000000				
00D190 _H	OSID9[R] W ----- 00---00 00000000				
00D194 _H	OSID10[R] W ----- 00---00 00000000				
00D198 _H	OSID11[R] W ----- 00---00 00000000				
00D19C _H	OSID12[R] W ----- 00---00 00000000				
00D1A0 _H	OSID13[R] W ----- 00---00 00000000				
00D1A4 _H	OSID14[R] W ----- 00---00 00000000				
00D1A8 _H	OSID15[R] W ----- 00---00 00000000				
00D1AC _H	-				Reserved
00D1B0 _H	NMV1[R] W 00000000 00000000 00000000 00000000				FlexRay NEM ⁵
00D1B4 _H	NMV2[R] W 00000000 00000000 00000000 00000000				
00D1B8 _H	NMV3[R] W 00000000 00000000 00000000 00000000				
00D1BC _H 00D2FC _H	-				Reserved
00D300 _H	MRC[R/W] W ----001 10000000 00000000 00000000				FlexRay MHD ⁵
00D304 _H	FRF[R/W] W -----1 10000000 ---00000 00000000				
00D308 _H	FRFM[R/W] W ----- ---00000 000000--				
00D30C _H	FCL[R/W] W ----- 10000000				
00D310 _H	MHDS[R/W] W -0000000 -00000000 -00000000 00000000				
00D314 _H	LDTS[R] W ----000 00000000 ----000 00000000				
00D318 _H	FSR[R] W ----- 00000000 ----000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D31C _H	MHDF[R/W] W -----0 00000000				FlexRay MHD *5
00D320 _H	TXRQ1[R] W 00000000 00000000 00000000 00000000				
00D324 _H	TXRQ2[R] W 00000000 00000000 00000000 00000000				
00D328 _H	TXRQ3[R] W 00000000 00000000 00000000 00000000				
00D32C _H	TXRQ4[R] W 00000000 00000000 00000000 00000000				
00D330 _H	NDAT1[R] W 00000000 00000000 00000000 00000000				
00D334 _H	NDAT2[R] W 00000000 00000000 00000000 00000000				
00D338 _H	NDAT3[R] W 00000000 00000000 00000000 00000000				
00D33C _H	NDAT4[R] W 00000000 00000000 00000000 00000000				
00D340 _H	MBSC1[R] W 00000000 00000000 00000000 00000000				
00D344 _H	MBSC2[R] W 00000000 00000000 00000000 00000000				
00D348 _H	MBSC3[R] W 00000000 00000000 00000000 00000000				
00D34C _H	MBSC4[R] W 00000000 00000000 00000000 00000000				
00D350 _H 00D3EC _H	-				Reserved
00D3F0 _H	CREL[R] W 00010000 00111001 00000010 00000110				FlexRay GIF *5
00D3F4 _H	ENDN[R] W 10000111 01100101 01000011 00100001				
00D3F8 _H 00D3FC _H	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D400 _H 00D4FC _H	WRDSn[1-64][R/W] W 00000000 00000000 00000000 00000000				FlexRay IBF ^{*5}
00D500 _H	WRHS1[R/W] W --000000 -00000000 -----000 00000000				
00D504 _H	WRHS2[R/W] W ----- -00000000 -----000 00000000				
00D508 _H	WRHS3[R/W] W ----- -00000000 -----000 00000000				
00D50C _H	-				
00D510 _H	IBCM[R/W] W ----- -00 ----- -000				
00D514 _H	IBCR[R/W] W 0----- -00000000 0----- -00000000				
00D518 _H 00D5FC _H	-				Reserved
00D600 _H 00D6FC _H	RDDSn[1-64][R] W 00000000 00000000 00000000 00000000				FlexRay OBF ^{*5}
00D700 _H	RDHS1[R] W --000000 -00000000 -----000 00000000				
00D704 _H	RDHS2[R] W -00000000 -00000000 -----000 00000000				
00D708 _H	RDHS3[R] W --000000 --000000 -----000 00000000				
00D70C _H	MBS[R] W --000000 --000000 00-000000 00000000				
00D710 _H	OBCM[R/W] W ----- -00 ----- -00				
00D714 _H	OBCR[R/W] W ----- -00000000 0----- -00 -00000000				
00D718 _H 00D7FC _H	-				Reserved
00D800 _H 00EFFC _H	-				Reserved
00F000 _H 00FEFC _H	-				Reserved [S]
00FF00 _H	DSUCR[R/W] B,H,W ----- -0	-	-	-	OCDU [S]
00FF04 _H 00FF0C _H	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00FF10 _H	PCSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FF14 _H	PSSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00FF18 _H 00FFF4 _H	-	-	-	-	Reserved [S]
00FFF8 _H	EDIR1[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FFFC _H	EDIR0[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated when reading and writing to these registers in the user mode.

*5: For FlexRay, the CY91F583AMG/F584AMG/F585AMG/F583AMJ/F584AMJ/F585AMJ has corresponding functions. The following registers are reserved registers for models without the FlexRay function.
 000125_H IRPR2L[5:4], 000E68_H, 0004E8_H-0004EF_H, 00D000_H-00D717_H

■ I/O Map (CY91F583AS/F584AS/F585AS)

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000000 _H	-	PDR01[R/W] B,H,W XXXXXXXX	PDR02[R/W] B,H,W XXXXXXXX	PDR03[R/W] B,H,W XXXXXXXX	Port data register
000004 _H	PDR04[R/W] B,H,W XXXXXXXX	PDR05[R/W] B,H,W -XXXXXXXX	-	PDR07[R/W] B,H,W ----XXX	
000008 _H	-	PDR09[R/W] B,H,W ---XX---	-	-	
00000C _H	-	-	-	-	
000010 _H 000038 _H	-	-	-	-	Reserved
00003C _H	WDTCR0[R/W] B,H,W -0-0000	WDTCPR0[W] B,H,W 00000000	WDTCR1[R] B,H,W ----0010	WDTCPR1[W] B,H,W 00000000	Watchdog timer [S]
000040 _H	-	-	-	-	Reserved
000044 _H	DICR[R/W] B -----0	-	-	-	Delay interrupt
000048 _H 00005C _H	-	-	-	-	Reserved
000060 _H	TMRLRA0[R/W] H XXXXXXXX XXXXXXXX		TMR0[R] H XXXXXXXX XXXXXXXX		Reload timer 0
000064 _H	TMRLRB0[R/W] H XXXXXXXX XXXXXXXX		TMCSR0[R/W] B,H,W 00000000 0-000000		
000068 _H 00007C _H	-	-	-	-	Reserved
000080 _H	BT0TMR[R] H 00000000 00000000		BT0TMCR[R/W] H -0000000 00000000		Base timer 0
000084 _H	BT0TMCR2 [R/W] B -----0	BT0STC [R/W] B -0-0-0-0	-	-	
000088 _H	BT0PCSR/BT0PRLL [R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
00008C _H	-	-	-	-	
000090 _H	BT1TMR[R] H 00000000 00000000		BT1TMCR[R/W] H -0000000 00000000		Base timer 1
000094 _H	BT1TMCR2 [R/W] B -----0	BT1STC [R/W] B -0-0-0-0	-	-	
000098 _H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
00009C _H	BTSEL01[R/W] B ----0000	-	BTSSSR[W] B,H -----11		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0000A0 _H 0000FC _H	-	-	-	-	Reserved
000100 _H	TMRLRA1[R/W] H XXXXXXXX XXXXXXXX		TMR1[R] H XXXXXXXX XXXXXXXX		Reload timer 1
000104 _H	TMRLRB1[R/W] H XXXXXXXX XXXXXXXX		TMCSR1[R/W] B,H,W 00000000 0-000000		
000108 _H	TMRLRA2[R/W] H XXXXXXXX XXXXXXXX		TMR2[R] H XXXXXXXX XXXXXXXX		Reload timer 2
00010C _H	TMRLRB2[R/W] H XXXXXXXX XXXXXXXX		TMCSR2[R/W] B,H,W 00000000 0-000000		
000110 _H	TMRLRA3[R/W] H XXXXXXXX XXXXXXXX		TMR3[R] H XXXXXXXX XXXXXXXX		Reload timer 3
000114 _H	TMRLRB3[R/W] H XXXXXXXX XXXXXXXX		TMCSR3[R/W] B,H,W 00000000 0-000000		
000118 _H 00011C _H	-	-	-	-	Reserved
000120 _H	IRPR0H[R] B,H,W 00-----	IRPR0L[R] B,H,W 00-----	IRPR1H[R] B,H,W 00-----	IRPR1L[R] B,H,W -----	Interrupt request batch read register
000124 _H	IRPR2H[R] B,H,W -----	IRPR2L[R] B,H,W ⁵ 0000---	IRPR3H[R] B,H,W 00-----	IRPR3L[R] B,H,W 00-----	
000128 _H	IRPR4H[R] B,H,W 00-----	IRPR4L[R] B,H,W 000000--	IRPR5H[R] B,H,W 00-----	IRPR5L[R] B,H,W 00-----	
00012C _H	IRPR6H[R] B,H,W 0000----	IRPR6L[R] B,H,W 00-----	IRPR7H[R] B,H,W 00-----	IRPR7L[R] B,H,W -----	
000130 _H	IRPR8H[R] B,H,W -----	IRPR8L[R] B,H,W 00-----	IRPR9H[R] B,H,W 00-----	IRPR9L[R] B,H,W 00-----	
000134 _H	IRPR10H[R] B,H,W 00-----	IRPR10L[R] B,H,W 00-----	IRPR11H[R] B,H,W 00-----	IRPR11L[R] B,H,W 0000000-	
000138 _H	IRPR12H[R] B,H,W 0000000-	IRPR12L[R] B,H,W 00000000	IRPR13H[R] B,H,W 0000000-	IRPR13L[R] B,H,W ---00---	
00013C _H	IRPR14H[R] B,H,W 00-----	IRPR14L[R] B,H,W 00-----	IRPR15H[R] B,H,W 00000000	IRPR15L[R] B,H,W 0000----	
000140 _H	IRPR16H[R] B,H,W 00-----	IRPR16L[R] B,H,W -----	IRPR17H[R] B,H,W -----	IRPR17L[R] B,H,W -----	
000144 _H	IRPR18H[R]B,H,W -----	IRPR18L[R]B,H,W 000000--	-	-	
000148 _H 0001FC _H	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000200 _H	PCN0[R/W] B,H,W 00000000 000000-0		PCSR0[W] H,W XXXXXXXX XXXXXXXX		PPG0
000204 _H	PDUT0[W] H,W XXXXXXXX XXXXXXXX		PTMR0[R] H,W 11111111 11111111		
000208 _H	PCN1[R/W] B,H,W 00000000 000000-0		PCSR1[W] H,W XXXXXXXX XXXXXXXX		PPG1
00020C _H	PDUT1[W] H,W XXXXXXXX XXXXXXXX		PTMR1[R] H,W 11111111 11111111		
000210 _H	PCN2[R/W] B,H,W 00000000 000000-0		PCSR2[W] H,W XXXXXXXX XXXXXXXX		PPG2
000214 _H	PDUT2[W] H,W XXXXXXXX XXXXXXXX		PTMR2[R] H,W 11111111 11111111		
000218 _H	PCN3[R/W] B,H,W 00000000 000000-0		PCSR3[W] H,W XXXXXXXX XXXXXXXX		PPG3
00021C _H	PDUT3[W] H,W XXXXXXXX XXXXXXXX		PTMR3[R] H,W 11111111 11111111		
000220 _H	PCN4[R/W] B,H,W 00000000 000000-0		PCSR4[W] H,W XXXXXXXX XXXXXXXX		PPG4
000224 _H	PDUT4[W] H,W XXXXXXXX XXXXXXXX		PTMR4[R] H,W 11111111 11111111		
000228 _H	PCN5[R/W] B,H,W 00000000 000000-0		PCSR5[W] H,W XXXXXXXX XXXXXXXX		PPG5
00022C _H	PDUT5[W] H,W XXXXXXXX XXXXXXXX		PTMR5[R] H,W 11111111 11111111		
000230 _H 0002BC _H	-		-		Reserved
0002C0 _H	GTRS0[R/W] B,H,W -0000000 -0000000		GTRS1[R/W] B,H,W -0000000 -0000000		PPG Control
0002C4 _H	GTRS2[R/W] B,H,W -0000000 -0000000		-		
0002C8 _H	-		-		
0002CC _H	-		-		
0002D0 _H	-		-		
0002D4 _H	-		-		
0002D8 _H	GTREN0[R/W] H,W -----000000		-		
0002DC _H	-		-		Reserved
0002E0 _H	-		GATEC0[R/W] B,H,W -----00	GATEC2[R/W] B,H,W -----00	PPG GATE Control
0002E4 _H	-		GATEC4[R/W] B,H,W -----00	-	
0002E8 _H	-		-	-	
0002EC _H	-		-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0002F0 _H	RCRH0[W] H,W 00000000	RCRL0[W] B,H,W 00000000	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	U/D counter 0
0002F4 _H	CCR0[R/W] B,H 00000000 -0001000		-	CSR0[R] B 00000000	
0002F8 _H	RCRH1[W] H,W 00000000	RCRL1[W] B,H,W 00000000	UDCRH1[R] H,W 00000000	UDCRL1[R] B,H,W 00000000	U/D counter 1
0002FC _H	CCR1[R/W] B,H 00000000 -0001000		-	CSR1[R] B 00000000	
000300 _H	-				Reserved
000304 _H	-				Reserved
000308 _H	-				Reserved
00030C _H	-				
000310 _H	-		MPUCR[R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314 _H	-				
000318 _H	-				
00031C _H	-				
000320 _H	DPVAR[R] W XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX				
000324 _H	-		DPVSR[R/W] H ----- 0000--0		
000328 _H	DEAR[R] W XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX				
00032C _H	-		DESR[R/W] H ----- 0000--0		
000330 _H	PABR0[R/W] W XXXXXXXXXXXXXXXXXXXXXXXXXXXX0000				
000334 _H	-		PACR0[R/W] H 000000-0 0000--0		
000338 _H	PABR1[R/W] W XXXXXXXXXXXXXXXXXXXXXXXXXXXX0000				
00033C _H	-		PACR1[R/W] H 000000-0 0000--0		
000340 _H	PABR2[R/W] W XXXXXXXXXXXXXXXXXXXXXXXXXXXX0000				
000344 _H	-		PACR2[R/W] H 000000-0 0000--0		
000348 _H	PABR3[R/W] W XXXXXXXXXXXXXXXXXXXXXXXXXXXX0000				
00034C _H	-		PACR3[R/W] H 000000-0 0000--0		
000350 _H	PABR4[R/W] W XXXXXXXXXXXXXXXXXXXXXXXXXXXX0000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000354 _H	-	-	PACR4[R/W] H 000000-0 00000--0		MPU [S] (Only the CPU can access this area)
000358 _H	PABR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00035C _H	-	-	PACR5[R/W] H 000000-0 00000--0		
000360 _H	PABR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364 _H	-	-	PACR6[R/W] H 000000-0 00000--0		
000368 _H	PABR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00036C _H	-	-	PACR7[R/W] H 000000-0 00000--0		
000370 _H	-	-	-	-	
000374 _H	-	-	-	-	
000378 _H	-	-	-	-	
00037C _H	-	-	-	-	
000380 _H	-	-	-	-	
000384 _H	-	-	-	-	
000388 _H	-	-	-	-	
00038C _H	-	-	-	-	
000390 _H	-	-	-	-	
000394 _H	-	-	-	-	Reserved [S]
000398 _H	-	-	-	-	
00039C _H	-	-	-	-	
0003A0 _H	-	-	-	-	
0003A4 _H	-	-	-	-	
0003A8 _H	-	-	-	-	
0003AC _H	-	-	-	-	Reserved [S]
0003B0 _H	-	-	-	-	
0003CC _H	-	-	-	-	Reserved [S]
0003D0 _H	-	-	-	-	
0003D4 _H	-	-	-	-	
0003D8 _H	-	-	-	-	
0003DC _H	-	-	-	-	Reserved [S]
0003E0 _H	-	-	-	-	
0003FC _H	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000400 _H	ICSEL0[R/W] B,H,W -----000	ICSEL1[R/W] B,H,W -----0	ICSEL2[R/W] B,H,W -----0	ICSEL3[R/W] B,H,W -----0	Generation and clear of DMA transfer request
000404 _H	ICSEL4[R/W] B,H,W -----0	ICSEL5[R/W] B,H,W -----0	ICSEL6[R/W] B,H,W -----0	ICSEL7[R/W] B,H,W -----000	
000408 _H	ICSEL8[R/W] B,H,W -----0	ICSEL9[R/W] B,H,W -----0	ICSEL10[R/W] B,H,W -----00	ICSEL11[R/W] B,H,W -----0	
00040C _H	ICSEL12[R/W] B,H,W -----0	ICSEL13[R/W] B,H,W -----0	ICSEL14[R/W] B,H,W -----0	ICSEL15[R/W] B,H,W -----0	
000410 _H	ICSEL16[R/W] B,H,W -----0	ICSEL17[R/W] B,H,W -----0	ICSEL18[R/W] B,H,W -----0	ICSEL19[R/W] B,H,W -----0	
000414 _H	ICSEL20[R/W] B,H,W -----0	ICSEL21[R/W] B,H,W -----000	ICSEL22[R/W] B,H,W -----000	ICSEL23[R/W] B,H,W -----000	
000418 _H	ICSEL24[R/W] B,H,W -----000	ICSEL25[R/W] B,H,W -----000	ICSEL26[R/W] B,H,W -----0	ICSEL27[R/W] B,H,W -----0	
00041C _H	-	-	-	-	
000420 _H	-	-	-	-	
000424 _H 00043C _H	-	-	-	-	
000440 _H	ICR00[R/W] B,H,W ---11111	ICR01[R/W] B,H,W ---11111	ICR02[R/W] B,H,W ---11111	ICR03[R/W] B,H,W ---11111	Interrupt controller [S]
000444 _H	ICR04[R/W] B,H,W ---11111	ICR05[R/W] B,H,W ---11111	ICR06[R/W] B,H,W ---11111	ICR07[R/W] B,H,W ---11111	
000448 _H	ICR08[R/W] B,H,W ---11111	ICR09[R/W] B,H,W ---11111	ICR10[R/W] B,H,W ---11111	ICR11[R/W] B,H,W ---11111	
00044C _H	ICR12[R/W] B,H,W ---11111	ICR13[R/W] B,H,W ---11111	ICR14[R/W] B,H,W ---11111	ICR15[R/W] B,H,W ---11111	
000450 _H	ICR16[R/W] B,H,W ---11111	ICR17[R/W] B,H,W ---11111	ICR18[R/W] B,H,W ---11111	ICR19[R/W] B,H,W ---11111	
000454 _H	ICR20[R/W] B,H,W ---11111	ICR21[R/W] B,H,W ---11111	ICR22[R/W] B,H,W ---11111	ICR23[R/W] B,H,W ---11111	
000458 _H	ICR24[R/W] B,H,W ---11111	ICR25[R/W] B,H,W ---11111	ICR26[R/W] B,H,W ---11111	ICR27[R/W] B,H,W ---11111	
00045C _H	ICR28[R/W] B,H,W ---11111	ICR29[R/W] B,H,W ---11111	ICR30[R/W] B,H,W ---11111	ICR31[R/W] B,H,W ---11111	
000460 _H	ICR32[R/W] B,H,W ---11111	ICR33[R/W] B,H,W ---11111	ICR34[R/W] B,H,W ---11111	ICR35[R/W] B,H,W ---11111	
000464 _H	ICR36[R/W] B,H,W ---11111	ICR37[R/W] B,H,W ---11111	ICR38[R/W] B,H,W ---11111	ICR39[R/W] B,H,W ---11111	
000468 _H	ICR40[R/W] B,H,W ---11111	ICR41[R/W] B,H,W ---11111	ICR42[R/W] B,H,W ---11111	ICR43[R/W] B,H,W ---11111	
00046C _H	ICR44[R/W] B,H,W ---11111	ICR45[R/W] B,H,W ---11111	ICR46[R/W] B,H,W ---11111	ICR47[R/W] B,H,W ---11111	
000470 _H 00047C _H	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000480 _H	RSTRR[R] B,H,W XXXX--XX	RSTCR[R/W] B,H,W 111----0	STBCR[R/W] B,H,W 000---11 *	-	Reset control [S] Power consumption control [S] * Writing to STBCR by DMA is disabled.
000484 _H	-	-	-	-	Reserved [S]
000488 _H	DIVR0[R/W] B,H,W 000-----	-	DIVR2[R/W] B,H,W 0011----	-	Clock control [S]
00048C _H	-	-	-	-	Reserved [S]
000490 _H	IORR0[R/W] B,H,W -0000000	IORR1[R/W] B,H,W -0000000	IORR2[R/W] B,H,W -0000000	IORR3[R/W] B,H,W -0000000	DMA transfer request from a peripheral [S]
000494 _H	IORR4[R/W] B,H,W -0000000	IORR5[R/W] B,H,W -0000000	IORR6[R/W] B,H,W -0000000	IORR7[R/W] B,H,W -0000000	
000498 _H	-	-	-	-	
00049C _H	-	-	-	-	
0004A0 _H	-	-	-	-	Reserved
0004A4 _H	CANPRE[R/W] B,H,W ---00000	-	-	-	CAN prescaler
0004A8 _H 0004AC _H	-	-	-	-	Reserved
0004B0 _H	-	-	-	-	Reserved
0004B4 _H 0004C0 _H	-	-	-	-	Reserved
0004C4 _H	CUCR1[R/W] B,H,W -----0--00		CUTD1[R/W] B,H,W 11000011 01010000		WDT1 calibration
0004C8 _H	CUTR1[R] B,H,W ----- 00000000 00000000 00000000				
0004CC _H 0004DC _H	-	-	-	-	Reserved
0004E0 _H	-	-	CSCFG[R/W] B,H,W ---0----	CMCFG[R/W] B,H,W 00000000	Clock monitor
0004E4 _H	-	-	-	-	
0004E8 _H	PLL2DIVM[R/W] B,H,W ----0000	PLL2DIVN[R/W] B,H,W -0000000	PLL2DIVG[R/W] B,H,W ----0000	PLL2MULG[R/W] B,H,W 00000000	FlexRay clock control ⁵
0004EC _H	PLL2CTRL[R/W] B,H,W ----0000	PLL2DIVK[R/W] B,H,W B,H,W -----0	CLKR2[R/W] B,H,W 000--000	-	
0004F0 _H 0004FC _H	-	-	-	-	Reserved
000500 _H	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000504 _H	-				Reserved
000508 _H 00050C _H	-				Reserved
000510 _H	CSELR[R/W] B,H,W -0----00	CMONR[R] B,H,W -01---00	MTMCR[R/W] B,H,W 00001111	-	Clock control [S]
000514 _H	PLLCR[R/W] B,H,W 00-00000 11110000		CSTBR[R/W] B,H,W ----0000	PTMCR[R/W] B,H,W 00-----	
000518 _H	-	-	CPUAR[R/W] B,H,W 0---XXXX	-	Reset [S]
00051C _H	-				Reserved [S]
000520 _H	CCPSSELR[R/W] B,H,W -----0	-	-	CCPSDIVR[R/W] B,H,W -000-000	Clock control 2
000524 _H	-	CCPLLFB[R/W] B,H,W -0000000	CCSSFBR0[R/W] B,H,W --000000	CCSSFBR1[R/W] B,H,W ---00000	
000528 _H	-	CCSSCCR0[R/W] B,H,W ----0000	CCSSCCR1[R/W] B,H,W 000-----		
00052C _H	-	CCCGRCR0[R/W] B,H,W 00----00	CCCGRCR1[R/W] B,H,W 00000000	CCCGRCR2[R/W] B,H,W 00000000	
000530 _H	-	-	CCPMUCR0[R/W] B,H,W 0----00	CCPMUCR1[R/W] B,H,W 0--00000	
000534 _H	-	-	-	-	
000538 _H 00053C _H	-	-	-	-	
000540 _H 00054C _H	-				Reserved
000550 _H	EIRRO[R/W] B,H,W -XXXXXXX	ENIRO[R/W] B,H,W -0000000	ELVR0[R/W] B,H,W --000000 00000000		External interrupt (INT0 to 6)
000554 _H 000568 _H	-				Reserved
00056C _H	-	CSVCR[R/W] B -0-1--0	-	-	CSV
000570 _H	CRTR[R/W] B,H,W 01111111	-	-	-	WDT1 calibration (trimming)
000574 _H 00057C _H	-				Reserved
000580 _H	REGSEL[R/W] B,H,W 01--110-	-	-	-	Regulator control

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000584 _H	LVD5R[R/W] B,H,W -----1	LVD5F[R/W] B,H,W 001100-1	LVD[R/W] B,H,W 01000--0	-	Low-voltage detection
000588 _H 00058C _H	-	-	-	-	Reserved
000590 _H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00----	PWRMCTL[R/W] B,H,W -----011	-	PMU
000594 _H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00-----	-	
000598 _H	-	-	-	-	
00059C _H	-	-	-	-	
0005A0 _H 0005FC _H	-	-	-	-	Reserved
000600 _H 00060C _H	-	-	-	-	Reserved [S]
000610 _H 00063C _H	-	-	-	-	Reserved [S]
000640 _H 00064C _H	-	-	-	-	Reserved [S]
000650 _H 00067C _H	-	-	-	-	Reserved [S]
000680 _H 00068C _H	-	-	-	-	Reserved [S]
000690 _H 0006BC _H	-	-	-	-	Reserved [S]
0006C0 _H 0006CC _H	-	-	-	-	Reserved [S]
0006D0 _H 0006F0 _H	-	-	-	-	Reserved
0006F4 _H	-	-	-	-	Reserved
0006F8 _H 0006FC _H	-	-	-	-	Reserved
000700 _H	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000704 _H 00070C _H	-	-	-	-	Reserved
000710 _H	BPC CRA[R/W] B 00000000	BPC CRB[R/W] B 00000000	BPC CRC[R/W] B 00000000	-	Bus performance counter
000714 _H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718 _H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
00071C _H	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				
000720 _H 0007F8 _H	-	-	-	-	Reserved
0007FC _H	BMODR[R] B,H,W XXXXXXXX	-	-	-	Operation mode
000800 _H 00083C _H	-	-	-	-	Reserved [S]
000840 _H	FCTLR[R/W] H -0--1000 0--0----		-	FSTR[R/W] B -----001	Flash memory register [S]
000844 _H	-	-	-	-	Reserved [S]
000848 _H 000854 _H	-	-	-	-	Reserved [S]
000858 _H	-	-	WREN[R/W] H 00000000 00000000		Wild register [S]
00085C _H 00087C _H	-	-	-	-	Reserved [S]
000880 _H	WRAR00[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884 _H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888 _H	WRAR01[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
00088C _H	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890 _H	WRAR02[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
000894 _H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898 _H	WRAR03[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
00089C _H	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0008A0 _H	WRAR04[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
0008A4 _H	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008A8 _H	WRAR05[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008AC _H	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B0 _H	WRAR06[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008B4 _H	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B8 _H	WRAR07[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008BC _H	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C0 _H	WRAR08[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008C4 _H	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C8 _H	WRAR09[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008CC _H	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D0 _H	WRAR10[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008D4 _H	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D8 _H	WRAR11[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008DC _H	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E0 _H	WRAR12[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008E4 _H	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E8 _H	WRAR13[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008EC _H	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F0 _H	WRAR14[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				
0008F4 _H	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F8 _H	WRAR15[R/W] W ----- --XXXXXX XXXXXXXX XXXXXX--				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0008FC _H	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild register [S]
000900 _H 000BF8 _H	-	-	-	-	Reserved
000BFC _H	-		UER[W] B,H,W -----X		OCDU
000C00 _H	DCCR0[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
000C04 _H	DCSR0[R/W] H 0-----000		DTCR0[R/W] H 00000000 00000000		
000C08 _H	DSAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C0C _H	DDAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C10 _H	DCCR1[R/W] W 0----000 --00--00 00000000 0-000000				
000C14 _H	DCSR1[R/W] H 0-----000		DTCR1[R/W] H 00000000 00000000		
000C18 _H	DSAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C1C _H	DDAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C20 _H	DCCR2[R/W] W 0----000 --00--00 00000000 0-000000				
000C24 _H	DCSR2[R/W] H 0-----000		DTCR2[R/W] H 00000000 00000000		
000C28 _H	DSAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C2C _H	DDAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C30 _H	DCCR3[R/W] W 0----000 --00--00 00000000 0-000000				
000C34 _H	DCSR3[R/W] H 0-----000		DTCR3[R/W] H 00000000 00000000		
000C38 _H	DSAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C3C _H	DDAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C40 _H	DCCR4[R/W] W 0----000 --00--00 00000000 0-000000				
000C44 _H	DCSR4[R/W] H 0-----000		DTCR4[R/W] H 00000000 00000000		

Address	Address offset value/Register name				Block	
	+0	+1	+2	+3		
000C48 _H	DSAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA controller [S]	
000C4C _H	DDAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000C50 _H	DCCR5[R/W] W 0----000 --00--00 00000000 0-000000					
000C54 _H	DCSR5[R/W] H 0----- ----000		DTCR5[R/W] H 00000000 00000000			
000C58 _H	DSAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000C5C _H	DDAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000C60 _H	DCCR6[R/W] W 0----000 --00--00 00000000 0-000000					
000C64 _H	DCSR6[R/W] H 0----- ----000		DTCR6[R/W] H 00000000 00000000			
000C68 _H	DSAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000C6C _H	DDAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000C70 _H	DCCR7[R/W] W 0----000 --00--00 00000000 0-000000					
000C74 _H	DCSR7[R/W] H 0----- ----000		DTCR7[R/W] H 00000000 00000000			
000C78 _H	DSAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000C7C _H	DDAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000C80 _H 000DF0 _H	-	-	-	-		
000DF4 _H	-	-	DNMIR[R/W] B 0-----0	DILVR[R/W] B ---11111		
000DF8 _H	DMACR[R/W] W 0----- ----0 0----- ----0					
000DFC _H	-	-	-	-		Reserved [S]
000E00 _H	-	DDR01[R/W] B,H 00000000	DDR02[R/W] B,H 00000000	DDR03[R/W] B,H 00000000		Data direction register
000E04 _H	DDR04[R/W] B,H 00000000	DDR05[R/W] B,H -0000000	-	DDR07[R/W] B,H ----000		
000E08 _H	-	DDR09[R/W] B,H ---00---	-	-		
000E0C _H	-	-	-	-		
000E10 _H 000E1C _H	-	-	-	-	Reserved	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000E20 _H	-	PFR01[R/W] B,H 00000000	PFR02[R/W] B,H 00000000	PFR03[R/W] B,H 00000000	Port function register
000E24 _H	PFR04[R/W] B,H 00000000	PFR05[R/W] B,H -0000000	-	PFR07[R/W] B,H -----000	
000E28 _H	-	PFR09[R/W] B,H ---00---	-	-	
000E2C _H	-	-	-	-	
000E30 _H 000E3C _H	-	-	-	-	Reserved
000E40 _H	-	PDDR01[R] B,H,W XXXXXXXX	PDDR02[R] B,H,W XXXXXXXX	PDDR03[R] B,H,W XXXXXXXX	Input data direct read register
000E44 _H	PDDR04[R] B,H,W XXXXXXXX	PDDR05[R] B,H,W -XXXXXXXX	-	PDDR07[R] B,H,W -----XXX	
000E48 _H	-	PDDR09[R] B,H,W ---XX---	-	-	
000E4C _H	-	-	-	-	
000E50 _H 000E5C _H	-	-	-	-	Reserved
000E60 _H	EPFR00[R/W] B,H -----0	EPFR01[R/W] B,H -----00	EPFR02[R/W] B,H -----000	EPFR03[R/W] B,H --000000	Extended port function register
000E64 _H	-	-	EPFR06[R/W] B,H -----00	EPFR07[R/W] B,H ----0000	
000E68 _H	EPFR08[R/W] B,H *5 ----0000	EPFR09[R/W] B,H -----0	EPFR10[R/W] B,H -0000000	-	
000E6C _H	-	-	-	-	
000E70 _H	-	-	-	-	
000E74 _H	-	-	-	-	
000E78 _H	-	-	-	-	
000E7C _H	-	-	-	-	
000E80 _H	-	-	-	-	
000E84 _H 000EBC _H	-	-	-	-	
000EC0 _H	-	PPER01[R/W] B,H 00000000	PPER02[R/W] B,H 00000000	PPER03[R/W] B,H 00000000	Port pull-up/down enable register
000EC4 _H	PPER04[R/W] B,H 00000000	PPER05[R/W] B,H -0000000	-	PPER07[R/W] B,H -----000	
000EC8 _H	-	PPER09[R/W] B,H ---00---	-	-	
000ECC _H	-	-	-	-	
000ED0 _H 000EDC _H	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000EE0 _H	-	PILR01[R/W] B,H 11111111	PILR02[R/W] B,H 11111111	PILR03[R/W] B,H 11111111	Port input level selection register
000EE4 _H	PILR04[R/W] B,H 11111111	PILR05[R/W] B,H -1111111	-	PILR07[R/W] B,H -----111	
000EE8 _H	-	PILR09[R/W] B,H ---11---	-	-	
000EEC _H	-	-	-	-	
000EF0 _H 000EFC _H	-	-	-	-	Reserved
000F00 _H 000F1C _H	-	-	-	-	Reserved
000F20 _H	-	PODR01[R/W] B,H 00000000	PODR02[R/W] B,H 00000000	PODR03[R/W] B,H 00000000	Port output drive register
000F24 _H	PODR04[R/W] B,H 00000000	PODR05[R/W] B,H -0000000	-	PODR07[R/W] B,H -----000	
000F28 _H	-	PODR09[R/W] B,H ---00---	-	-	
000F2C _H	-	-	-	-	
000F30 _H 000F3C _H	-	-	-	-	Reserved
000F40 _H	PORTEN[R/W] B,H,W -----00	-	-	-	Port input enable register
000F44 _H	KEYCDR[R/W] H 00000000 00000000		-	-	Port key code
000F48 _H	ADERH[R/W] B,H -----11---		ADERL[R/W] B,H -1111111 11111111		Analog input enable register
000F4C _H	DAER[R/W] B,H -----0	-	-	-	Analog output enable register
000F50 _H 000FFC _H	-	-	-	-	Reserved
001000 _H	SACR[R/W] B,H,W -----0	PICD[R/W] B,H,W ----0011	-	-	Synchronous/asynchronous switch control
001004 _H 0010BC _H	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0010C0 _H	-	-	-	CRCCR[R/W] B,H,W -0000000	CRC arithmetic operation 0
0010C4 _H	CRCINIT[R/W] B,H,W 11111111 11111111 11111111 11111111				
0010C8 _H	CRCIN[R/W] B,H,W 00000000 00000000 00000000 00000000				
0010CC _H	CRCCR[R] B,H,W 11111111 11111111 11111111 11111111				
0010D0 _H	-	-	-	CRCCR1[R/W] B,H,W -0000000	CRC arithmetic operation 1
0010D4 _H	CRCINIT1[R/W] B,H,W 11111111 11111111 11111111 11111111				
0010D8 _H	CRCIN1[R/W] B,H,W 00000000 00000000 00000000 00000000				
0010DC _H	CRCCR1[R] B,H,W 11111111 11111111 11111111 11111111				
0010E0 _H 0010FC _H	-	-	-	-	Reserved
001100 _H	TCGS[R/W] B,H,W -----00	-	-	TCGSE[R/W] B,H,W --000000	Free-run timer simultaneous activation
001104 _H	CPCLRB0/CPCLR0[R/W] H,W 11111111 11111111		TCDT0[R/W] H,W 00000000 00000000		Free-run timer 0
001108 _H	TCCS0[R/W] B,H,W 00000000 01000000 ----0000 -----				
00110C _H	CPCLRB1/CPCLR1[R/W] H,W 11111111 11111111		TCDT1[R/W] H,W 00000000 00000000		Free-run timer 1
001110 _H	TCCS1[R/W] B,H,W 00000000 01000000 ----0000 -----				
001114 _H	CPCLRB2/CPCLR2[R/W] H,W 11111111 11111111		TCDT2[R/W] H,W 00000000 00000000		Free-run timer 2
001118 _H	TCCS2[R/W] B,H,W 00000000 01000000 ----0000 -----				
00111C _H	CPCLRB3/CPCLR3[R/W] H,W 11111111 11111111		TCDT3[R/W] H,W 00000000 00000000		Free-run timer 3
001120 _H	TCCS3[R/W] B,H,W 00000000 01000000 ----0000 -----				
001124 _H	CPCLRB4/CPCLR4[R/W] H,W 11111111 11111111		TCDT4[R/W] H,W 00000000 00000000		Free-run timer 4
001128 _H	TCCS4[R/W] B,H,W 00000000 01000000 ----0000 -----				
00112C _H	CPCLRB5/CPCLR5[R/W] H,W 11111111 11111111		TCDT5[R/W] H,W 00000000 00000000		Free-run timer 5
001130 _H	TCCS5[R/W] B,H,W 00000000 01000000 ----0000 -----				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001134 _H	FRS0[R/W] B,H,W ----- -000-000 -000-000 -000-000				Free-run timer selection
001138 _H	FRS1[R/W] B,H,W ----- -000-000 -000-000				
00113C _H	FRS2[R/W] B,H,W ----- -000-000 -000-000 -000-000				
001140 _H	-				
001144 _H	FRS4[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001148 _H	FRS5[R/W] B,H,W ----000 -000-000 -000-000 -000-000				
00114C _H	FRS6[R/W] B,H,W ----- -000 -000-----				
001150 _H	-				
001154 _H	OCCPB0/OCCP0[R/W] H,W 00000000 00000000		OCCPB1/OCCP1[R/W] H,W 00000000 00000000		Output compare 0/1
001158 _H	OCS01[R/W] B,H,W -110--00 00001100		-	OCMOD01[R/W] B,H,W -----00	
00115C _H	OCCPB2/OCCP2[R/W] H,W 00000000 00000000		OCCPB3/OCCP3[R/W] H,W 00000000 00000000		Output compare 2/3
001160 _H	OCS23[R/W] B,H,W -110--00 00001100		-	OCMOD23[R/W] B,H,W -----00	
001164 _H	OCCPB4/OCCP4[R/W] H,W 00000000 00000000		OCCPB5/OCCP5[R/W] H,W 00000000 00000000		Output compare 4/5
001168 _H	OCS45[R/W] B,H,W -110--00 00001100		-	OCMOD45[R/W] B,H,W -----00	
00116C _H	OCCPB6/OCCP6[R/W] H,W 00000000 00000000		OCCPB7/OCCP7[R/W] H,W 00000000 00000000		Output compare 6/7
001170 _H	OCS67[R/W] B,H,W -110--00 00001100		-	OCMOD67[R/W] B,H,W -----00	
001174 _H	OCCPB8/OCCP8[R/W] H,W 00000000 00000000		OCCPB9/OCCP9[R/W] H,W 00000000 00000000		Output compare 8/9
001178 _H	OCS89[R/W] B,H,W -110--00 00001100		-	OCMOD89[R/W] B,H,W -----00	
00117C _H	OCCPB10/OCCP10[R/W] H,W 00000000 00000000		OCCPB11/OCCP11[R/W] H,W 00000000 00000000		Output compare 10/11
001180 _H	OCS1011[R/W] B,H,W -110--00 00001100		-	OCMOD1011 [R/W] B,H,W -----00	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001184 _H	IPCP0[R] H,W 00000000 00000000		IPCP1[R] H,W 00000000 00000000		Input capture 0/1
001188 _H	ICS01[R/W] B,H,W -----00 00000000		-	LSYNS[R/W] B,H,W -----00	
00118C _H	IPCP2[R] H,W 00000000 00000000		IPCP3[R] H,W 00000000 00000000		Input capture 2/3
001190 _H	ICS23[R/W] B,H,W -----00 00000000		-	-	
001194 _H	-				Reserved
001198 _H	-				
00119C _H	-				Reserved
0011A0 _H	-				
0011A4 _H	DTSR[R/W] B,H,W -----10	-	-	-	DTTI selection
0011A8 _H	TMRR0[R/W] H,W 00000000 00000001		TMRR1[R/W] H,W 00000000 00000001		Waveform generator 0/1/2
0011AC _H	TMRR2[R/W] H,W 00000000 00000001		-	-	
0011B0 _H	DTSCR0[R/W] B,H,W 00000000	DTSCR1[R/W] B,H,W 00000000	DTSCR2[R/W] B,H,W 00000000	-	
0011B4 _H	-	DTIR0[R/W] B,H,W 000000--	-	DTMNS0[R/W] B,H,W 00--000	
0011B8 _H	-	SIGCR10[R/W] B,H,W 00000000	-	SIGCR20[R/W] B,H,W 000000-1	
0011BC _H	PICS0[R/W] B,H,W 000000-- -----				
0011C0 _H	TMRR3[R/W] H,W 00000000 00000001		TMRR4[R/W] H,W 00000000 00000001		Waveform generator 3/4/5
0011C4 _H	TMRR5[R/W] H,W 00000000 00000001		-	-	
0011C8 _H	DTSCR3[R/W] B,H,W 00000000	DTSCR4[R/W] B,H,W 00000000	DTSCR5[R/W] B,H,W 00000000	-	
0011CC _H	-	DTIR1[R/W] B,H,W 000000--	-	DTMNS1[R/W] B,H,W 00--000	
0011D0 _H	-	SIGCR11[R/W] B,H,W 00000000	-	SIGCR21[R/W] B,H,W -----1	
0011D4 _H	-				
0011D8 _H	-				
0011DC _H	ADTSS[R/W] B,H,W -----0	-	-	-	12-bit A/D converter
0011E0 _H	ADTSE[R/W] B,H,W ----- --00--- -0000000 00000000				
0011E4 _H	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0011E8 _H	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		12-bit A/D converter
0011EC _H	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		
0011F0 _H	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		
0011F4 _H	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		
0011F8 _H	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		
0011FC _H	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		
001200 _H	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		-		
001204 _H	-		-		
001208 _H	-		ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000		
00120C _H	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000		-		
001210 _H	-		-		
001214 _H	-	-	-	-	
001218 _H	-	-	-	-	
00121C _H	-	-	-	-	
001220 _H	-	-	-	-	
001224 _H	ADTCS0[R/W] B,H,W 00000000 0010-000		ADTCS1[R/W] B,H,W 00000000 0010-000		
001228 _H	ADTCS2[R/W] B,H,W 00000000 0010-000		ADTCS3[R/W] B,H,W 00000000 0010-000		
00122C _H	ADTCS4[R/W] B,H,W 00000000 0010-000		ADTCS5[R/W] B,H,W 00000000 0010-000		
001230 _H	ADTCS6[R/W] B,H,W 00000000 0010-000		ADTCS7[R/W] B,H,W 00000000 0010-000		
001234 _H	ADTCS8[R/W] B,H,W 00000000 0010-000		ADTCS9[R/W] B,H,W 00000000 0010-000		
001238 _H	ADTCS10[R/W] B,H,W 00000000 0010-000		ADTCS11[R/W] B,H,W 00000000 0010-000		
00123C _H	ADTCS12[R/W] B,H,W 00000000 0010-000		ADTCS13[R/W] B,H,W 00000000 0010-000		
001240 _H	ADTCS14[R/W] B,H,W 00000000 0010-000		-		
001244 _H	-		-		
001248 _H	-		ADTCS19[R/W] B,H,W 00000000 00100000		
00124C _H	ADTCS20[R/W] B,H,W 00000000 00100000		-		
001250 _H	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001254 _H	-	-	-	-	12-bit A/D converter
001258 _H	-	-	-	-	
00125C _H	-	-	-	-	
001260 _H	-	-	-	-	
001264 _H	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001268 _H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		
00126C _H	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001270 _H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
001274 _H	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
001278 _H	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
00127C _H	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
001280 _H	ADTCD14[R] B,H,W 10--0000 00000000		-		
001284 _H	-		-		
001288 _H	-		ADTCD19[R] B,H,W 10--0000 00000000		
00128C _H	ADTCD20[R] B,H,W 10--0000 00000000		-		
001290 _H	-		-		
001294 _H	-	-	-	-	
001298 _H	-	-	-	-	
00129C _H	-	-	-	-	
0012A0 _H	-	-	-	-	
0012A4 _H	ADCS0[R/W] B,H,W 0-----		ADCH0[R] B,H,W -----000	ADMD0[R/W] B,H,W ----0000	
0012A8 _H	ADCS1[R/W] B,H,W 0-----		ADCH1[R] B,H,W -----000	ADMD1[R/W] B,H,W ----0000	
0012AC _H	ADCS2[R/W] B,H,W 0-----		ADCH2[R] B,H,W -----000	ADMD2[R/W] B,H,W ----0000	
0012B0 _H	MTRCSR[R/W] B,H,W -----0	-	-	-	
0012B4 _H	RTOSEL0[R/W] B,H,W --000000	RTOSEL1[R/W] B,H,W -----0	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0012B8 _H 0012FC _H	-	-	-	-	Reserved
001300 _H	-	-	-	-	Reserved
001304 _H	-	-	-	-	
001308 _H	-	-	-	-	
00130C _H	-	-	-	-	
001310 _H	-	-	-	-	
001314 _H	-	-	-	-	
001318 _H	-	-	-	-	
00131C _H	-	-	-	-	
001320 _H	-	-	-	-	
001324 _H	-	-	-	-	
001328 _H 00132C _H	-	-	-	-	
001330 _H	-	-	-	-	
001334 _H 0013FC _H	-	-	-	-	Reserved
001400 _H	DACR[R/W] B,H,W -----0	-	DADR[R/W] H,W -----XX XXXXXXXX	-	DAC
001404 _H 0014FC _H	-	-	-	-	Reserved
001500 _H	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000000-0	SSR0 [R/W] B,H,W 0--00011	ESCR0/(IBSR0) [R/W] B,H,W 00000000	Multi Function Serial I/F 0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I ² C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001504 _H	-/(RDR10/(TDR10))[R/W] B,H,W ----- *3		RDR00/(TDR00)[R/W] B,H,W -----0 00000000 *1		
001508 _H	SACSR0[R/W] B,H,W 0----000 00000000		STMCR0[R] B,H,W 00000000 00000000		
00150C _H	STMCR0[R/W] B,H,W 00000000 00000000		-/(SFUR0) [R/W] B,H,W ----- *4		
001510 _H	-	-	-/(SFLR10) [R/W] B,H,W ----- *4	-/(SFLR00) [R/W] B,H,W ----- *4	
001514 _H	-	-	-	-	
001518 _H	-	-	-	-	
00151C _H	BGR0[R/W] H,W 00000000 00000000		-/(ISMK0)[R/W] B,H,W ----- *2	-/(ISBA0)[R/W] B,H,W ----- *2	
001520 _H	FCR10[R/W] B,H,W 00-00100	FCR00[R/W] B,H,W -0000000	FBYTE20[R/W] B,H,W 00000000	FBYTE10[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001524 _H	SCR1[R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000000-0	SSR1[R/W] B,H,W 0--00011	ESCR1[R/W] B,H,W 00000000	Multi Function Serial I/F 1 *1: Byte access is possible only for access to lower 8 bits. *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001528 _H	-/(RDR11/(TDR11))[R/W] B,H,W ----- *3		RDR01/(TDR01)[R/W] B,H,W -----0 00000000 *1		
00152C _H	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		
001530 _H	STMCR1[R/W] B,H,W 00000000 00000000		-/(SCSCR1/SFUR1) [R/W] B,H,W ----- *3 *4		
001534 _H	-/(SCSTR31) [R/W] B,H,W ----- *3	-/(SCSTR21) [R/W] B,H,W ----- *3	-/(SCSTR11/ SFLR11) [R/W] B,H,W ----- *3 *4	-/(SCSTR01/ SFLR01) [R/W] B,H,W ----- *3 *4	
001538 _H	-	-	-	-	
00153C _H	-	-	-	TBYTE01[R/W] B,H,W 00000000	
001540 _H	BGR1[R/W] H,W 00000000 00000000		-	-	
001544 _H	FCR11[R/W] B,H,W 00-00100	FCR01[R/W] B,H,W -0000000	FBYTE21[R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	
001548 _H 001FFC _H	-	-	-	-	
002000 _H	CTRLR0[R/W] B,H,W ----- 000-0001		STATR0[R/W] B,H,W ----- 00000000		CAN 0 64msb
002004 _H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0[R/W] B,H,W -0100011 00000001		
002008 _H	INTRO[R] B,H,W 00000000 00000000		TESTR0[R/W] B,H,W ----- X00000--		
00200C _H	BRPER0[R/W] B,H,W ----- ----0000		-		
002010 _H	IF1CREQ0[R/W] B,H,W 0----- 00000001		IF1CMSK0[R/W] B,H,W ----- 00000000		
002014 _H	IF1MSK20[R/W] B,H,W 11-11111 11111111		IF1MSK10[R/W] B,H,W 11111111 11111111		
002018 _H	IF1ARB20[R/W] B,H,W 00000000 00000000		IF1ARB10[R/W] B,H,W 00000000 00000000		
00201C _H	IF1MCTR0[R/W] B,H,W 00000000 0---0000		-		
002020 _H	IF1DTA10[R/W] B,H,W 00000000 00000000		IF1DTA20[R/W] B,H,W 00000000 00000000		
002024 _H	IF1DTB10[R/W] B,H,W 00000000 00000000		IF1DTB20[R/W] B,H,W 00000000 00000000		
002028 _H , 00202C _H	-		-		
002030 _H , 002034 _H	Reserved (IF1 data mirror)				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002038 _H , 00203C _H	-	-	-	-	CAN 0 64msb
002040 _H	IF2CREQ0[R/W] B,H,W 0----- 00000001		IF2CMSK0[R/W] B,H,W ----- 00000000		
002044 _H	IF2MSK20[R/W] B,H,W 11-11111 11111111		IF2MSK10[R/W] B,H,W 11111111 11111111		
002048 _H	IF2ARB20[R/W] B,H,W 00000000 00000000		IF2ARB10[R/W] B,H,W 00000000 00000000		
00204C _H	IF2MCTR0[R/W] B,H,W 00000000 0---0000		-		
002050 _H	IF2DTA10[R/W] B,H,W 00000000 00000000		IF2DTA20[R/W] B,H,W 00000000 00000000		
002054 _H	IF2DTB10[R/W] B,H,W 00000000 00000000		IF2DTB20[R/W] B,H,W 00000000 00000000		
002058 _H , 00205C _H	-		-		
002060 _H , 002064 _H	Reserved (IF2 data mirror)				
002068 _H 00207C _H	-		-		
002080 _H	TREQR20[R] B,H,W 00000000 00000000		TREQR10[R] B,H,W 00000000 00000000		
002084 _H	TREQR40[R] B,H,W 00000000 00000000		TREQR30[R] B,H,W 00000000 00000000		
002088 _H	-		-		
00208C _H	-		-		
002090 _H	NEWDT20[R] B,H,W 00000000 00000000		NEWDT10[R] B,H,W 00000000 00000000		
002094 _H	NEWDT40[R] B,H,W 00000000 00000000		NEWDT30[R] B,H,W 00000000 00000000		
002098 _H	-		-		
00209C _H	-		-		
0020A0 _H	INTPND20[R] B,H,W 00000000 00000000		INTPND10[R] B,H,W 00000000 00000000		
0020A4 _H	INTPND40[R] B,H,W 00000000 00000000		INTPND30[R] B,H,W 00000000 00000000		
0020A8 _H	-		-		
0020AC _H	-		-		
0020B0 _H	MSGVAL20[R] B,H,W 00000000 00000000		MSGVAL10[R] B,H,W 00000000 00000000		
0020B4 _H	MSGVAL40[R] B,H,W 00000000 00000000		MSGVAL30[R] B,H,W 00000000 00000000		
0020B8 _H	-		-		
0020BC _H	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0020C0 _H 0020FC _H	-	-	-	-	CAN 0 64msb
002100 _H 0022FC _H	-	-	-	-	Reserved
002300 _H	DFCTLR[R/W] B,H,W -0-----		-	DFSTR[R/W] B,H,W ----001	WorkFlash
002304 _H	-	-	-	-	
002308 _H	FLIFCTLR[R/W] B,H,W ---0--00	-	FLIFFER1[R/W] B,H,W -----	FLIFFER2[R/W] B,H,W -----	
00230C _H 002FFC _H	-	-	-	-	Reserved
003000 _H	SEEARX[R] B,H,W --000000 00000000		DEEARX[R] B,H,W --000000 00000000		XBS RAM ECC control register
003004 _H	EECSR[R/W] B,H,W ----00-0	-	EFEARX[R/W] B,H,W --000000 00000000		
003008 _H	-	EFECRX[R/W] B,H,W -----0 00000000 00000000			
00300C _H	TEAR0X[R] B,H,W 000----- --000000 00000000				XBS RAM diagnosis register
003010 _H	TEAR1X[R] B,H,W 000----- --000000 00000000				
003014 _H	TEAR2X[R] B,H,W 000----- --000000 00000000				
003018 _H	TAEARX[R/W] B,H,W --101111 11111111		TASARX[R/W] B,H,W --000000 00000000		
00301C _H	TFECRX[R/W] B,H,W ----0000	TICRX[R/W] B,H,W ----0000	TTCRX[R/W] B,H,W -----00 00001100		
003020 _H	TSRCRX[R/W] B,H,W 0-----	-	-	TKCCRX[R/W] B,H,W 00----00	
003024 _H	SEEARA[R] B,H,W --000000 00000000		DEEARA[R] B,H,W --000000 00000000		Backup RAM ECC control register
003028 _H	EECSRA[R/W] B,H,W ----00-0	-	EFEARA[R/W] B,H,W --000000 00000000		
00302C _H	-	EFECRA[R/W] B,H,W -----0 00000000 00000000			

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
003030 _H	TEAR0A[R] B,H,W 000-----000 00000000				Backup RAM diagnosis register
003034 _H	TEAR1A[R] B,H,W 000-----000 00000000				
003038 _H	TEAR2A[R] B,H,W 000-----000 00000000				
00303C _H	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		
003040 _H	TFECRA[R/W] B,H,W ----0000	TICRA[R/W] B,H,W ----0000	TTCRA[R/W] B,H,W -----00 00001100		
003044 _H	TSRCRA[R/W] B,H,W 0-----	-	-	TKCCRA[R/W] B,H,W 00----00	
003048 _H 0030FC _H	-	-	-	-	Reserved
003100 _H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		Bus diagnosis
003104 _H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108 _H	BUSADR0[R] W 00000000 00000000 00000000 00000000				
00310C _H	BUSADR1[R] W 00000000 00000000 00000000 00000000				
003110 _H	BUSADR2[R] W 00000000 00000000 00000000 00000000				
003114 _H	-		BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118 _H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--0000 00000000		
00311C _H	-				
003120 _H	BUSADR3[R] W 00000000 00000000 00000000 00000000				
003124 _H	BUSADR4[R] W 00000000 00000000 00000000 00000000				
003128 _H 003FFC _H	-	-	-	-	Reserved
004000 _H 005FFC _H	Backup RAM				Backup RAM area
006000 _H 00CFFC _H	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D000 _H	CIF0[R] W 00000100 11111111 01011011 11111111				FlexRay CIF ^{*5}
00D004 _H	CIF1[R/W] W 00000000 -----0 -0000000 -----				
00D008 _H 00D00C _H	-	-	-	-	Reserved
00D010 _H	-				FlexRay GIF ^{*5}
00D014 _H	-				
00D018 _H	-	-	-	-	
00D01C _H	LCK[R/W] W ----- 00000000				FlexRay INT ^{*5}
00D020 _H	EIR[R/W] W ----000 ----000 ----0000 00000000				
00D024 _H	SIR[R/W] W ----00 ----00 00000000 00000000				
00D028 _H	EILS[R/W] W ----000 ----000 ----0000 00000000				
00D02C _H	SILS[R/W] W ----11 ----11 11111111 11111111				
00D030 _H	EIES[R/W] W ----000 ----000 ----0000 00000000				
00D034 _H	EIER[R/W] W ----000 ----000 ----0000 00000000				
00D038 _H	SIES[R/W] W ----00 ----00 00000000 00000000				
00D03C _H	SIER[R/W] W ----00 ----00 00000000 00000000				
00D040 _H	ILE[R/W] W ----- -----00				
00D044 _H	TOC[R/W] W --000000 00000000 -0000000 -----00				
00D048 _H	T1C[R/W] W --000000 00000010 -----00				
00D04C _H	STPW1[R/W] W --000000 00000000 --000000 -0000000				
00D050 _H	STPW2[R] W ----000 00000000 ----000 00000000				
00D054 _H 00D07C _H	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D080 _H	SUCC1[R/W] W ----1100 01000000 00010-00 1---0000				FlexRay SUC ^{*5}
00D084 _H	SUCC2[R/W] W ----0001 ---00000 00000101 00000100				
00D088 _H	SUCC3[R/W] W ----- ----- 00010001				
00D08C _H	NEMC[R/W] W ----- ----- -0000				FlexRay NEM ^{*5}
00D090 _H	PRTC1[R/W] W 000010-0 01001100 0000-110 00110011				FlexRay PRT ^{*5}
00D094 _H	PRTC2[R/W] W --001111 00101101 --001010 --001110				
00D098 _H	MHDC[R/W] W ---00000 00000000 ----- -0000000				FlexRay MHD ^{*5}
00D09C _H	-				Reserved
00D0A0 _H	GTUC1[R/W] W ----- -0000 00000010 10000000				FlexRay GTU ^{*5}
00D0A4 _H	GTUC2[R/W] W ----- -0010 --000000 00001010				
00D0A8 _H	GTUC3[R/W] W -0000010 -0000010 00000000 00000000				
00D0AC _H	GTUC4[R/W] W --000000 00001000 --000000 00000111				
00D0B0 _H	GTUC5[R/W] W 00001110 ---00000 00000000 00000000				
00D0B4 _H	GTUC6[R/W] W ----000 00000010 -----000 00000000				
00D0B8 _H	GTUC7[R/W] W -----00 00000010 -----00 00000100				
00D0BC _H	GTUC8[R/W] W ---00000 00000000 ----- --000010				
00D0C0 _H	GTUC9[R/W] W ----- -00 ---00001 --000001				
00D0C4 _H	GTUC10[R/W] W ----000 00000010 --000000 00000101				
00D0C8 _H	GTUC11[R/W] W ----000 ----000 -----00 -----00				
00D0CC _H 00D0FC _H	-				Reserved
00D100 _H	CCSV[R] W --000000 00010000 -100--00 00000000				FlexRay SUC ^{*5}
00D104 _H	CCEV[R] W ----- ----- ---00000 00--0000				
00D108 _H 00D10C _H	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D110 _H	SCV[R] W -----000 00000000 -----000 00000000				FlexRay GTU ^{*5}
00D114 _H	MTCCV[R] W ----- --000000 --000000 00000000				
00D118 _H	RCV[R] W ----- ----- ----0000 00000000				
00D11C _H	OCV[R] W ----- ----000 00000000 00000000				
00D120 _H	SFS[R] W ----- ----0000 00000000 00000000				
00D124 _H	SWNIT[R] W ----- ----- ----0000 00000000				
00D128 _H	ACS[R/W] W ----- ----- ---00000 ---00000				
00D12C _H	-				
00D130 _H	ESID1[R] W ----- ----- 00----00 00000000				
00D134 _H	ESID2[R] W ----- ----- 00----00 00000000				
00D138 _H	ESID3[R] W ----- ----- 00----00 00000000				
00D13C _H	ESID4[R] W ----- ----- 00----00 00000000				
00D140 _H	ESID5[R] W ----- ----- 00----00 00000000				
00D144 _H	ESID6[R] W ----- ----- 00----00 00000000				
00D148 _H	ESID7[R] W ----- ----- 00----00 00000000				
00D14C _H	ESID8[R] W ----- ----- 00----00 00000000				
00D150 _H	ESID9[R] W ----- ----- 00----00 00000000				
00D154 _H	ESID10[R] W ----- ----- 00----00 00000000				
00D158 _H	ESID11[R] W ----- ----- 00----00 00000000				
00D15C _H	ESID12[R] W ----- ----- 00----00 00000000				
00D160 _H	ESID13[R] W ----- ----- 00----00 00000000				
00D164 _H	ESID14[R] W ----- ----- 00----00 00000000				
00D168 _H	ESID15[R] W ----- ----- 00----00 00000000				
00D16C _H	-				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D170 _H	OSID1[R] W ----- 00---00 00000000				FlexRay GTU *5
00D174 _H	OSID2[R] W ----- 00---00 00000000				
00D178 _H	OSID3[R] W ----- 00---00 00000000				
00D17C _H	OSID4[R] W ----- 00---00 00000000				
00D180 _H	OSID5[R] W ----- 00---00 00000000				
00D184 _H	OSID6[R] W ----- 00---00 00000000				
00D188 _H	OSID7[R] W ----- 00---00 00000000				
00D18C _H	OSID8[R] W ----- 00---00 00000000				
00D190 _H	OSID9[R] W ----- 00---00 00000000				
00D194 _H	OSID10[R] W ----- 00---00 00000000				
00D198 _H	OSID11[R] W ----- 00---00 00000000				
00D19C _H	OSID12[R] W ----- 00---00 00000000				
00D1A0 _H	OSID13[R] W ----- 00---00 00000000				
00D1A4 _H	OSID14[R] W ----- 00---00 00000000				
00D1A8 _H	OSID15[R] W ----- 00---00 00000000				
00D1AC _H	-				Reserved
00D1B0 _H	NMV1[R] W 00000000 00000000 00000000 00000000				FlexRay NEM *5
00D1B4 _H	NMV2[R] W 00000000 00000000 00000000 00000000				
00D1B8 _H	NMV3[R] W 00000000 00000000 00000000 00000000				
00D1BC _H 00D2FC _H	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D300 _H	MRC[R/W] W -----001 10000000 00000000 00000000				FlexRay MHD *5
00D304 _H	FRF[R/W] W -----1 10000000 ---00000 00000000				
00D308 _H	FRFM[R/W] W ----- ----- ---00000 000000--				
00D30C _H	FCL[R/W] W ----- ----- 10000000				
00D310 _H	MHDS[R/W] W -0000000 -0000000 -0000000 00000000				
00D314 _H	LDTS[R] W -----000 00000000 -----000 00000000				
00D318 _H	FSR[R] W ----- ----- 00000000 -----000				
00D31C _H	MHDF[R/W] W ----- -----0 00000000				
00D320 _H	TXRQ1[R] W 00000000 00000000 00000000 00000000				
00D324 _H	TXRQ2[R] W 00000000 00000000 00000000 00000000				
00D328 _H	TXRQ3[R] W 00000000 00000000 00000000 00000000				
00D32C _H	TXRQ4[R] W 00000000 00000000 00000000 00000000				
00D330 _H	NDAT1[R] W 00000000 00000000 00000000 00000000				
00D334 _H	NDAT2[R] W 00000000 00000000 00000000 00000000				
00D338 _H	NDAT3[R] W 00000000 00000000 00000000 00000000				
00D33C _H	NDAT4[R] W 00000000 00000000 00000000 00000000				
00D340 _H	MBSC1[R] W 00000000 00000000 00000000 00000000				
00D344 _H	MBSC2[R] W 00000000 00000000 00000000 00000000				
00D348 _H	MBSC3[R] W 00000000 00000000 00000000 00000000				
00D34C _H	MBSC4[R] W 00000000 00000000 00000000 00000000				
00D350 _H 00D3EC _H	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00D3F0 _H	CREL[R] W 00010000 00111001 00000010 00000110				FlexRay GIF ^{*5}
00D3F4 _H	ENDN[R] W 10000111 01100101 01000011 00100001				
00D3F8 _H 00D3FC _H	-				Reserved
00D400 _H 00D4FC _H	WRDSn[1-64][R/W] W 00000000 00000000 00000000 00000000				FlexRay IBF ^{*5}
00D500 _H	WRHS1[R/W] W --000000 -0000000 -----000 00000000				
00D504 _H	WRHS2[R/W] W ----- -0000000 -----000 00000000				
00D508 _H	WRHS3[R/W] W ----- -0000000 -----000 00000000				
00D50C _H	-				
00D510 _H	IBCM[R/W] W ----- -00 -----000				
00D514 _H	IBCR[R/W] W 0----- -0000000 0----- -0000000				
00D518 _H 00D5FC _H	-				Reserved
00D600 _H 00D6FC _H	RDDSn[1-64][R] W 00000000 00000000 00000000 00000000				FlexRay OBF ^{*5}
00D700 _H	RDHS1[R] W --000000 -0000000 -----000 00000000				
00D704 _H	RDHS2[R] W -0000000 -0000000 -----000 00000000				
00D708 _H	RDHS3[R] W --000000 --000000 -----000 00000000				
00D70C _H	MBS[R] W --000000 --000000 00-00000 00000000				
00D710 _H	OBCM[R/W] W ----- -00 -----00				
00D714 _H	OBCR[R/W] W ----- -0000000 0-----00 -0000000				
00D718 _H 00D7FC _H	-				Reserved
00D800 _H 00EFFC _H	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00F00 _H 00FEFC _H	-				Reserved [S]
00FF0 _H	DSUCR[R/W] B,H,W -----0		-	-	OCDU [S]
00FF04 _H 00FF0C _H	-	-	-	-	Reserved [S]
00FF10 _H	PCSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FF14 _H	PSSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00FF18 _H 00FF14 _H	-	-	-	-	Reserved [S]
00FF18 _H	EDIR1[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FF1C _H	EDIR0[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated when reading and writing to these registers in the user mode.

*5: For FlexRay, the CY91F583ASG/F584ASG/F585ASG/F583ASJ/F584ASJ/F585ASJ has corresponding functions. The following registers are reserved registers for models without the FlexRay function.
 000125_H IRPR2L[5:4], 000E68_H, 0004E8_H-0004EF_H, 00D000_H-00D717_H

10. Interrupt Vector Table

■ CY91F583AM/F584AM/F585AM

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN ^{*1}	Interrupt request batch read target
	Decimal	Hexa decimal					
Reset	0	00	-	3FC _H	000FFFFC _H	-	-
System reserved	1	01	-	3F8 _H	000FFFF8 _H	-	-
System reserved	2	02	-	3F4 _H	000FFFF4 _H	-	-
System reserved	3	03	-	3F0 _H	000FFF0 _H	-	-
System reserved	4	04	-	3EC _H	000FFFE _C	-	-
FPU exception	5	05	-	3E8 _H	000FFFE8 _H	-	-
Instruction access protection violation exception	6	06	-	3E4 _H	000FFFE4 _H	-	-
Data access protection violation exception	7	07	-	3E0 _H	000FFFE0 _H	-	-
Data access error interrupts	8	08	-	3DC _H	000FFFD _C	-	-
INTE instruction	9	09	-	3D8 _H	000FFFD8 _H	-	-
Instruction break	10	0A	-	3D4 _H	000FFFD4 _H	-	-
System reserved	11	0B	-	3D0 _H	000FFFD0 _H	-	-
System reserved	12	0C	-	3CC _H	000FFFC _C	-	-
System reserved	13	0D	-	3C8 _H	000FFFC8 _H	-	-
Exception of invalid instruction	14	0E	-	3C4 _H	000FFFC4 _H	-	-
NMI request Error generation at internal bus diagnosis RAM double-bit error Backup RAM double-bit error	15	0F	15(F _H) Fixed	3C0 _H	000FFFC0 _H	-	○
External interrupt 0-7	16	10	ICR00	3BC _H	000FFFB _C	0	-
Reload timer 0 / 1	17	11	ICR01	3B8 _H	000FFFB8 _H	1	○
Reload timer 2 / 3	18	12	ICR02	3B4 _H	000FFFB4 _H	2	○
Multifunction serial interface ch.0 (reception completed)/ Multifunction serial interface ch.0 (status)	19	13	ICR03	3B0 _H	000FFFB0 _H	3 ²	○
Multifunction serial interface ch.0 (transmission completed)	20	14	ICR04	3AC _H	000FFFA _C	4	-
Multifunction serial interface ch.1 (reception completed)/ Multifunction serial interface ch.1 (status)	21	15	ICR05	3A8 _H	000FFFA8 _H	5 ²	○
Multifunction serial interface ch.1 (transmission completed)	22	16	ICR06	3A4 _H	000FFFA4 _H	6	-
Multifunction serial interface ch.2 (reception completed)/ Multifunction serial interface ch.2 (status)	23	17	ICR07	3A0 _H	000FFFA0 _H	7 ²	○
Multifunction serial interface ch.2 (transmission completed)	24	18	ICR08	39C _H	000FFF9 _C	8	-
Multifunction serial interface ch.3 (reception completed)/ Multifunction serial interface ch.3 (status)	25	19	ICR09	398 _H	000FFF98 _H	9 ²	○
Multifunction serial interface ch.3 (transmission completed)	26	1A	ICR10	394 _H	000FFF94 _H	10	-
*4	27	1B	ICR11	390 _H	000FFF90 _H	-	-
*4	28	1C	ICR12	38C _H	000FFF8 _C	-	-
CAN 0	29	1D	ICR13	388 _H	000FFF88 _H	-	-
CAN 1	30	1E	ICR14	384 _H	000FFF84 _H	-	-
FlexRay 0 ^{*5}	31	1F	ICR15	380 _H	000FFF80 _H	-	-
FlexRay 1 ^{*5}	32	20	ICR16	37C _H	000FFF7 _C	-	-
FlexRay timer 0 ^{*5}	33	21	ICR17	378 _H	000FFF78 _H	-	-
FlexRay timer 1 ^{*5}	34	22	ICR18	374 _H	000FFF74 _H	-	-
RAM diagnosis completed RAM initialization completed Error generation at RAM diagnosis Backup RAM diagnosis completed Backup RAM initialization completed Error generation at Backup RAM diagnosis	35	23	ICR19	370 _H	000FFF70 _H	-	○

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN*1	Interrupt request batch read target
	Decimal	Hexa decimal					
Main timer/PLL timer/ PLL gear for FlexRay*5/ PLL alarm for FlexRay*5	36	24	ICR20	36C _H	000FFF6C _H	20*3	○
Clock calibration unit (CR oscillation)	37	25	ICR21	368 _H	000FFF68 _H	-	-
U/D counter 0 / 1	38	26	ICR22	364 _H	000FFF64 _H	22	○
Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23	○
Free-run timer 1 (0 detection) / (compare clear)	40	28	ICR24	35C _H	000FFF5C _H	24	○
Free-run timer 2 (0 detection) / (compare clear) PPG 0 / 1 / 2 / 3	41	29	ICR25	358 _H	000FFF58 _H	25	○
Free-run timer 3 (0 detection) / (compare clear)	42	2A	ICR26	354 _H	000FFF54 _H	26	○
Free-run timer 4 (0 detection) / (compare clear)	43	2B	ICR27	350 _H	000FFF50 _H	27	○
Free-run timer 5 (0 detection) / (compare clear) PPG 4 / 5	44	2C	ICR28	34C _H	000FFF4C _H	28	○
ICU 0 (fetching) / ICU 1 (fetching)	45	2D	ICR29	348 _H	000FFF48 _H	29	○
ICU 2 (fetching) / ICU 3 (fetching)	46	2E	ICR30	344 _H	000FFF44 _H	30	○
*4	47	2F	ICR31	340 _H	000FFF40 _H	-	-
*4	48	30	ICR32	33C _H	000FFF3C _H	-	-
OCU 0 (match) / OCU 1 (match)	49	31	ICR33	338 _H	000FFF38 _H	33	○
OCU 2 (match) / OCU 3 (match)	50	32	ICR34	334 _H	000FFF34 _H	34	○
OCU 4 (match) / OCU 5 (match)	51	33	ICR35	330 _H	000FFF30 _H	35	○
OCU 6 (match) / OCU 7 (match)	52	34	ICR36	32C _H	000FFF2C _H	36	○
OCU 8 (match) / OCU 9 (match)	53	35	ICR37	328 _H	000FFF28 _H	37	○
OCU 10 (match) / OCU 11 (match)	54	36	ICR38	324 _H	000FFF24 _H	38	○
WG dead timer underflow 0 / 1 / 2 WG dead timer reload 0 / 1 / 2 WG DTTI 0	55	37	ICR39	320 _H	000FFF20 _H	39	○
WG dead timer underflow 3 / 4 / 5 WG dead timer reload 3 / 4 / 5 WG DTTI 1	56	38	ICR40	31C _H	000FFF1C _H	40	○
AD converter 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	57	39	ICR41	318 _H	000FFF18 _H	41	○
AD converter 8 / 9 / 10 / 11 / 12 / 13 / 14	58	3A	ICR42	314 _H	000FFF14 _H	42	○
AD converter 16 / 17 / 18 / 19 / 20 / 21 / 22 / 23	59	3B	ICR43	310 _H	000FFF10 _H	43	○
Base timer 0 IRQ 0/ base timer 0 IRQ 1	60	3C	ICR44	30C _H	000FFF0C _H	44	○
Base timer 1 IRQ 0/ base timer 1 IRQ 1	61	3D	ICR45	308 _H	000FFF08 _H	45	○
DMAC 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	62	3E	ICR46	304 _H	000FFF04 _H	-	○
Delay interrupt	63	3F	ICR47	300 _H	000FFF00 _H	-	-
System reserved	64	40	-	2FC _H	000FFEFC _H	-	-
System reserved	65	41	-	2F8 _H	000FFE8 _H	-	-
Used with the INT instruction.	66	42	-	2F4 _H	000FEF4 _H	-	-
	255	FF	-	000 _H	000FFC00 _H	-	-

*1 :Does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (resource number) is assigned.

*2 :The multi-function serial interface status does not support DMA transfer caused by I²C reception.

*3 : "PLL gear for FlexRay" and "PLL alarm for FlexRay" do not support DMA transfer.

*4 :For CY91F583AM/F584AM/F585AM, the interrupt vectors are unused.

*5 :For FlexRay, the CY91F583AMG/F584AMG/F585AMG/F583AMJ/F584AMJ/F585AMJ have corresponding functions.

■ CY91F583AS/F584AS/F585AS

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN ^{*1}	Interrupt request batch read target
	Decimal	Hexa decimal					
Reset	0	00	-	3FC _H	000FFFC _H	-	-
System reserved	1	01	-	3F8 _H	000FFF8 _H	-	-
System reserved	2	02	-	3F4 _H	000FFF4 _H	-	-
System reserved	3	03	-	3F0 _H	000FFF0 _H	-	-
System reserved	4	04	-	3EC _H	000FFFE _C	-	-
FPU exception	5	05	-	3E8 _H	000FFE8 _H	-	-
Instruction access protection violation exception	6	06	-	3E4 _H	000FFE4 _H	-	-
Data access protection violation exception	7	07	-	3E0 _H	000FFE0 _H	-	-
Data access error interrupts	8	08	-	3DC _H	000FFDC _H	-	-
INTE instruction	9	09	-	3D8 _H	000FFD8 _H	-	-
Instruction break	10	0A	-	3D4 _H	000FFD4 _H	-	-
System reserved	11	0B	-	3D0 _H	000FFD0 _H	-	-
System reserved	12	0C	-	3CC _H	000FFCC _H	-	-
System reserved	13	0D	-	3C8 _H	000FFC8 _H	-	-
Exception of invalid instruction	14	0E	-	3C4 _H	000FFC4 _H	-	-
NMI request Error generation at internal bus diagnosis RAM double-bit error Backup RAM double-bit error	15	0F	15(F _H) Fixed	3C0 _H	000FFC0 _H	-	○
External interrupt 0-6	16	10	ICR00	3BC _H	000FFBC _H	0	-
Reload timer 0 / 1	17	11	ICR01	3B8 _H	000FFB8 _H	1	○
Reload timer 2 / 3	18	12	ICR02	3B4 _H	000FFB4 _H	2	○
Multifunction serial interface ch.0 (reception completed)/ Multifunction serial interface ch.0 (status)	19	13	ICR03	3B0 _H	000FFB0 _H	3 ^{*2}	○
Multifunction serial interface ch.0 (transmission completed)	20	14	ICR04	3AC _H	000FFAC _H	4	-
Multifunction serial interface ch.1 (reception completed)/ Multifunction serial interface ch.1 (status)	21	15	ICR05	3A8 _H	000FFA8 _H	5 ^{*2}	○
Multifunction serial interface ch.1 (transmission completed)	22	16	ICR06	3A4 _H	000FFA4 _H	6	-
*4	23	17	ICR07	3A0 _H	000FFA0 _H	-	-
*4	24	18	ICR08	39C _H	000FF9C _H	-	-
*4	25	19	ICR09	398 _H	000FF98 _H	-	-
*4	26	1A	ICR10	394 _H	000FF94 _H	-	-
*4	27	1B	ICR11	390 _H	000FF90 _H	-	-
*4	28	1C	ICR12	38C _H	000FF8C _H	-	-
CAN 0	29	1D	ICR13	388 _H	000FF88 _H	-	-
*4	30	1E	ICR14	384 _H	000FF84 _H	-	-
FlexRay 0 ^{*5}	31	1F	ICR15	380 _H	000FF80 _H	-	-
FlexRay 1 ^{*5}	32	20	ICR16	37C _H	000FF7C _H	-	-
FlexRay timer 0 ^{*5}	33	21	ICR17	378 _H	000FF78 _H	-	-
FlexRay timer 1 ^{*5}	34	22	ICR18	374 _H	000FF74 _H	-	-

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN ^{*1}	Interrupt request batch read target
	Decimal	Hexa decimal					
RAM diagnosis completed RAM initialization completed Error generation at RAM diagnosis Backup RAM diagnosis completed Backup RAM initialization completed Error generation at Backup RAM diagnosis	35	23	ICR19	370 _H	000FFF70 _H	-	○
Main timer/PLL timer/ PLL gear for FlexRay ^{*5} / PLL alarm for FlexRay ^{*5}	36	24	ICR20	36C _H	000FFF6C _H	20 ^{*3}	○
Clock calibration unit (CR oscillation)	37	25	ICR21	368 _H	000FFF68 _H	-	-
U/D counter 0 / 1	38	26	ICR22	364 _H	000FFF64 _H	22	○
Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360 _H	000FFF60 _H	23	○
Free-run timer 1 (0 detection) / (compare clear)	40	28	ICR24	35C _H	000FFF5C _H	24	○
Free-run timer 2 (0 detection) / (compare clear) PPG 0 / 1 / 2 / 3	41	29	ICR25	358 _H	000FFF58 _H	25	○
Free-run timer 3 (0 detection) / (compare clear)	42	2A	ICR26	354 _H	000FFF54 _H	26	○
Free-run timer 4 (0 detection) / (compare clear)	43	2B	ICR27	350 _H	000FFF50 _H	27	○
Free-run timer 5 (0 detection) / (compare clear) PPG 4 / 5	44	2C	ICR28	34C _H	000FFF4C _H	28	○
ICU 0 (fetching) / ICU 1 (fetching)	45	2D	ICR29	348 _H	000FFF48 _H	29	○
ICU 2 (fetching) / ICU 3 (fetching)	46	2E	ICR30	344 _H	000FFF44 _H	30	○
*4	47	2F	ICR31	340 _H	000FFF40 _H	-	-
*4	48	30	ICR32	33C _H	000FFF3C _H	-	-
OCU 0 (match) / OCU 1 (match)	49	31	ICR33	338 _H	000FFF38 _H	33	○
OCU 2 (match) / OCU 3 (match)	50	32	ICR34	334 _H	000FFF34 _H	34	○
OCU 4 (match) / OCU 5 (match)	51	33	ICR35	330 _H	000FFF30 _H	35	○
OCU 6 (match) / OCU 7 (match)	52	34	ICR36	32C _H	000FFF2C _H	36	○
OCU 8 (match) / OCU 9 (match)	53	35	ICR37	328 _H	000FFF28 _H	37	○
OCU 10 (match) / OCU 11 (match)	54	36	ICR38	324 _H	000FFF24 _H	38	○
WG dead timer underflow 0 / 1 / 2 WG dead timer reload 0 / 1 / 2 WG DTTI 0	55	37	ICR39	320 _H	000FFF20 _H	39	○
WG dead timer underflow 3 / 4 / 5 WG dead timer reload 3 / 4 / 5 WG DTTI 1	56	38	ICR40	31C _H	000FFF1C _H	40	○
AD converter 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	57	39	ICR41	318 _H	000FFF18 _H	41	○
AD converter 8 / 9 / 10 / 11 / 12 / 13 / 14	58	3A	ICR42	314 _H	000FFF14 _H	42	○
AD converter 19 / 20	59	3B	ICR43	310 _H	000FFF10 _H	43	○
Base timer 0 IRQ 0/ base timer 0 IRQ 1	60	3C	ICR44	30C _H	000FFF0C _H	44	○
Base timer 1 IRQ 0/ base timer 1 IRQ 1	61	3D	ICR45	308 _H	000FFF08 _H	45	○
DMAC 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	62	3E	ICR46	304 _H	000FFF04 _H	-	○

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN*1	Interrupt request batch read target
	Decimal	Hexa decimal					
Delay interrupt	63	3F	ICR47	300 _H	000FFF00 _H	-	-
System reserved	64	40	-	2FC _H	000FFEFC _H	-	-
System reserved	65	41	-	2F8 _H	000FEF8 _H	-	-
Used with the INT instruction.	66	42	-	2F4 _H	000FEF4 _H	-	-
	255	FF		000 _H	000FFC00 _H		

*1 :Does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (resource number) is assigned.

*2 :The multi-function serial interface status does not support DMA transfer caused by I²C reception.

*3 : "PLL gear for FlexRay" and "PLL alarm for FlexRay" do not support DMA transfer.

*4 :For CY91F583AS/F584AS/F585AS, the interrupt vectors are unused.

*5 :For FlexRay, the CY91F583ASG/F584ASG/F585ASG/F583ASJ/F584ASJ/F585ASJ have corresponding functions

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage ^{*1, *2}	V _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	
Analog power supply voltage ^{*1, *2}	AV _{CC}	V _{SS} -0.3	V _{SS} +6.0	V	AV _{CC} ≤ V _{CC}
Analog reference voltage ^{*1}	AVRH	V _{SS} -0.3	V _{SS} +6.0	V	AVRH ≤ AV _{CC}
Input voltage ^{*1}	V _I	V _{SS} -0.3	V _{CC} +0.3	V	
Analog pin input voltage ^{*1}	V _{IA}	V _{SS} -0.3	V _{CC} +0.3	V	
Output voltage ^{*1}	V _O	V _{SS} -0.3	V _{CC} +0.3	V	
Maximum clamp current	I _{CLAMP}	-	4	mA	*9
Total maximum clamp current	∑ I _{CLAMP}	-	20	mA	*9
"L" level maximum output current ^{*3}	I _{OL1}	-	7	mA	When setting to 2mA ^{*6}
	I _{OL2}	-	14	mA	When setting to 4mA ^{*7}
	I _{OL3}	-	17.5	mA	When setting to 5mA ^{*8}
"L" level average output current ^{*4}	I _{OLAV1}	-	2	mA	When setting to 2mA ^{*6}
	I _{OLAV2}	-	4	mA	When setting to 4mA ^{*7}
	I _{OLAV3}	-	5	mA	When setting to 5mA ^{*8}
"L" level total output current ^{*5}	∑I _{OL}	-	50	mA	*6
"H" level maximum output current ^{*3}	I _{OH1}	-	-7	mA	When setting to 2mA ^{*6}
	I _{OH2}	-	-14	mA	When setting to 4mA ^{*7}
	I _{OH3}	-	-17.5	mA	When setting to 5mA ^{*8}
"H" level average output current ^{*4}	I _{OHAV1}	-	-2	mA	When setting to 2mA ^{*6}
	I _{OHAV2}	-	-4	mA	When setting to 4mA ^{*7}
	I _{OHAV3}	-	-5	mA	When setting to 5mA ^{*8}
"H" level total output current ^{*5}	∑I _{OH}	-	-50	mA	*6
Power consumption	P _D	-	690	mW	
Operating temperature	T _A	-40	+125	°C	*10, *11
Storage temperature	T _{stg}	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS}=0.0V.

*2: Caution must be taken that AV_{CC} does not exceed V_{CC}.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: Corresponding pins: General-purpose ports

*7: Corresponding pins: General-purpose ports of P021 to P023, P025 to P027

*8: Corresponding pins: General-purpose ports other than those of P021 to P023, P025 to P027

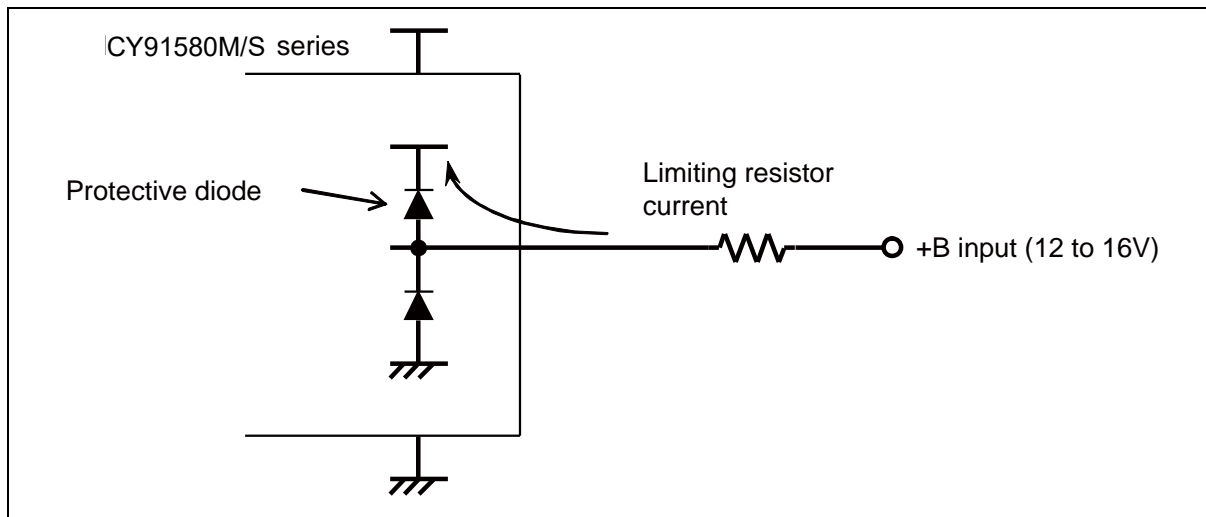
*9: • Corresponding pins: General-purpose ports

• Use the devices within recommended operating conditions.

• Use the devices with direct voltage (current).

- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low-power consumption modes, the + B input potential can increase the potential at the Vcc pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

Sample recommended circuit



*10: To use this product at $T_A=125^{\circ}\text{C}$, equip this on a multilayer board with four or more layers.

To equip this on a single-layer board, change the operating conditions (operating frequency, power supply voltage, etc) to use this at the power consumption $P_D=415\text{mW}$ or lower, or use this at $T_A=105^{\circ}\text{C}$ or lower.

*11: When it is used exceeding $T_A=125^{\circ}\text{C}$, contact your sales representative.

WARNING

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

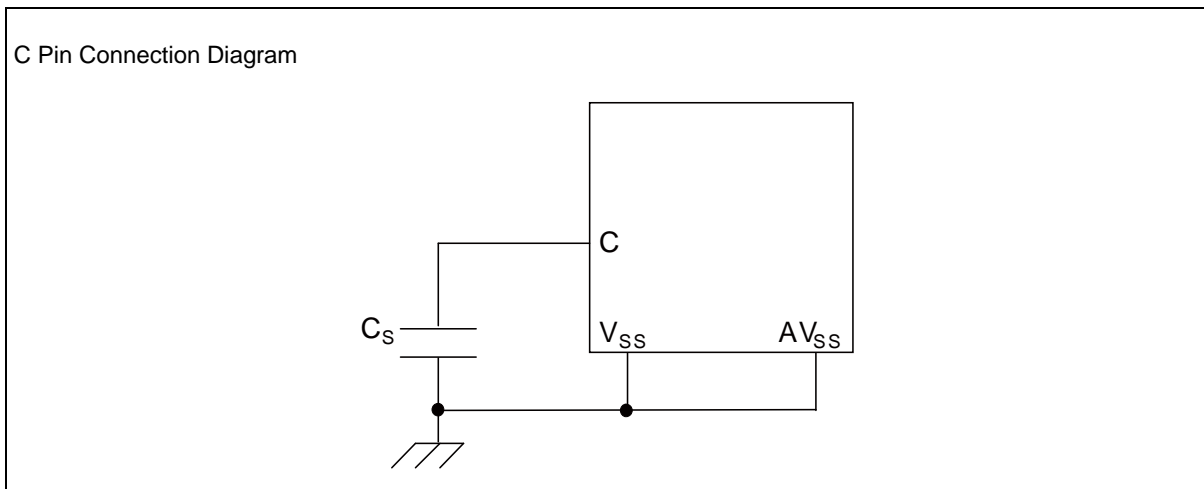
11.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V _{CC}	4.5	5.5	V	Recommended operation guarantee range
	AV _{CC}	4.5	5.5	V	
	V _{CC}	3.7	5.5	V	Operation guarantee range
	AV _{CC}	3.7	5.5	V	
Smoothing capacitor*1	C _S	4.7 (tolerance within ±50%)		μF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C _S as the smoothing capacitor on the VCC pin.
Operating temperature	T _A	-40	+125	°C	*2

*1: For connection of smoothing capacitor C_S, see the figure below.

*2: When it is used exceeding T_A=125°C, contact your sales representative.



WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

11.3 DC Characteristics

(TA: Recommended operating conditions, Vcc=5.0V±10%, Vss= AVss=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V _{IH1}	P000 to P007*, P010 to P017, P020, P024, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	When CMOS schmitt input level is selected	0.7 × V _{CC}	-	V _{CC} +0.3	V	
	V _{IH2}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	When Automotive input level is selected	0.8 × V _{CC}	-	V _{CC} +0.3	V	
	V _{IH3}	P021 to P023, P025 to P027	When FlexRay input level is selected	0.7 × V _{CC}	-	V _{CC} +0.3	V	
	V _{IH4}	RSTX, NMIX	-	0.7 × V _{CC}	-	V _{CC} +0.3	V	
	V _{IH5}	MD0, MD1	-	0.7 × V _{CC}	-	V _{CC} +0.3	V	
	V _{IH6}	DEBUGIF	-	2.0	-	V _{CC} +0.3	V	

*: Only available with CY91F583AM/F584AM/F585AM

(T_A: Recommended operating conditions, V_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage	V _{IL1}	P000 to P007*, P010 to P017, P020, P024, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	When CMOS schmitt input level is selected	V _{SS} -0.3	-	0.3 × V _{CC}	V	
	V _{IL2}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	When Automotive input level is selected	V _{SS} -0.3	-	0.5 × V _{CC}	V	
	V _{IL3}	P021 to P023, P025 to P027	When FlexRay input level is selected	V _{SS} -0.3	-	0.3 × V _{CC}	V	
	V _{IL4}	RSTX, NMIX	-	V _{SS} -0.3	-	0.3 × V _{CC}	V	
	V _{IL5}	MD0, MD1	-	V _{SS} -0.3	-	0.3 × V _{CC}	V	
	V _{IL6}	DEBUGIF	-	V _{SS} -0.3	-	0.8	V	

*: Only available with CY91F583AM/F584AM/F585AM

(T_A: Recommended operating conditions, V_{CC}=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V _{OH1}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	V _{CC} =4.5V I _{OH} =-2.0mA	V _{CC} -0.5	-	V _{CC}	V	
	V _{OH2}	P021 to P023, P025 to P027	V _{CC} =4.5V I _{OH} =-4.0mA	V _{CC} -0.5	-	V _{CC}	V	When FlexRay is selected
	V _{OH3}	P000 to P007*, P010 to P017, P020, P024, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	V _{CC} =4.5V I _{OH} =-5.0mA	V _{CC} -0.5	-	V _{CC}	V	

*: Only available with CY91F583AM/F584AM/F585AM

(TA: Recommended operating conditions, Vcc=5.0V±10%, Vss=AVss=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V _{OL1}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	Vcc=4.5V I _{OL} =2.0mA	0	-	0.4	V	
	V _{OL2}	P021 to P023, P025 to P027	Vcc=4.5V I _{OL} =4.0mA	0	-	0.4	V	When FlexRay is selected
	V _{OL3}	P000 to P007*, P010 to P017, P020, P024, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	Vcc=4.5V I _{OL} =5.0mA	0	-	0.4	V	
	V _{OL4}	P040, P041, P063*, P064*, P080*, P081*, P083*, P084*	Vcc=4.5V I _{OL} =3.0mA	0	-	0.4	V	I ² C shared pin (when I ² C is selected)
	V _{OL5}	DEBUGIF	Vcc=2.7V I _{OL} =25.0mA	0	-	0.25	V	

*: Only available with CY91F583AM/F584AM/F585AM

(T_A: Recommended operating conditions, V_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input Leak Current	I _{IL}	All input pins	V _{CC} = AV _{CC} =5.5V V _{SS} < V _I < V _{CC}	-5	-	+5	μA	
Pull-up resistance	R _{UP1}	RSTX, NMIX	-	25	-	100	kΩ	
	R _{UP2}	P000 to P007*, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P056, P060 to P066*, P070 to P072, P080 to P087*, P090 to P092*, P093, P094, P095 to P097*, P100 to P102*	When pull-up resistance is selected	25	-	100	kΩ	
Input Capacitor	C _{IN}	Other than VCC, VSS, AVCC, AVSS, C	-	-	5	15	pF	

*: Only available with CY91F583AM/F584AM/F585AM

(T_A: Recommended operating conditions, V_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I _{CC}	VCC5	Normal operations F _{CP} =128MHz, F _{CPM} =128MHz, F _{CPP} =32MHz	-	80	110	mA	FlexRay =ON
				-	73	103	mA	FlexRay =OFF
			Normal operations F _{CP} =128MHz, F _{CPM} =32MHz, F _{CPP} =32MHz	-	77	107	mA	FlexRay =ON
				-	70	100	mA	FlexRay =OFF
			Normal operations F _{CP} =80MHz, F _{CPM} =80MHz, F _{CPP} =40MHz	-	62	89	mA	FlexRay =ON
				-	57	85	mA	FlexRay =OFF
			Normal operations F _{CP} =80MHz, F _{CPM} =40MHz, F _{CPP} =40MHz	-	61	88	mA	FlexRay =ON
				-	56	84	mA	FlexRay =OFF
			Flash write F _{CP} =128MHz, F _{CPM} =128MHz, F _{CPP} =32MHz	-	95	125	mA	*
			Flash erase F _{CP} =128MHz, F _{CPM} =128MHz, F _{CPP} =32MHz	-	95	125	mA	*

*: This series has 2 types of flash; main flash and WorkFlash; however, this is the specification when only one of those is written/erased.

(T_A: Recommended operating conditions, V_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I _{CCS}	VCC5	CPU sleep F _{CP} =128MHz, F _{CPm} =128MHz, F _{CPP} =32MHz	-	41	66	mA	*1, *2, *3, *4
	I _{CCBS}		Bus sleep F _{CP} =128MHz, F _{CPm} =128MHz, F _{CPP} =32MHz	-	19	45	mA	*1, *2, *3, *4
	I _{CCt}		Clock mode 4MHz source oscillation	-	1.2	1.8	mA	When using external clock*5 T _A =25°C, *1, *2, *3, *4
				-	2.7	3.3	mA	When using crystal T _A =25°C, *1, *2, *3, *4
	I _{CCtS}		Clock mode shutdown 4MHz source oscillation	-	0.3	0.4	mA	When using external clock*5 T _A =25°C, *1, *2
				-	1.8	1.9	mA	When using crystal T _A =25°C, *1, *2
				-	0.7	0.8	mA	When using external clock*5 T _A =25°C, *3, *4
				-	2.2	2.3	mA	When using crystal T _A =25°C, *3, *4
	I _{CCH}		STOP mode	-	0.6	1.1	mA	T _A =25°C, *1, *2
				-	1.0	1.6	mA	T _A =25°C, *3, *4
	I _{CCHS}		STOP mode shutdown	-	0.1	0.2	mA	T _A =25°C, *1, *2
				-	0.5	0.6	mA	T _A =25°C, *3, *4

*1:CY91F583AMG/F584AMG/F585AMG/F583AMH/F584AMH/F585AMH

*2:CY91F583ASG/F584ASG/F585ASG/F583ASH/F584ASH/F585ASH

*3:CY91F583AMJ/F584AMJ/F585AMJ/F583AMK/F584AMK/F585AMK

*4:CY91F583ASJ/F584ASJ/F585ASJ/F583ASK/F584ASK/F585ASK

*5: The power supply current is the current value when the external clock is supplied from the X1 pin. Note that the power supply current value when using the external clock is different from that using the oscillator.

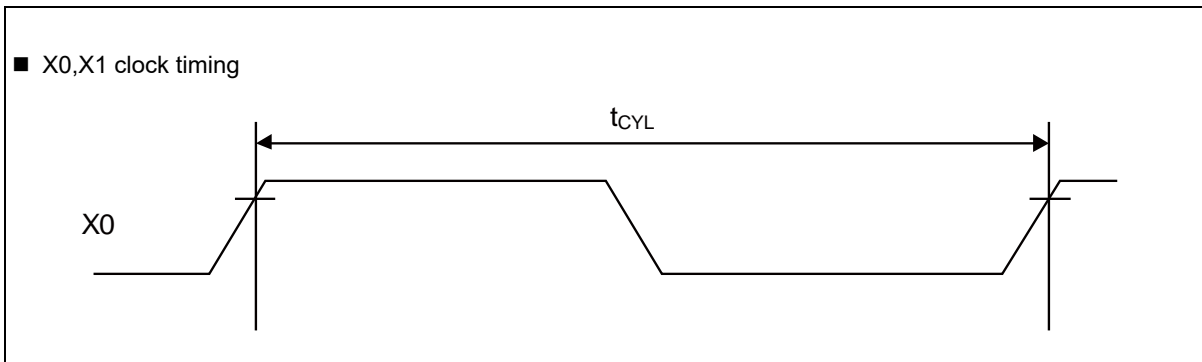
11.4 AC Characteristics

11.4.1 Main Clock Timing

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

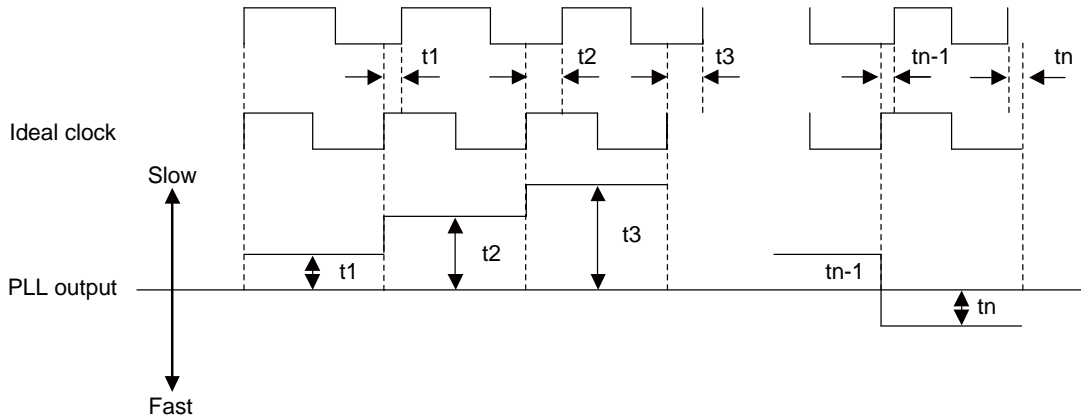
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F _C	X0, X1	-	4	-	20	MHz	
Source oscillation clock cycle time	t _{CYL}	X0, X1	-	50	-	250	ns	
Internal operating clock frequency*	F _{CP}	-	-	-	-	128	MHz	CPU clock
	F _{CPP}	-	-	-	-	40	MHz	Peripheral bus clock
	F _{CPM}	-	-	-	-	128	MHz	Motor clock
Internal operating clock cycle time*	t _{CP}	-	-	7.82	-	-	ns	CPU clock
	t _{CPP}	-	-	25	-	-	ns	Peripheral bus clock
	t _{CPM}	-	-	7.82	-	-	ns	Motor clock
CAN PLL jitter (during lock)	t _{PJ}	-	-	-10	-	+10	ns	
Built-in CR oscillation frequency	F _{CCR}	-	-	50	100	150	kHz	

*: The maximum/minimum value is defined when using the main clock and PLL clock.



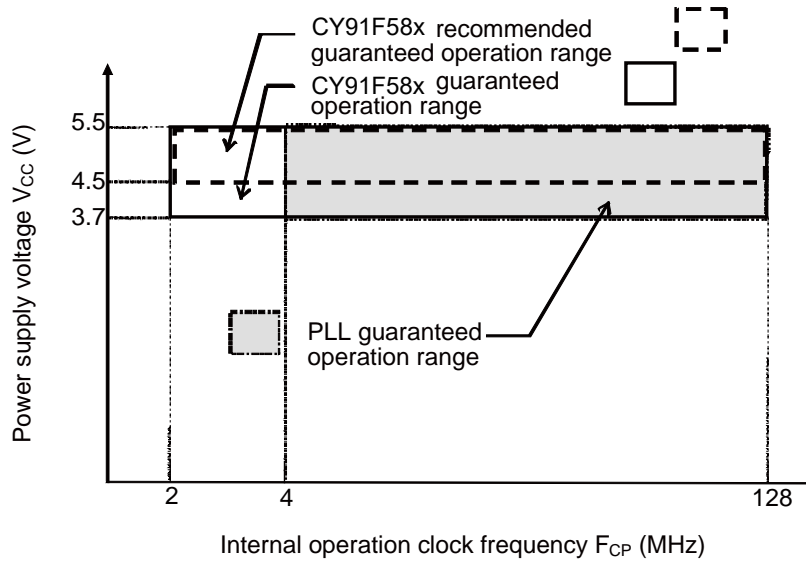
■ CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20,000 cycles.



■ Guaranteed operation range

Internal operation clock frequency vs. Power supply voltage

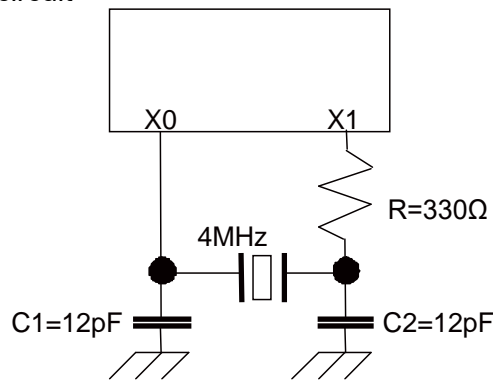


Note: The CPU will be reset at the power supply voltage of the low-voltage detection setting voltage or less.

Oscillation clock frequency vs. Internal operation clock frequency

		Internal operation clock frequency								
		Main clock	PLL clock							
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 20	...	Multiplied by 32
Oscillation clock frequency	4MHz z	2MHz z	4MHz	8MHz	12MHz	16MHz	...	80MHz	...	128MHz

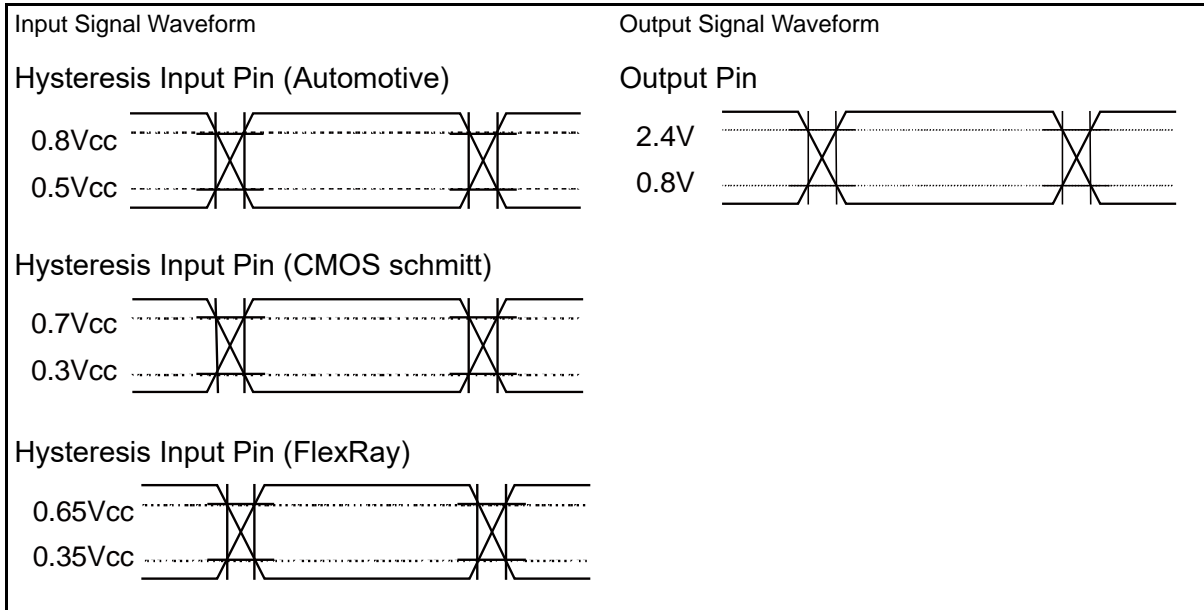
● Example of oscillation circuit



Note: If it is impossible to start the oscillation within or equal to 20ms when starting from the oscillation stop state, the clock supervisor performs a detection of oscillation stop and moves to the fail safe operation.

Design your print circuit board so that the oscillator can start oscillation within 20ms. In addition, when configuring the oscillator circuit, it is recommended to ask matching evaluation of the circuit to oscillator manufacturers for the design.

AC characteristics are specified by the following measurement reference voltage values.

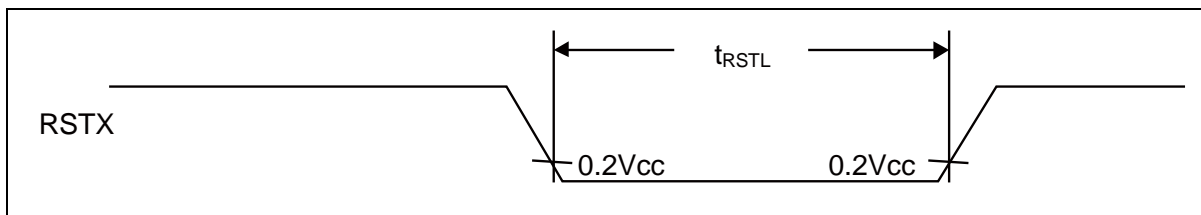


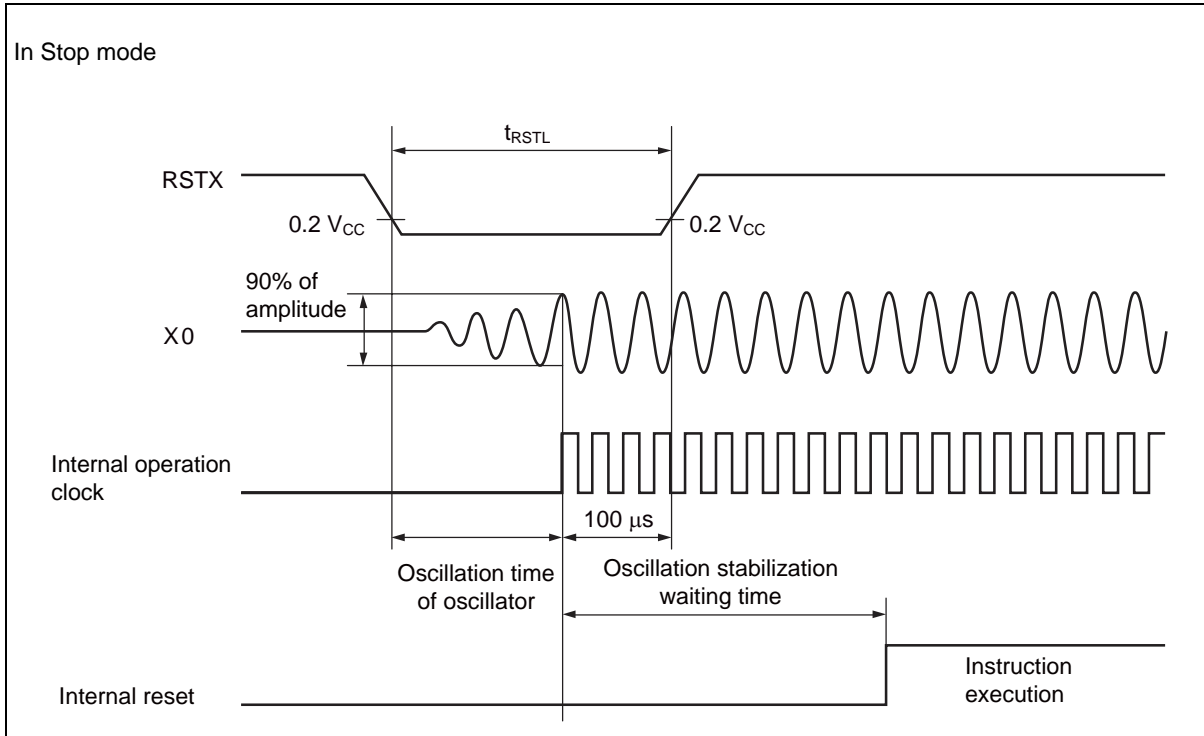
11.4.2 Reset input

(T_A: Recommended operating conditions, V_{cc} = 5.0V±10%, V_{ss}=AV_{ss}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks	
				Min	Max			
Reset input time	t _{RSTL}	RSTX	-	10	-	μs	During normal operation	
				Oscillation time of oscillator* +0.1		-	ms	At Stop mode
				100	-	μs	At Clock mode	
Reset input removal width				1	-	μs		

*: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred μs and several ms, and for an external clock, the time is 0 ms.





11.4.3 Power-on Conditions

(T_A: Recommended operating conditions, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC5	-	2.024	2.200	2.376	V	When turning on power
Level detection hysteresis width	-	VCC5	-	-	100	-	mV	During voltage drop
Level detection time	-	-	-	-	-	30	μs	*1
Slope detection undetected standard	-	VCC5	V _{CC} =level detection release level	-	-	4	mV/μs	*2
Power off time	t _{OFF}	VCC5	-	50	-	-	ms	*3

*1: If the fluctuation of the power supply is faster than the low-voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: When setting the power supply fluctuation to this standard or less, it is possible to suppress the slope detection. This is the standard when the power supply fluctuation is stable.

*3: This time is to start the slope detection at next power on after power down and internal charge loss.

11.4.4 Multi-function Serial CSIO timing (SMR:MD2-0="010"b)

Normal synchronous transfer (SCR:SPI=0) and serial clock output signal detect level "H" (SMR:SCINV=0)

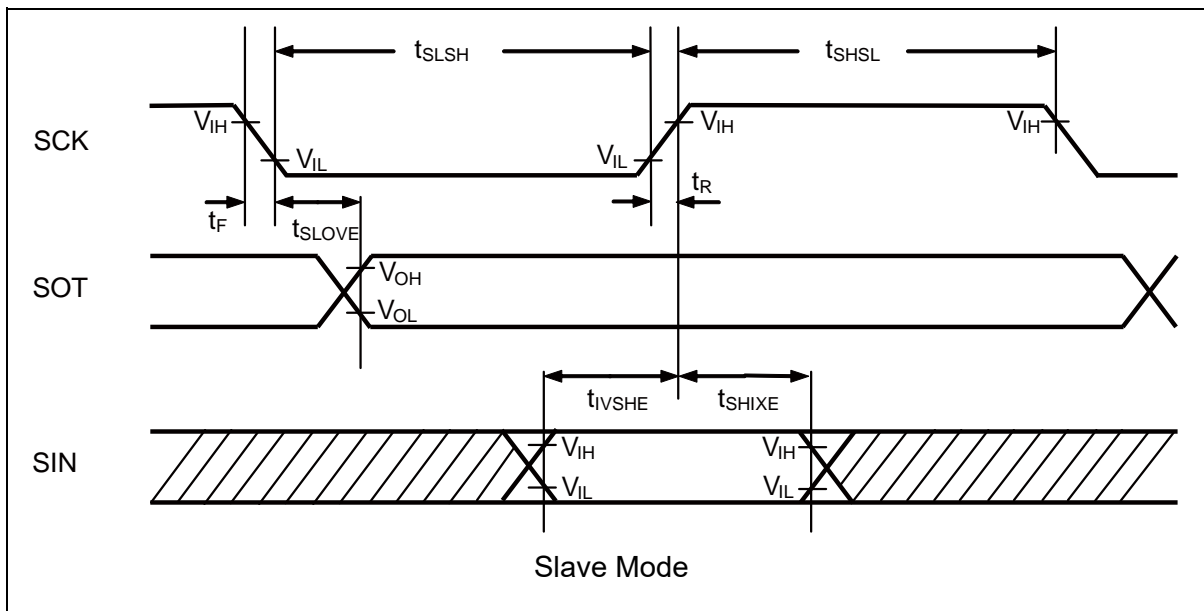
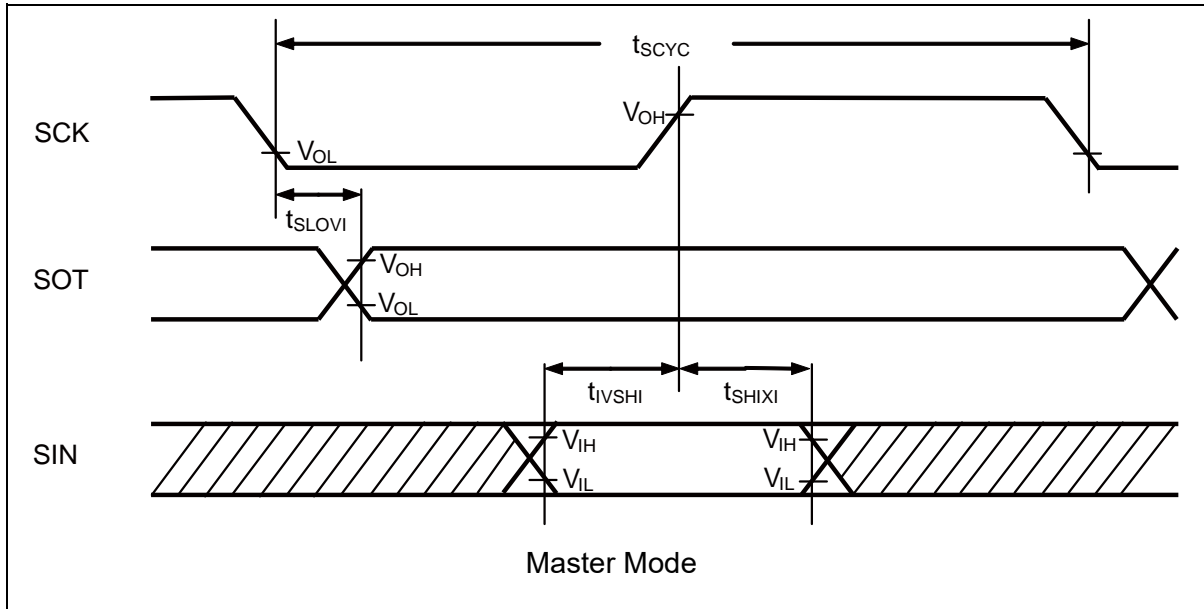
 (T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Master mode C _L =50pF	4t _{CPP}	-	ns	
SCK ↓ ⇒ SOT delay time	t _{SLOVI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-30	+30	ns	
Valid SIN ⇒ SCK ↑ setup time	t _{IVSHI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		30	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t _{SHIXI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		0	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Slave mode C _L =50pF	t _{CPP} +10	-	ns	
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	-	ns	
SCK ↓ ⇒ SOT delay time	t _{SLOVE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-	30	ns	
Valid SIN ⇒ SCK ↑ setup time	t _{IVSHE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		10	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t _{SHIXE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		20	-	ns	
SCK fall time	t _F	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	
SCK rise time	t _R	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	

*: Only available with CY91F583AM/F584AM/F585AM

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Normal synchronous transfer (SCR:SPI=0) and serial clock output signal detect level "L" (SMR:SCINV=1)

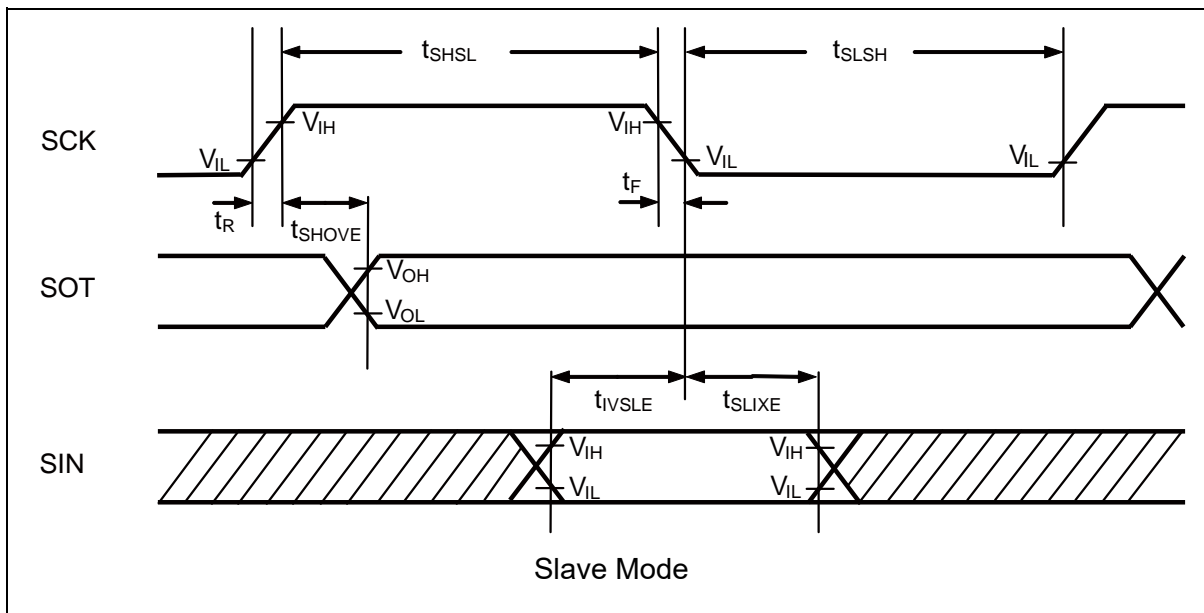
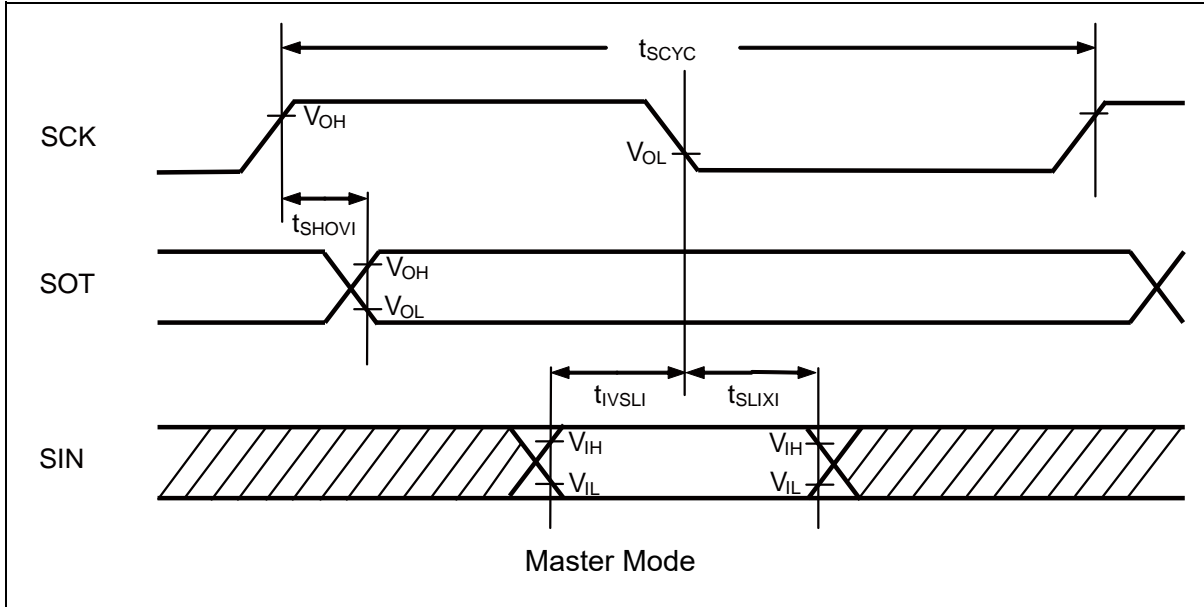
(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Master mode C _L =50pF	4t _{CPP}	-	ns	
SCK ↑ ⇒ SOT delay time	t _{SHOVI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-30	+30	ns	
Valid SIN ⇒ SCK ↓ setup time	t _{IVSLI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		30	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t _{SLIXI}			0	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Slave mode C _L =50pF	t _{CPP} +10	-	ns	
Serial clock "L" pulse width	t _{SLSH}			2t _{CPP} -10	-	ns	
SCK ↑ ⇒ SOT delay time	t _{SHOVE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-	30	ns	
Valid SIN ⇒ SCK ↓ setup time	t _{IVSLE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		10	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t _{SLIXE}			20	-	ns	
SCK fall time	t _F	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	
SCK rise time	t _R	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	

*: Only available with CY91F583AM/F584AM/F585AM

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



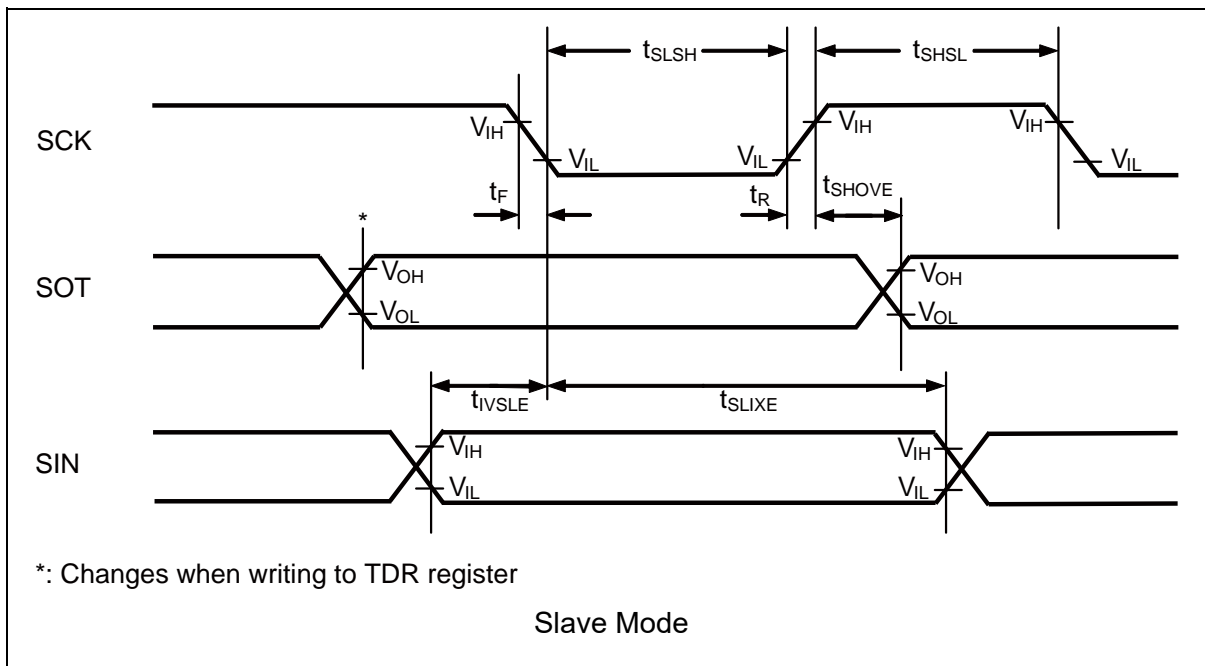
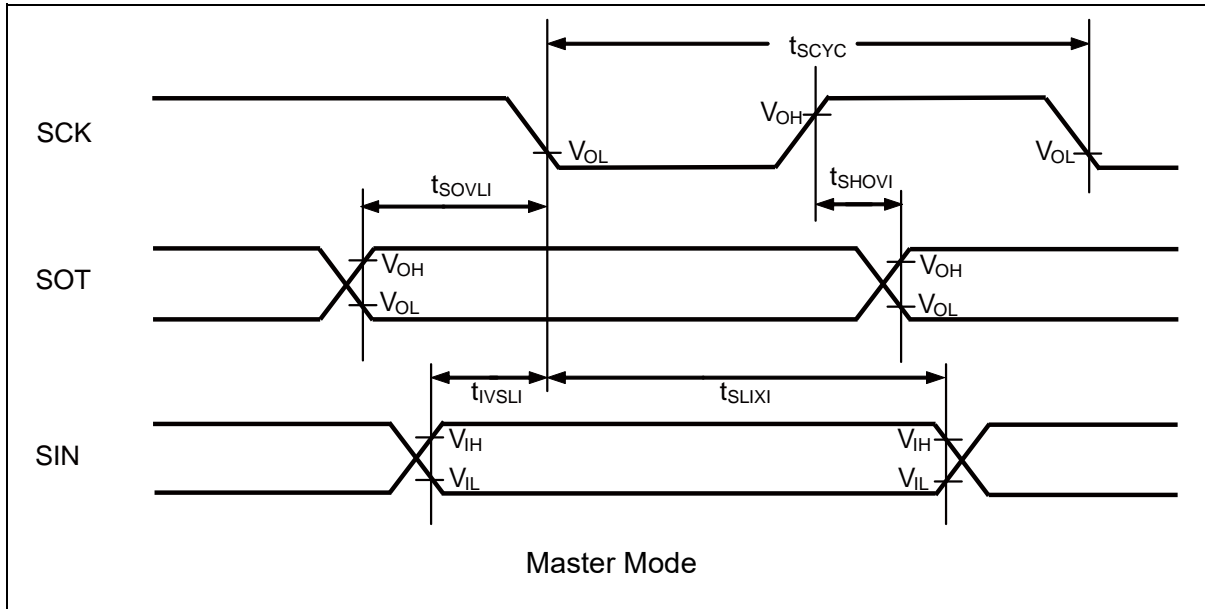
SPI compatible (SCR:SPI=1) and serial clock output signal detect level "H" (SMR:SCINV=0)

 (T_A: Recommended operating conditions, V_{CC} =5.0V±10% , V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Master mode C _L =50pF	4t _{CPP}	-	ns	
SCK ↑ ⇒ SOT delay time	t _{SHOVI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-30	+30	ns	
Valid SIN ⇒ SCK ↓ setup time	t _{IVSLI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		30	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t _{SLIXI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		0	-	ns	
SOT ⇒ SCK ↓ delay time	t _{SOVLI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		2t _{CPP} -30	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		t _{CPP} +10	-	ns	
Serial clock "L" pulse width	t _{SLSH}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	2t _{CPP} -10	-	ns		
SCK ↑ ⇒ SOT delay time	t _{SHOVE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*	-	30	ns		
Valid SIN ⇒ SCK ↓ setup time	t _{IVSLE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*	10	-	ns		
SCK ↓ ⇒ Valid SIN hold time	t _{SLIXE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*	20	-	ns		
SCK fall time	t _F	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	-	5	ns		
SCK rise time	t _R	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	-	5	ns		

*: Only available with CY91F583AM/F584AM/F585AM

- Notes:
- This is the AC characteristic in CLK synchronized mode.
 - C_L is the load capacitance applied to pins during testing.
 - The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



SPI compatible (SCR:SPI=1) and serial clock output signal detect level "L" (SMR:SCINV=1)

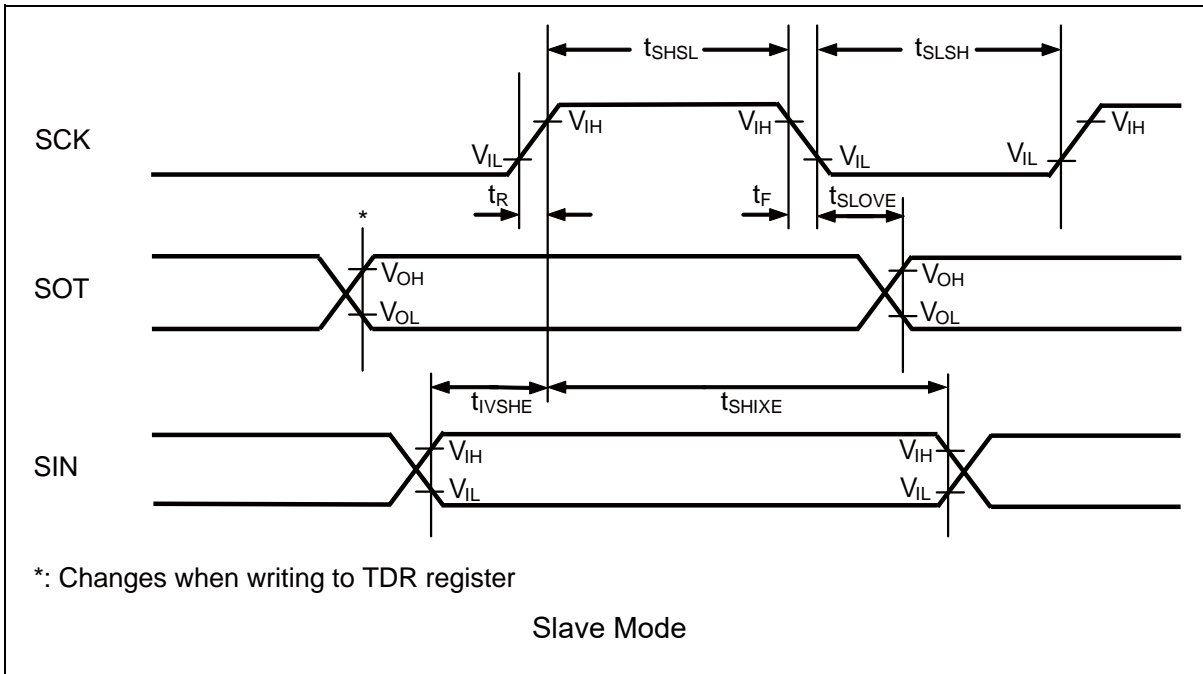
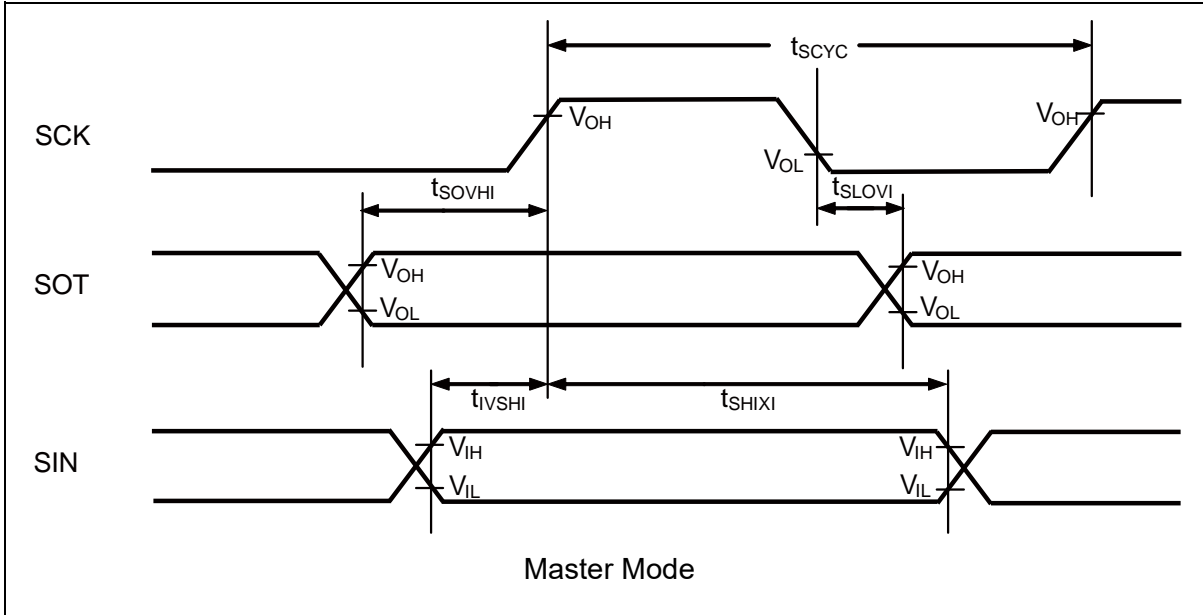
 (T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t _{SCYC}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Master mode C _L =50pF	4t _{CPP}	-	ns	
SCK ↓ ⇒ SOT delay time	t _{SLOVI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-30	+30	ns	
Valid SIN ⇒ SCK ↑ setup time	t _{IVSHI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		30	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t _{SHIXI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		0	-	ns	
SOT ⇒ SCK ↑ delay time	t _{SOVHI}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		2t _{CPP} -30	-	ns	
Serial clock "H" pulse width	t _{SHSL}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*	Slave mode C _L =50pF	t _{CPP} +10	-	ns	
Serial clock "L" pulse width	t _{SLSH}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		2t _{CPP} -10	-	ns	
SCK ↓ ⇒ SOT delay time	t _{SLOVE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SOT0_0, SOT0_1*, SOT1, SOT2*, SOT3*		-	30	ns	
Valid SIN ⇒ SCK ↑ setup time	t _{IVSHE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		10	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t _{SHIXE}	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*, SIN0_0, SIN0_1*, SIN1, SIN2*, SIN3*		20	-	ns	
SCK fall time	t _F	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	
SCK rise time	t _R	SCK0_0, SCK0_1*, SCK1, SCK2*, SCK3*		-	5	ns	

*: Only available with CY91F583AM/F584AM/F585AM

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "H" (SMR:SCINV=0)
- Serial chip select inactive level "H" (SCSCR:CSLVL=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ ⇒ SCK ↓ setup time	t _{CSSI}	SCK1, SCK2 ^{*4} , SCK3 ^{*4} ,	Master mode C _L =50pF	t _{CSSU} ^{*1} +0	t _{CSSU} ^{*1} +50	ns	
SCK ↑ ⇒ SCS ↑ hold time	t _{CSDI}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		t _{CSDI} ^{*2} -50	t _{CSDI} ^{*2} +0	ns	
SCS deselect time	t _{CSDI}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		-50+5t _{CPP} +t _{CSDS} ^{*3}	+50+5t _{CPP} +t _{CSDS} ^{*3}	ns	
SCS ↓ ⇒ SCK ↓ setup time	t _{CSSE}	SCK1, SCK2 ^{*4} , SCK3 ^{*4} ,	Slave mode C _L =50pF	3t _{CPP} +30	-	ns	
SCK ↑ ⇒ SCS ↑ hold time	t _{CSHE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		0	-	ns	
SCS deselect time	t _{CSDE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		3t _{CPP} +30	-	ns	
SCS ↓ ⇒ SOT delay time	t _{DSE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4} ,		-	40	ns	
SCS ↑ ⇒ SOT delay time	t _{DEE}	SOT1, SOT2 ^{*4} , SOT3 ^{*4}		0	-	ns	

*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock

*2: t_{CSDI}=SCSTR:CSHD7-0 × Serial chip select timing operation clock

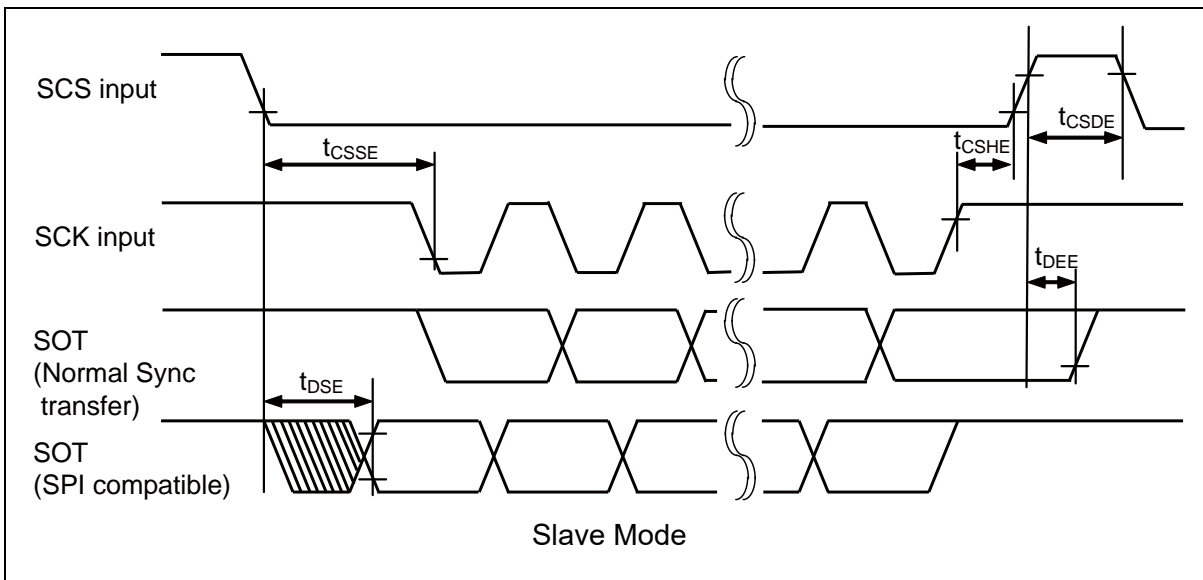
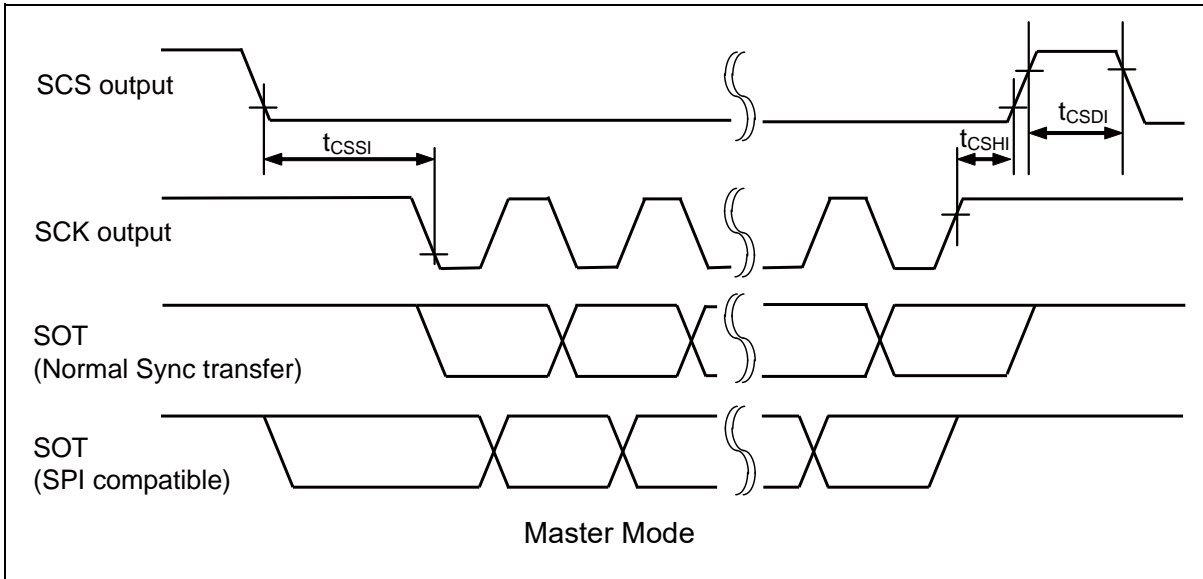
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock

*4: Only available with CY91F583AM/F584AM/F585AM

For details of *1, *2 and *3 above, see Hardware Manual.

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "L" (SMR:SCINV=1)
- Serial chip select inactive level "H" (SCSCR:CSLVL=1)

(TA: Recommended operating conditions, $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = AVSS = 0.0V$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ ⇒ SCK ↑ setup time	t_{CSSI}	SCK1, SCK2 ^{*4} , SCK3 ^{*4} ,	Master mode $C_L = 50pF$	$t_{CSSU}^{*1} + 0$	$t_{CSSU}^{*1} + 50$	ns	
SCK ↓ ⇒ SCS ↑ hold time	t_{CSHI}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		$t_{CSHD}^{*2} - 50$	$t_{CSHD}^{*2} + 0$	ns	
SCS deselect time	t_{CSDI}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		$-50 + 5t_{CPP} + t_{CSDS}^{*3}$	$+50 + 5t_{CPP} + t_{CSDS}^{*3}$	ns	
SCS ↓ ⇒ SCK ↑ setup time	t_{CSSE}	SCK1, SCK2 ^{*4} , SCK3 ^{*4} ,	Slave mode $C_L = 50pF$	$3t_{CPP} + 30$	-	ns	
SCK ↓ ⇒ SCS ↑ hold time	t_{CSHE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		0	-	ns	
SCS deselect time	t_{CSDE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		$3t_{CPP} + 30$	-	ns	
SCS ↓ ⇒ SOT delay time	t_{DSE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4} ,		-	40	ns	
SCS ↑ ⇒ SOT delay time	t_{DEE}	SOT1, SOT2 ^{*4} , SOT3 ^{*4}		0	-	ns	

*1: $t_{CSSU} = SCSTR:CSSU7-0 \times$ Serial chip select timing operation clock

*2: $t_{CSHD} = SCSTR:CSHD7-0 \times$ Serial chip select timing operation clock

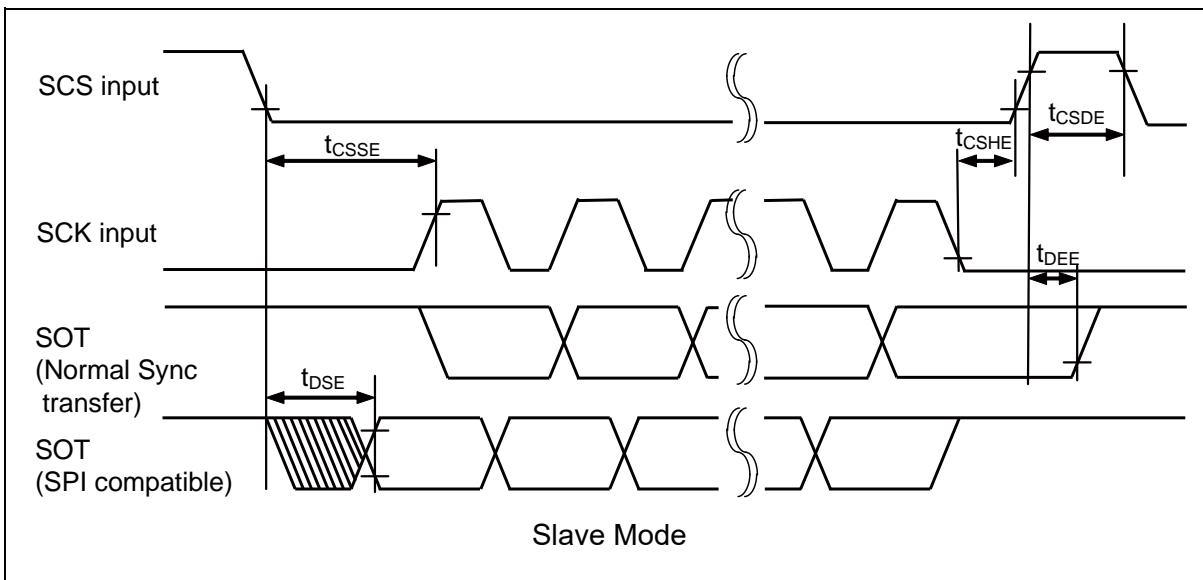
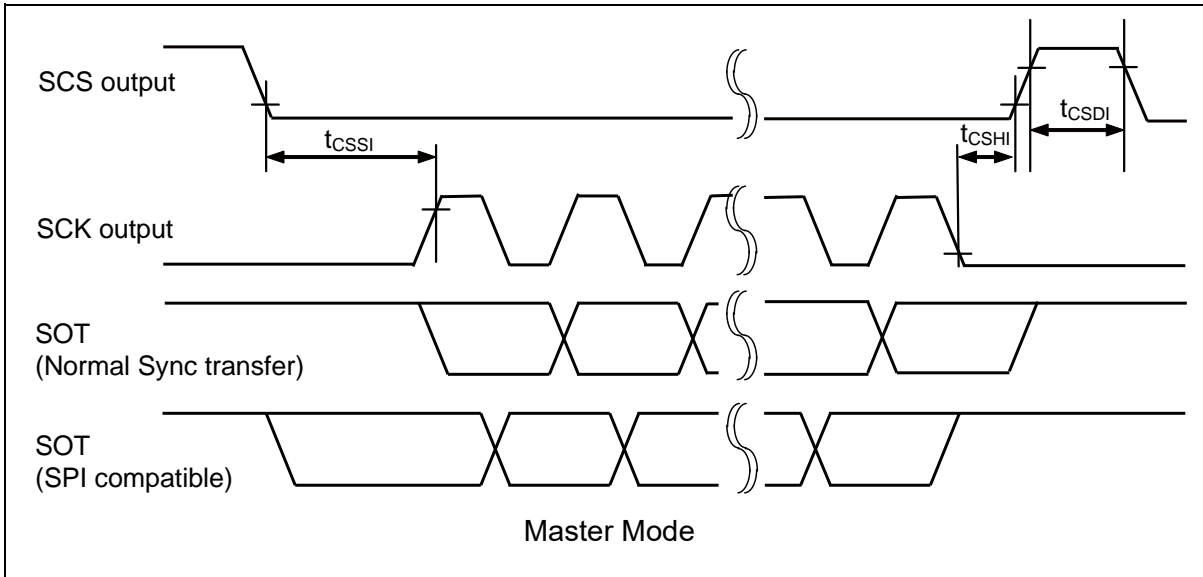
*3: $t_{CSDS} = SCSTR:CSDS15-0 \times$ Serial chip select timing operation clock

*4: Only available with CY91F583AM/F584AM/F585AM

For details of *1, *2 and *3 above, see Hardware Manual.

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "H" (SMR:SCINV=0)
- Serial chip select inactive level "L" (SCSCR:CSLVL=0)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ ⇒ SCK ↓ setup time	t _{CSSI}	SCK1, SCK2 ^{*4} , SCK3 ^{*4} ,	Master mode C _L =50pF	t _{CSSU} ^{*1} +0	t _{CSSU} ^{*1} +50	ns	
SCK ↑ ⇒ SCS ↓ hold time	t _{CSDI}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		t _{CSDI} ^{*2} -50	t _{CSDI} ^{*2} +0	ns	
SCS deselect time	t _{CSDI}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		-50+5t _{CPP} +t _{CSDS} ^{*3}	+50+5t _{CPP} +t _{CSDS} ^{*3}	ns	
SCS ↑ ⇒ SCK ↓ setup time	t _{CSSE}	SCK1, SCK2 ^{*4} , SCK3 ^{*4} ,	Slave mode C _L =50pF	3t _{CPP} +30	-	ns	
SCK ↑ ⇒ SCS ↓ hold time	t _{CSHE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		0	-	ns	
SCS deselect time	t _{CSDE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		3t _{CPP} +30	-	ns	
SCS ↑ ⇒ SOT delay time	t _{DSE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4} , SOT1, SOT2 ^{*4} ,		-	40	ns	
SCS ↓ ⇒ SOT delay time	t _{DEE}	SOT3 ^{*4}		0	-	ns	

*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock

*2: t_{CSDI} =SCSTR:CSHD7-0 × Serial chip select timing operation clock

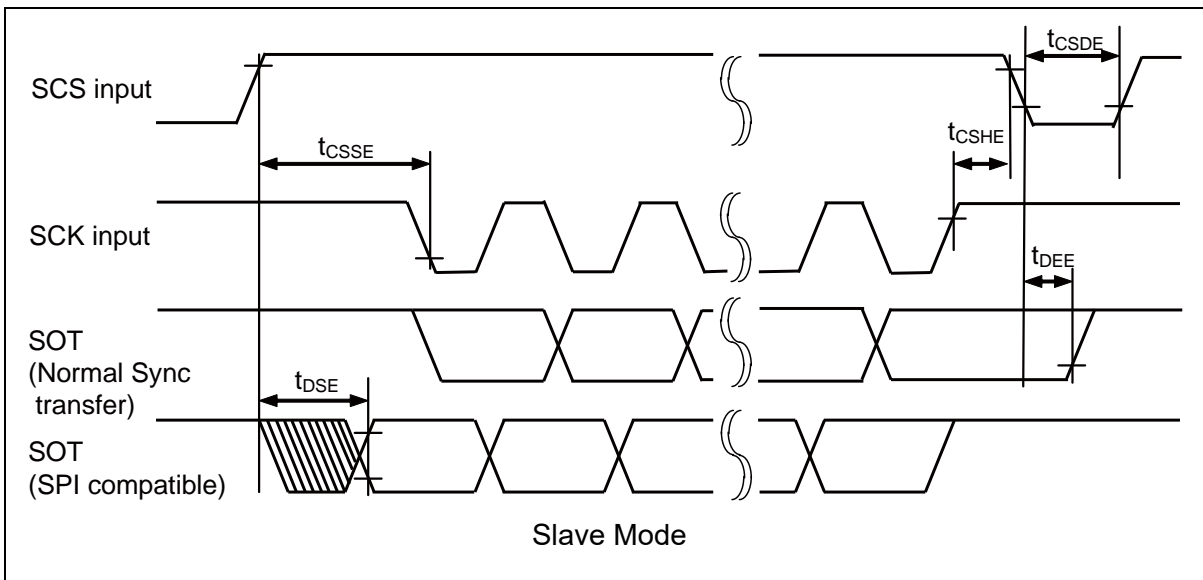
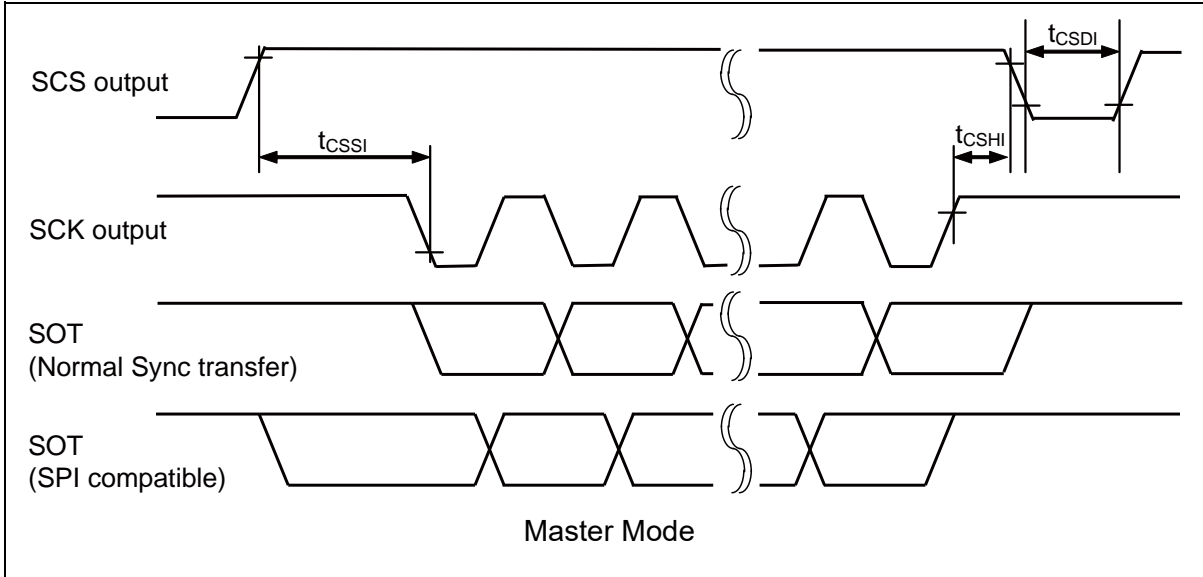
*3: t_{CSDS} =SCSTR:CSDS15-0 × Serial chip select timing operation clock

*4: Only available with CY91F583AM/F584AM/F585AM

For details of *1, *2 and *3 above, see Hardware Manual.

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "L" (SMR:SCINV=1)
- Serial chip select inactive level "L" (SCSCR:CSLVL=0)

(TA: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ ⇒ SCK ↑ setup time	t _{CSSI}	SCK1, SCK2 ^{*4} , SCK3 ^{*4} ,	Master mode C _L =50pF	t _{CSSU} ^{*1} +0	t _{CSSU} ^{*1} +50	ns	
SCK ↓ ⇒ SCS ↓ hold time	t _{CSDI}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		t _{CSDI} ^{*2} -50	t _{CSDI} ^{*2} +0	ns	
SCS deselect time	t _{CSDI}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		-50+5t _{CPP} +t _{CSDS} ^{*3}	+50+5t _{CPP} +t _{CSDS} ^{*3}	ns	
SCS ↑ ⇒ SCK ↑ setup time	t _{CSSE}	SCK1, SCK2 ^{*4} , SCK3 ^{*4} ,	Slave mode C _L =50pF	3t _{CPP} +30	-	ns	
SCK ↓ ⇒ SCS ↓ hold time	t _{CSHE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		0	-	ns	
SCS deselect time	t _{CSDE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4}		3t _{CPP} +30	-	ns	
SCS ↑ ⇒ SOT delay time	t _{DSE}	SCS1, SCS2 ^{*4} , SCS3 ^{*4} ,		-	40	ns	
SCS ↓ ⇒ SOT delay time	t _{DEE}	SOT1, SOT2 ^{*4} , SOT3 ^{*4}		0	-	ns	

*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock

*2: t_{CSDI}=SCSTR:CSHD7-0 × Serial chip select timing operation clock

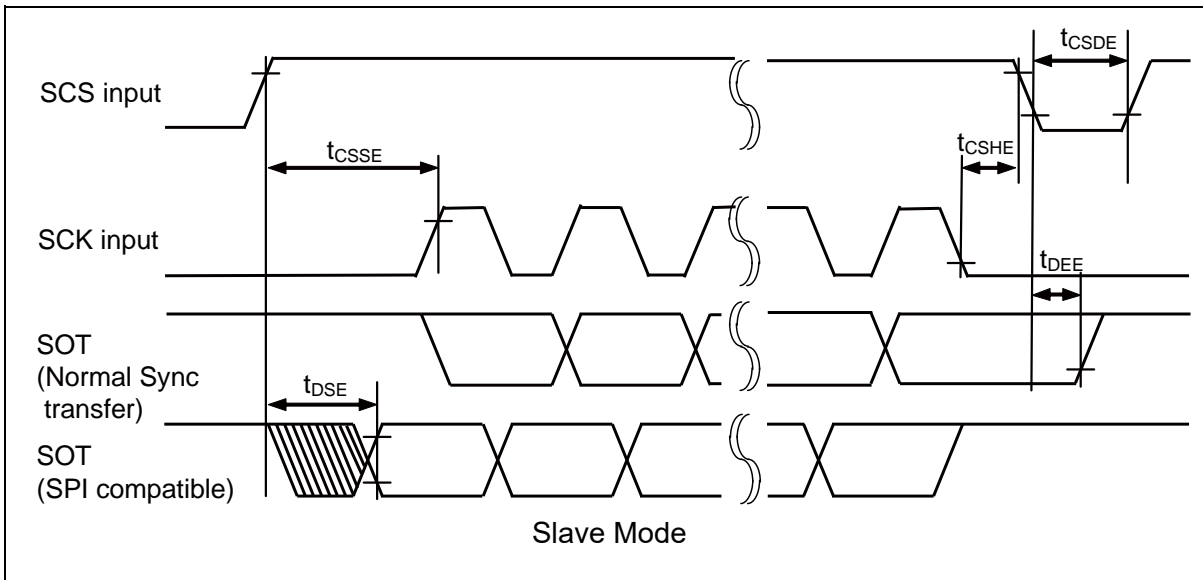
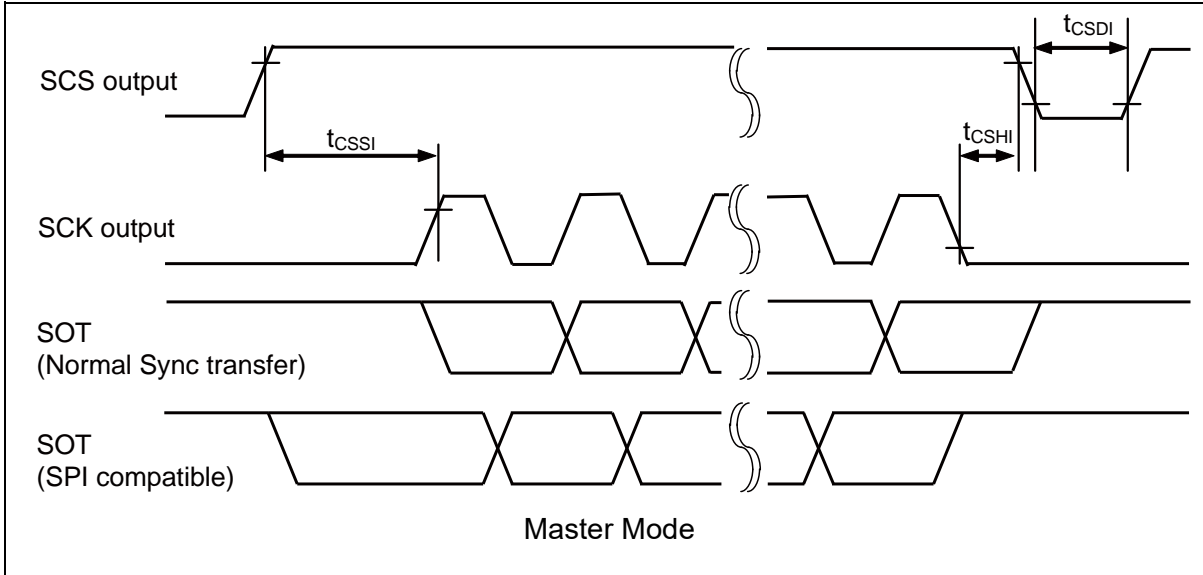
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock

*4: Only available with CY91F583AM/F584AM/F585AM

For details of *1, *2 and *3 above, see Hardware Manual.

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



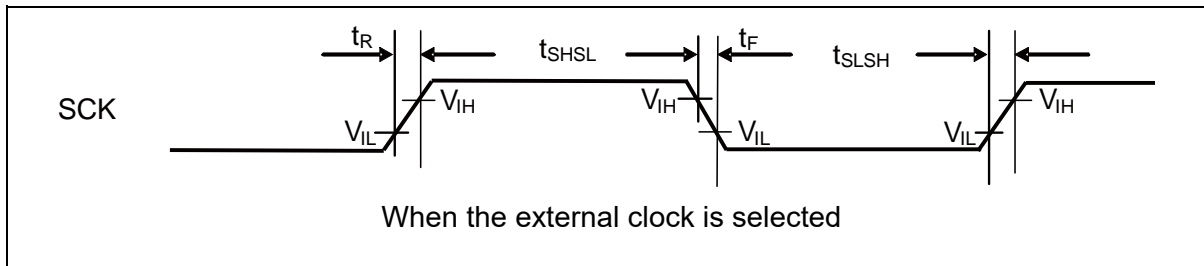
UART (Async Serial Interface) timing (SMR:MD2-0="000"b, "001"b)

When the external clock is selected (BGR:EXT=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t _{SLSH}	SCK0_0, SCK0_1', SCK1, SCK2', SCK3'	C _L =50pF	t _{CPP} +10	-	ns	
Serial clock "H" pulse width	t _{SHSL}			t _{CPP} +10	-	ns	
SCK fall time	t _F			-	5	ns	
SCK rise time	t _R			-	5	ns	

*: Only available with CY91F583AM/F584AM/F585AM



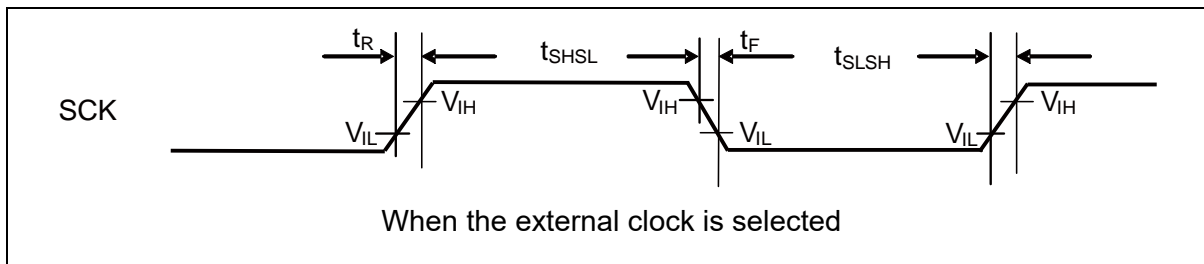
LIN interface (v2.1)(LIN Communication Control Interface (v2.1)) timing (SMR:MD2-0="011"b)

When the external clock is selected (BGR:EXT=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t _{SLSH}	SCK0_0, SCK0_1', SCK1, SCK2', SCK3'	C _L =50pF	t _{CPP} +10	-	ns	
Serial clock "H" pulse width	t _{SHSL}			t _{CPP} +10	-	ns	
SCK fall time	t _F			-	5	ns	
SCK rise time	t _R			-	5	ns	

*: Only available with CY91F583AM/F584AM/F585AM



I²C timing (SMR:MD2-0="100"b)

 (T_A: Recommended operating conditions, V_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Standard mode		High-speed mode ³		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f _{SCL}	SCK0_0, SCK0_1 ⁵ , SCK2 ⁵ , SCK3 ⁵ (SCL)	C _L =50pF R=(V _P /I _{OL}) ^{*1}	0	100	0	400	kHz	
"Repeat START condition" hold time SDA ↓ → SCL ↓	t _{HDSTA}	SCK0_0, SCK0_1 ⁵ , SCK2 ⁵ , SCK3 ⁵ (SCL) SOT0_0, SOT0_1 ⁵ , SOT2 ⁵ , SOT3 ⁵ (SDA)		4.0	-	0.6	-	μs	
"L" width for SCL clock	t _{LOW}	SCK0_0, SCK0_1 ⁵ , SCK2 ⁵ , SCK3 ⁵ (SCL)		4.7	-	1.3	-	μs	
"H" width for SCL clock	t _{HIGH}	(SCL)		4.0	-	0.6	-	μs	
"Repeat START condition" setup time SCL ↑ → SDA ↓	t _{SUSTA}	SCK0_0, SCK0_1 ⁵ , SCK2 ⁵ , SCK3 ⁵ (SCL)		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}			0	3.45 ^{*2}	0	0.90 ^{*3}	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t _{SUDAT}	SOT0_0, SOT0_1 ⁵ , SOT2 ⁵ , SOT3 ⁵ (SDA)		250	-	100	-	ns	
"STOP condition" setup time SCL ↑ → SDA ↑	t _{SUSTO}	(SDA)		4.0	-	0.6	-	μs	
Bus free time between "STOP condition" and "START condition"	t _{BUF}	-		4.7	-	1.3	-	μs	
Noise filter	t _{SP}	-		2t _{CPP} ^{*4}	-	2t _{CPP} ^{*4}	-	ns	

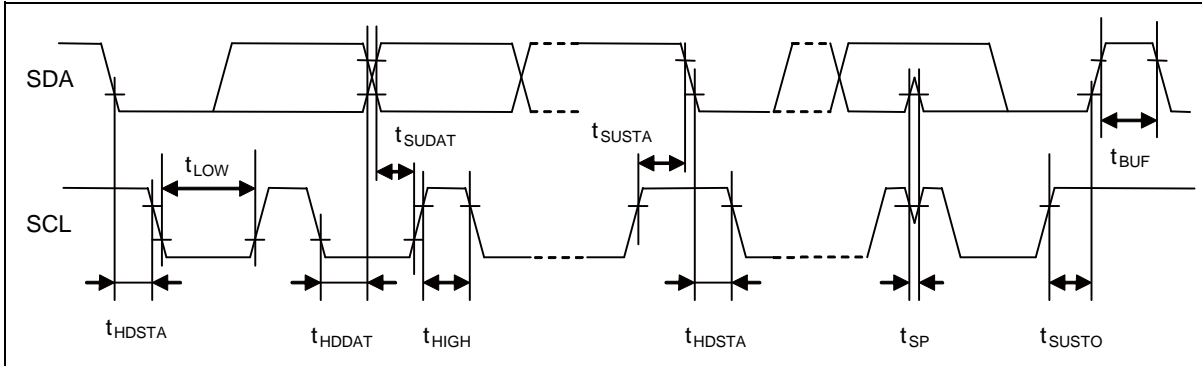
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. V_P shows that the power supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust t_{clock} of the peripheral bus to 8MHz or more when using I²C.

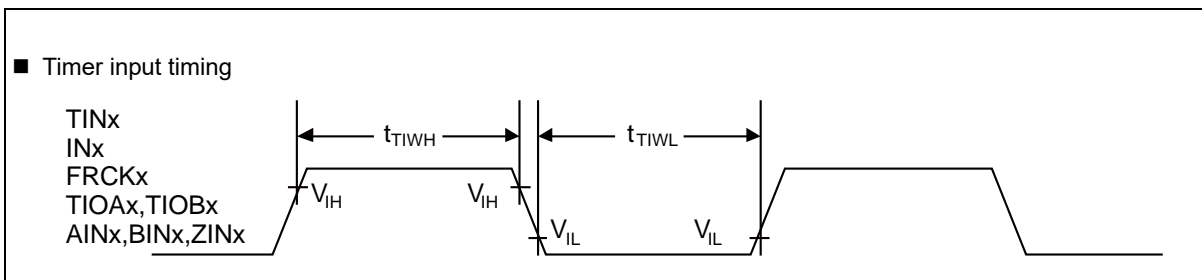
*5: Only available with CY91F583AM/F584AM/F585AM



11.4.5 Timer Input Timing

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{TIWH}	TIN0 to TIN3, IN0 to IN3, FRCK0 to FRCK5, TIOA1, TIOB0, TIOB1	-	4t _{CPP}	-	ns	
	t _{TIWL}	AIN0,AIN1, BIN0,BIN1, ZIN0,ZIN1	-	2t _{CPP}	-	ns	

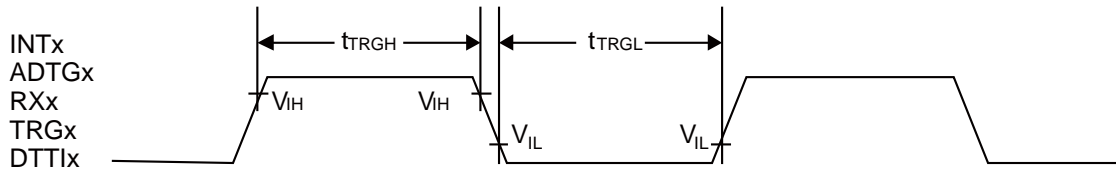


11.4.6 Trigger Input Timing

(T_A: Recommended operating conditions, V_{CC} =5.0V±10% V_{SS}=AV_{SS}=0.0V)

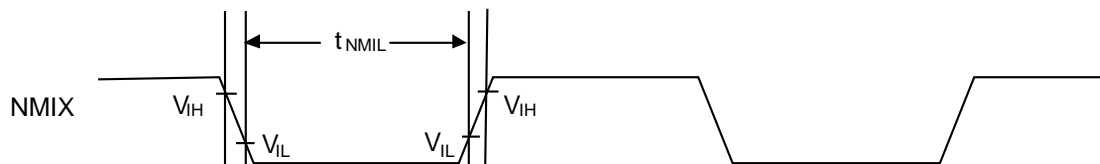
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t _{TRGH}	INT0 to INT6, INT7*, ADTG0 to ADTG2,	-	5t _{CPP}	-	ns	
	t _{TRGL}	RX0, RX1*, TRG0, TRG1,		1	-	µs	

*: Only available with CY91F583AM/F584AM/F585AM

Trigger input timing

11.4.7 NMI Input Timing

(T_A : Recommended operating conditions, $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0V$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	-	$4t_{CPP}$	-	ns	

NMIX input timing


11.4.8 Low-voltage Detection (External Low-voltage Detection)

 (TA: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V _{DP5}	VCC5	-	3.7	-	5.5	V	
Detection voltage	V _{DL}	VCC5	*1	-8%	3.9	+8%	V	When power supply voltage falls and detection level is set initially
Hysteresis width	V _{HYS}	VCC5	-	-	0.1	-	V	When power supply voltage rises
Low-voltage detection time	T _d	-	-	-	-	30	μs	
Power supply voltage fluctuation rate	-	VCC5	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (T_d), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: In order to perform the low-voltage detection at the detection voltage (V_{DL}), be sure to suppress fluctuation of the power supply within the limits of the power supply voltage fluctuation rate.

11.4.9 Low-voltage Detection (Internal Low-voltage Detection)

 (TA: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V _{RDP5}	-	-	1.1	-	1.3	V	
Detection voltage	V _{RDL}	-	*	0.8	0.9	1.0	V	When power supply voltage falls
Hysteresis width	V _{RHYS}	-	-	-	0.1	-	V	When power supply voltage rises
Low-voltage detection time	-	-	-	-	-	30	μs	

*: If the fluctuation of the power supply is faster than the low-voltage detection time, there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

11.5 A/D Converter

11.5.1 Electrical Characteristics

(TA: Recommended operating conditions, V_{CC} =5.0V±10%, AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Non linearity error	-	-	-4.0	-	+4.0	LSB	
Differential linearity error	-	-	-1.9	-	+1.9	LSB	
Zero transition voltage	V _{OT}	AN0 to AN14, AN16 to AN18 ³ , AN19, AN20, AN21 to AN23 ³	AVRL+ 0.5LSB-20	-	AVRL+ 0.5LSB+20	mV	1LSB= (VFST-VOT)/4094
Full-scale transition voltage	V _{FST}	AN0 to AN14, AN16 to AN18 ³ , AN19, AN20, AN21 to AN23 ³	AVRH- 1.5LSB-20	-	AVRH- 1.5LSB+20	mV	
Sampling time	t _{SMP}	-	0.3	-	12	μs	*1
Compare time	t _{CMP}	-	0.7	-	28	μs	*1
A/D conversion time	t _{CNV}	-	1.0	-	40	μs	*1
Analog port input current	I _{AIN}	AN0 to AN14, AN16 to AN18 ³ , AN19, AN20, AN21 to AN23 ³	-1.0	-	1.0	μA	V _{AVSS} ≤ V _{AIN} ≤ V _{AVCC}
Analog input voltage	V _{AIN}	AN0 to AN14, AN16 to AN18 ³ , AN19, AN20, AN21 to AN23 ³	AV _{SS}	-	AVRH	V	
Reference voltage	AVRH	AVRH0, AVRH1	4.5	-	5.5	V	Avcc ≥ AVRH
	AVRL	AVRL0, AVRL1,	-	0.0	-	V	
Power supply current	I _A	AVCC0,	-	1.5	2.1	mA	3 units operating
	I _{AH}	AVCC1	-	-	25	μA	3 units operating ^{*2}
	I _R	AVRH0,	-	3	6	mA	3 units operating
	I _{RH}	AVRH1	-	-	4.8	μA	3 units operating ^{*2}
Variation between channels	-	AN0 to AN14, AN16 to AN18 ³ , AN19, AN20, AN21 to AN23 ³	-	-	4	LSB	Every 1 unit ^{*4}

*1: Time for each channel.

*2: The Power supply current (V_{CC}=AV_{CC}=5.0V) is specified if the A/D converter is not operating and CPU is stopped.

*3: Only available with CY91F583AM/F584AM/F585AM

*4: Unit0 AN0 to AN7

Unit1 AN8 to AN14

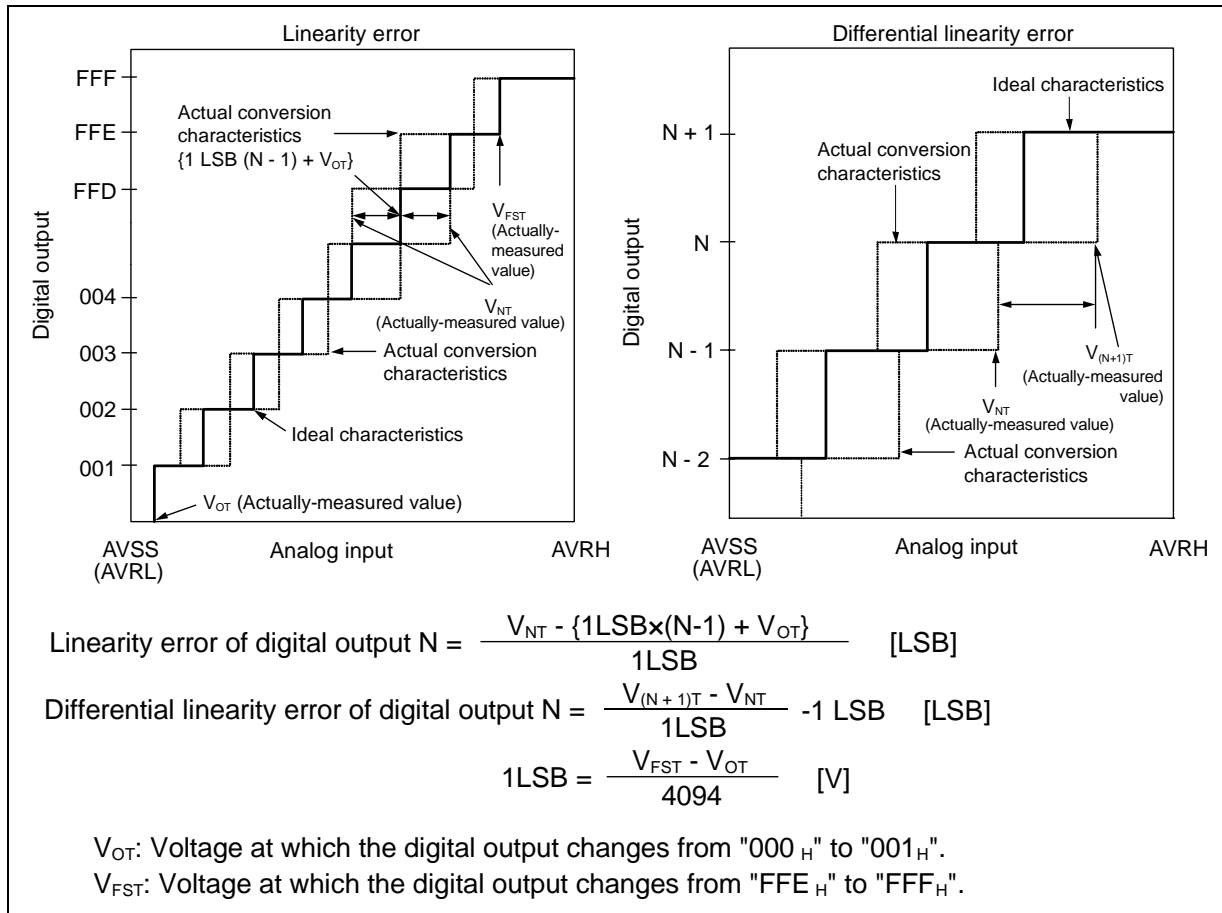
Unit2 AN16 to AN23

11.5.2 Definition of Terms

Resolution: Analog variation that is recognized by an A/D converter.

Linearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000" ↔ "0000 0000 0001") to the full-scale transition point ("1111 1111 1110" ↔ "1111 1111 1111").

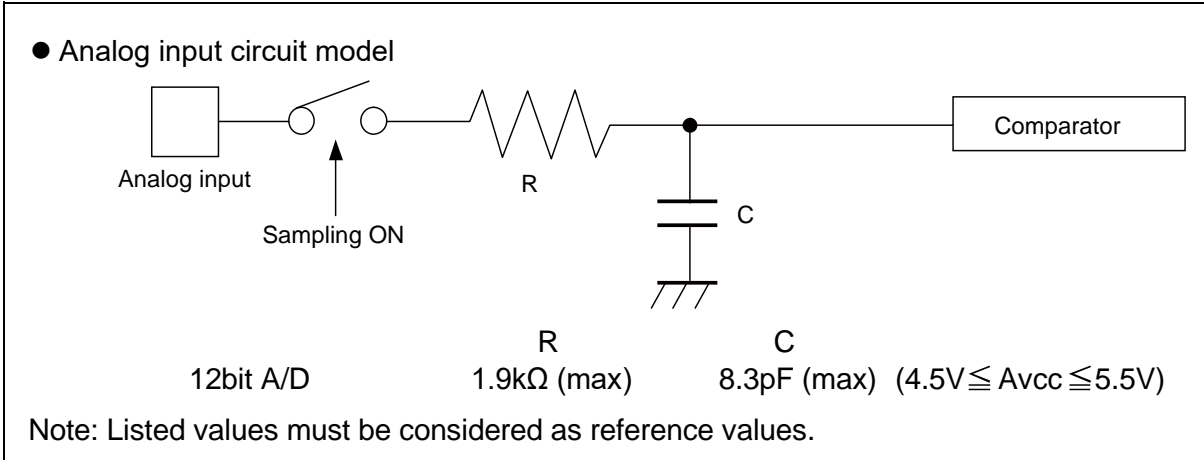
Differential linearity error: Deviation of the input voltage from the ideal value that is required to change the output code by 1LSB.



11.5.3 Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling time for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 μF) to the analog input pin.



11.6 D/A Converter

(T_A: Recommended operating conditions, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Differential linearity error	-	-	-4.0	-	+4.0	LSB	When the analog output voltage is 0.5V to 4.5V

11.7 Flash memory

11.7.1 Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	200	800	ms	8 Kbyte sector ^{*1} excluding internal preprogramming time
	-	300	1100	ms	8 Kbyte sector ^{*1} including internal preprogramming time
	-	400	2000	ms	64 Kbyte sector ^{*1} excluding internal preprogramming time
	-	700	3700	ms	64 Kbyte sector ^{*1} including internal preprogramming time
8-bit writing time	-	9	288	μs	Excluding overhead time at system level ^{*1}
16-bit writing time	-	12	384	μs	Excluding overhead time at system level ^{*1}
ECC writing time	-	9	288	μs	Excluding overhead time at system level ^{*1}
Erase cycle ^{*2} / Data retention time	1,000 cycles/20 years, 10,000 cycles/10 years, 100,000 cycles/5 years	-	-	-	Average temperature T _A =+85°C ^{*3}

*1: The guaranteed value for erase up to 100,000 cycles

*2: Number of erase cycles for each sector

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

11.7.2 Notes

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited.

In the application system where V_{CC} might disappear while writing or erasing, be sure to turn the power off by using an external low-voltage detection function.

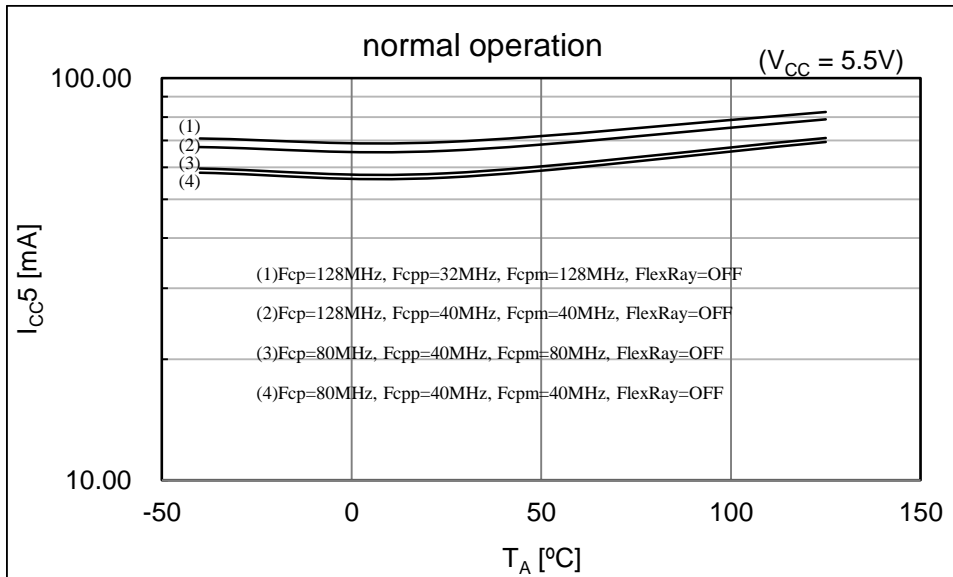
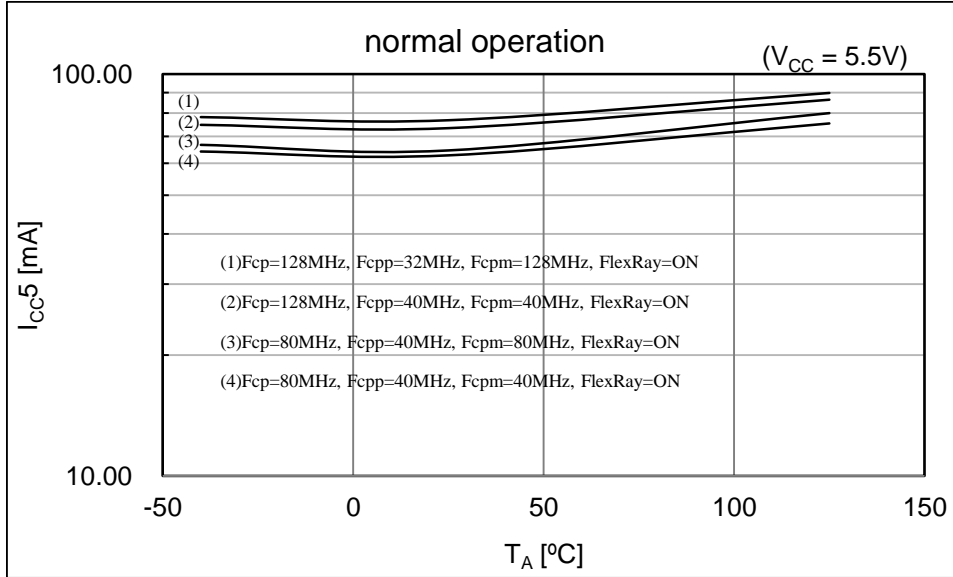
To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}^{*}), hold V_{CC} at 2.7V or more within the duration calculated by the following expression:

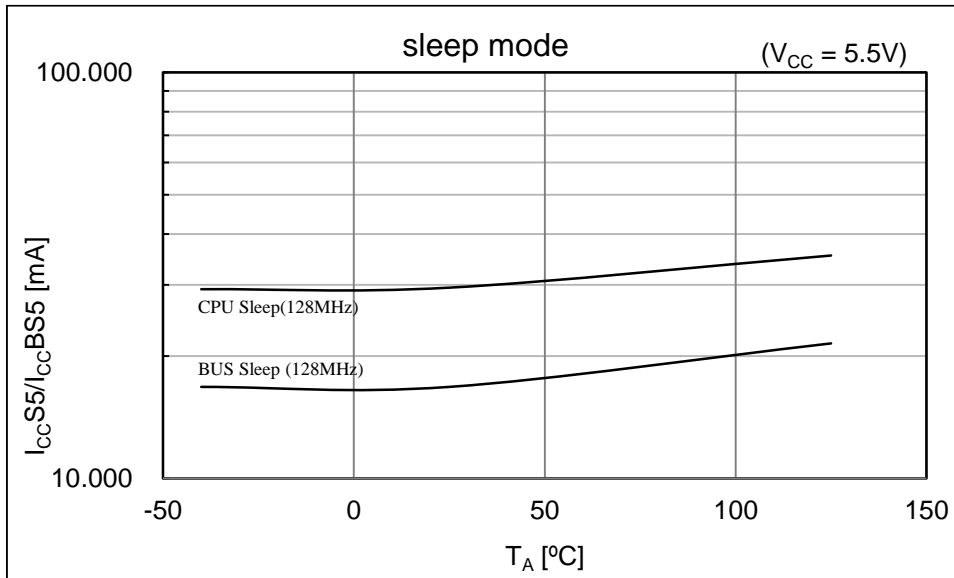
$$T_d^*[\mu s] + (PCLK \text{ cycle}[\mu s] \times 257) + 50[\mu s]$$

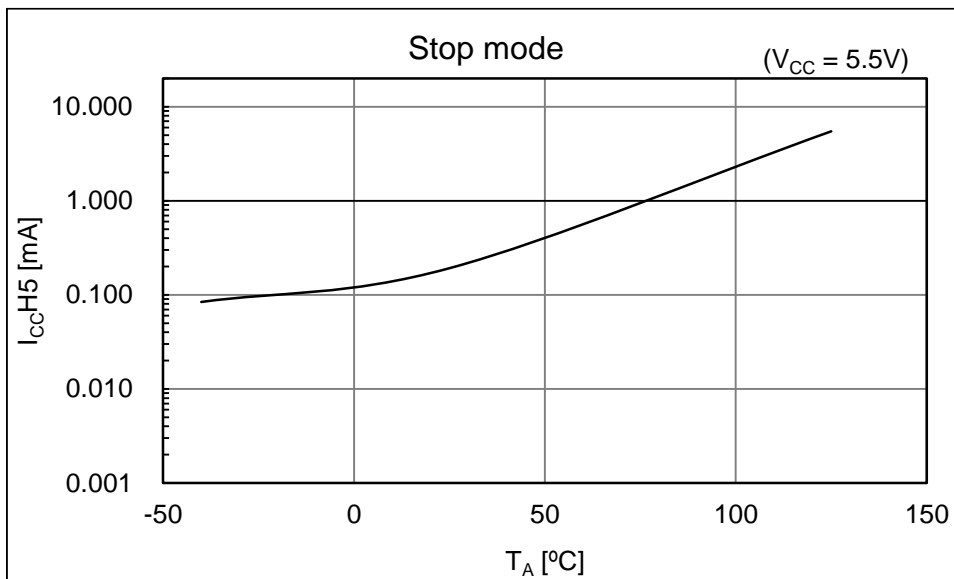
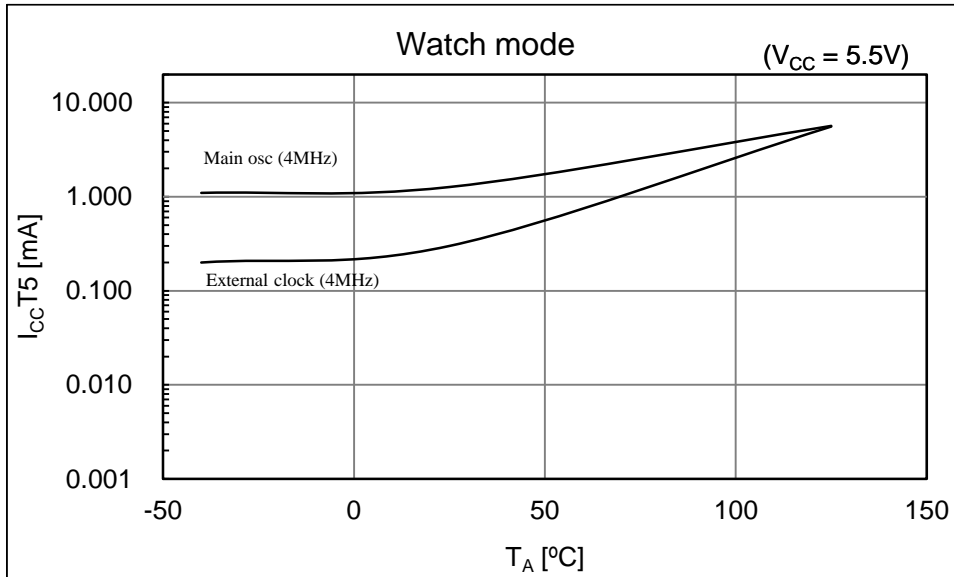
*: See "4. AC characteristics (8) Low-voltage detection (External low-voltage detection)."

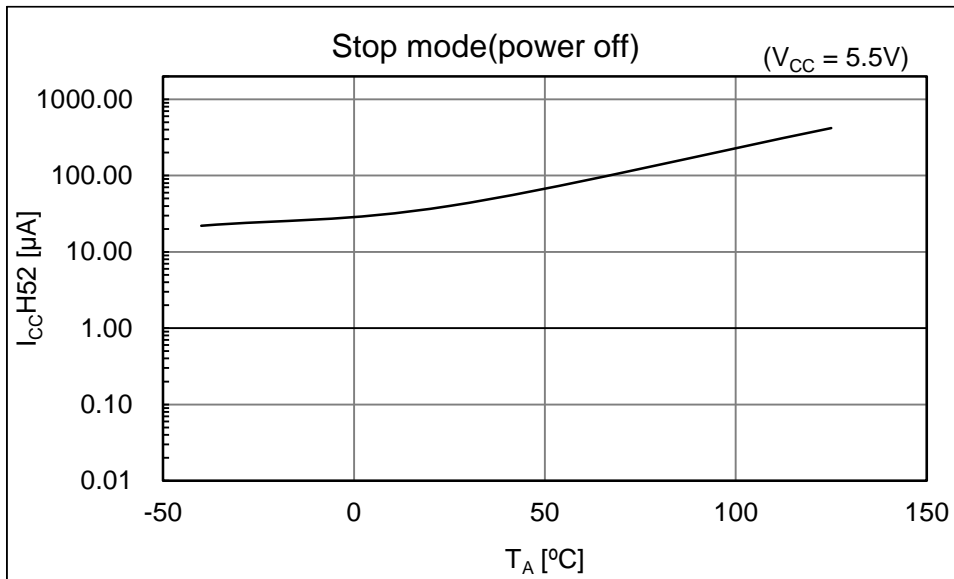
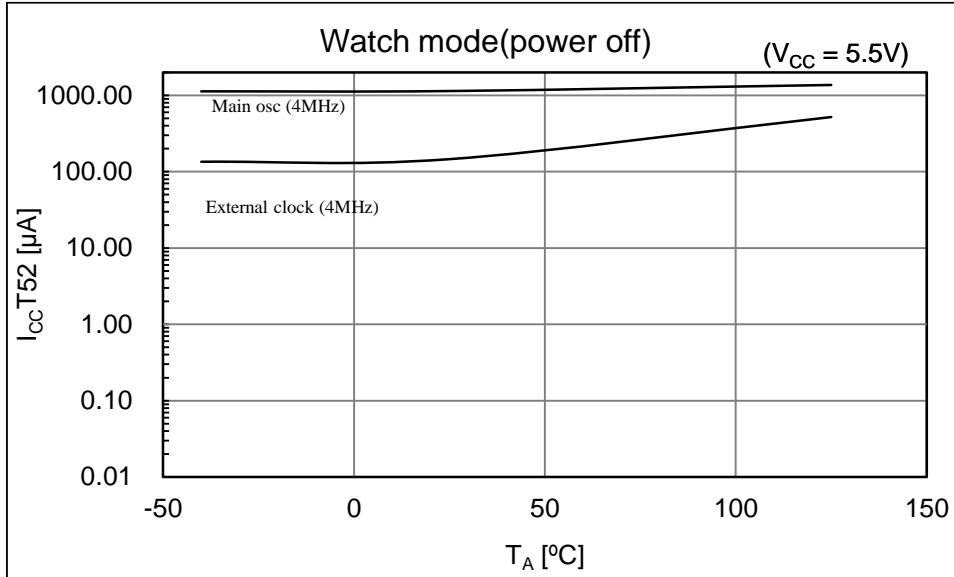
12. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.









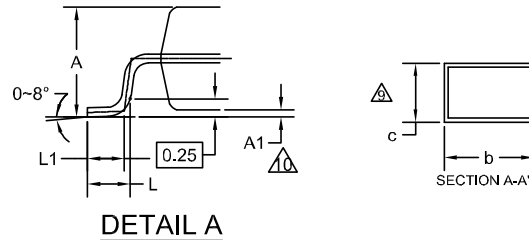
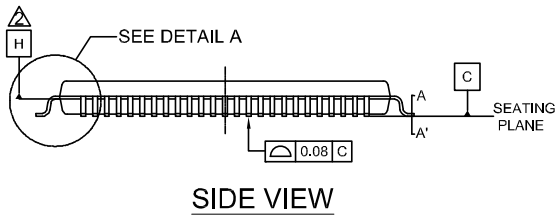
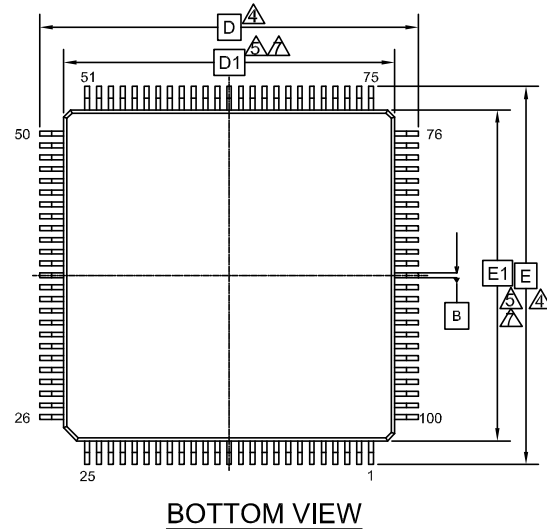
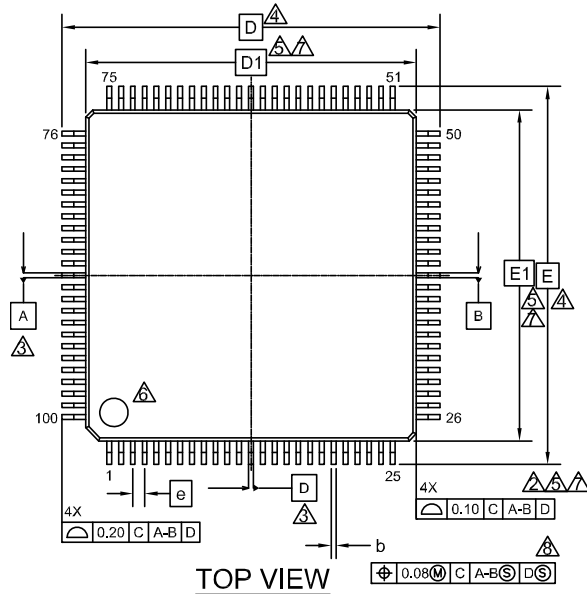
13. Ordering Information

Part number	Package*
CY91F583AMGPMC-GTE1 CY91F584AMGPMC-GTE1 CY91F585AMGPMC-GTE1 CY91F583AMHPMC-GTE1 CY91F584AMHPMC-GTE1 CY91F585AMHPMC-GTE1 CY91F583AMJPMC-GTE1 CY91F584AMJPMC-GTE1 CY91F585AMJPMC-GTE1 CY91F583AMKPMC-GTE1 CY91F584AMKPMC-GTE1 CY91F585AMKPMC-GTE1	100-pin plastic LQFP (LQI100)
CY91F583ASGPMC1-GTE1 CY91F584ASGPMC1-GTE1 CY91F585ASGPMC1-GTE1 CY91F583ASHPMC1-GTE1 CY91F584ASHPMC1-GTE1 CY91F585ASHPMC1-GTE1 CY91F583ASJPMC1-GTE1 CY91F584ASJPMC1-GTE1 CY91F585ASJPMC1-GTE1 CY91F583ASKPMC1-GTE1 CY91F584ASKPMC1-GTE1 CY91F585ASKPMC1-GTE1	64-pin plastic LQFP (LQD064)

*: For details of the package, see Package Dimensions

14. Package Dimensions

Package Type	Package Code
LQFP 100	LQ1100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.25
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

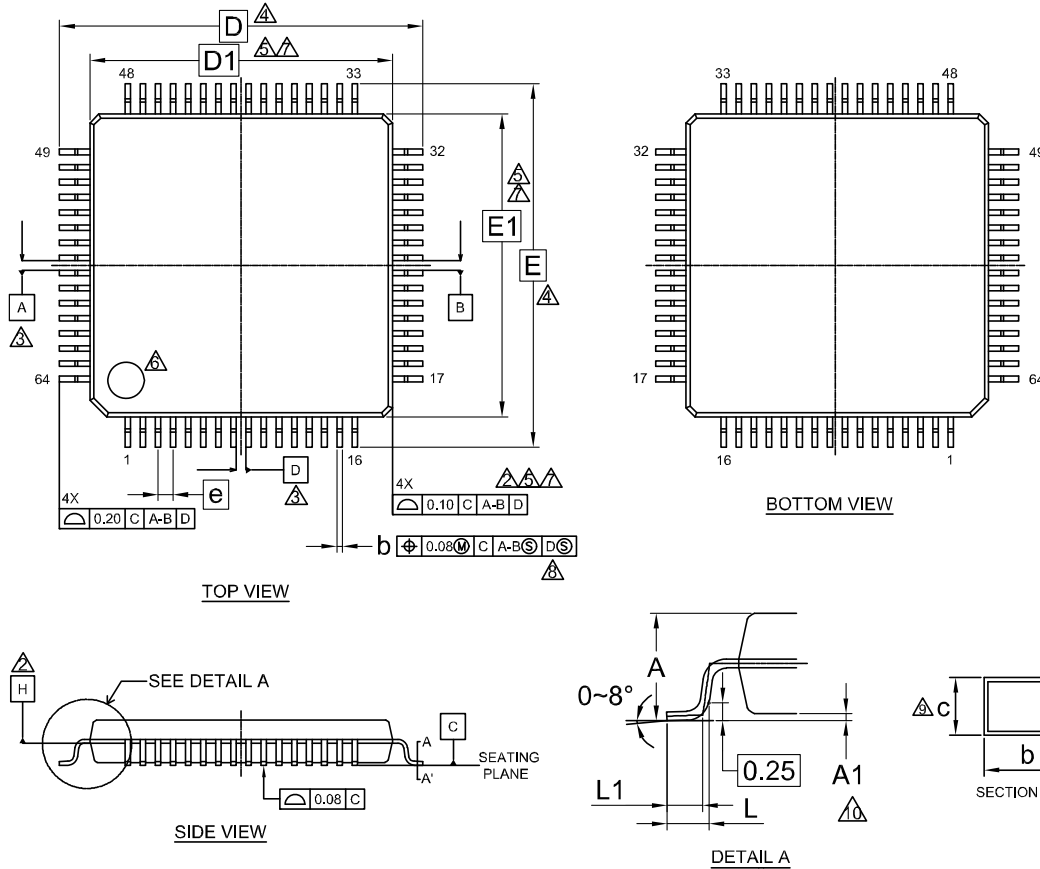
NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-25980 **

PACKAGE OUTLINE, 100 LEAD LQFP
14,0X14,0X1,7 MM LQ1100 for legacy MB product

Package Type	Package Code
LQFP 64	LQD064



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.25
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC.		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-25982 **

PACKAGE OUTLINE: 64 LEAD LQFP
10.0X10.0X1.7 MM LQD064 for Legacy M3 product

15. Major Changes

Spancion Publication Number: MB91F585AMG_DS705-00013

Page	Section	Change Results																																																
Revision 1.0																																																		
-	-	Initial release																																																
Revision 2.0																																																		
-	-	<p>The product series name should be corrected.</p> <table border="0"> <tr><td>MB91F585MG</td><td>MB91F585AMG</td></tr> <tr><td>MB91F585MH</td><td>MB91F585AMH</td></tr> <tr><td>MB91F585MJ</td><td>MB91F585AMJ</td></tr> <tr><td>MB91F585MK</td><td>MB91F585AMK</td></tr> <tr><td>MB91F584MG</td><td>MB91F584AMG</td></tr> <tr><td>MB91F584MH</td><td>MB91F584AMH</td></tr> <tr><td>MB91F584MJ</td><td>MB91F584AMJ</td></tr> <tr><td>MB91F584MK</td><td>MB91F584AMK</td></tr> <tr><td>MB91F583MG</td><td>MB91F583AMG</td></tr> <tr><td>MB91F583MH</td><td>MB91F583AMH</td></tr> <tr><td>MB91F583MJ</td><td>MB91F583AMJ</td></tr> <tr><td>MB91F583MK</td><td>→ MB91F583AMK</td></tr> <tr><td>MB91F585SG</td><td>MB91F585ASG</td></tr> <tr><td>MB91F585SH</td><td>MB91F585ASH</td></tr> <tr><td>MB91F585SJ</td><td>MB91F585ASJ</td></tr> <tr><td>MB91F585SK</td><td>MB91F585ASK</td></tr> <tr><td>MB91F584SG</td><td>MB91F584ASG</td></tr> <tr><td>MB91F584SH</td><td>MB91F584ASH</td></tr> <tr><td>MB91F584SJ</td><td>MB91F584ASJ</td></tr> <tr><td>MB91F584SK</td><td>MB91F584ASK</td></tr> <tr><td>MB91F583SG</td><td>MB91F583ASG</td></tr> <tr><td>MB91F583SH</td><td>MB91F583ASH</td></tr> <tr><td>MB91F583SJ</td><td>MB91F583ASJ</td></tr> <tr><td>MB91F583SK</td><td>MB91F583ASK</td></tr> </table>	MB91F585MG	MB91F585AMG	MB91F585MH	MB91F585AMH	MB91F585MJ	MB91F585AMJ	MB91F585MK	MB91F585AMK	MB91F584MG	MB91F584AMG	MB91F584MH	MB91F584AMH	MB91F584MJ	MB91F584AMJ	MB91F584MK	MB91F584AMK	MB91F583MG	MB91F583AMG	MB91F583MH	MB91F583AMH	MB91F583MJ	MB91F583AMJ	MB91F583MK	→ MB91F583AMK	MB91F585SG	MB91F585ASG	MB91F585SH	MB91F585ASH	MB91F585SJ	MB91F585ASJ	MB91F585SK	MB91F585ASK	MB91F584SG	MB91F584ASG	MB91F584SH	MB91F584ASH	MB91F584SJ	MB91F584ASJ	MB91F584SK	MB91F584ASK	MB91F583SG	MB91F583ASG	MB91F583SH	MB91F583ASH	MB91F583SJ	MB91F583ASJ	MB91F583SK	MB91F583ASK
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2	Features	<p>The features of CR oscillation should be corrected.</p> <p>Oscillation frequency: 100kHz, with frequency accuracy ± 10%</p> <p style="text-align: center;">↓</p> <p>Oscillation frequency: 100kHz, with frequency accuracy ± 50% (pre-trimming)</p>																																																
22	I/O Circuit Type	<p>The specification of "H" level input voltage and "L" level input voltage of FlexRay should be corrected.</p> <p>FlexRay input (0.65Vcc/0.35Vcc)</p> <p style="text-align: center;">↓</p> <p>FlexRay input (0.7Vcc/0.3Vcc)</p>																																																
33	Memory Map	<p>The memory map should be corrected.</p> <p>The address of "Reset vector table" and "Interrupt vector table" should be added</p>																																																
54,85	I/O Map Address:00150C _H	<p>The register name should be corrected.</p> <p>STMCR00 → STMCR0</p>																																																

Page	Section	Change Results
54,55,85	I/O Map Address: 00150 E _H , 001510 _H , 001511 _H , 001512 _H , 001513 _H	The registers should be deleted. SCS CR0,SCSTR30,SCSTR20,SCSTR10,SCSTR00
63,92	I/O Map Address:00D310 _H	The initial values of MHDS should be corrected. -0000000 -0000000 -0000000 10000000 ↓ -0000000 -0000000 -0000000 00000000
104	Electrical Characteristics DC Caharacteristics	The specification of "H" level input voltage of P021-P023,P025-P027 should be corrected. Min:0.65 xVcc ↓ Min: 0.7 x Vcc
105	Electrical Characteristics DC Caharacteristics	The specification of "L" level input voltage of P021-P023,P025-P027 should be corrected. Max: 0.35 x Vcc ↓ Max: 0.3 x Vcc
111	Electrical Characteristics AC Characteristics Main Clock Timing	The remarks of "CAN PLL jitter" should be deleted.
111	Electrical Characteristics AC Characteristics Main Clock Timing	The specifications of "The Built-in CR oscillation frequency" should be corrected. Min: 90kHz, Max: 110kHz ↓ Min:50kHz Max:150kHz,
-	-	Company name and layout design change

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: CY91F583AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK, CY91F584AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK, CY91F585AMG/AMH/AMJ/AMK/ASG/ASH/ASJ/ASK, CY91580M/S Series FR81S, 32-bit Microcontroller Datasheet

Document Number: 002-04665

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	KOJM	04/18/2014	Migrated to Cypress and assigned document number 002-04665. No change to document contents or format.
*A	5139690	KOJM	03/29/2016	Updated to Cypress template
*B	6508924	KOJM	03/20/2019	Marketing Part Numbers changed from prefix MB to prefix CY. Updated the 100-pin, 64-pin Package Dimensions.

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