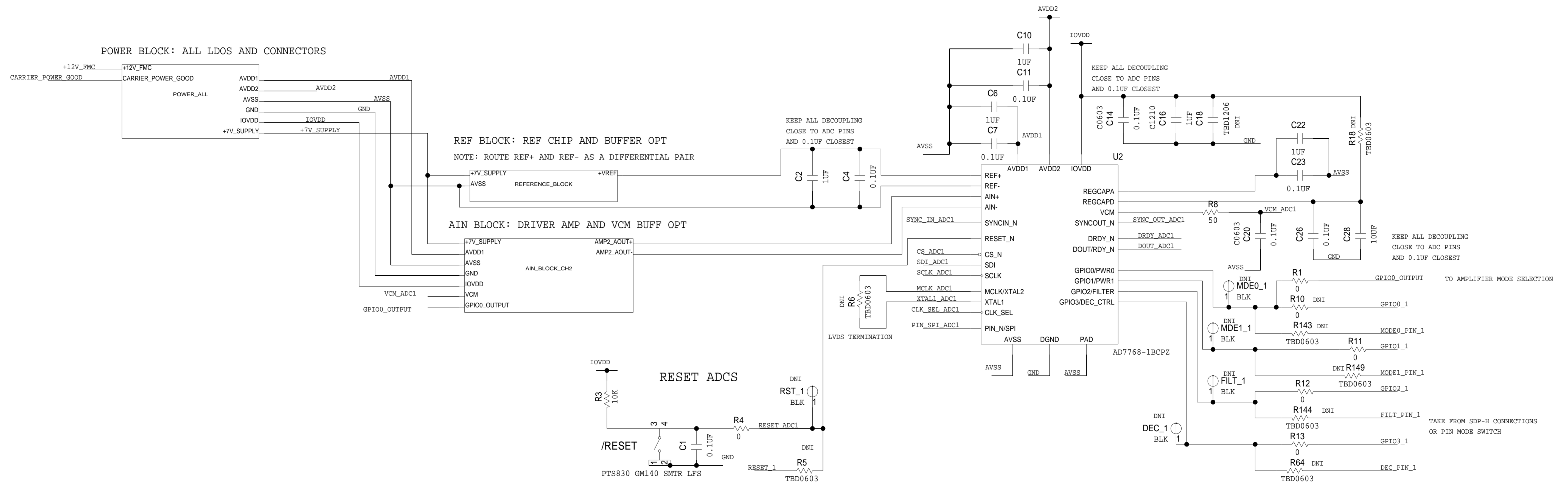


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

MAIN CONNECTIONS



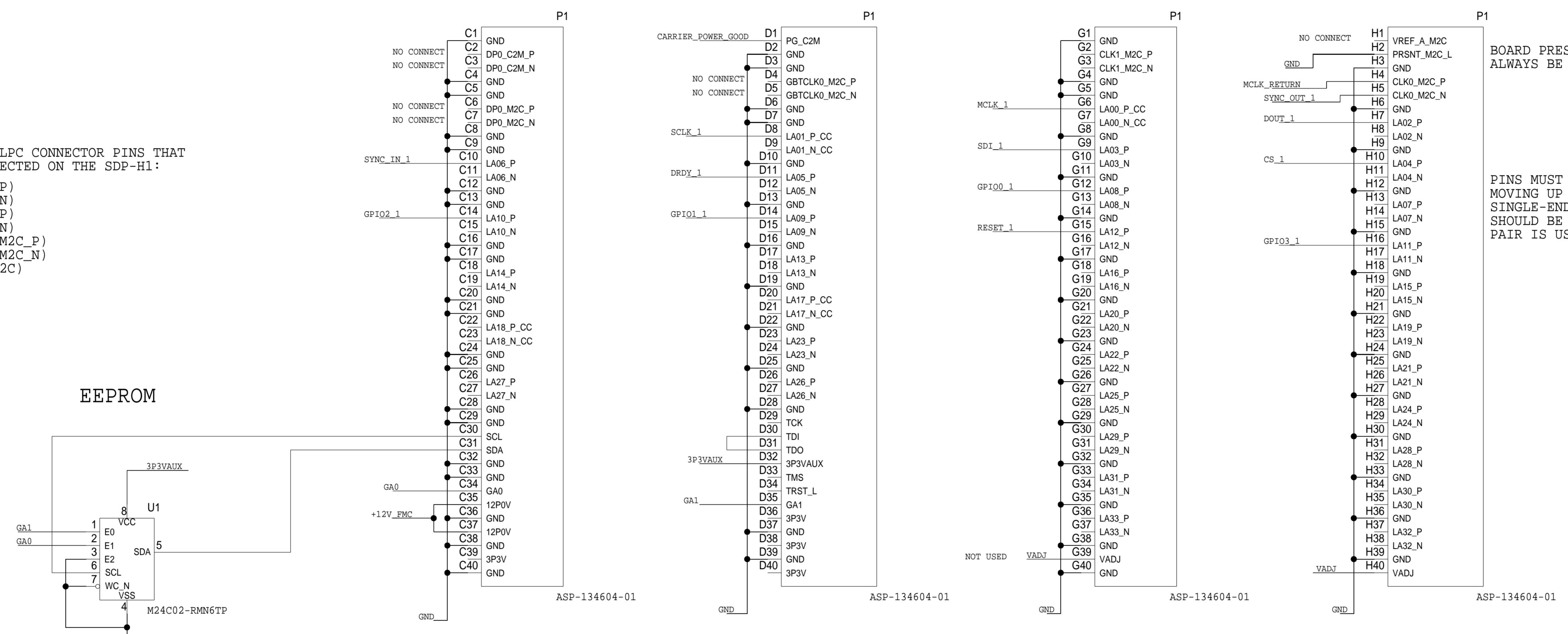
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	HW TYPE : Customer Evaluation Product(s): AD7768-1 : Modulator out version		
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_044287	REV E	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 2 OF 15

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

FPGA FMC CONNECTIONS

LIST OF FMC-LPC CONNECTOR PINS THAT ARE NOT CONNECTED ON THE SDP-H1:

- C2 (DP0_C2M_P)
- C3 (DP0_C2M_N)
- C6 (DP0_M2C_P)
- C7 (DP0_M2C_N)
- D4 (GBTCLK0_M2C_P)
- D5 (GBTCLK0_M2C_N)
- H1 (VREF_A_M2C)



BOARD PRESENT PIN (H2) MUST ALWAYS BE TIED TO GROUND

PINS MUST BE ASSIGNED STARTING WITH LA00 AND MOVING UP THE LA BUS UNTIL IT IS FULL. WHEN SINGLE-ENDED SIGNALING IS USED, THE _P LINE SHOULD BE USED BEFORE THE _N LINE OF THE SAME PAIR IS USED.

IF EVAL BOARD DOES NOT USE JTAG TDI AND TDO THEN THEY MUST BE SHORTED TOGETHER (AS SHOWN) SO AS NOT TO BREAK JTAG CHAIN

POWER SUPPLIES:
 12P0V. 1A MAX CURRENT LIMIT
 3P3V. 3A MAX CURRENT LIMIT
 VADJ. 2A MAX CURRENT LIMIT. 1.2V TO 3.3V.

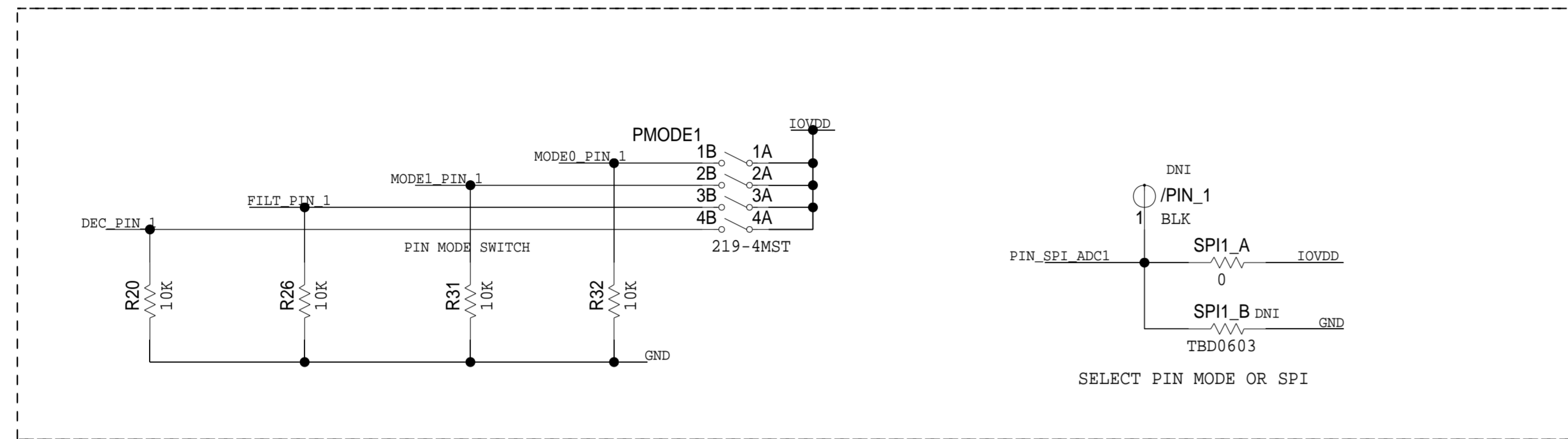
EEPROM REQUIRED IN VITA57.1 STANDARD.
 I2C LINE PULL-UP RESISTORS ON FPGA BOARD.
 I2C ADDRESS SET BY CONTROLLER BOARD.

	SCHEMATIC		
	HW TYPE : Customer Evaluation Product(s): Ad7768-1 : Modulator out version		
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_044287	REV E	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 3 OF 15

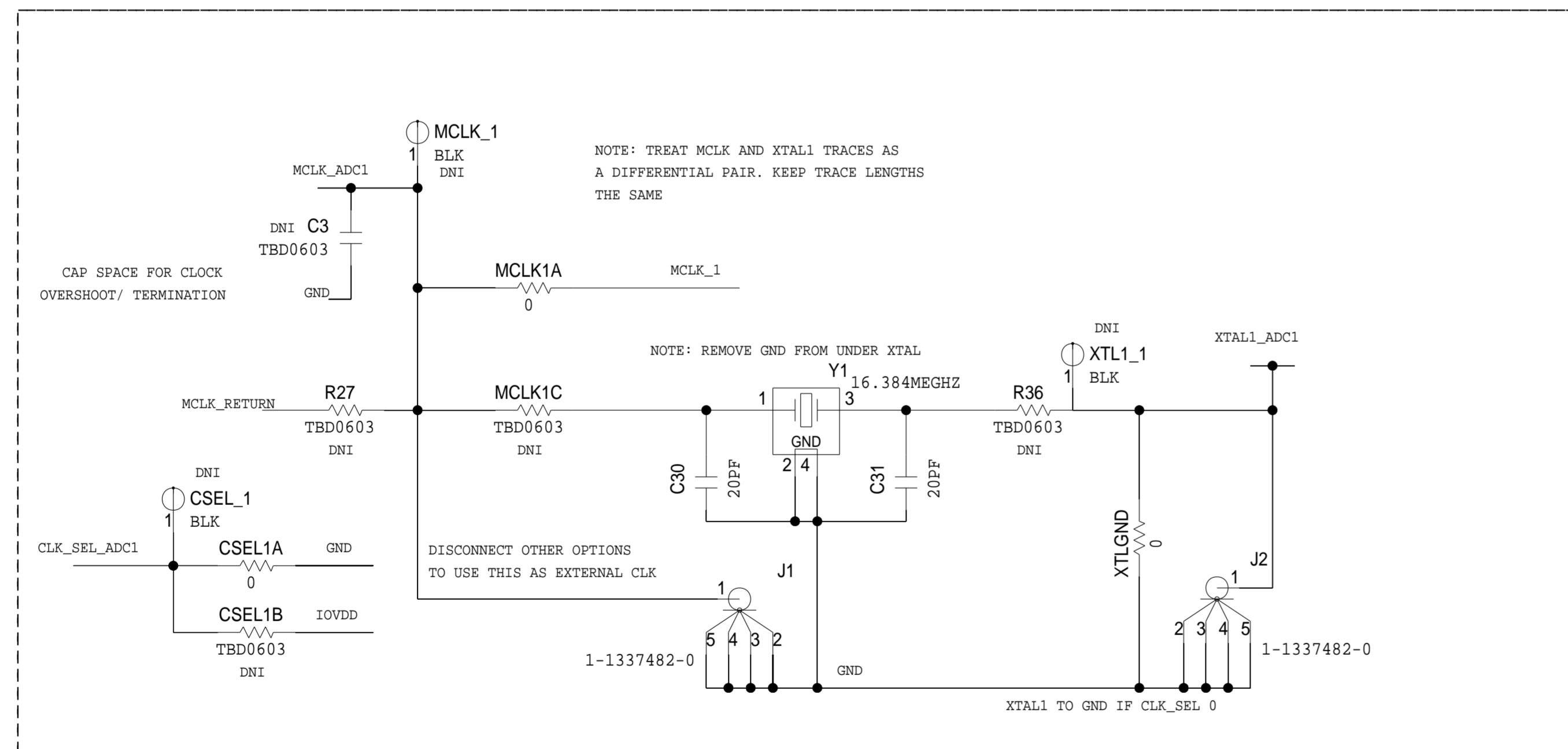
ADC DIGITAL CONNECTIONS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

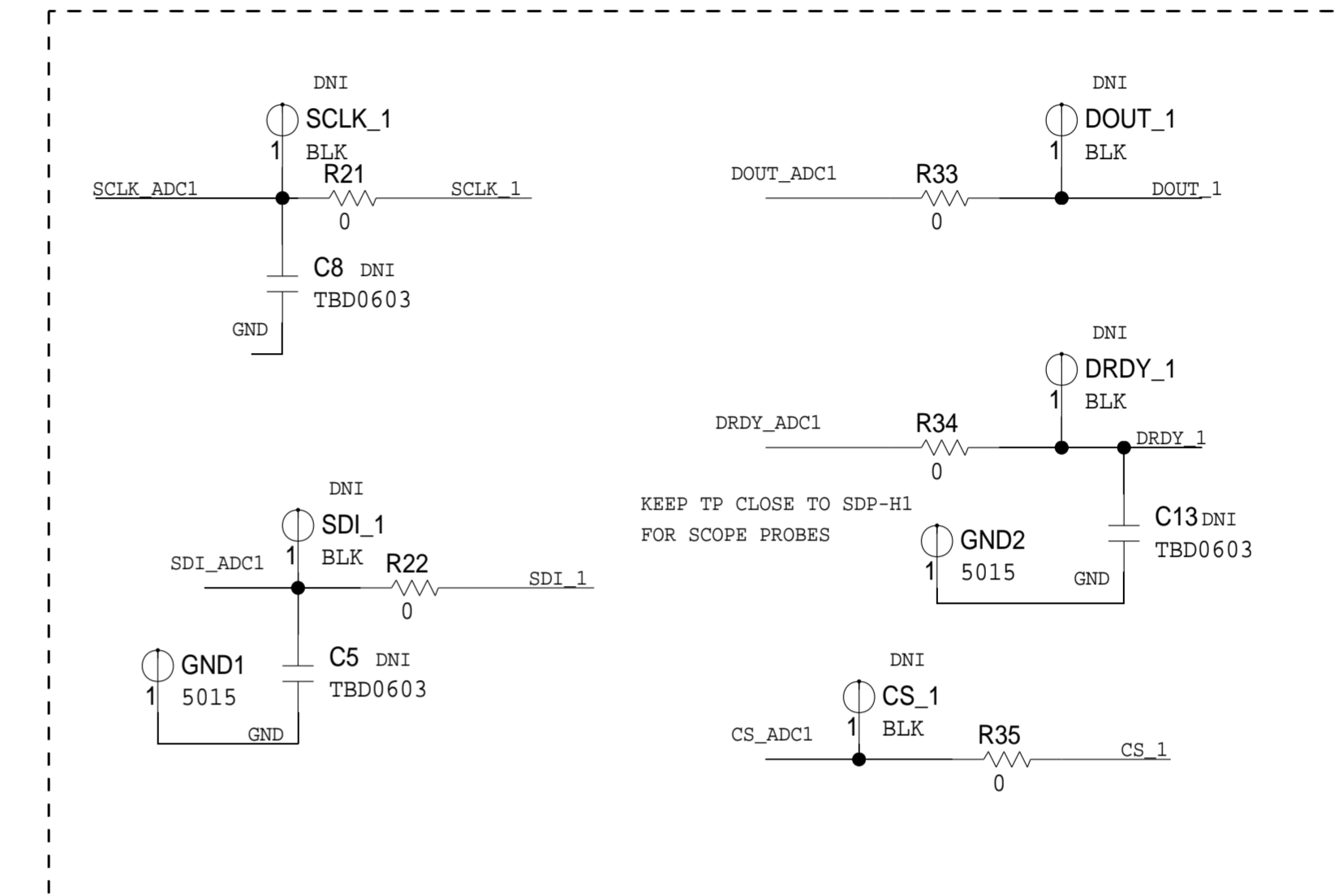
PIN MODE OPTIONS



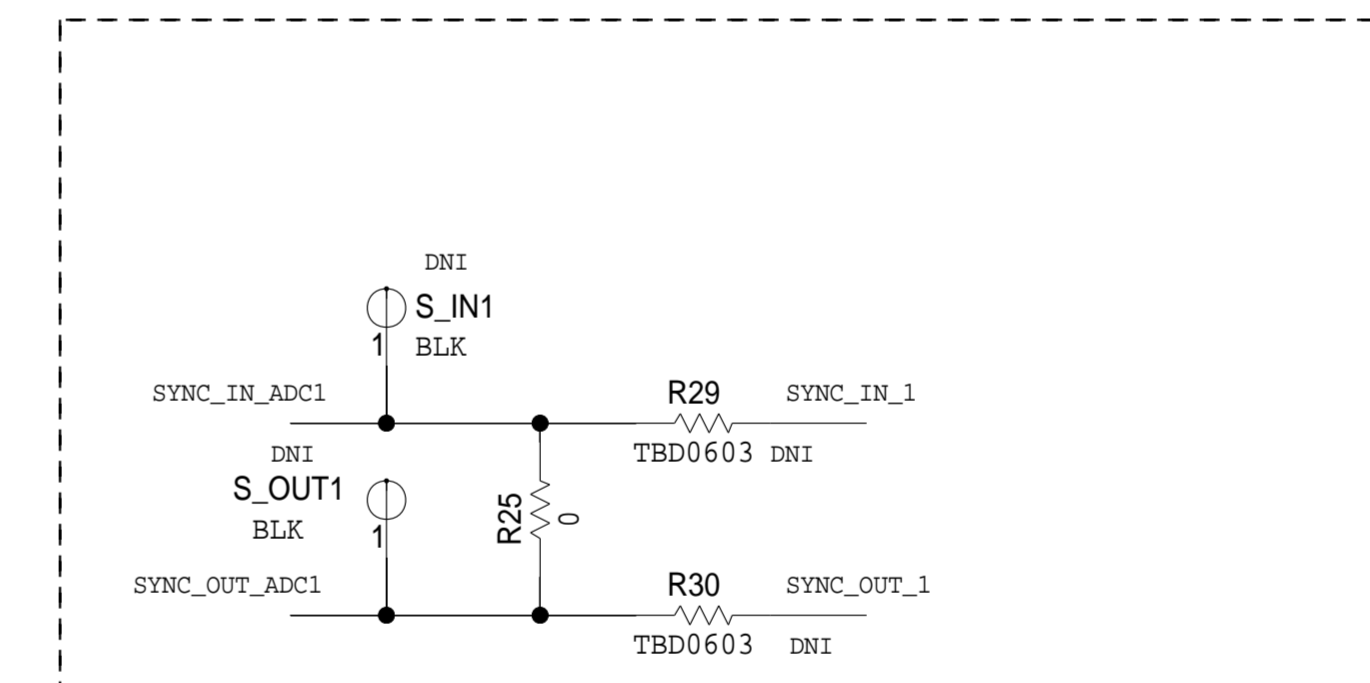
MCLK SELECTION



DATA INTERFACE



SYNC IN/OUT

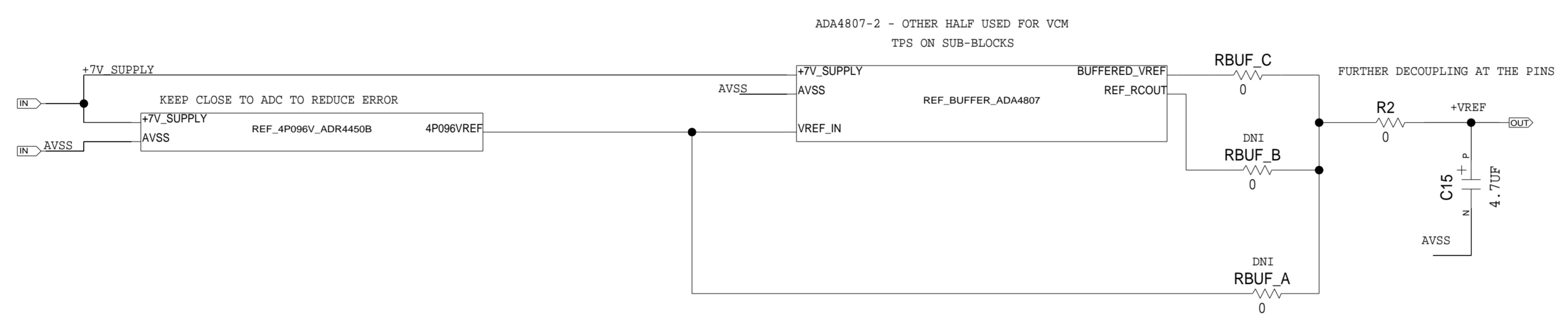


ANALOG DEVICES		SCHEMATIC		
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PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 4 OF 15	

8 7 6 5 4 3 2 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

REFERENCE BLOCK - ALL



D
C
B
A

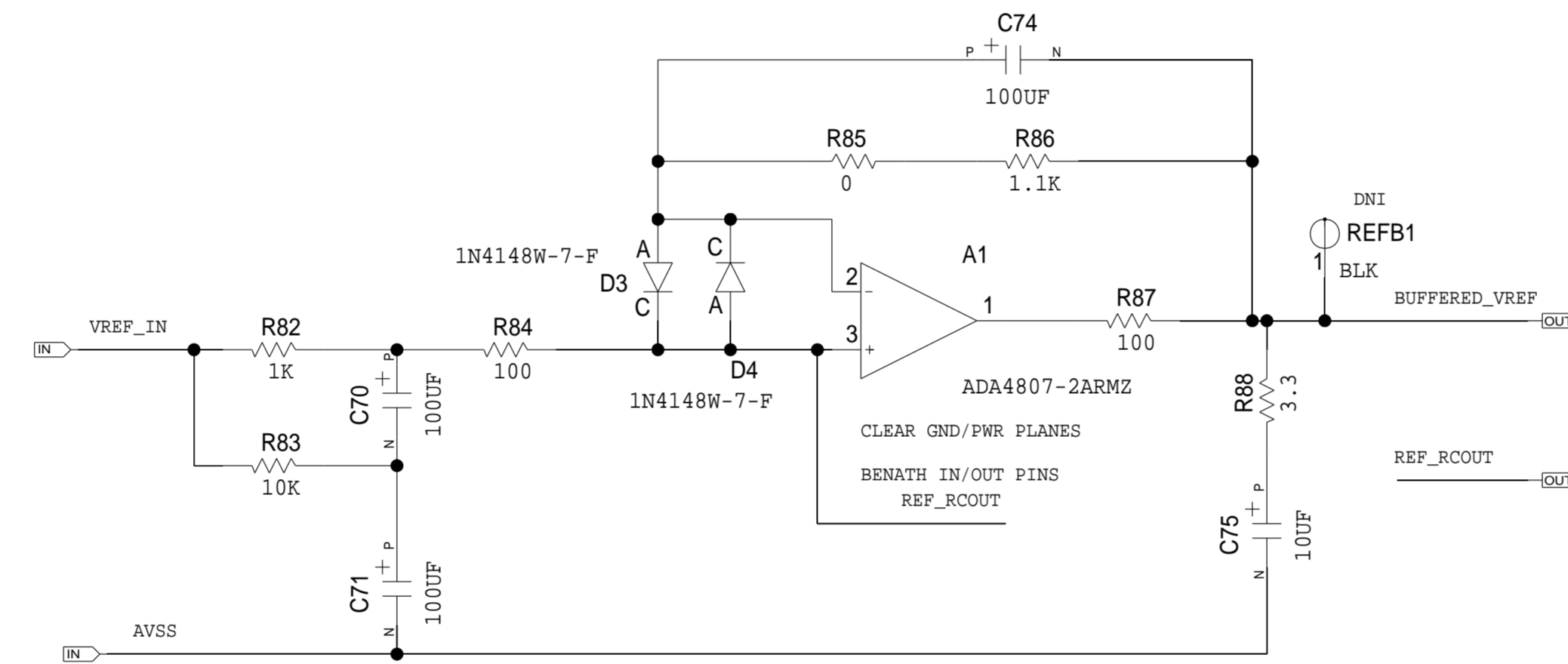
D
C
B
A

8 7 6 5 4 3 2 1

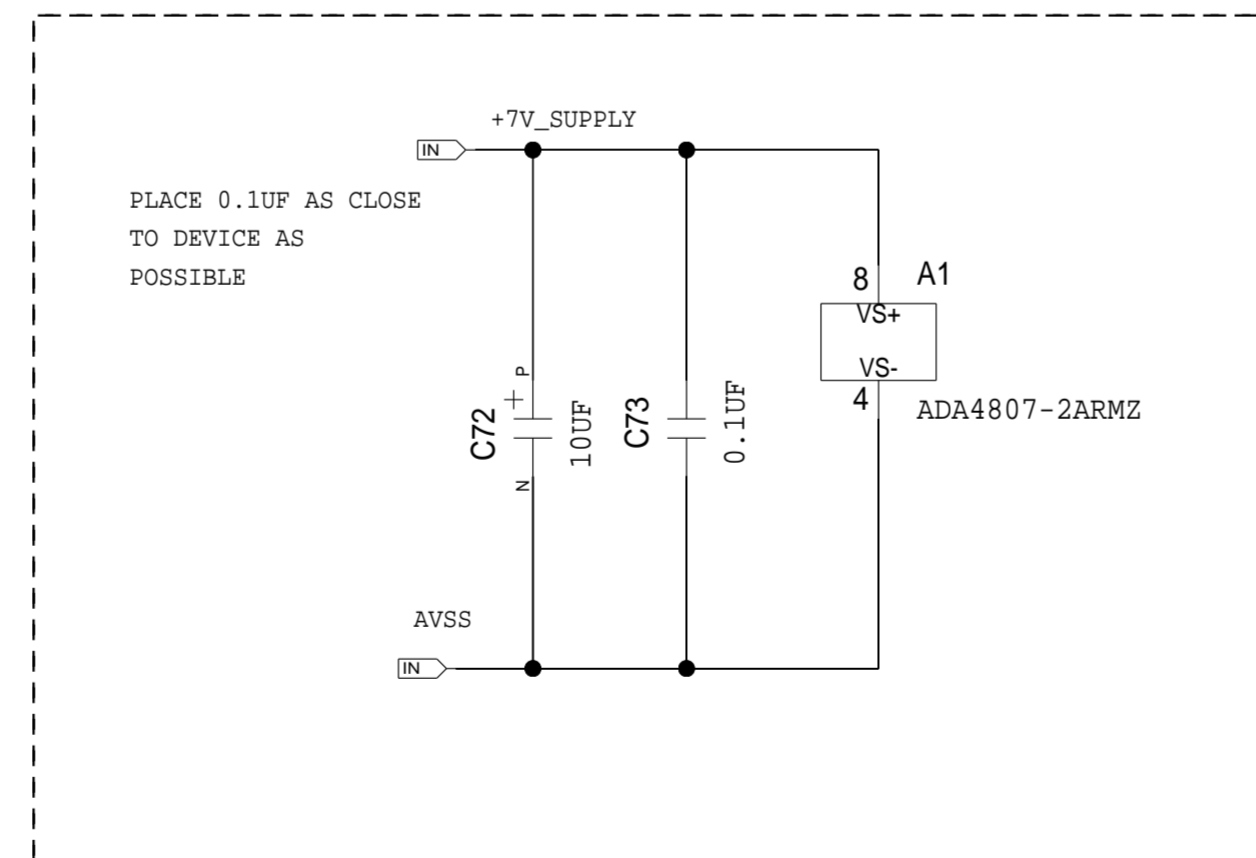
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	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1
		SHEET 5 OF 15	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ADA4807 - REF BUFFER



REF/VCM BUFF SUPPLIES

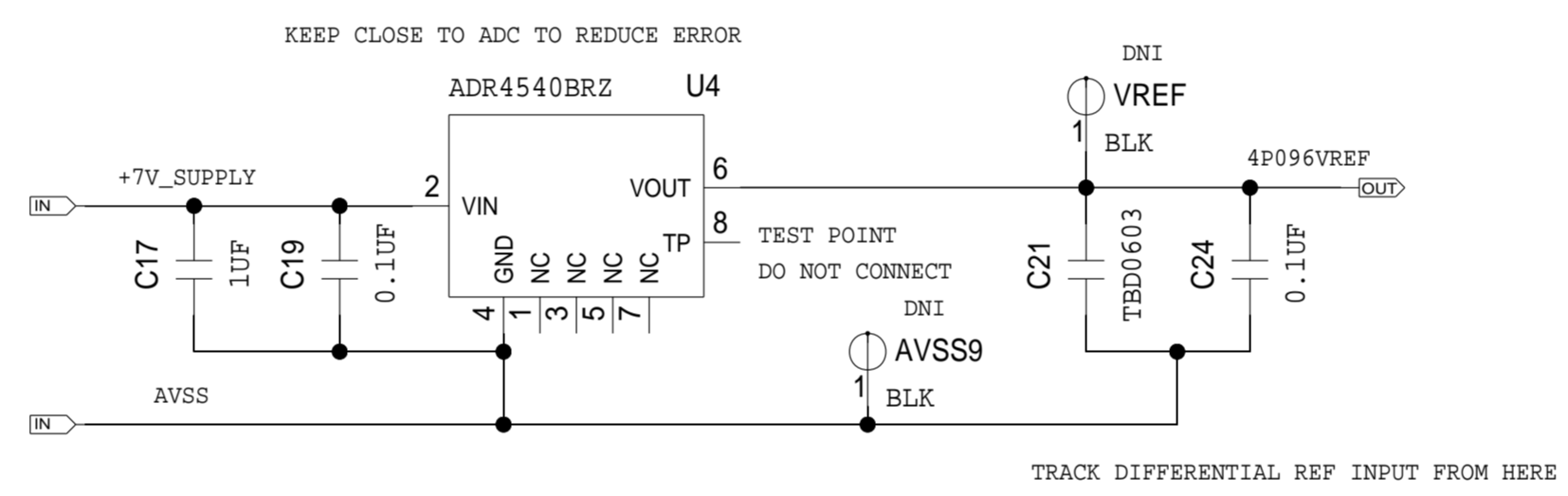


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		SHEET 6 OF 15	

8 7 6 5 4 3 2 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

4.096V REFERENCE



D
C
B
A

D
C
B
A

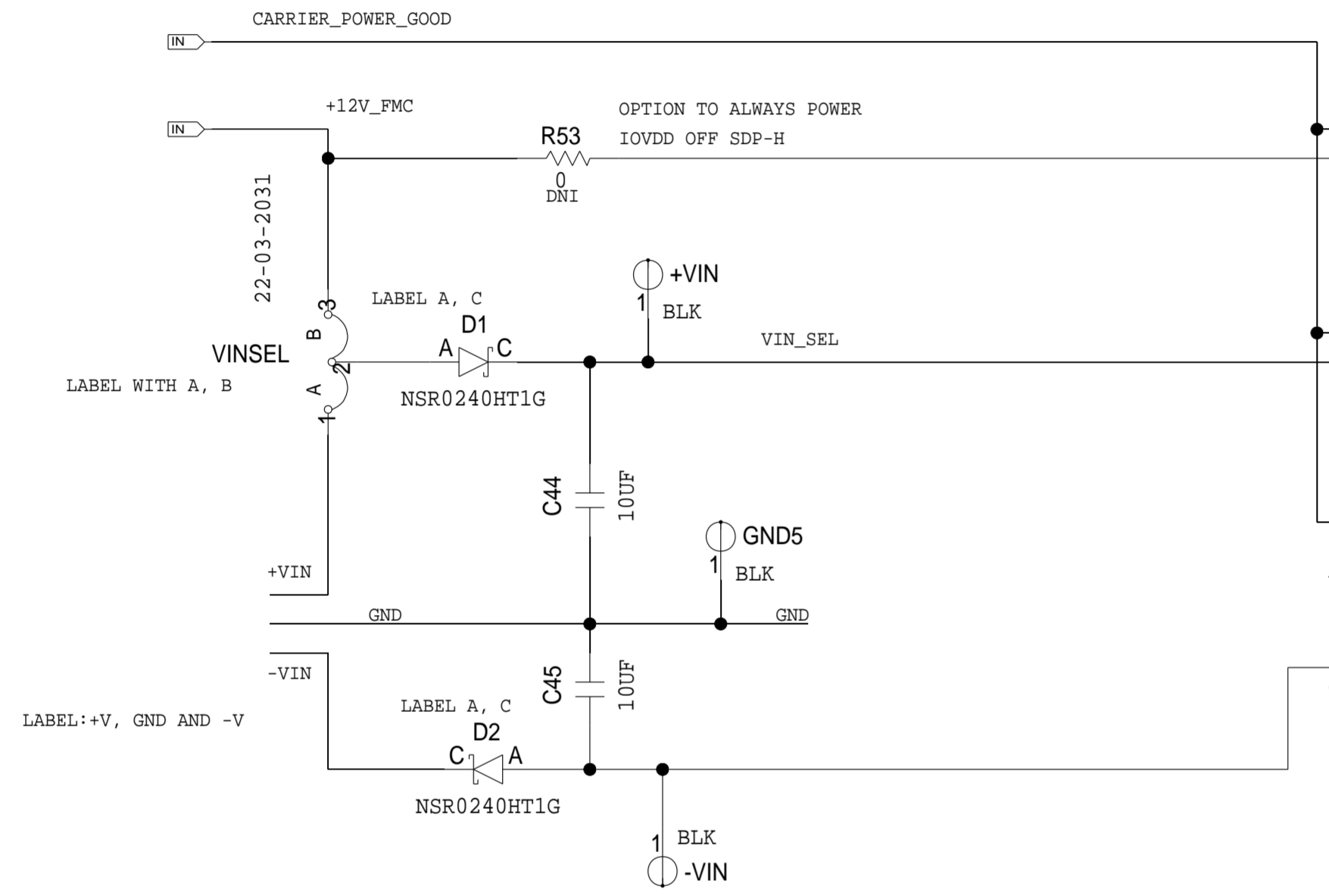
8 7 6 5 4 3 2 1

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		SHEET 7 OF 15	

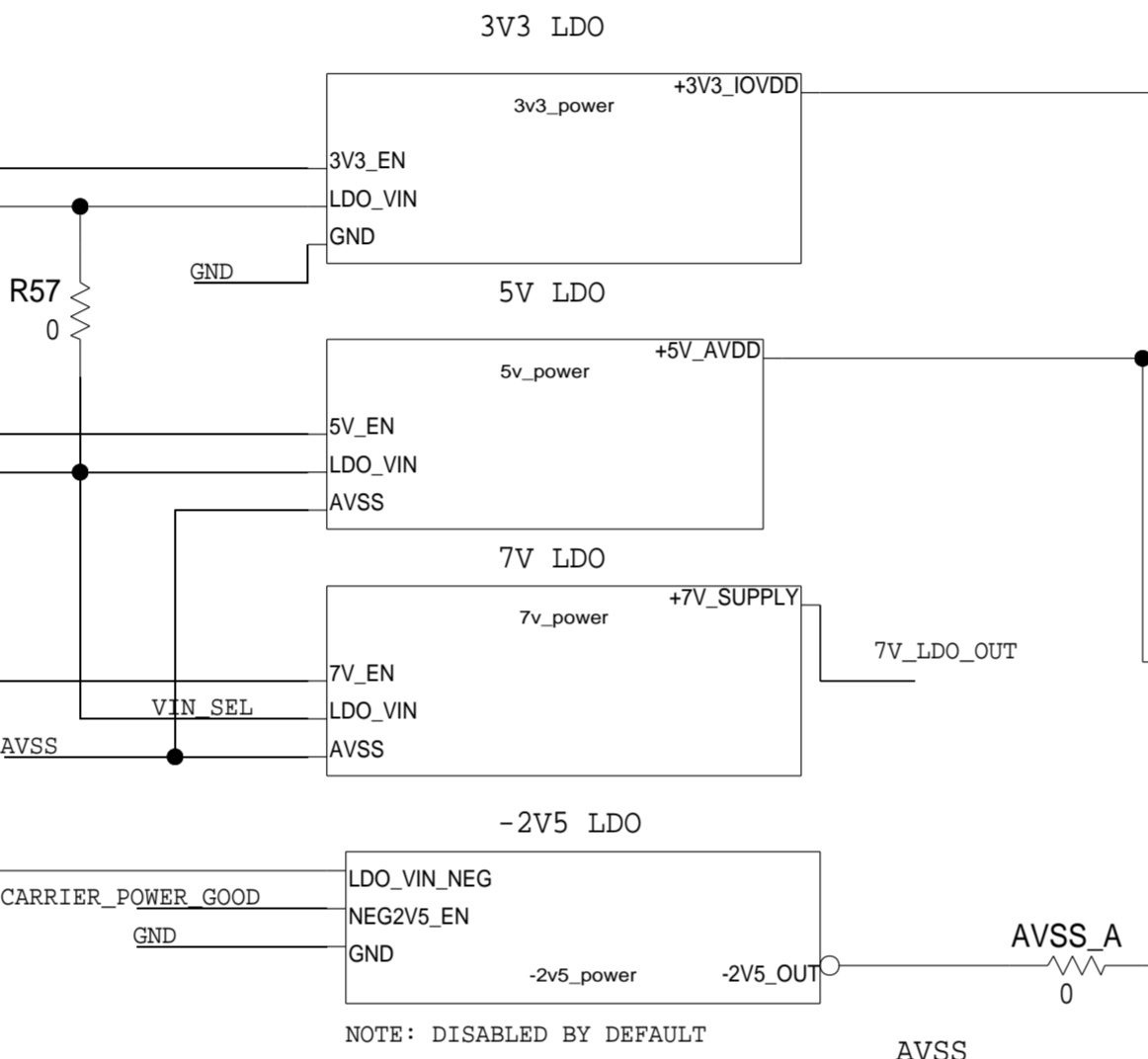
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER - ALL

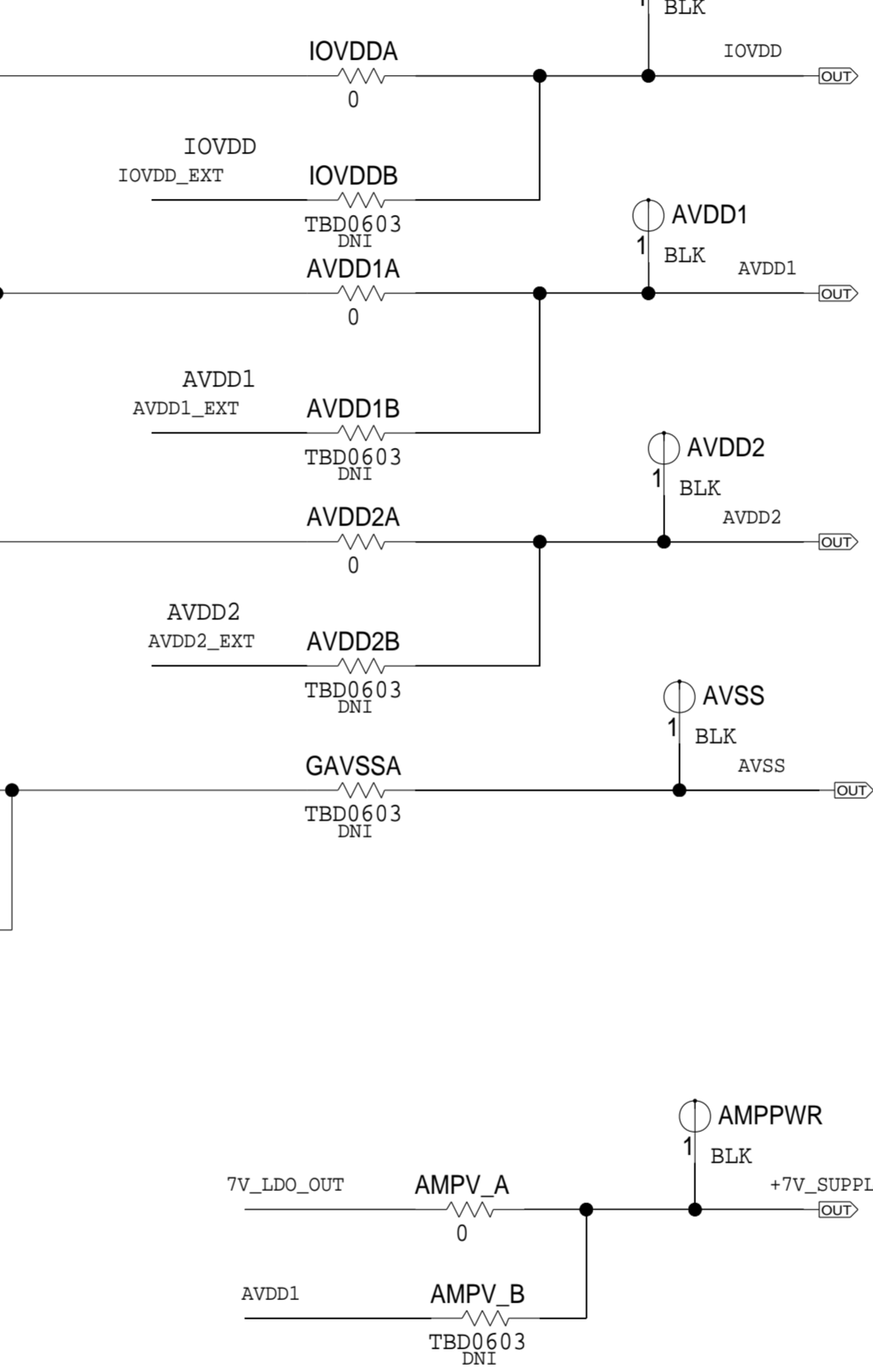
INPUT VOLTAGE OPTIONS



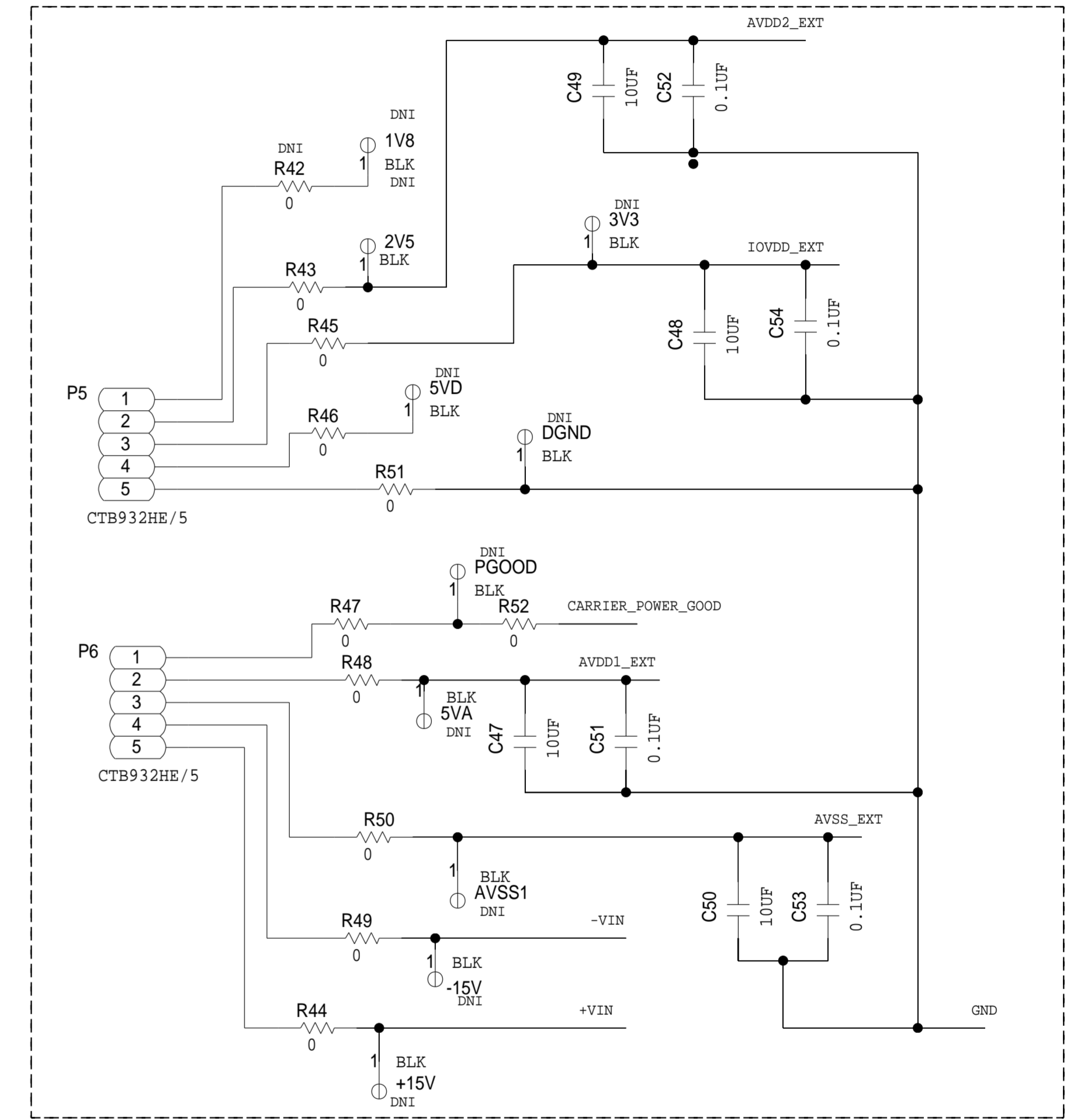
LDOs



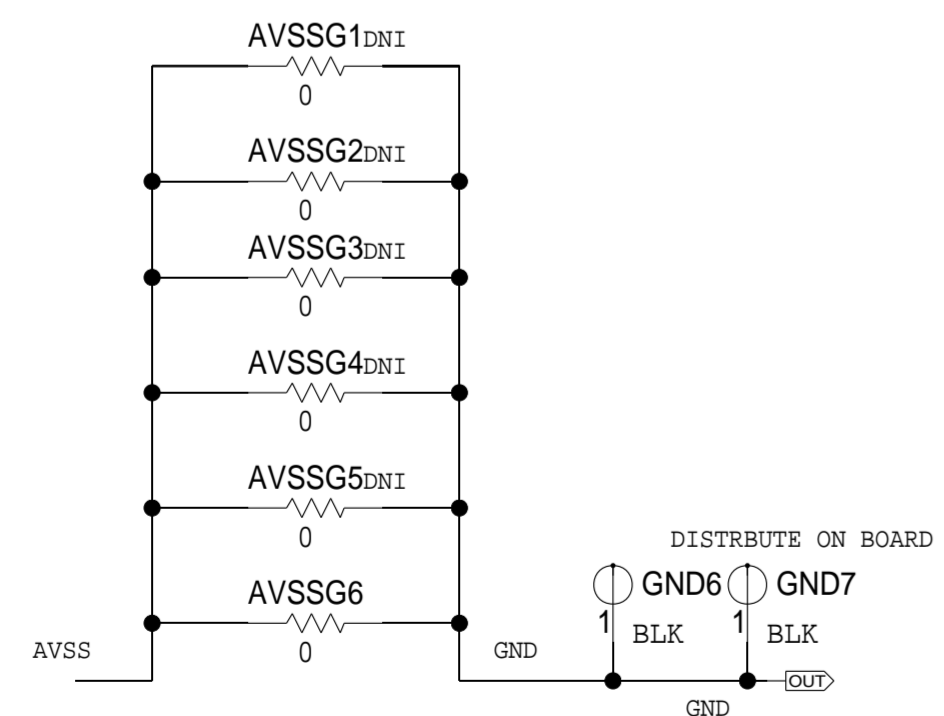
RESISTOR OPTIONS



INDIVIDUAL SUPPLY - SET EXTERNALLY



AVSS GROUNDED BY DEFAULT



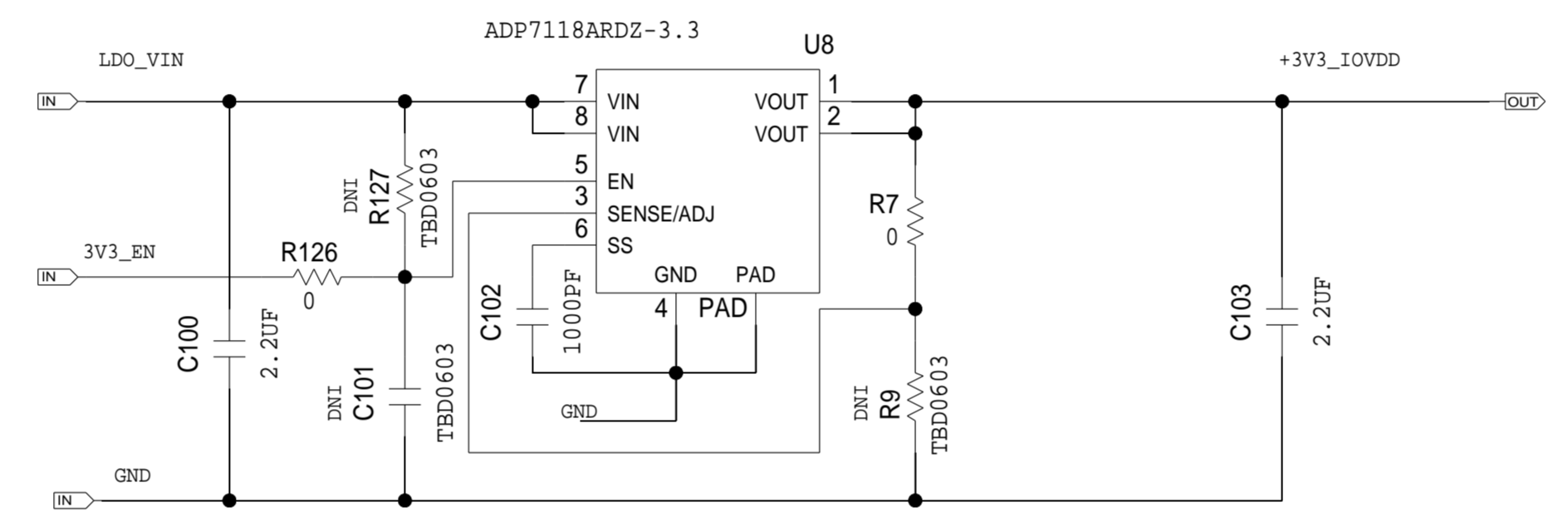
ONE STAR POINT GND HERE
STITCHES AVSS AND GND
PLANE TOGETHER

NOTE: DISTRIBUTE THROUGHOUT THE BOARD

ANALOG DEVICES		SCHEMATIC		
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PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 8 OF 15	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

3V3 SUPPLY



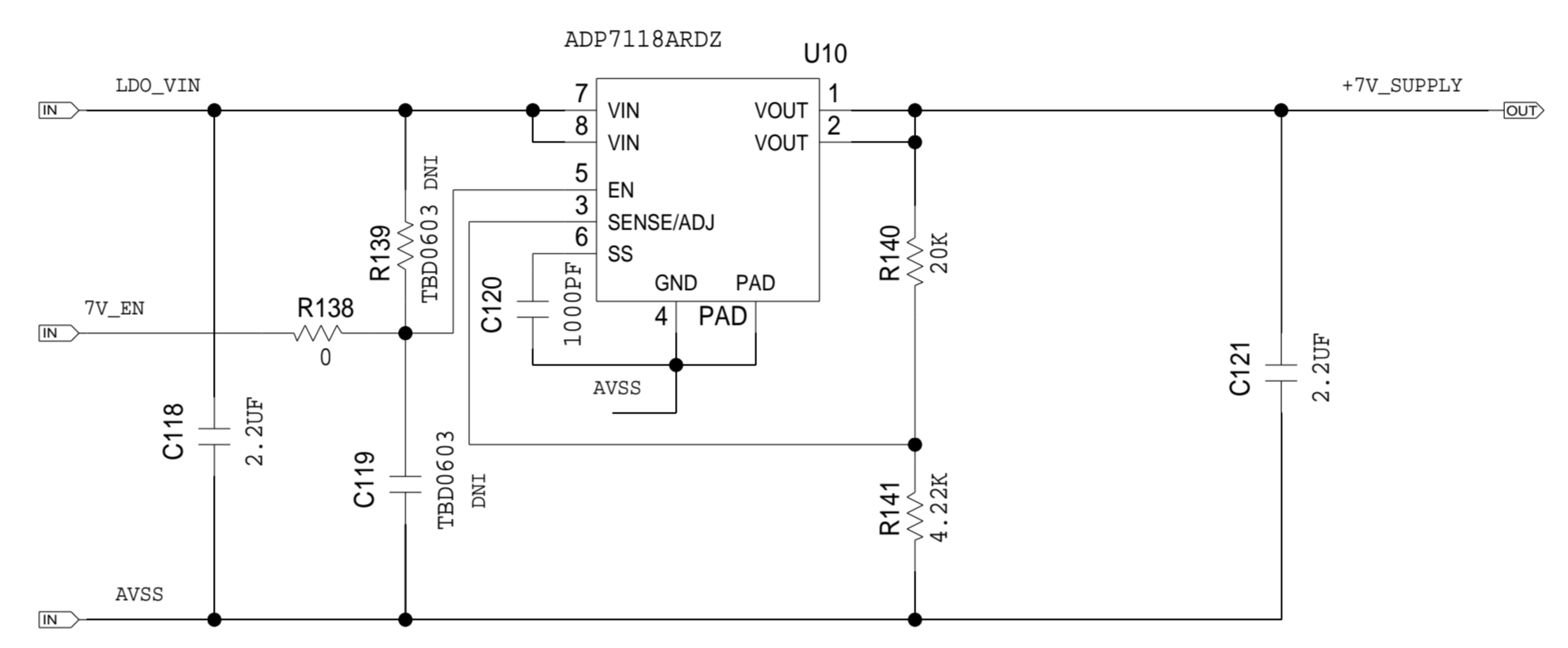
ADJUSTABLE OPTION:
 ONLY HIGHER THAN NOMINAL POSSIBLE
 EG GREATER THAN 3.3V FOR -3.3 OPTION

	SCHEMATIC		
	HW TYPE : Customer Evaluation Product(s): AD7768-1 : Modulator out version		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_044287	REV E
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1
		SHEET 9 OF 15	

8 7 6 5 4 3 2 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

7V SUPPLY



$V_{OUT} = 1.2(1 + (R1/R2))$
 $V_{OUT} = 1.2(1 + (20K/4.22K)) = 6.89V \approx 7V$
 $V_{OUT} = 1.2(1 + (20K/7.32K)) = 4.48V \approx 4.5V$

D
C
B
A

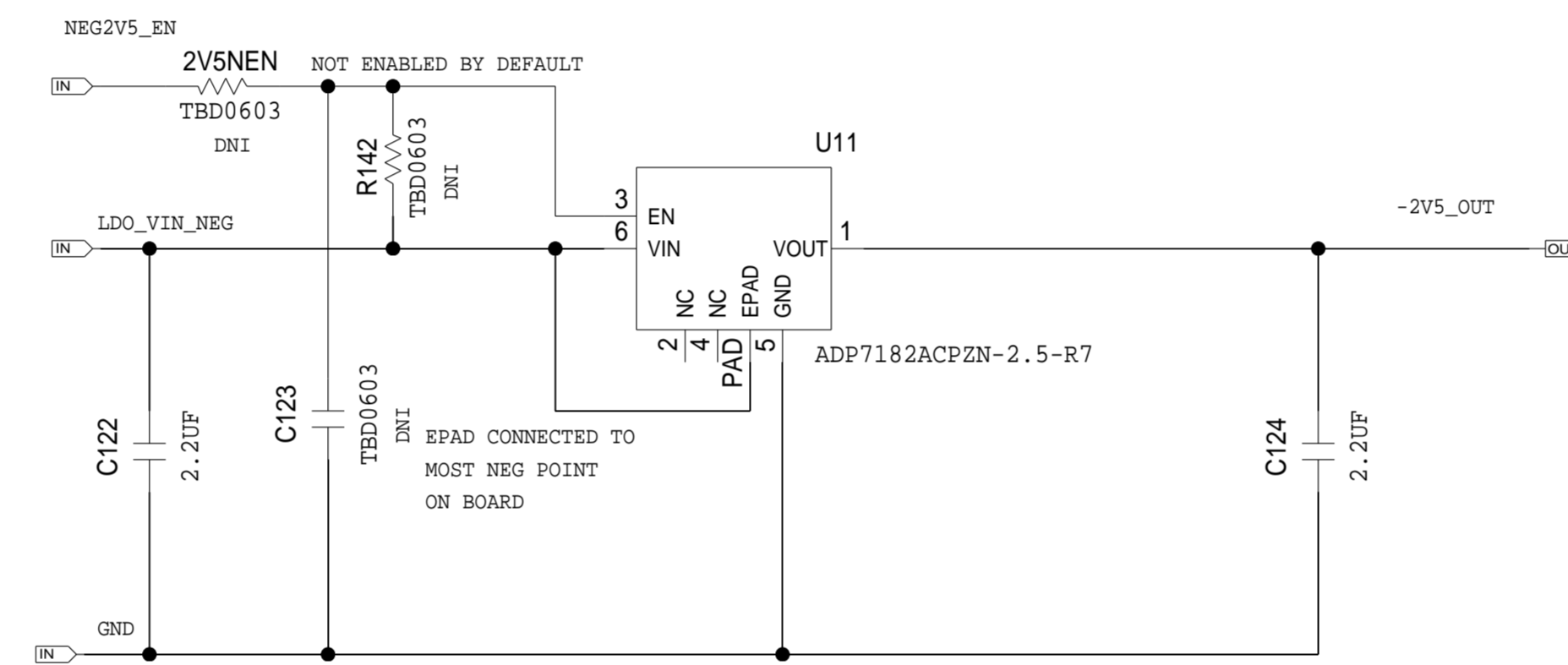
D
C
B
A

8 7 6 5 4 3 2 1

	SCHEMATIC		
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		SHEET 11 OF 15	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

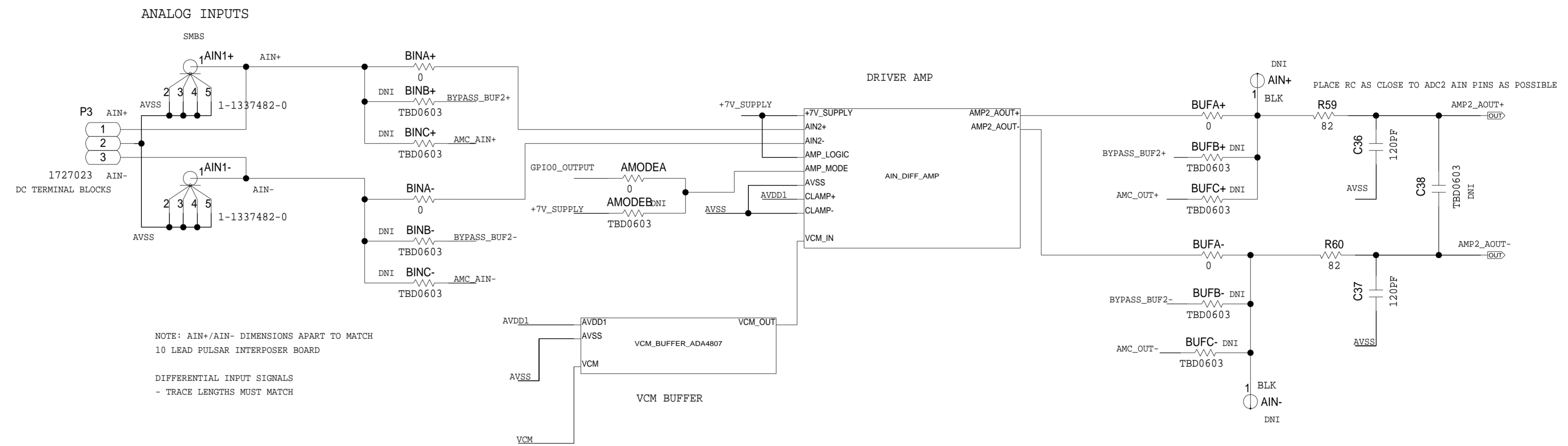
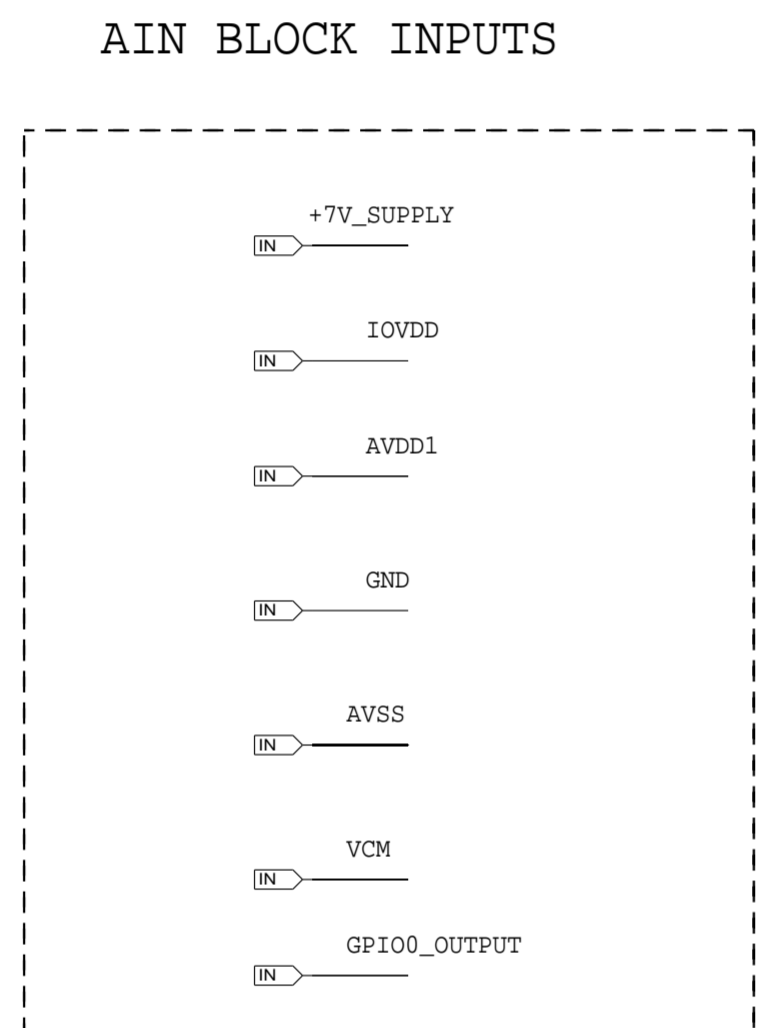
-2.5V SUPPLY



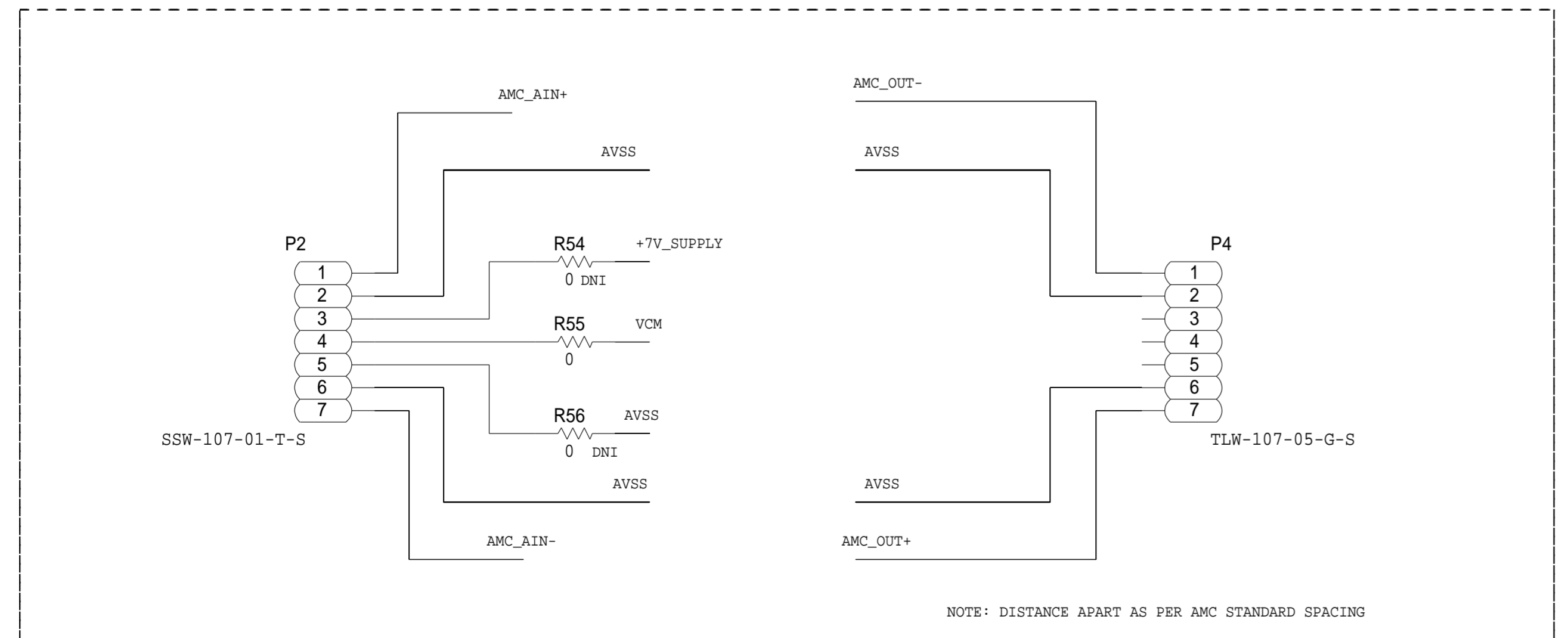
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	HW TYPE : Customer Evaluation Product(s): AD7768-1 : Modulator out version		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_044287	REV E
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1
		SHEET 12 OF 15	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

AIN ADC 2 - ADA4940



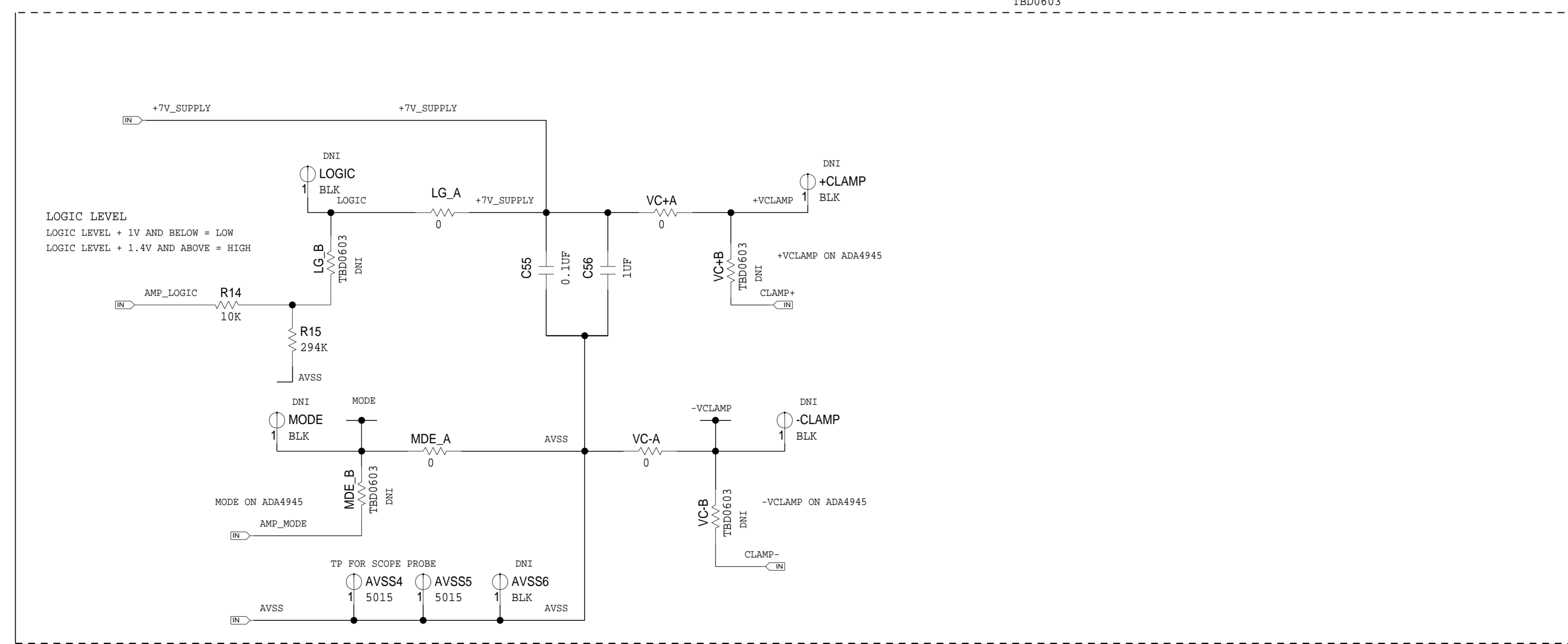
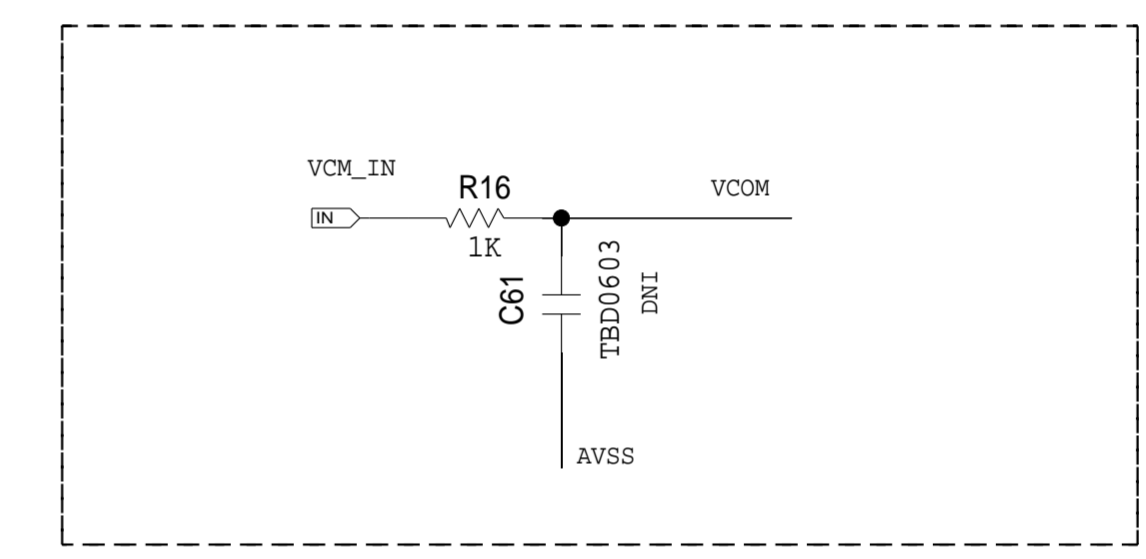
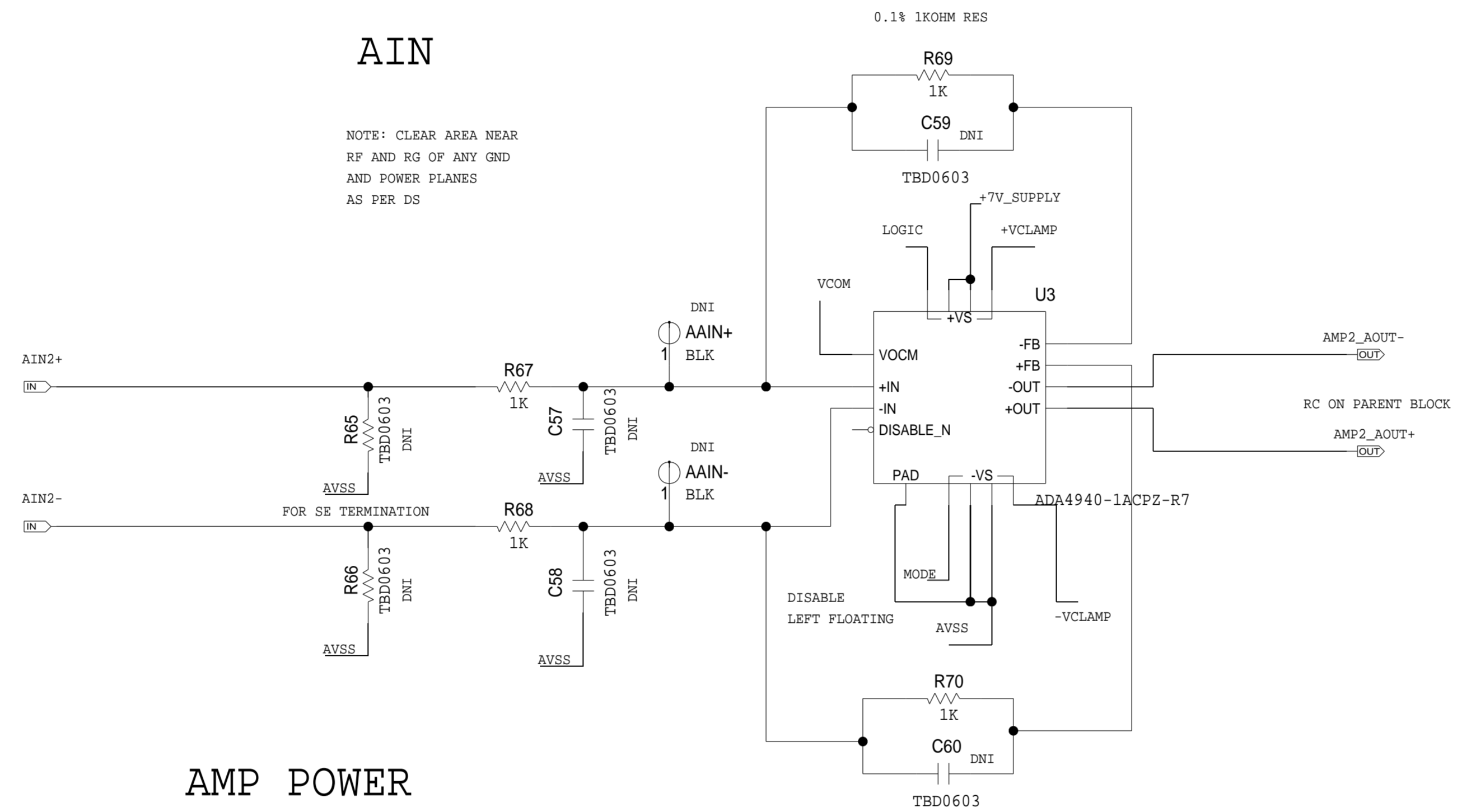
AMPLIFIER MEZZANINE CARD - OPTIONAL



	SCHEMATIC		
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PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 13 OF 15

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

ADC DRIVER AMPLIFIER

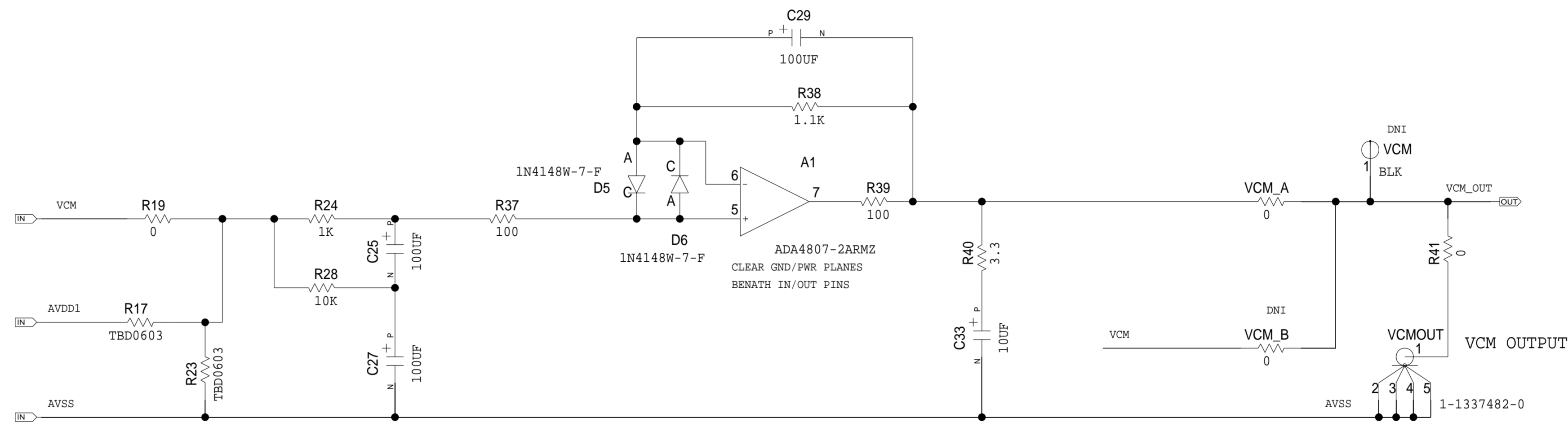


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PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 14 OF 15

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

VCM BUFFER

DEFAULT: STRAIGHT THROUGH UNBUFFERED



	SCHEMATIC		
	HW TYPE : Customer Evaluation Product(s): AD7768-1 : Modulator out version		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_044287	REV E
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		SHEET 15 OF 15	