



Product Change Notification / SYST-20PKXE959

Date:

23-Mar-2023

Product Category:

Clock and Timing - Clock and Data Distribution

PCN Type:

Document Change

Notification Subject:

Data Sheet - Low-Skew, Low Additive Jitter, 12 Output HCSL/LVDS/LVPECL Fanout Buffer with Per-Output Enable Control

Affected CPNs:

[SYST-20PKXE959_Affected_CPN_03232023.pdf](#)

[SYST-20PKXE959_Affected_CPN_03232023.csv](#)

Notification Text:

SYST-20PKXE959

Microchip has released a new Datasheet for the Low-Skew, Low Additive Jitter, 12 Output HCSL/LVDS/LVPECL Fanout Buffer with Per-Output Enable Control of devices. If you are using one of these devices please read the document located at [Low-Skew, Low Additive Jitter, 12 Output HCSL/LVDS/LVPECL Fanout Buffer with Per-Output Enable Control](#)

Notification Status: Final

Description of Change:

Updated Figures 2-1 and 2-7 and removed the "Detect Clock Low Timeout" row from Table 4-25 as requested by Tyler Bailey. Updated package marking drawing to use MSCC logo instead of MCHP logo as per Dan Holzman. Also changed all instances of master/slave to host/client and corrected TOC page numbers.

Impacts to Data Sheet: See above details.

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 23 Mar 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

Low-Skew, Low Additive Jitter, 12 Output HCSL/LVDS/LVPECL Fanout Buffer with Per-Output Enable Control

Please contact your local **Microchip sales office** with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ZL40272LDG1

ZL40272LDF1