2.5 V/3.3 V SiGe Differential Smart Gate with Output Level Select

NB7L86A

The NB7L86A is a multi−function differential Logic Gate which can be configured as an AND/NAND, OR/NOR, XOR/XNOR, or 2:1 MUX. This device is part of the GigaComm™ family of high performance Silicon Germanium products. The device is housed in a 3 x 3 mm 16 pin QFN package.

Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVCMOS/LVTTL, CML, or LVDS. The Output Level Select (OLS) input is used to program the peak−to−peak output amplitude between 0 and 800 mV in five discrete steps.

The NB7L86A employs input default circuitry so that under open input condition (Dx, $\overline{Dx}$, VTDx, $\overline{VTDx}$, VTSEL) the Outputs of the device remains stable.

Features

- Maximum Input Clock Frequency > 8 GHz Typical
- Maximum Input Data Rate > 8 Gb/s Typical
- 165 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- Selectable Swing PECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Selectable Swing NECL Output with NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
- Selectable Output Level (0 V, 200 mV, 400 mV, 600 mV, or 800 mV Peak−to−Peak Output)
- 50 Ω Internal Input Termination Resistors
- This is a Pb−Free Device

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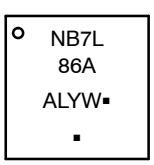
QFN16 3x3, 0.5P
CASE 485G

MARKING DIAGRAM



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

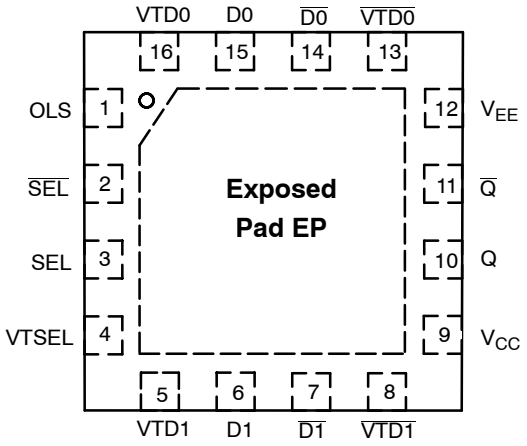


Figure 1. QFN16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	OLS (Note 3)	Input	Input for OLS (Output Level Select) Pin. Refer Table 2
2	$\overline{SEL}$	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input for Select Logic Pin, Single Ended or Inverted Differential
3	SEL	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input for Select Logic Pin, Single Ended or non−Inverted Differential
4	VTSEL (Note 1)		Pin with a common internal 50 Ω termination from SEL/$\overline{SEL}$ Pins. Refer Table 7 for usage with different Interface options
5	VTD1 (Note 1)		Pin with an internal 50 Ω termination from D1 Pin. Refer Table 7 for usage with different Interface options
6	D1	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Non−inverted Differential or Single Ended with internal 75 kΩ connected to V_{EE}
7	$\overline{D1}$	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Inverted Differential or Single Ended with internal 75 kΩ connected to V_{EE} and 36.5 kΩ connected to V_{CC}
8	$\overline{VTD1}$ (Note 1)		Pin with an internal 50 Ω termination from D1 Pin. Refer Table 7 for usage with different Interface options
9	V_{CC} (Note 2)		Positive Supply Voltage
10	Q	Output: Reduced Swing ECL	Output Pin, non−inverted Differential Output with typical 50 Ω termination to $V_{TT} = V_{CC} - 2$ V
11	Q	Output: Reduced Swing ECL	Output Pin, inverted Differential Output with typical 50 Ω termination to $V_{TT} = V_{CC} - 2$ V
12	V_{EE} (Note 2)		Negative Supply Voltage
13	$\overline{VTD0}$ (Note 1)		Pin with an internal 50 Ω termination from D0 Pin. Refer Table 7 for usage with different Interface options
14	$\overline{D0}$	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Inverted Differential or Single Ended with internal 75 kΩ connected to V_{EE} and 36.5 kΩ connected to V_{CC}
15	D0	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Non−inverted Differential or Single Ended with internal 75 kΩ connected to V_{EE}
16	VTD0 (Note 1)		Pin with an internal 50 Ω termination from D0 Pin. Refer Table 7 for usage with different Interface options
	EP		Exposed Pad (EP) is thermally connected to the die for improved heat transfer out of the package. The exposed pad can be connected electrically to V_{EE} on the PCB board

1. In the differential configuration when the input termination pins (VTD0/1, $\overline{VTD0/1}$, VTSEL) are connected to a common termination voltage, or left open, and if no signal is applied then the device will be susceptible to self−oscillation.
2. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
3. When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, 2 kΩ resistor should be connected from OLS pin to V_{EE}.

Table 2. OUTPUT LEVEL SELECT OLS

OLS	Q/$\overline{Q}$ VPP	OLS Sensitivity
V_{CC}	800 mV	OLS − 75 mV
V_{CC} − 0.4 V	200 mV	OLS ± 150 mV
V_{CC} − 0.8 V	600 mV	OLS ± 100 mV
V_{CC} − 1.2 V	0 mV	OLS ± 75 mV
V_{EE} (Note 4)	400 mV	OLS ± 100 mV
Float	600 mV	N/A

4. When an output level of 400 mV is desired and V_{CC} − V_{EE} > 3.0 V, 2 kΩ resistor should be connected from OLS to to V_{EE}.

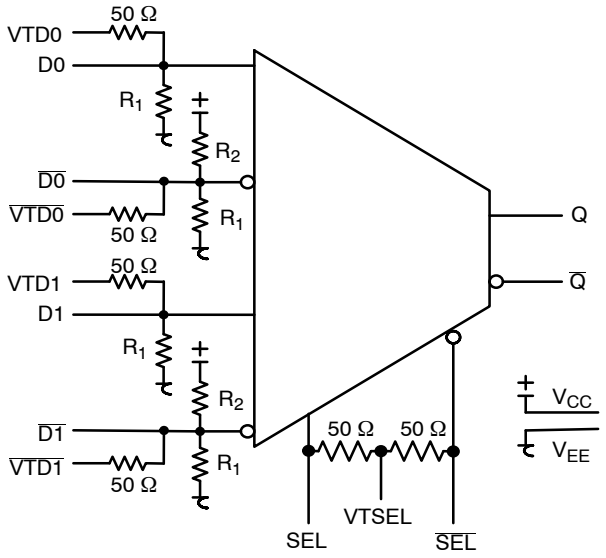


Figure 2. Logic Diagram

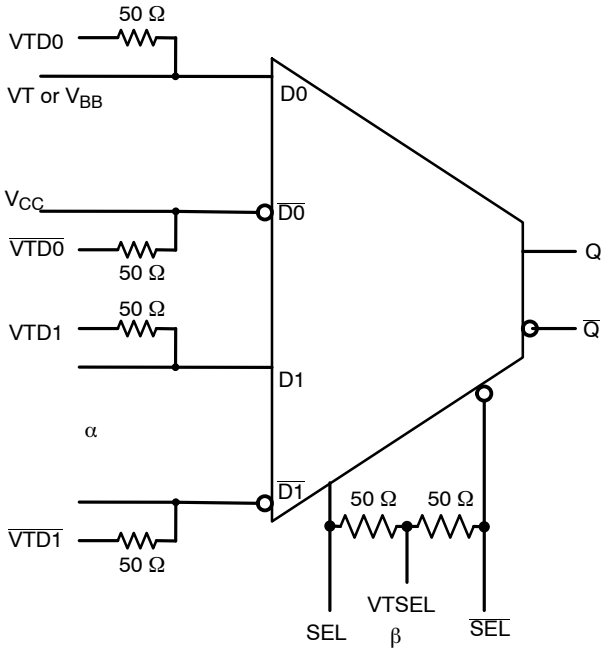


Figure 3. Configuration for AND/NAND Function

Table 3. AND/NAND TRUTH TABLE (Note 5)

	α	β	α * β
D0	**D1**	**SEL**	**Q**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

5. D0, D1, SEL are inverse of $\overline{D0}$, $\overline{D1}$, $\overline{SEL}$ unless specified otherwise.

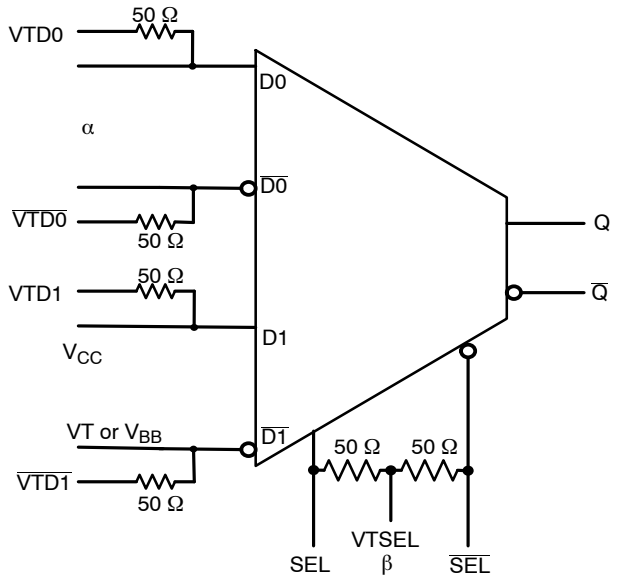


Figure 4. Configuration for OR/NOR Function

Table 4. OR/NOR TRUTH TABLE (*)

α		β	α **or** β
D0	**D1**	**SEL**	**Q**
0	1	0	0
0	1	1	1
1	1	0	1
1	1	1	1

*D0, D1, SEL are inverse of $\overline{D0}$, $\overline{D1}$, $\overline{SEL}$ unless specified otherwise.

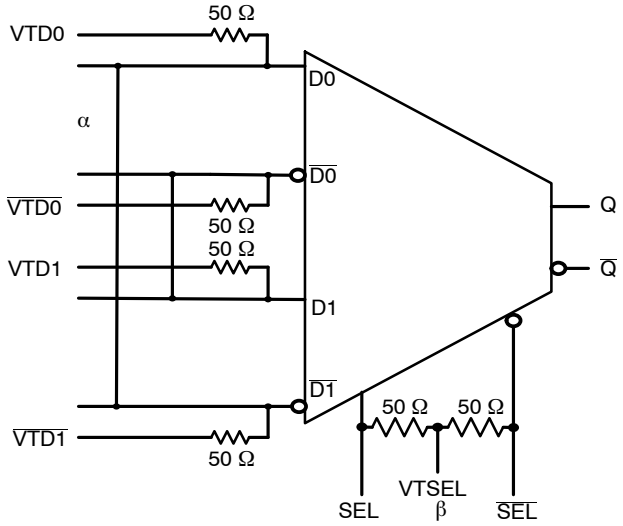


Figure 5. Configuration for XOR/XNOR Function

Table 5. XOR/XNOR TRUTH TABLE (*)

α		*β*	*α* **XOR** *β*
D0	**D1**	**SEL**	**Q**
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0

*D0, D1, SEL are inverse of $\overline{D0}$, $\overline{D1}$, $\overline{SEL}$ unless specified otherwise.

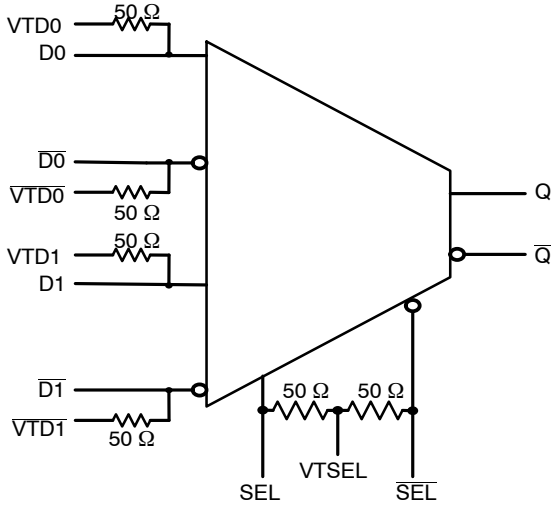


Figure 6. Configuration for 2:1 MUX Function

Table 6. 2:1 MUX TRUTH TABLE (*)

SEL	**Q**
1	D1
0	D0

*D0, D1, SEL are inverse of $\overline{D0}$, $\overline{D1}$, $\overline{SEL}$ unless specified otherwise.

Table 7. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect $\overline{VTD0}$, VTD0, VTSEL, $\overline{VTD1}$, VTD1 TO V_{CC}
LVDS	Connect $\overline{VTD0}$, VTD0, $\overline{VTD1}$, and VTD1 together. Leave VTSEL open
AC−COUPLED	Bias $\overline{VTD0}$, VTD0, VTSEL, $\overline{VTD1}$, VTD1 and VTSEL inputs within the Common Mode range (VIHCMR)
RSECL, PECL, NECL	Standard ECL termination techniques
LVTTL, LVCMOS	An external voltage should be applied to the unused complementary differential input. Nominal voltage of 1.5 V for LVTTL and $V_{CC}/2$ for LVCMOS inputs

Table 8. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistors (R_1)	75 kΩ
Internal Input Pullup Resistor (R_2)	37.5 kΩ
ESD Protection: Human Body Model Charged Device Model Machine Model	 ≥ 4 kV ≥ 2 kV ≥ 200 V
Moisture Sensitivity (Note 6), Pb−Free	Level 1
Flammability Rating, Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

6. For additional information, see Application Note AND8003/D.

Table 9. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−3.6	V
V_I	Positive Input	V_{EE} = 0 V	$V_I \le V_{CC}$	3.6	V
	Negative Input	V_{CC} = 0 V	$V_I \ge V_{EE}$	−3.6	V
V_{INPP}	Differential Input Voltage $\lvert Dn - \overline{Dn}\rvert$, $\lvert SEL - \overline{SEL}\rvert$	$V_{CC} - V_{EE} \ge 2.8$ V		2.8	V
		$V_{CC} - V_{EE} \le 2.8$ V		$\lvert V_{CC} - V_{EE}\rvert$	
I_{IN}	Input Current through RT (50 Ω Resistor)	Static		45	mA
		Surge		80	mA
I_{OUT}	Output Current	Continuous		25	mA
		Surge		50	mA
T_A	Operating Temperature Range			−40 to +85	°C
Tstg	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 7)	0 lfpm		41.6	°C/W
		500 lfpm		35.2	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P (Note 7)		4	°C/W
Tsol	Wave Solder (Pb−Free)	< 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

7. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 10. DC CHARACTERISTICS, INPUT WITH LVPECL OUTPUT: V_{CC} = 2.5 V; V_{EE} = 0 V, T_A = −40°C to +85°C (Note 8)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	23	30	39	23	30	39	23	30	39	mA
LVPECL OUTPUTS (Note 9)											
V_{OH}	Output HIGH Voltage	1460	1510	1570	1490	1540	1600	1515	1565	1625	mV
V_{OL}	Output LOW Voltage										mV
	(OLS = V_{CC})	555	705	855	595	745	895	625	775	925	
	(OLS = V_{CC} − 0.4 V)	1235	1295	1385	1270	1330	1420	1295	1355	1445	
	(OLS = V_{CC} − 0.8 V, OLS = FLOAT)	775	895	1015	810	930	1050	840	960	1080	
	(OLS = V_{CC} − 1.2 V)	1455	1505	1585	1490	1540	1620	1510	1560	1640	
	(OLS = V_{EE})	1005	1095	1215	1040	1130	1250	1065	1155	1275	
V_{OUTPP}	Output Voltage Amplitude										mV
	(OLS = V_{CC})	670	800		660	795		655	790		
	(OLS = V_{CC} − 0.4 V)	125	215		120	210		120	210		
	(OLS = V_{CC} − 0.8 V, OLS = FLOAT)	510	615		505	610		500	605		
	(OLS = V_{CC} − 1.2 V)	0	5		0	0		0	5		
	(OLS = V_{EE})	325	415		320	410		320	410		
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE ENDED (Figure 11 & 13) (Note 10)											
V_{IH}	Input HIGH Voltage (Single−Ended): D, $\overline{D}$, SEL, $\overline{SEL}$	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage (Single−Ended): D, $\overline{D}$, SEL, $\overline{SEL}$	0		V_{CC} − 150	0		V_{CC} − 150	0		V_{CC} − 150	mV
Vth	Input Threshold Reference Voltage Range (Note 11)	950		V_{CC} −75	950		V_{CC} −75	950		V_{CC} −75	mV
V_{ISE}	Single−Ended Input Voltage (V_{IH} − V_{IL})	150		2600	150		2600	150		2600	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figure 12) (Note 12)											
V_{IHD}	Differential Input HIGH Voltage (D, $\overline{D}$, SEL, $\overline{SEL}$)	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage (D, $\overline{D}$, SEL, $\overline{SEL}$)	0		V_{CC} − 75	0		V_{CC} − 75	0		V_{CC} − 75	mV
V_{ID}	Differential Input Voltage (V_{IHD}–V_{ILD}) (D, $\overline{D}$, SEL, $\overline{SEL}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13) (Figure 15)	1200		2500	1200		2500	1200		2500	mV
I_{IH}	Input HIGH Current (@ V_{IH}) D, $\overline{D}$,		30	100		30	100		30	100	μA
	SEL, $\overline{SEL}$		5	50		5	50		5	50	
I_{IL}	Input LOW Current (@ V_{IL}) D, $\overline{D}$,		20	100		20	100		20	100	μA
	SEL, $\overline{SEL}$		5	50		5	50		5	50	
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

8. Input and output parameters vary 1:1 with V_{CC}.
9. LVPECL outputs loaded with 50 Ω to (V_{CC} − 2 V) for proper operation.
10. V_{th}, V_{IH}, $V_{IL,}$, and V_{ISE} parameters must be complied with simultaneously.
11. V_{th} is applied to the complementary input when operating in single−ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.
12. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 11. DC CHARACTERISTICS, INPUT WITH LVPECL OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V, T_A = −40°C to +85°C (Note 14)

Symbol	Characteristics	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	23	30	39	23	30	39	23	30	39	mA
LVPECL OUTPUTS (Note 15)											
V_{OH}	Output HIGH Voltage	2260	2310	2370	2290	2340	2400	2315	2365	2425	mV
V_{OL}	Output LOW Voltage:										mV
	(OLS = V_{CC})	1320	1470	1620	1360	1510	1660	1390	1540	1690	
	(OLS = V_{CC} − 0.4 V)	2030	2090	2180	2065	2125	2215	2090	2150	2240	
	(OLS = V_{CC} − 0.8 V, OLS = FLOAT)	1550	1670	1790	1585	1705	1825	1615	1735	1855	
	(OLS = V_{CC} − 1.2 V)	2260	2310	2390	2290	2340	2420	2315	2365	2445	
	(OLS = V_{EE}) (Note 20)	1785	1875	1995	1820	1910	2030	1850	1940	2060	
V_{OUTPP}	Output Amplitude Voltage:										mV
	(OLS = V_{CC})	705	815		695	805		690	800		
	(OLS = V_{CC} − 0.4 V)	130	220		125	215		125	215		
	(OLS = V_{CC} − 0.8 V, OLS = FLOAT)	535	640		530	635		525	630		
	(OLS = V_{CC} − 1.2 V)	0	0		0	0		0	0		
	(OLS = V_{EE}) (Note 20)	345	435		340	430		335	425		
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE−ENDED (Figure 11 & 13) (Note 16)											
V_{IH}	Input HIGH Voltage (Single−Ended) D, $\overline{D}$, SEL, $\overline{SEL}$	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{IL}	Input LOW Voltage (Single−Ended) D, $\overline{D}$, SEL, $\overline{SEL}$	0		V_{CC}− 150	0		V_{CC}− 150	0		V_{CC}− 150	mV
V_{th}	Input Threshold Reference Voltage Range (Note 17)	950		V_{CC}–75	950		V_{CC}–75	950		V_{CC}–75	mV
V_{ISE}	Single−Ended Input Voltage (V_{IH} − V_{IL})	150		2600	150		2600	150		2600	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figure 12) (Note 18)											
V_{IHD}	Differential Input HIGH Voltage (D, $\overline{D}$, SEL, $\overline{SEL}$)	1200		V_{CC}	1200		V_{CC}	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage (D, $\overline{D}$, SEL, $\overline{SEL}$)	0		V_{CC}− 75	0		V_{CC}− 75	0		V_{CC}− 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD}) (D, $\overline{D}$, SEL, $\overline{SEL}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 19) (Figure 15)	1200		3300	1200		3300	1200		3300	mV
I_{IH}	Input HIGH Current (@V_{IH}) D, $\overline{D}$		30	100		30	100		30	100	μA
	SEL, $\overline{SEL}$		5	50		5	50		5	50	
I_{IL}	Input LOW Current (@V_{IL}) D, $\overline{D}$		20	100		20	100		20	100	μA
	SEL, $\overline{SEL}$		5	50		5	50		5	50	
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

14. Input and output parameters vary 1:1 with V_{CC}.
15. LVPECL outputs loaded with 50 Ω to (V_{CC} − 2 V) for proper operation.
16. V_{th}, V_{IH}, $V_{IL,}$, and V_{ISE} parameters must be complied with simultaneously.
17. V_{th} is applied to the complementary input when operating in single−ended mode. V_{th} = (V_{IH} − V_{IL}) / 2.
18. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
19. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
20. When an output level of 400 mV is desired and V_{CC} − V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

Table 12. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT

V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V, T_A = −40°C to +85°C (Note 21)

Symbol	Characteristics	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY CURRENT											
I_{EE}	Negative Power Supply Current	23	30	39	23	30	39	23	30	39	mA
LVPECL OUTPUTS (Note 22)											
V_{OH}	Output HIGH Voltage	−1040	−990	−930	−1010	−960	−900	−985	−935	−875	mV
V_{OL}	Output LOW Voltage:										mV
	−3.465 V ≤ V_{EE} ≤ −3.0 V										
	(V_{OLS} = V_{CC})	−1980	−1830	−1680	−1940	−1790	−1640	−1910	−1760	−1610	
	(V_{OLS} = V_{CC} − 0.4 V)	−1270	−1210	−1120	−1235	−1175	−1085	−1210	−1150	−1060	
	(V_{OLS} = V_{CC} − 0.8 V, OLS = FLOAT)	−1750	−1630	−1510	−1715	−1595	−1475	−1685	−1565	−1445	
	(V_{OLS} = V_{CC} − 1.2 V)	−1040	−990	−910	−1010	−960	−880	−985	−935	−855	
	(V_{OLS} = V_{EE}) (Note 27)	−1515	−1425	−1305	−1480	−1390	−1270	−1450	−1360	−1240	
	−3.0 V < V_{EE} ≤ −2.375 V										
	(V_{OLS} = V_{CC})	−1945	−1795	−1645	−1905	−1755	−1605	−1875	−1725	−1575	
	(V_{OLS} = V_{CC} − 0.4 V)	−1265	−1205	−1115	−1230	−1170	−1080	−1205	−1145	−1055	
	(V_{OLS} = V_{CC} − 0.8 V, OLS = FLOAT)	−1725	−1605	−1485	−1690	−1570	−1450	−1660	−1540	−1420	
	(V_{OLS} = V_{CC} − 1.2 V)	−1045	−995	−915	−1010	−960	−880	−990	−940	−860	
	(V_{OLS} = V_{EE})	−1495	−1405	−1285	−1460	−1370	−1250	−1435	−1345	−1225	
V_{OUTPP}	Output Voltage Amplitude:										mV
	−3.465 V ≤ V_{EE} ≤ −3.0 V										
	(V_{OLS} = V_{CC})	705	815		695	805		690	800		
	(V_{OLS} = V_{CC} − 0.4 V)	130	220		125	215		125	215		
	(V_{OLS} = V_{CC} − 0.8 V, OLS = FLOAT)	535	640		530	635		525	630		
	(V_{OLS} = V_{CC} − 1.2 V)	0	0		0	0		0	0		
	(V_{OLS} = V_{EE}) (Note 27)	345	435		340	430		335	425		
	−3.0 V < V_{EE} ≤ −2.375 V										
	(V_{OLS} = V_{CC})	670	800		660	795		655	790		
	(V_{OLS} = V_{CC} − 0.4 V)	125	215		120	210		120	210		
	(V_{OLS} = V_{CC} − 0.8 V, OLS = FLOAT)	510	615		505	610		500	605		
	(V_{OLS} = V_{CC} − 1.2 V)	0	5		0	0		0	5		
	(V_{OLS} = V_{EE})	325	415		320	410		320	410		
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE−ENDED (Figure 11 & 13) (Note 23)											
V_{IH}	Input HIGH Voltage (Single−Ended) D, $\overline{D}$, SEL, $\overline{SEL}$	V_{EE}+ 1200		V_{CC}	V_{EE}+ 1200		V_{CC}	V_{EE}+ 1200		V_{CC}	mV
V_{IL}	Input LOW Voltage (Single−Ended) D, $\overline{D}$, SEL, $\overline{SEL}$	V_{EE}		V_{IH}− 150	V_{EE}		V_{IH}− 150	VEE		V_{IH}− 150	mV
V_{th}	Input Threshold Reference Voltage Range (Note 24)	V_{EE} + 950		V_{CC} −75	V_{EE} + 950		V_{CC} −75	V_{EE}+ 950		V_{CC} −75	mV
V_{ISE}	Single−Ended Input Voltage (V_{IH} − V_{IL})	150		2600	150		2600	150		2600	mV

Table 12. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT

V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V, T_A = −40°C to +85°C (Note 21)

Symbol	Characteristics	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figure 12) (Note 25)											
V_{IHD}	Differential Input HIGH Voltage (D, $\overline{D}$, SEL, $\overline{SEL}$)	V_{EE}+ 1200		V_{CC}	V_{EE}+ 1200		V_{CC}	V_{EE}+ 120		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage (D, $\overline{D}$, SEL, $\overline{SEL}$)	V_{EE}		V_{CC}− 75	V_{EE}		V_{CC}− 75	V_{EE}		V_{CC}− 75	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$) (D, $\overline{D}$, SEL, $\overline{SEL}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 26) (Figure 15)	V_{EE} + 1200		0	V_{EE} + 1200		0	V_{EE} + 1200		0	μA
I_{IH}	(Input HIGH Current (@V_{IH}) D, $\overline{D}$,		30	100		30	100		30	100	μA
	SEL, $\overline{SEL}$		5	50		5	50		5	50	
I_{IL}	(Input LOW Current (@V_{IL}) D, $\overline{D}$,		20	100		20	100		20	100	μA
	SEL, $\overline{SEL}$		5	50		5	50		5	50	
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

21. Input and output parameters vary 1:1 with V_{CC}.
22. LVPECL outputs loaded with 50 Ω to (V_{CC} − 2 V) for proper operation.
23. V_{th}, V_{IH}, $V_{IL,}$ and V_{ISE} parameters must be complied with simultaneously.
24. V_{th} is applied to the complementary input when operating in single−ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.
25. V_{IHD}, $V_{ILD,}$ V_{ID} and V_{CMR} parameters must be complied with simultaneously.
26. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
27. When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

Table 13. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

Symbol	Characteristic		−40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Input Clock Frequency (See Figure 7) (Note 28)		7	8		7	8		7	8		GHz
V_{OUTPP}	Output Voltage Amplitude (OLS = V_{CC})	f_{in} < 7 GHz	590	730		470	720		540	700		mV
		f_{in} = 8 GHz	270	440		230	420		180	390		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential (Figure 15) D/SEL → Q		110	160	210	115	165	215	120	170	220	ps
t_{SKEW}	Duty Cycle Skew (Note 29)			5	15		5	15		5	15	ps
t_{SKEW}	Channel Skew	Q → D/SEL		5	20		5	20		5	20	ps
t_S	Set−Up Time (Dx to SEL)		30			30			30			ps
t_H	Hold−Up Time (Dx to SEL)		35			35			35			ps
t_{JITTER}	RMS Random Clock Jitter (See Figure 7) (Note 31) fin ≤ 7 GHz			0.5	1.5		0.5	1.5		0.5	1.5	ps
	Peak−to−Peak Data Dependent Jitter (Note 32) fin ≤ 7 Gb/s			12			12			12		
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 30)		75		1890	75		1890	75		1890	mV
t_r, t_f	Output Rise/ Fall Times	t_r	30	45	65	30	45	65	30	45	65	ps
	(20% − 80%) (Q, $\overline{Q}$) @ 1 GHz	t_f	17	35	65	17	35	65	17	35	65	

28. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V. Input edge rates 40 ps (20% − 80%).
29. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 15.
30. V_{INPP} (max) cannot exceed $V_{CC} - V_{EE}$.
31. Additive RMS jitter with 50% duty cycle clock signal at 7 GHz.
32. Additive Peak−to−Peak data dependent jitter with NRZ PRBS $2^{31}-1$ data rate at 7 Gb/s.

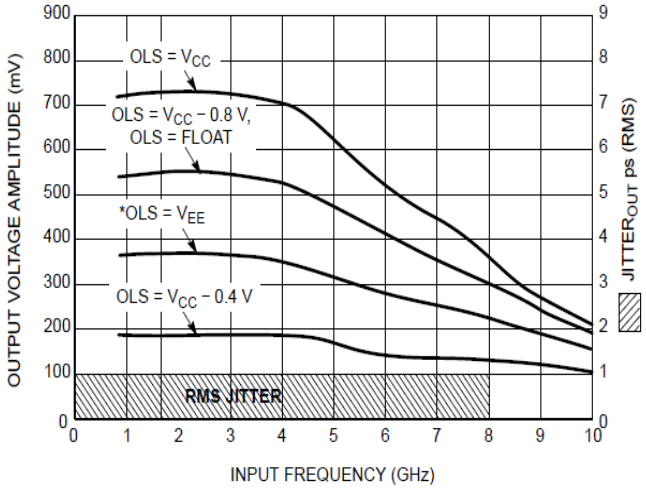
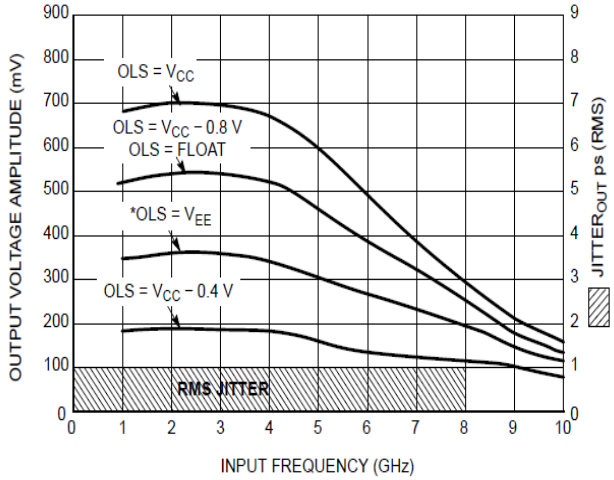


Figure 7. (V_{CC} − V_{EE} = 2.5 V @ 25°C)

NOTE: Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for 2:1 MUX Mode, Repetitive 1010 Input Data Pattern.
*When an output level of 400 mV is desired and V_{CC} − V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.



NOTE: Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for 2:1 MUX Mode, Repetitive 1010 Input Data Pattern.
*When an output level of 400 mV is desired and V_{CC} − V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

Figure 8. (V_{CC} − V_{EE} = 3.3 V @ 25°C)

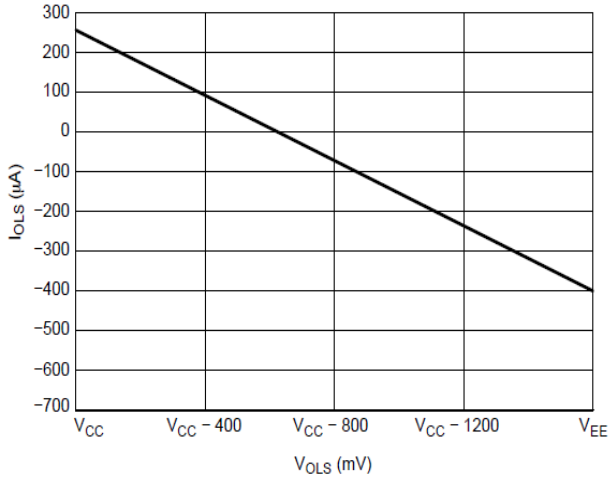


Figure 9. Typical OLS Input Current vs. OLS Input Voltage (V_{CC} − V_{EE} = 3.3 V @ 25°C)

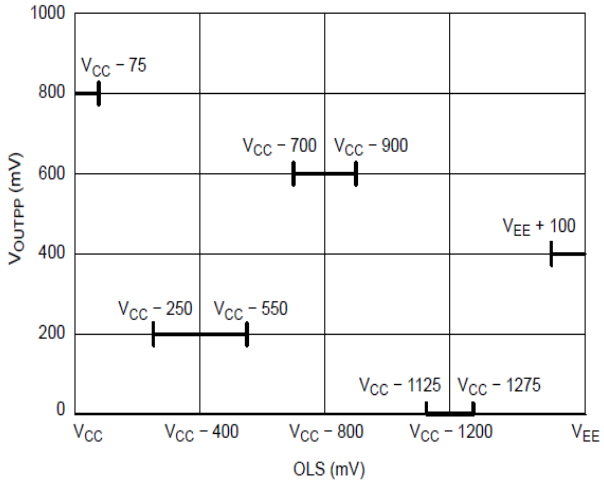


Figure 10. OLS Operating Area

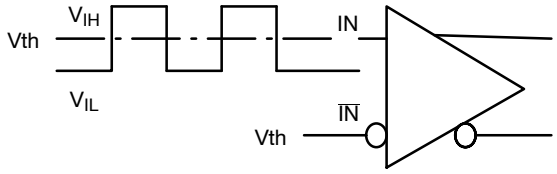


Figure 11. Differential Input Driven Single Ended

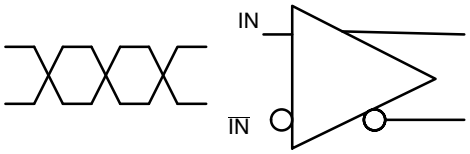


Figure 12. Differential Input Driven Differentially

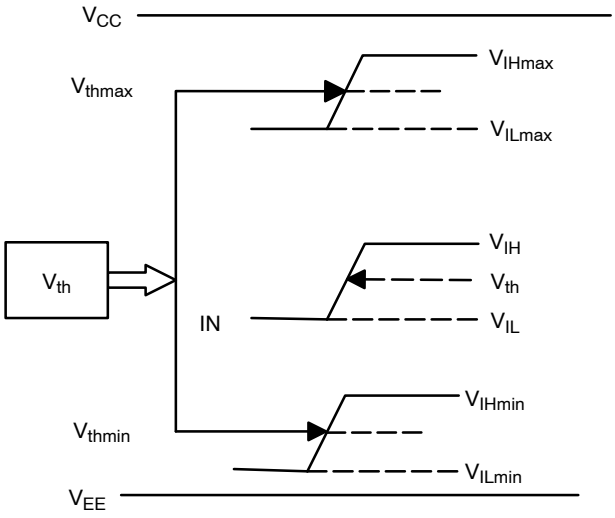


Figure 13. V_{TH} Diagram

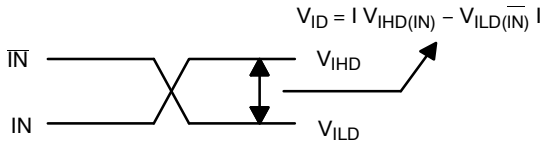


Figure 14. Differential Inputs Driven Differentially

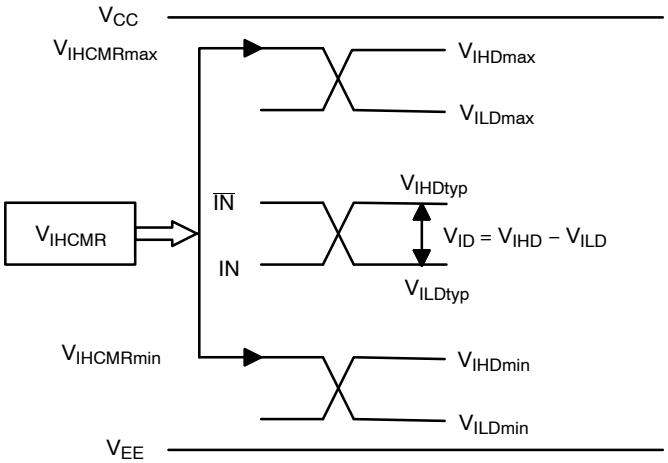


Figure 15. V_{IHCMR} Diagram

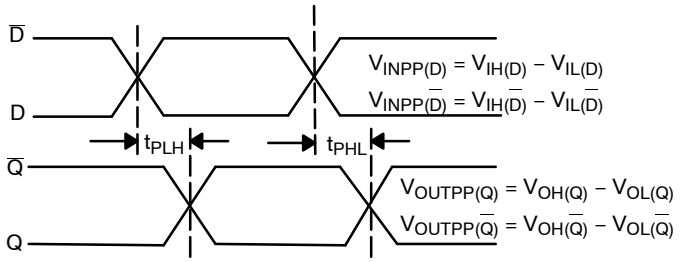


Figure 16. AC Reference Measurement

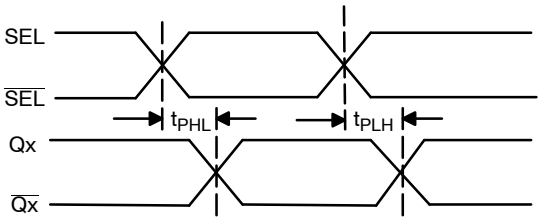


Figure 17. SEL_X to Q_X Timing Diagram

APPLICATION INFORMATION

All NB7L86A inputs can accept PECL, CML, LVTTL, LVCMOS and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are minimum input swing of 75 mV and the maximum input swing of 2500 mV. Within these conditions, the input voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a 50 Ω environment (Z = 50 Ω). For output termination and interface, refer to application note AND8020/D.

Table 14. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and VTD to V_{CC} (refer Figure 18)
LVDS	Connect VTD and VTD together. (refer Figure 19)
AC−COUPLED	Bias VTD and VTD inputs within the Common Mode range (V_{CMR}) (refer Figure 20)
RSECL, PECL, NECL	Standard ECL termination techniques (refer Figure 21)
LVTTL, LVCMOS	An external voltage (V_{THR}) should be applied to the unused complementary differential input. Nominal V_{THR} is 1.5 V for LVTTL and V_{CC}/2 for LVCMOS inputs. This voltage must be within the V_{THR} specification (refer Figure 22)

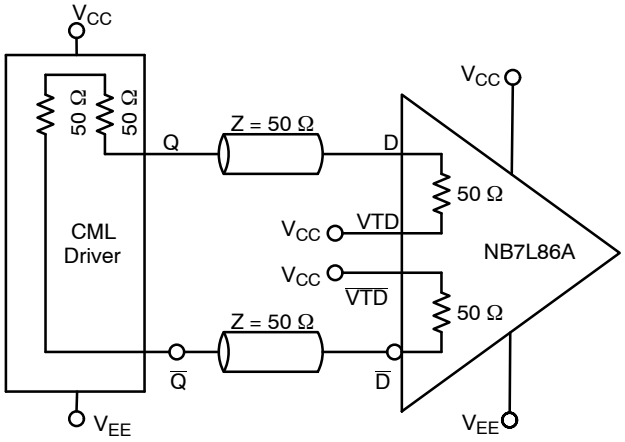


Figure 18. CML Interface

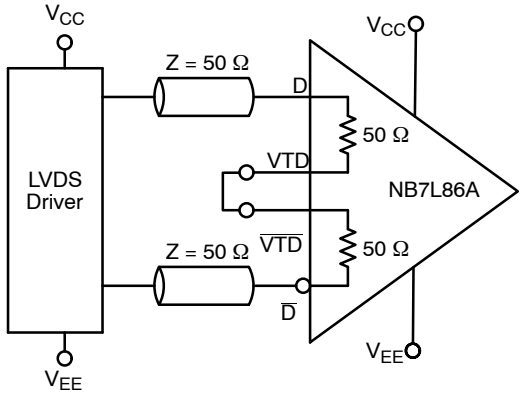
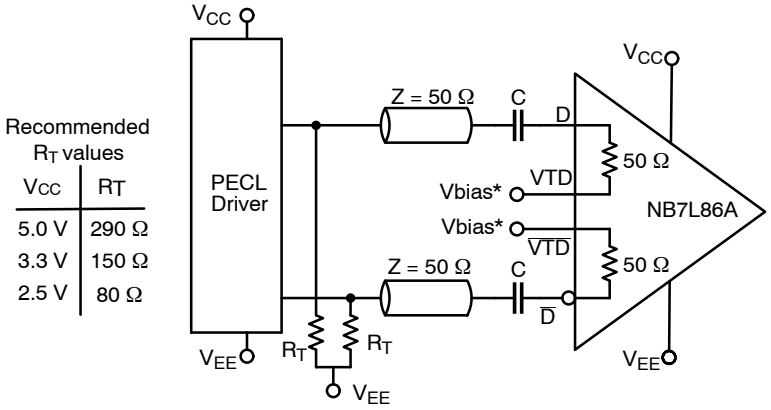


Figure 19. LVDS Interface



*Vbias must be within common mode range limits (V_{CMR})

Figure 20. PECL Interface

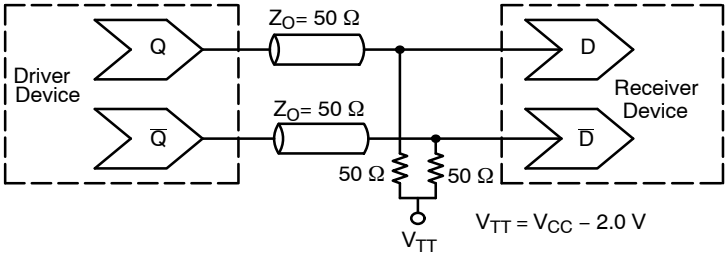


Figure 21. Typical termination for Output Driver and Device Evaluation (refer AND8020/D – termination of ECL Logic Devices)

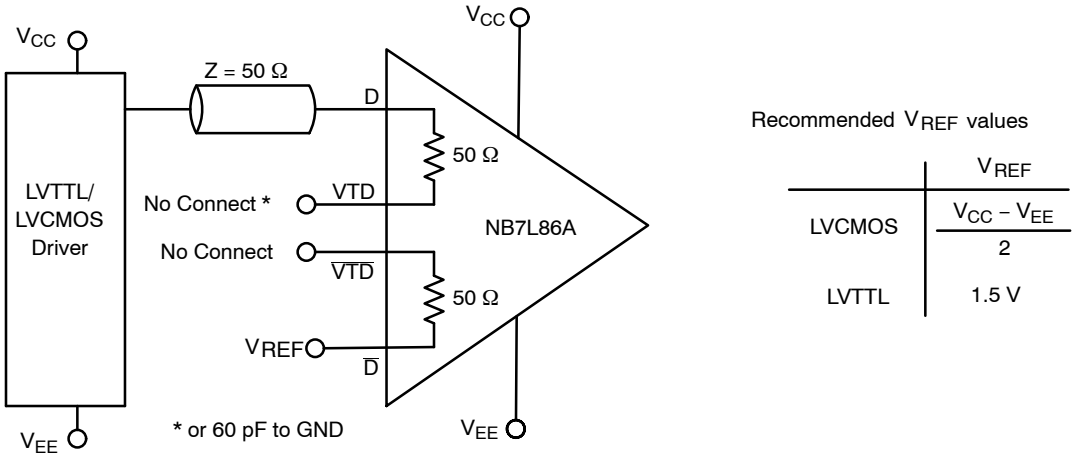


Figure 22. LVCMOS/LVTTL Interface

ORDERING INFORMATION

Device	Package Type	Shipping†
NB7L86AMNG	QFN16 (Pb−Free / Halide−Free)	123 Units / Rail
NB7L86AMNHTBG	QFN16 (Pb−Free / Halide−Free)	100 / Tape & Reel

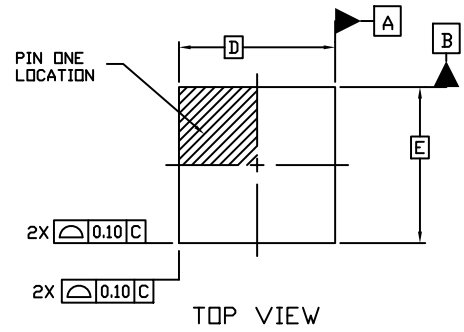
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

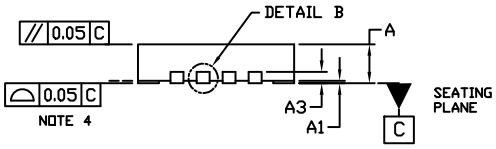
QFN16 3x3, 0.5P
CASE 485G
ISSUE G

DATE 08 OCT 2021

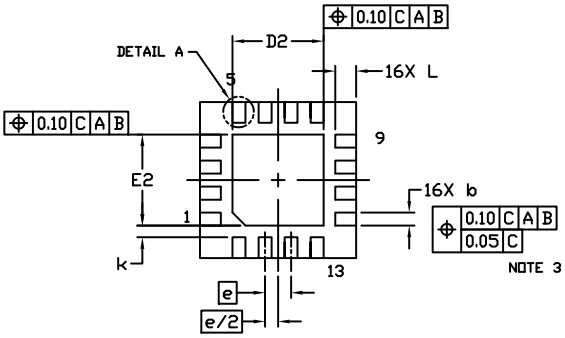
SCALE 2:1



TOP VIEW

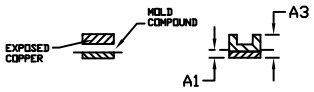


SIDE VIEW

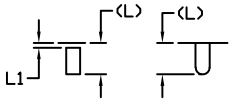


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



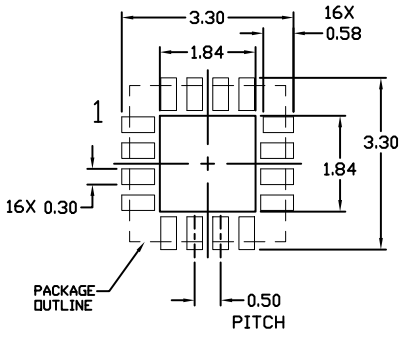
DETAIL B
ALTERNATE CONSTRUCTIONS



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.18	0.24	0.30
D		3.00 BSC	
D2	1.65	1.75	1.85
E		3.00 BSC	
E2	1.65	1.75	1.85
e		0.50 BSC	
k		0.18 TYP	
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**QFN16 3X3, 0.5P**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
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For additional information, please contact your local Sales Representative

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