

N-channel 620 V, 1.28 Ω typ., 5.0 A Power MOSFET in I²PAKFP and TO-220 packages

Datasheet – preliminary data

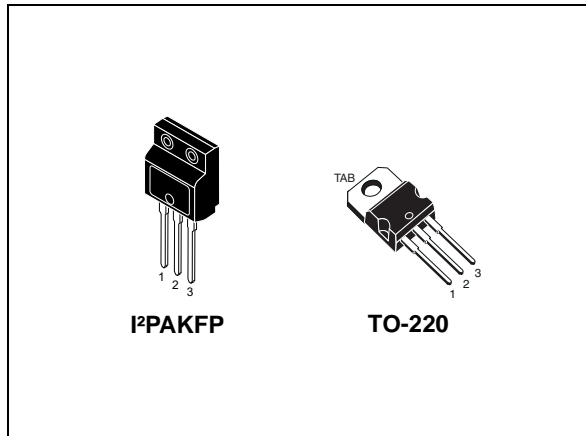
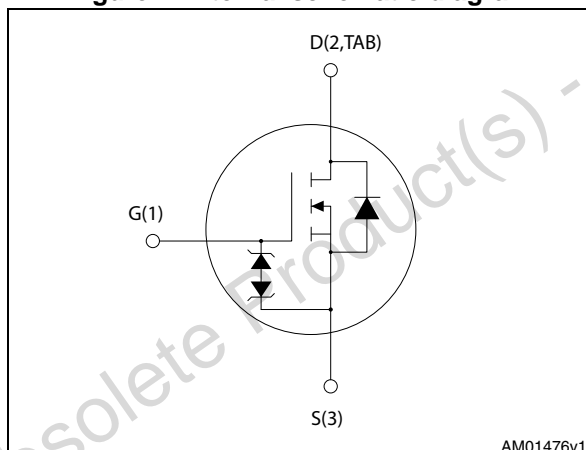


Figure 1. Internal schematic diagram



Features

Order codes	V _{DS}	R _{DS(on) max}	I _D	P _{TOT}
STFILED625	620 V	1.6 Ω	5.0 A	25 W
STPLED625				70 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- LED lighting applications

Description

These Power MOSFETs boast extremely low on-resistance and very good dv/dt capability, rendering them suitable for buck-boost and flyback topologies.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STFILED625	LED625	I ² PAKFP (TO-281)	Tube
STPLED625		TO-220	

Contents

- 1 Electrical ratings 3**
- 2 Electrical characteristics 4**
 - 2.1 Electrical characteristics (curves) 6
- 3 Test circuits 9**
- 4 Package mechanical data 10**
- 5 Revision history 14**

Obsolete Product(s) - Obsolete Product(s)



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		I ² PAKFP	TO-220	
V _{DS}	Drain- source voltage	620		V
V _{GS}	Gate- source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25 °C	5.0 ⁽¹⁾	5.0	A
I _D	Drain current (continuous) at T _C = 100 °C	3.5 ⁽¹⁾	3.5	A
I _{DM} ⁽²⁾	Drain current (pulsed)	20.0 ⁽¹⁾	20.0	A
P _{TOT}	Total dissipation at T _C = 25 °C	70	25	W
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J max)	4.2		A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	120		mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	12		V/ns
di/dt ⁽³⁾	Diode reverse recovery current slope	400		A/μs
V _{ISO}	Insulation withstand voltage (AC)	2500		V
T _J T _{stg}	Operating junction temperature Storage temperature	- 55 to 150		°C

- Limited only by maximum temperature allowed
- Pulse width limited by safe operating area
- I_{SD} ≤ I_D, peak V_{DS} ≤ V_{(BR)DSS}, V_{DD} = 80% V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		I ² PAKFP	TO-220	
R _{thj-case}	Thermal resistance junction-case max	5	1.79	°C/W
R _{thj-amb}	Thermal resistance junction-amb max	62.50		°C/W

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	620			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 620 V V _{DS} = 620 V, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V; V _{DS} = 0			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	3.6	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 2.1 A		1.28	1.6	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0	-	690	-	pF
C _{oss}	Output capacitance			52		
C _{rss}	Reverse transfer capacitance			8.5		
C _{OSS eq} ⁽¹⁾	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0 to 496 V		16.6		pF
R _g	Gate input resistance	f = 1 MHz open drain	-	4	-	Ω
Q _g	Total gate charge	V _{DD} = 496 V, I _D = 4.2 A,	-	27	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V		4		
Q _{gd}	Gate-drain charge	(see Figure 18)		16		

1. C_{OSS eq} is defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 310 V, I _D = 4.2 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 17)	-	12	-	ns
t _r	Rise time			8		
t _{d(off)}	Turn-off-delay time			40		
t _f	Fall time			21		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		4.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16.8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.2 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.2 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	290		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	1900		nC
I_{RRM}	Reverse recovery current	(see Figure 19)		13		A
t_{rr}	Reverse recovery time	$I_{SD} = 4.2 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	320		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ $T_J = 150 \text{ }^\circ\text{C}$	-	2200		nC
I_{RRM}	Reverse recovery current	(see Figure 19)		14		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for I²PAKFP

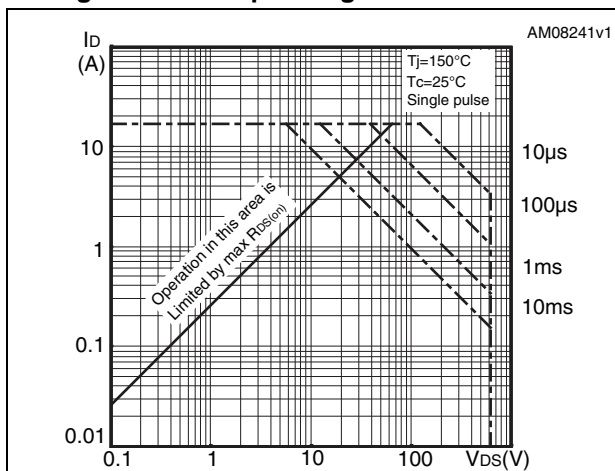


Figure 3. Thermal impedance for I²PAKFP

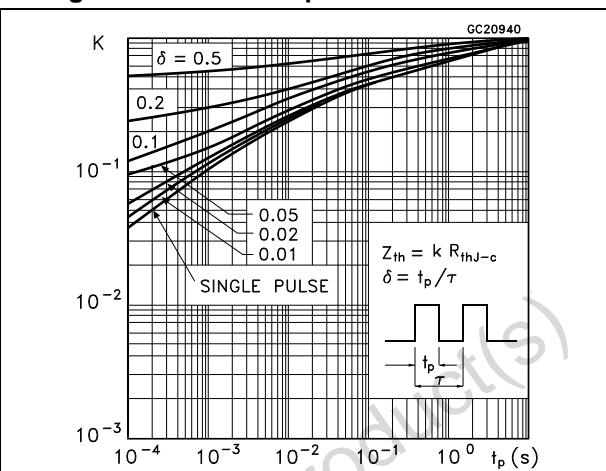


Figure 4. Safe operating area for TO-220

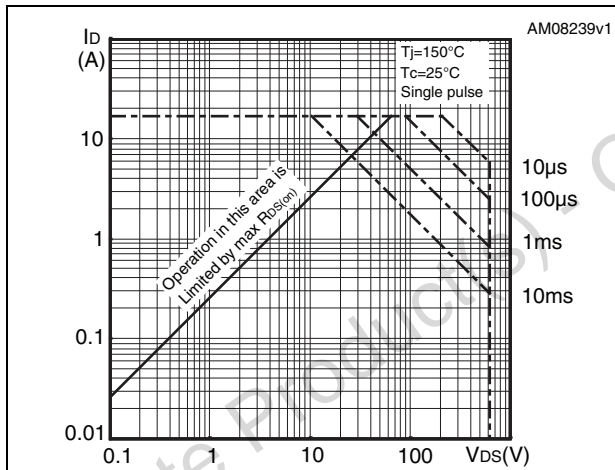


Figure 5. Thermal impedance TO-220

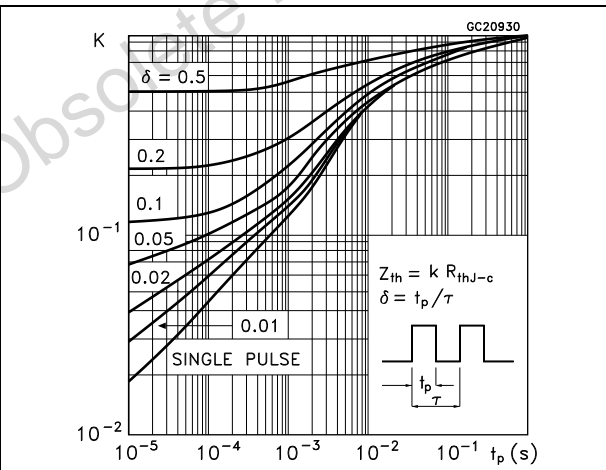


Figure 6. Output characteristics

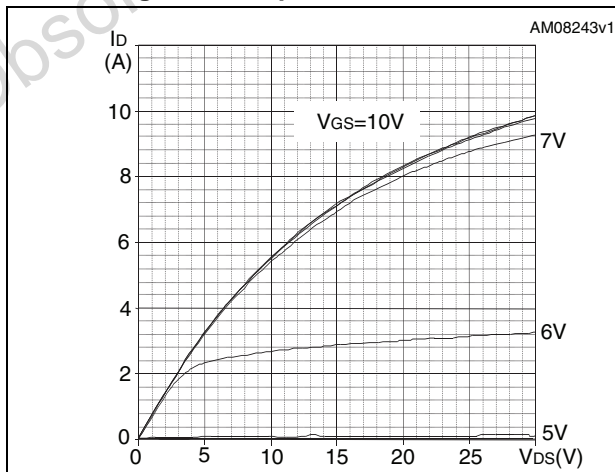


Figure 7. Transfer characteristics

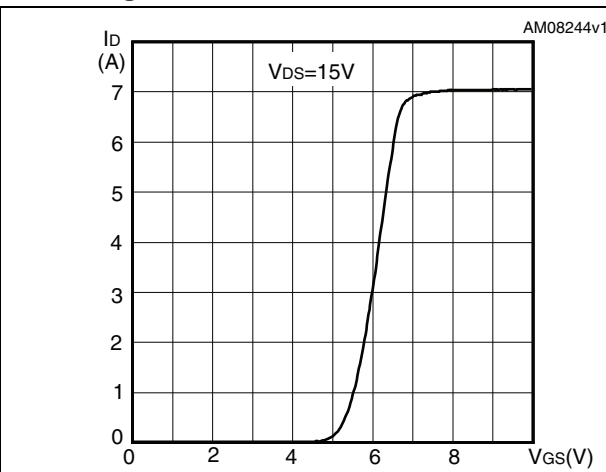


Figure 8. Gate charge vs gate-source voltage

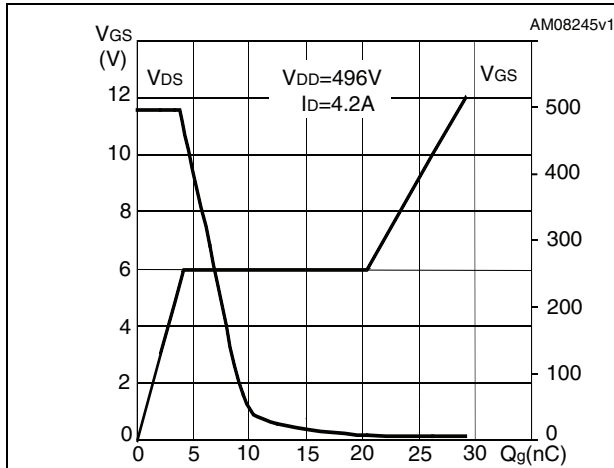


Figure 9. Static drain-source on-resistance

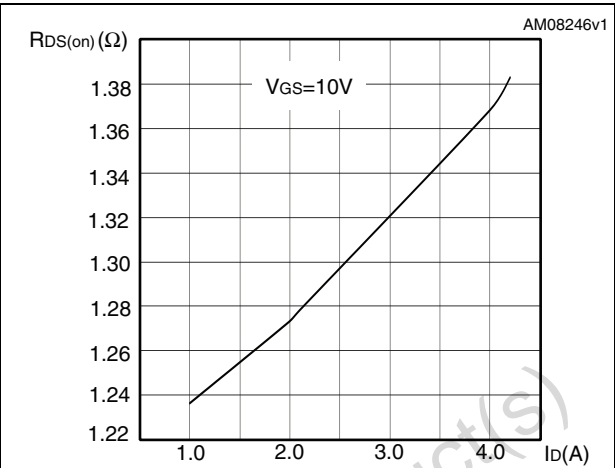


Figure 10. Capacitance variations

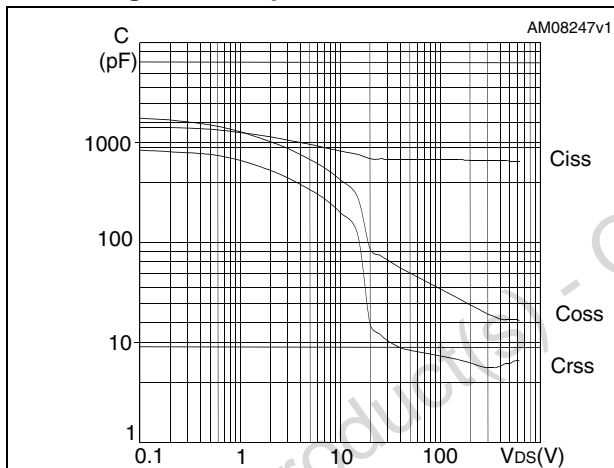


Figure 11. Output capacitance stored energy

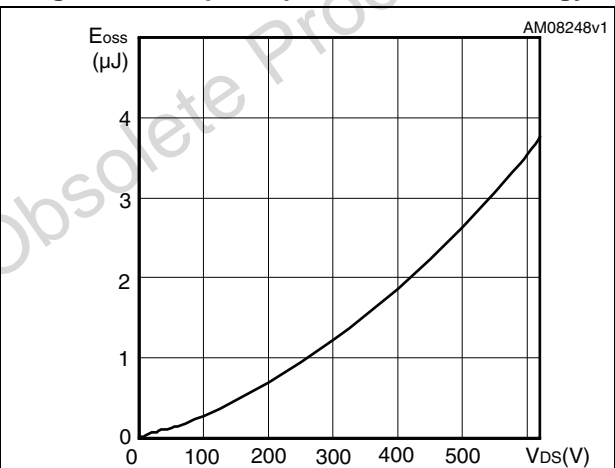


Figure 12. Normalized gate threshold voltage vs temperature

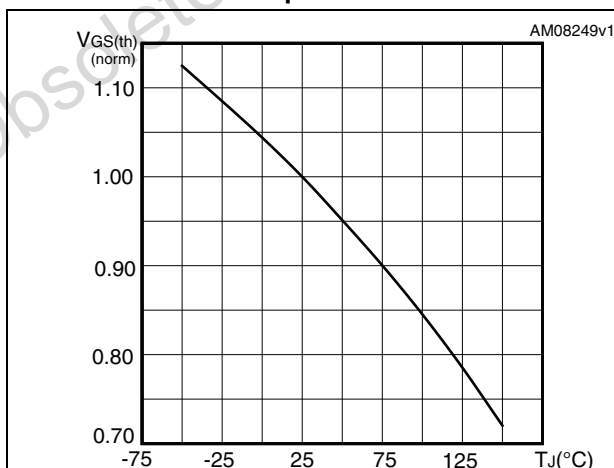


Figure 13. Normalized on-resistance vs temperature

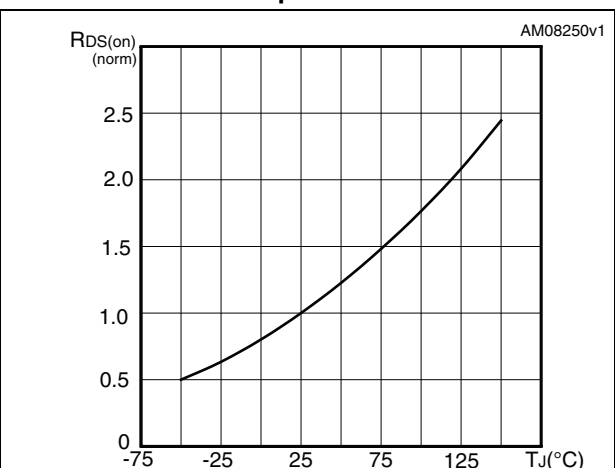


Figure 14. Source-drain diode forward characteristics

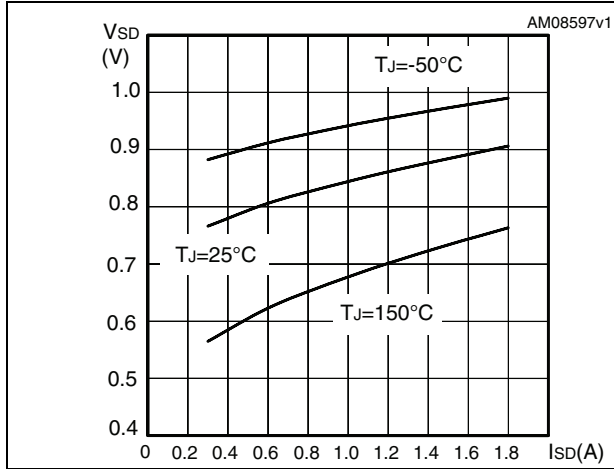


Figure 15. Normalized BV_{DSS} vs temperature

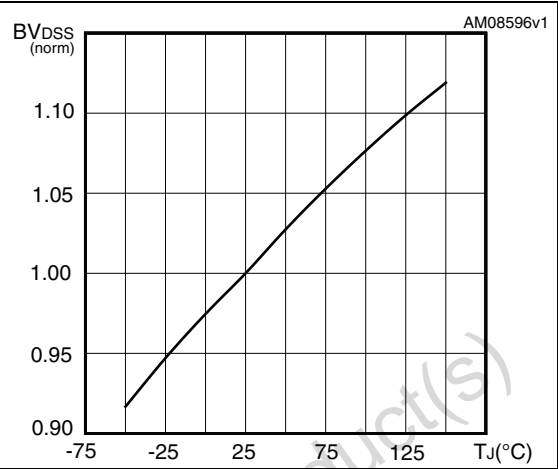
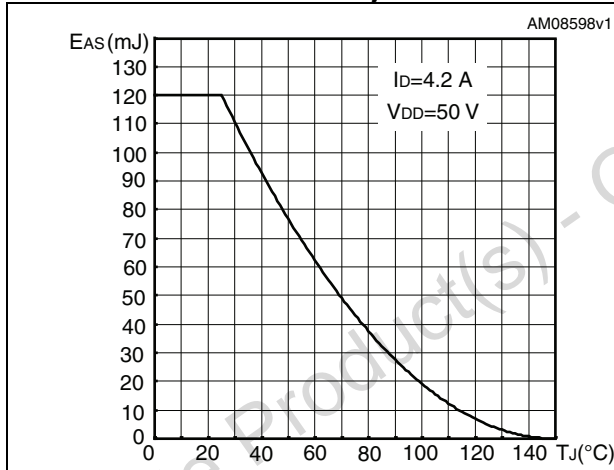


Figure 16. Maximum avalanche energy vs starting T_j



3 Test circuits

Figure 17. Switching times test circuit for resistive load

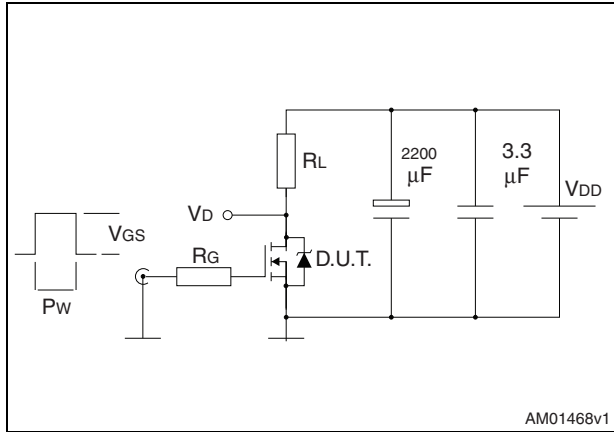


Figure 18. Gate charge test circuit

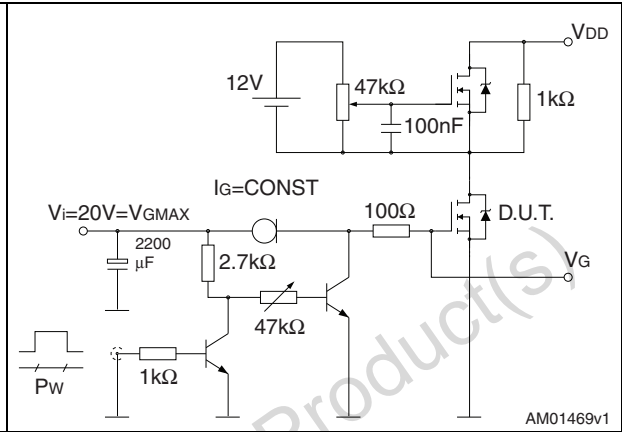


Figure 19. Test circuit for inductive load switching and diode recovery times

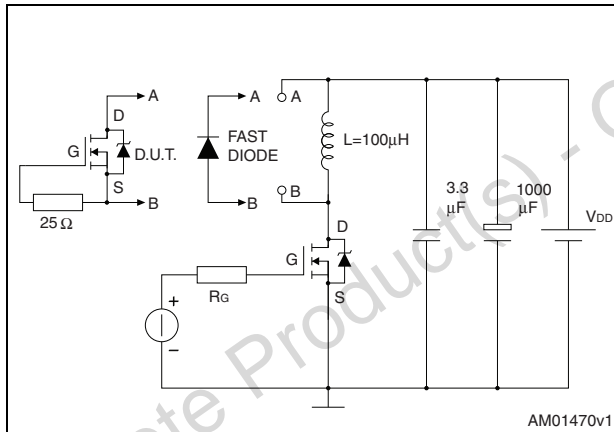


Figure 20. Unclamped inductive load test circuit

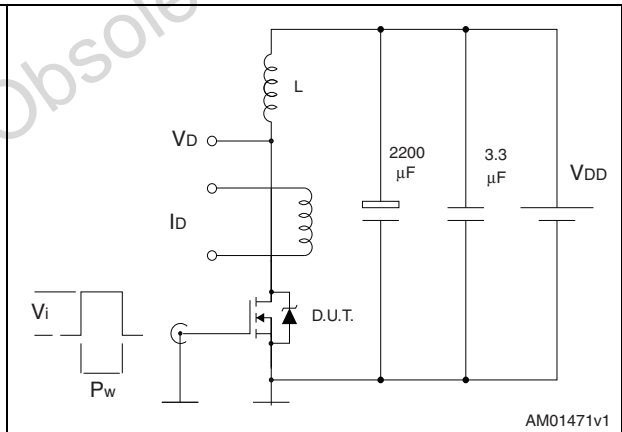


Figure 21. Unclamped inductive waveform

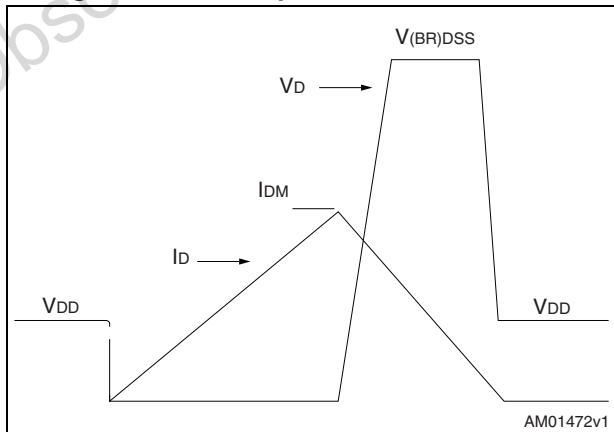


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Obsolete Product(s) - Obsolete Product(s)

Table 9. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 23. I²PAKFP (TO-281) drawing

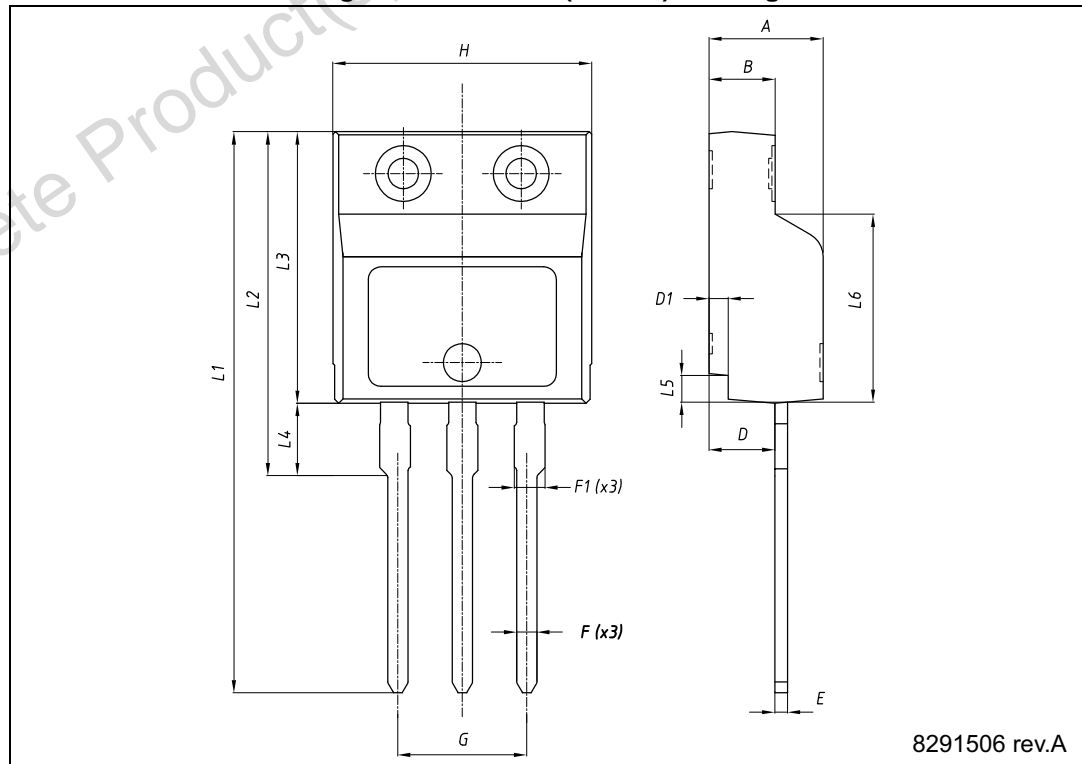
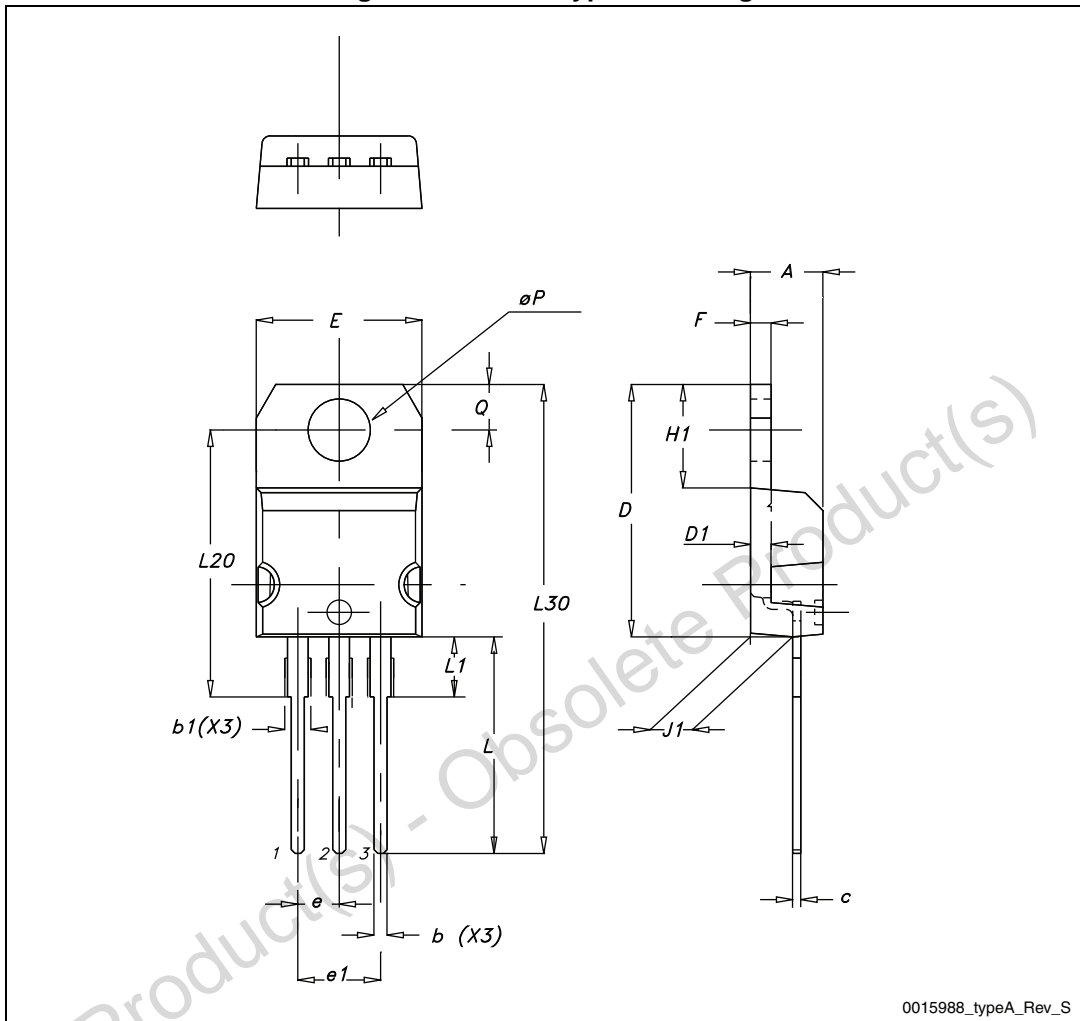


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 24. TO-220 type A drawing



0015988_typeA_Rev_S

5 Revision history

Table 11. Document revision history

Date	Revision	Changes
25-Mar-2013	1	First release.

Obsolete Product(s) - Obsolete Product(s)

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