

LTC3311S

3.3V to 1.2V at 12.5A, 2MHz Low EMI Buck Regulator in a 1.17cm² Solution

DESCRIPTION

Demonstration Circuit 3018A features the [LTC®3311S](#) 12.5A, low voltage, synchronous step-down Silent Switcher® 2 operating as a 2MHz 3.3V to 1.2V 12.5A buck regulator. The LTC3311S supports output voltages from 0.5V to V_{IN} with operating frequencies from 500kHz up to 5MHz. The LTC3311S is a compact, ultralow emission, high efficiency, and high speed synchronous monolithic step-down switching regulator. The integrated bypass capacitors optimize all the fast current loops and make it easier to minimize EMI/EMC emissions by reducing layout sensitivity. Fast minimum on-time of 35ns enables high V_{IN} to low V_{OUT} conversion at high frequency.

DC3018A is set up to run in forced continuous mode with a 2MHz switching frequency but can be configured to pulse skip mode or different switching frequencies. RT is connected to V_{IN} which sets the MODE/SYNC pin as an input and allows the LTC3311S to sync from an external clock. Connecting the MODE/SYNC pin to V_{IN} sets the mode to pulse skip mode and connecting the MODE/SYNC pin to GND sets the mode to forced continuous mode. The Efficiency vs Load graph shows the efficiency and

the power loss of the circuit with a 3.3V input in forced continuous mode operation.

The DC3018A also has an EMI filter to reduce conducted EMI. This EMI filter can be included by applying the input voltage at the V_{IN} EMI terminal. The EMI performance of the board is shown in the EMI Test Results section. The red lines in the EMI performance graphs illustrate the CISPR25 Class 5 peak limits for the conducted and radiated emission tests.

The LTC3311S data sheet gives a complete description of the part, operation and application information. The data sheet must be read in conjunction with this demo. The LTC3311S is assembled in a 3mm × 3mm LQFN package with exposed pads for low thermal resistance. The layout recommendations for low EMI operation and maximum thermal performance are available in the data sheet section Low EMI PCB Layout.

[Design files for this circuit board are available.](#)

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PERFORMANCE SUMMARY Specifications are at $T_A = 25^\circ\text{C}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		2.25		5.5	V
V_{OUT} Voltage Range*		1.176	1.2	1.224	V
OUTPUT Current	$V_{IN} > 3V$			12.5	A
Switching Frequency		1.8		2.2	MHz
Minimum On-Time			35	60	ns

*With 1% feedback resistors. Accuracy will improve to within 1% using 0.1% FB resistors.

QUICK START PROCEDURE

Demonstration circuit 3018A is easy to set up and evaluate the performance of the LTC3311S. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

NOTE: For accurate V_{IN} , V_{OUT} and efficiency measurements, measure V_{IN} at the VIN SNSE and GND SNSE turrets and V_{OUT} at the VOUT SNSE and GND SNSE turrets as illustrated as VM1 and VM2 in Figure 1. When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the output voltage ripple by touching the probe tip directly across the output turrets or to TP1 as shown in Figure 2.

1. Set the JP1 Jumper to the HI position.
2. With power off, connect the input power supply to VIN and GND. If the input EMI filter is desired, connect the input power supply to VIN EMI and GND.
3. Slowly increase PS1 to 1V. If AM1 reads less than 20mA, increase PS1 to 3.3V. Verify that VM1 reads 3.3V and VM2 reads 1.2V. Record VM1, VM2, VM3 AM1 and AM2. Connect an oscilloscope voltage probe as shown in Figure 2. Set Channel to AC-coupled, voltage scale to 20mV and time base to 10 μ s. Record V_{OUT} ripple voltage. Verify that PGOOD voltage is above 3V. Calculate die temperature using formula below:

$$T_J(^{\circ}\text{C}) = \frac{V_{SSTT}}{4\text{mV}} - 273$$

4. Increase the load by 1A intervals up to 12A and observe the voltage output regulation, ripple voltage, and the voltage on the SSTT turret. Observe the switching waveform by contacting a second voltage probe, set to 1V scale, to the SW node of UI pins 6, 7, 8 and 9 as shown in Figure 1.

5. If pulse skip mode is desired, set PS1 to 0V. Install a 100k resistor in the R3 location and remove R6 or short the MODE/SYNC turret to VIN. Repeat steps 1 through 4. In step 4 observe that the switching waveform is now operating in pulse skip mode at low currents.
6. To change the frequency, remove R4 and R6 if installed. Install the desired R_T resistor in the R7 location. Note, the MODE/SYNC pin is an output when R4 is installed and the MODE/SYNC pin should have high impedance to GND and VIN. Size the inductor, output capacitors and compensation components to provide the desired inductor ripple and a stable output. Refer to the LTC3311S data sheet and LTPowerCAD for more information on choosing the required components.
7. To test the transient response with a base load, add the desired resistor to produce a minimum load between VOUT and I_STEP turrets (R_L shown on Figure 1). Note that the total load resistance will be R_L plus R14 (50m Ω). Adjust a signal generator with a 10ms period, 10% duty cycle and an amplitude from 1V to 2V to start.
8. Measure the I_STEP voltage to observe the current, $V_{I_STEP}/50\text{m}\Omega$. Adjust the amplitude of the pulse to provide the desired transient. Adjust the rising and falling edge of the pulse to provide the desired ramp rate. Figure 3 shows a load step from 2.5A ($R_L = 0.43\Omega$) to 8A. Refer to the following equations:
$$I_{OUT} = \frac{V_{I_STEP}}{50\text{m}\Omega}$$
$$V_{GS} = V_{SG_INPUT} - V_{I_STEP}$$
9. Turn off PS1 and Load. Remove all connections to demo board.

QUICK START PROCEDURE

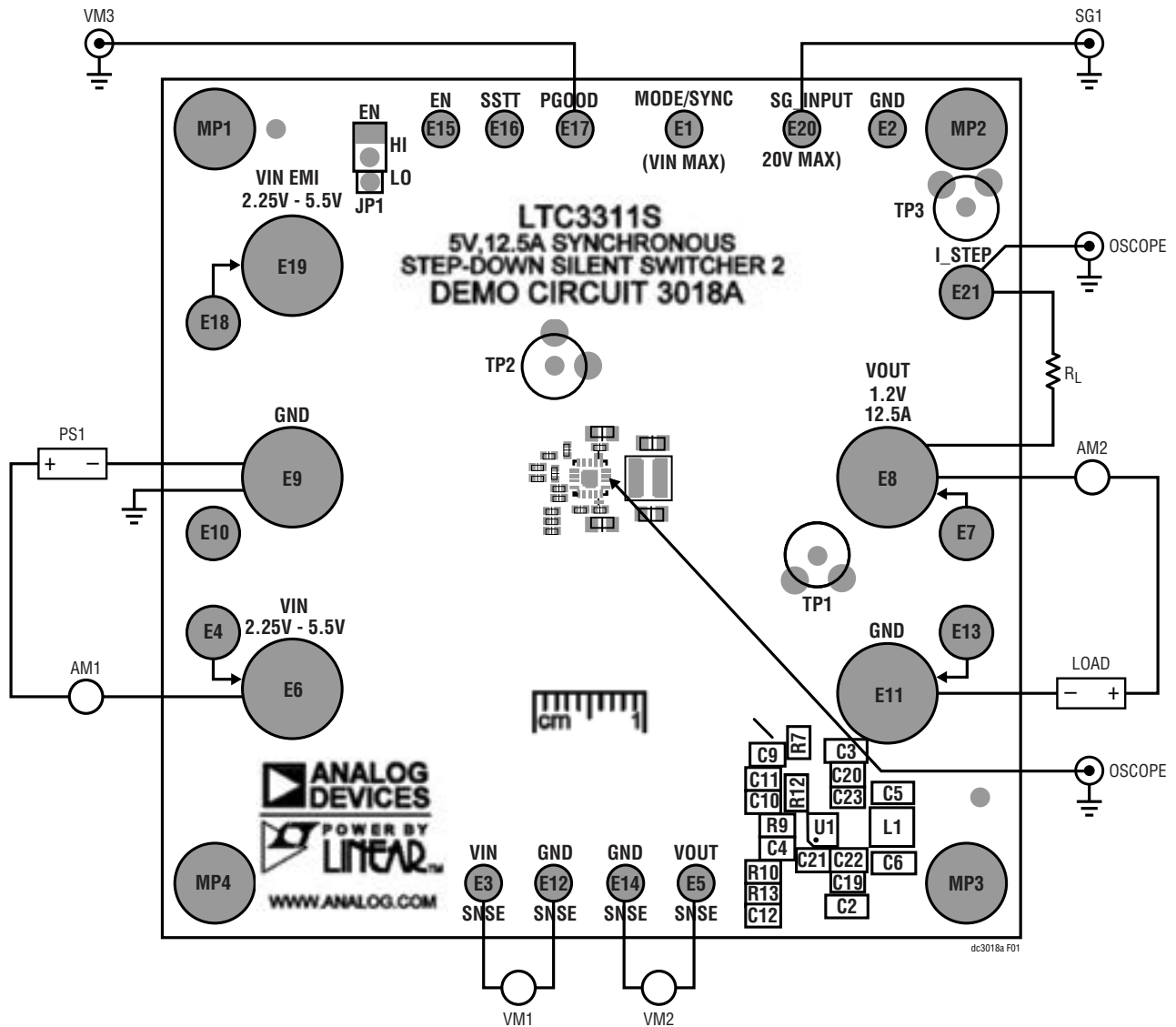


Figure 1. Test Setup for the DC3018A Demo board

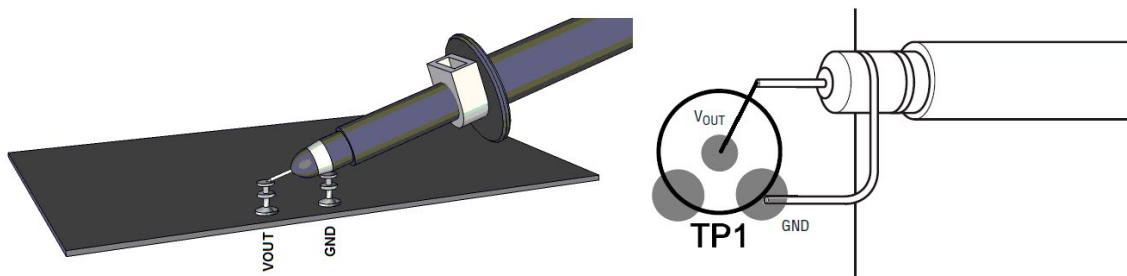


Figure 2. Technique for Measuring Output Ripple and Step Response

DEMO MANUAL DC3018A

QUICK START PROCEDURE

Load Transient Response Forced Continuous Mode

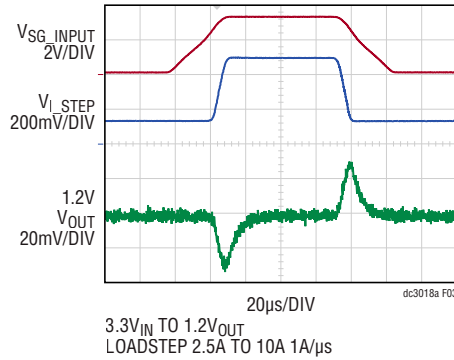
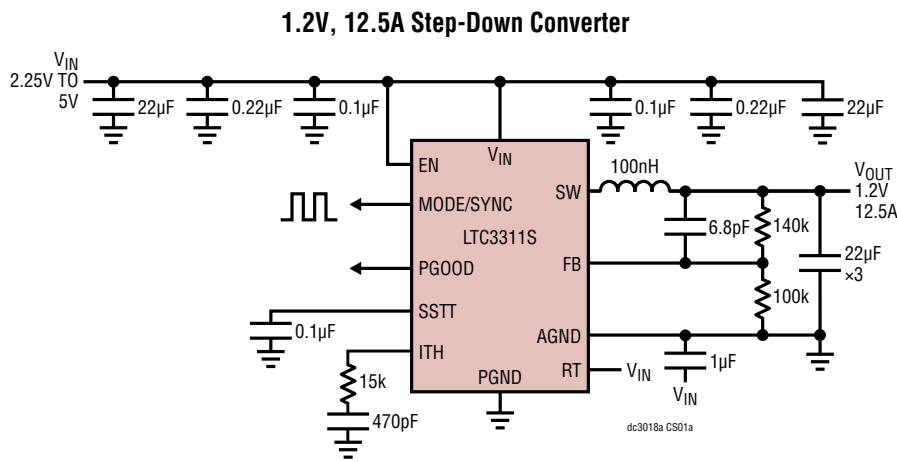
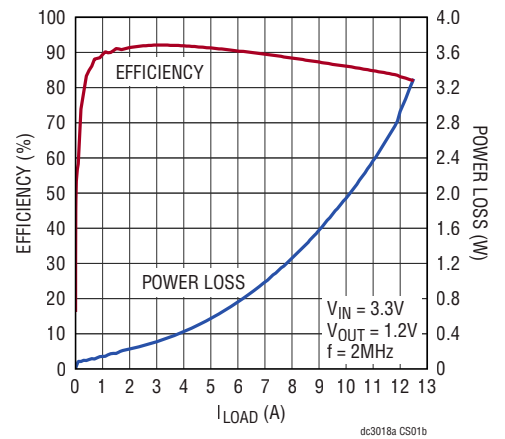


Figure 3. Technique for Measuring Load Step Response

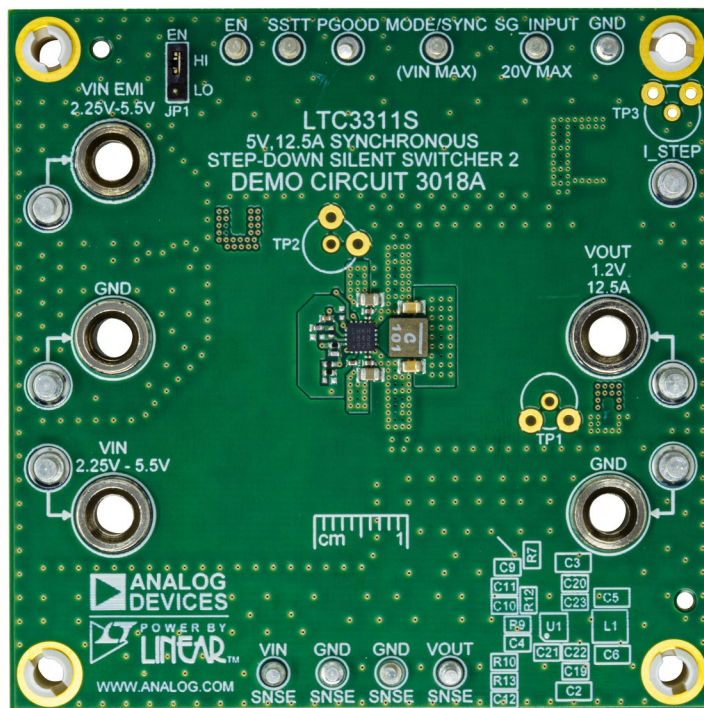
CIRCUIT SCHEMATIC



Efficiency vs Load Current

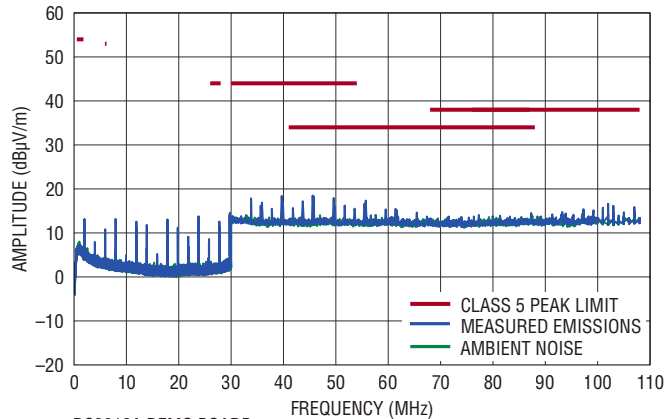


BOARD PHOTO



EMI TEST RESULTS

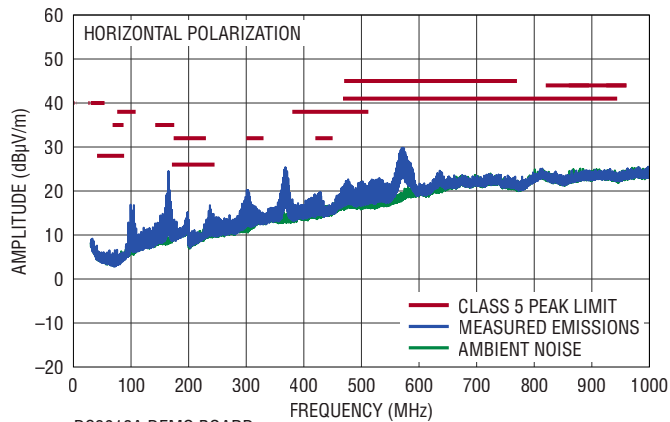
Conducted EMI Performance (CISPR25 Conducted Emission Test with Class 5 Peak Limits)



DC3018A DEMO BOARD
(WITH EMI FILTER INSTALLED)
3.3V INPUT TO 1.2V OUTPUT AT 10A, $f_{SW} = 2\text{MHz}$

dc3018a ETR01

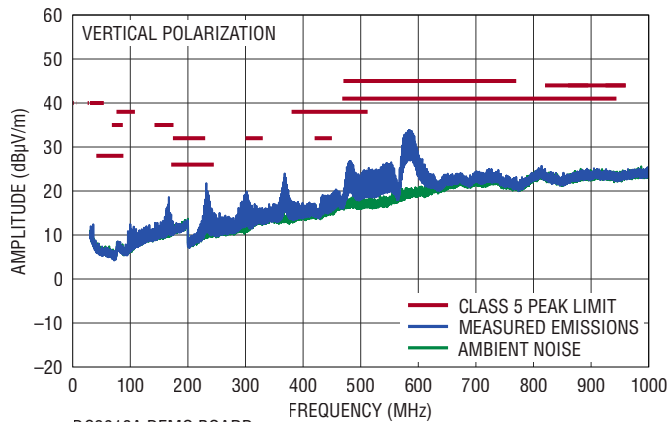
Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)



DC3018A DEMO BOARD
(WITH EMI FILTER INSTALLED)
3.3V INPUT TO 1.2V OUTPUT AT 10A, $f_{SW} = 2\text{MHz}$

dc3018a ETR02

Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits)



DC3018A DEMO BOARD
(WITH EMI FILTER INSTALLED)
3.3V INPUT TO 1.2V OUTPUT AT 10A, $f_{SW} = 2\text{MHz}$

dc3018a ETR03

THEORY OF OPERATION

Introduction to the DC3018A

The DC3018A demonstration circuit features the LTC3311S, a low voltage synchronous step-down Silent Switcher. The LTC3311S is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the internal ITH node. The error amplifier serves the ITH node by comparing the voltage on the VFB pin with an internal 500mV reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the ITH voltage until the average inductor current matches the new load current. When the top switch turns off, the synchronous power switch turns on until the next clock cycle begins or the inductor current falls to zero. If overload conditions result in excessive current flowing through the bottom switch, the next clock cycle will be delayed until the switch current returns to a safe level.

If the EN pin is low, the LT3311S is in shutdown and in a low quiescent current state. When the EN pin is above its threshold, the switching regulator will be enabled.

The MOD/SYNC pin synchronizes the switching frequency to an external clock, is a clock output or sets the PWM mode. The PWM modes of operation are either pulse skip or forced continuous. See the LTC3311S data sheet for more detailed information.

The maximum allowable operating frequency is influenced by the minimum on time of the top switch, the ratio of V_{OUT} to V_{IN} and the available inductor values. The

maximum allowable operating frequency may be calculated using a minimum t_{ON} of 35ns in the formula below.

$$f_{SW(MAX)} = \frac{V_{OUT}}{V_{IN(MAX)} \cdot t_{ON(MIN)}}$$

Select an operating switching frequency below $f_{SW(MAX)}$. Typically, it is desired to obtain an inductor current of 30% of the maximum LTC3311S operating load, 12.5A. Use the formulas below to calculate the inductor value to obtain a 30% (3.75A) inductor ripple for the operating frequency.

$$L \geq \frac{V_{OUT}}{3.75A \cdot f_{SW}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right) \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} \leq 0.5$$

$$L \geq \frac{0.25 \cdot V_{IN(MAX)}}{3.75A \cdot f_{SW}} \text{ for } \frac{V_{OUT}}{V_{IN(MAX)}} > 0.5$$

When determining the compensation components, C4, C10, C11 and R12, controlling the loop stability and transient response are the two main considerations. The LTC3311S has been designed to operate at a high bandwidth for fast transient response capabilities. This reduces output capacitance required to meet the desired transient response. The mid-band gain of the loop increases with R12 and the bandwidth of the loop increases with decreasing C11. C4 along with R4 provides a phase lead which will improve the phase margin. C10 along with R12 provide a high frequency pole to reduce the high frequency gain.

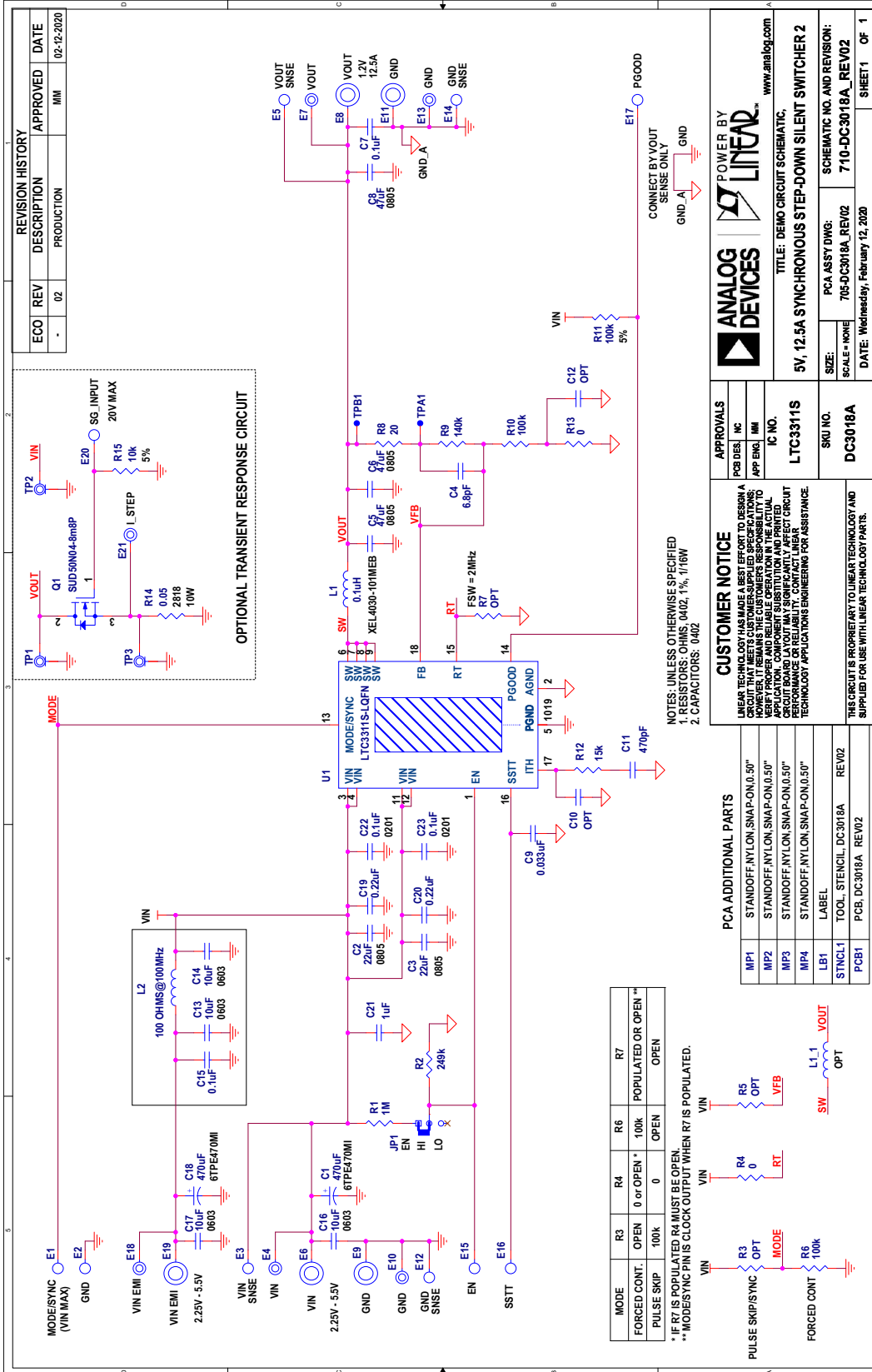
Loop stability is generally measured using the Bode plot method of plotting loop gain in dB and phase in degrees. The 0dB crossover frequency should be less than 1/6 of the operating frequency to reduce the effects of added phase shift of the modulator. The control loop phase margin goal should be 45° or greater and a gain margin goal of 8dB or greater.

DEMO MANUAL DC3018A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C2, C3	CAP., 22 μ F, X5R, 25V, 20%, 0805	AVX, 08053D226MAT2A
2	1	C4	CAP., 6.8pF, C0G, 50V, \pm 0.25pF, 0402	MURATA, GJM1555C1H6R8CB01D
3	3	C5, C6, C8	CAP., 47 μ F, X5R, 6.3V, 20%, 0805, AEC-Q200	MURATA, GRT21BR60J476ME13L
4	1	C9	CAP., 0.033 μ F, X7R, 25V, 10%, 0402	WURTH ELEKTRONIK, 885012205053
5	1	C11	CAP., 470pF, C0G, 50V, 5%, 0402, AEC-Q200	TDK, CGA2B2C0G1H471J050BA
6	1	L1	IND., 0.1 μ H, PWR, SHIELDED, 20%, 25.8A, 1.8m Ω , 4.3x4.3mm, XEL4030, AEC-Q200	COILCRAFT, XEL4030-101MEB
7	1	R9	RES., 140k, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402140KFKED
8	1	R10	RES., 100k, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402100KFKED
9	1	R12	RES., 15k, 1%, 1/16W, 0402	VISHAY, CRCW040215K0FKED
10	1	U1	IC, LOW VOLTAGE SYN. STEP-DOWN REG, LQFN-18	ANALOG DEVICES, LTC3311SEV#PBF
Additional Demo Board Circuit Components				
1	2	C1, C18	CAP., 470 μ F, TANT, POSCAP, 6.3V, 20%, 7343, 18m Ω , TPE	PANASONIC, 6TPE470MI
2	2	C7, C15	CAP., 0.1 μ F, X5R, 25V, 10%, 0402	AVX, 04023D104KAT2A
3	0	C10, C12	CAP., OPTION, 0402	
4	4	C13, C14, C16, C17	CAP., 10 μ F, X5R, 10V, 20%, 0603	AVX, 0603ZD106MAT2A
5	2	C19, C20	CAP., 0.22 μ F, X7R, 16V, 10%, 0402, AEC-Q200	MURATA, GCM155R71C224KE02D
6	1	C21	CAP., 1 μ F, X5R, 10V, 20%, 0402	MURATA, GRM153R61A105ME95D
7	2	C22, C23	CAP., 0.1 μ F, X7S, 16V, 10%, 0201	MURATA, GRM033C71C104KE14D
8	1	L2	IND., 100 Ω AT 100MHZ, FERRITE BEAD, 25%, 8A, 6m Ω , 1812	WURTH ELEKTRONIK, 74279226101
9	1	Q1	XSTR., MOSFET, N-CH, 40V, 14A, DPAK (TO-252)	VISHAY, SUD50N04-8M8P-4GE3
10	1	R1	RES., 1M, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW04021M00FKED
11	1	R2	RES., 249k, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402249KFKED
12	0	R3, R5, R7	RES., OPTION, 0402	
13	2	R4, R13	RES., 0 Ω , 1/16W, 0402, AEC-Q200	VISHAY, CRCW04020000Z0ED
14	2	R6, R11	RES., 100k, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW0402100KJNED
15	1	R8	RES., 20 Ω , 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040220R0FKED
16	1	R14	RES., 0.05 Ω , 1%, 10W, 2818, AEC-Q200, METAL, HP	VISHAY, WSHP2818R0500FEA
17	1	R15	RES., 10k, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040210K0JNED
Hardware: For Demo Board Only				
1	10	E1-E3, E5, E12, E14-E17, E20	TEST POINT, TURRET, 0.064" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2308-2-00-80-00-00-07-0
2	6	E4, E7, E10, E13, E18, E21	TEST POINT, TURRET, 0.094" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2501-2-00-80-00-00-07-0
3	5	E6, E8, E9, E11, E19	CONN., BANANA JACK, FEMALE, THT, NON-INSULATED, SWAGE, 0.218"	KEYSTONE, 575-4
4	1	JP1	CONN., HDR, MALE, 1x3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000311121
5	4	MP1-MP4	STANDOFF, NYLON, SNAP-ON, 0.50"	KEYSTONE, 8833
6	1	XJP4	CONN., SHUNT, FEMALE, 2 POS, 2mm	WURTH ELEKTRONIK, 60800213421

SCHEMATIC DIAGRAM





ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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