ADSANTEC
Ultra High-Speed Mixed Signal ASICs
Advanced Science And Novel Technology Company, Inc.
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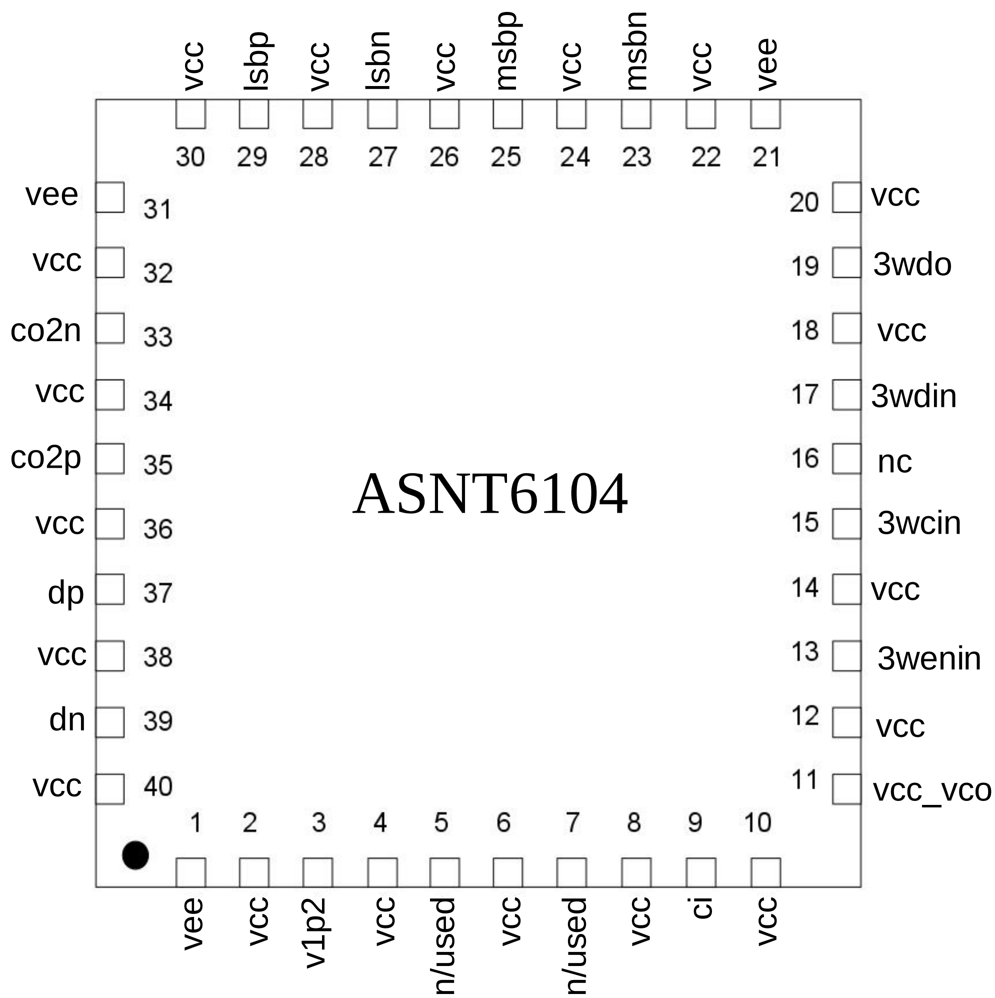
ASNT6104-PQB
32*Gbps*-16*Gbaud* PAM4 Decoder

- One high-speed input PAM4 signal to two binary output signals
- Half-rate clock output synchronized with two output data signals
- Adjustable threshold levels for input signal
- Fully differential CML input and output data
- Differential CML input clock interface
- 1.2*V* CMOS 3-wire interface for digital controls
- Single -3.3*V* or +3.3*V* power supply
- Power consumption: 2.4*W*
- Standard QFN 40-pin package



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DESCRIPTION

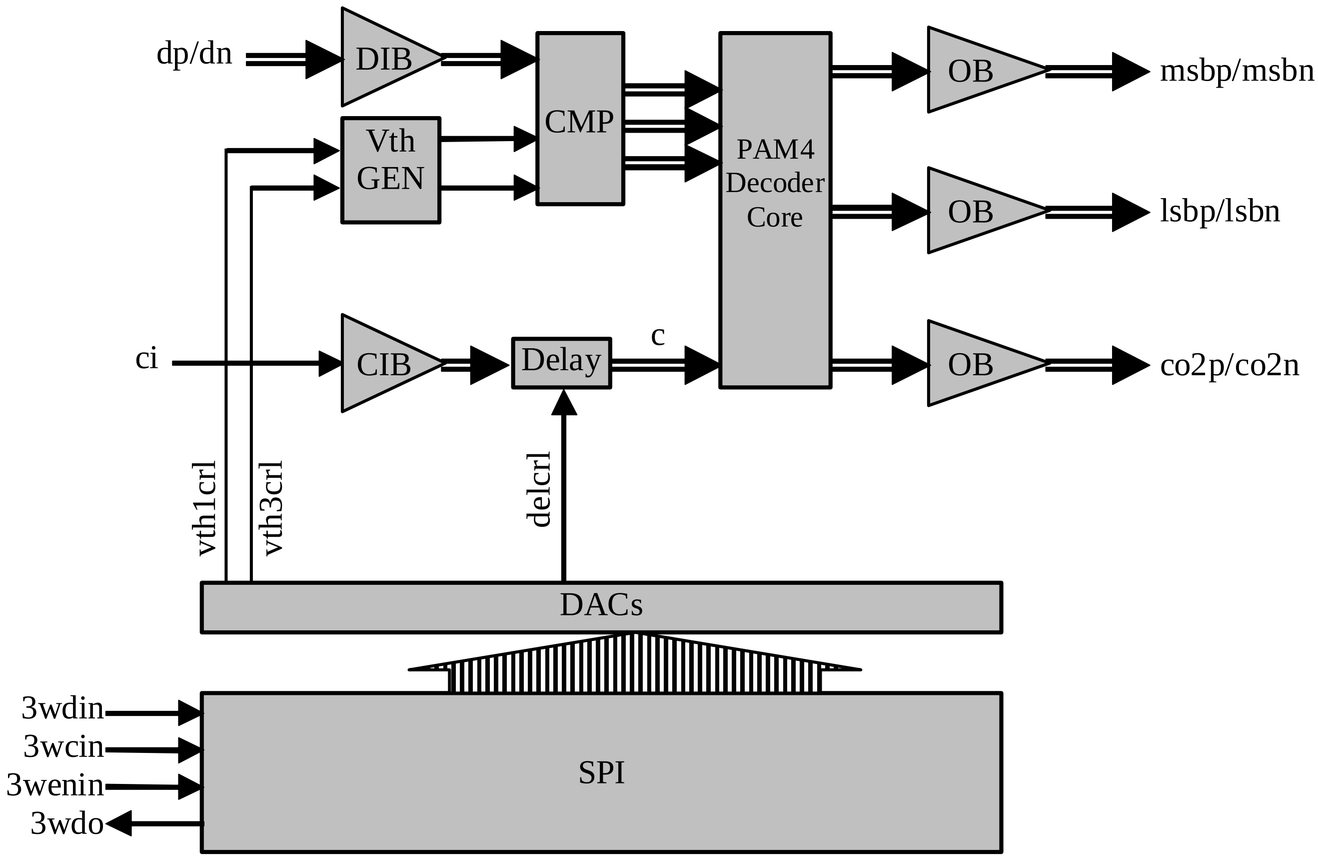

Fig. 1. Functional Block Diagram

The ASNT6104-PQB SiGe IC shown in Fig. 1 is a PAM4 decoder. The differential PAM4 input data signal dp/dn is processed by the linear input buffer (DIB) and is sent to the Comparator block (CMP). Three limiting buffers inside CMP process the 3-level PAM4 signal. One of the buffers processes the input signal differentially. The other two buffers compare single-ended data to their own threshold levels that are produced by the Voltage Threshold Generator block (Vth GEN). The three resulting differential binary data streams are sent to the PAM4 Decoder Core where they are retimed by D-type flip flops (DFFs) with a full-rate external clock, and delayed by the adjustable delay line block (Delay). The three differential signals are decoded into two differential data streams. The two signals are retimed again, and are sent to the output through Output Buffers (OB).

To reduce the physical number of control inputs to the chip, a shift register with a 3-wire input interface (SPI) has been included on chip. The SPI block provides all the digital controls for the chip. It also provides digital controls for digital-to-analog converters (DACs) that handle internal analog DC voltage adjustments.

DIB

The Data Input Buffer (DIB) can process an input analog CML data signal dp/dn in PAM4 format. It provides on-chip single-ended termination of 50*Ohms* to vcc for each input line. The buffer can also accept a single-ended signal to one of its input ports dp, or dn with a threshold voltage applied to the unused pin in case of DC termination.

CMP

CMP accepts a differential analog 4-level PAM4 signal from DIB. The purpose of CMP is to transform the signal to three binary digital data signals by utilizing two threshold levels that are generated by the Voltage Threshold Generator block. The first signal is generated after the positive single-ended version of the analog input PAM4 signal, and the DC voltage threshold signal vth1 go through a limiting buffer. The level of vth1 should be between the top level of the single-ended PAM4 signal after the input buffer, and the next lower level. The second digital output signal of CMP is formed by letting the differential input through a limiting buffer. The third signal is generated after the positive single-ended version of the analog input PAM4 signal, and the DC voltage threshold signal vth3 go through a limiting buffer. The level of vth3 should be between the bottom level of the single-ended PAM4 signal after the input buffer and the next higher level.

Vth GEN

The purpose of the Voltage Threshold Generator block (Vth GEN) is to form two threshold voltage levels for CMP. The levels are independently adjusted through two digital bytes of the SPI. The byte vth1crl controls the top level. The byte vth3crl controls the bottom level. Fig. 2 presents the dependence of the two levels on their own digital codes of the SPI.

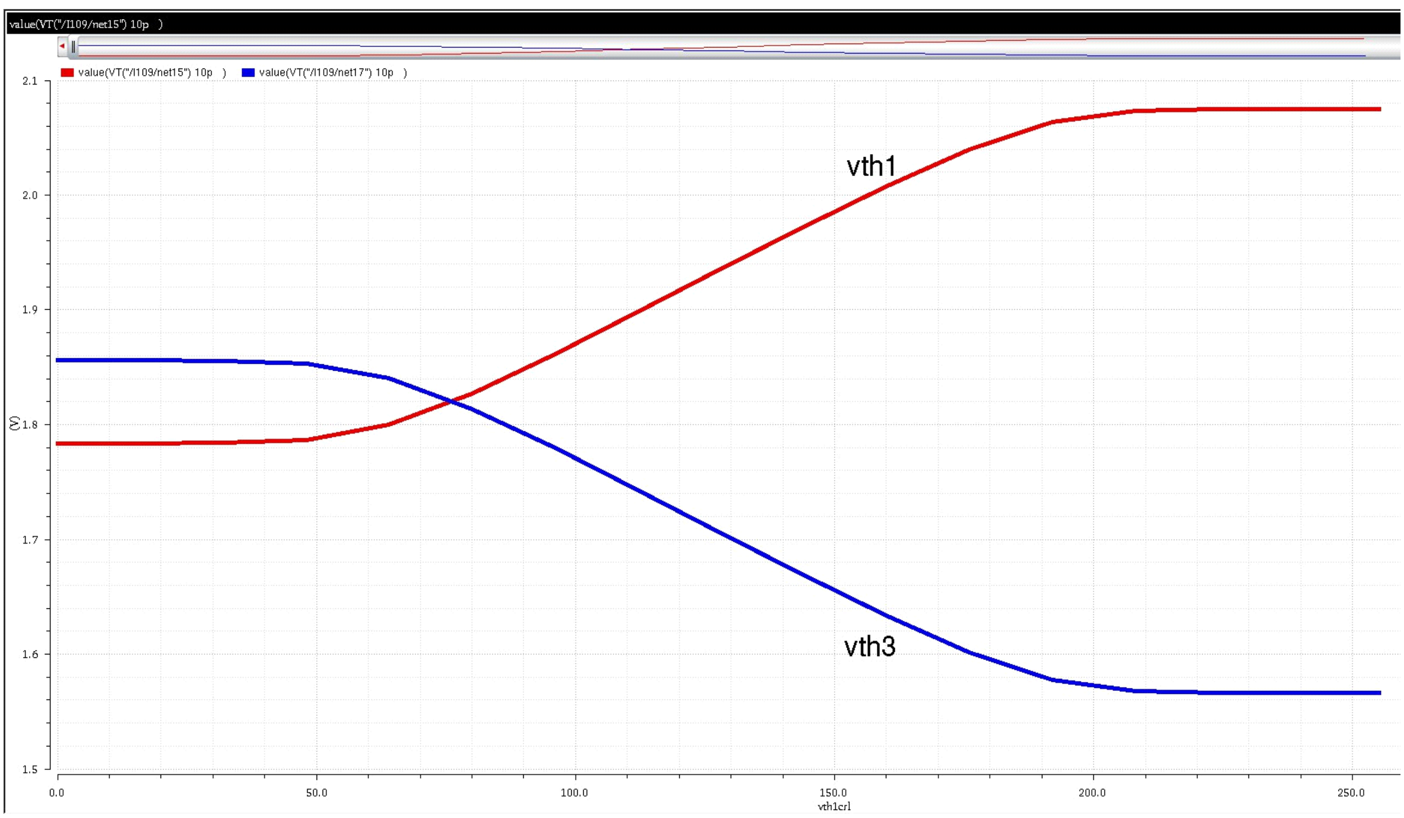

Fig. 2. Voltage Threshold Adjustment (vee=0V)

PAM4 Decoder Core

The three digital binary differential signals from CMP are retimed in the Core by the full-rate clock. Then the signals go through decoder logic to form two differential digital binary data signals. The signals are retimed by the shifted full-rate clock, and sent to the output buffers. The full-rate clock goes through the clock dvider-by-2, and is sent to an identical output buffer. The edges of the data, and clock signals are aligned.

External clock Input Buffer (CIB)

An external full-rate clock signal is required for the part operation. The clock buffer CIB has CML interface with internal 50*Ohm* terminations to vcc for both direct and inverted inputs. It accepts either differential or single-ended signal. DC common mode voltage for the input signal should match the values specified in ELECTRICAL CHARACTERISTICS. Otherwise, DC blocks are required.

Proper alignment of the external clock with the incoming data is critical for the correct data decoding. This can be achieved by means of the internal delay block described below.

Delay

The purpose of the delay block is to deliver the delayed version of the full-rate external clock to the decoder core. By utilizing the digital control byte delcrl, the phase of the clock can be shifted with respect to data to achieve optimal latching by the DFFs.

3-Wire Interface Control Block

To reduce the physical number of control inputs to the chip, a 5-byte shift register with a 3-wire input interface has been included on chip. The SPI block is powered by an internally generated supply voltage of +1.2*V* from vee. The supply voltage of the SPI can be monitored through pin v1p2. The digital control bits applied through 3wdin input are latched in, and shifted down the register with the clock 3wcin. Write enable signal 3wenin must be set to logic "0" during the data read-in phase. The SPI data can be monitored through the output 3wdo. Table 1 presents the byte order of the 3-wire interface block.

Table 1. Control Bytes

Byte Number	Bit Number							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	vth3crl(7:0)							
2	vth1crl(7:0)							
3	delcrl(7:0)							
4	00000000							
5	X	X	X	X	0	0	0	0

SPI load order is illustrated in Fig. 3.

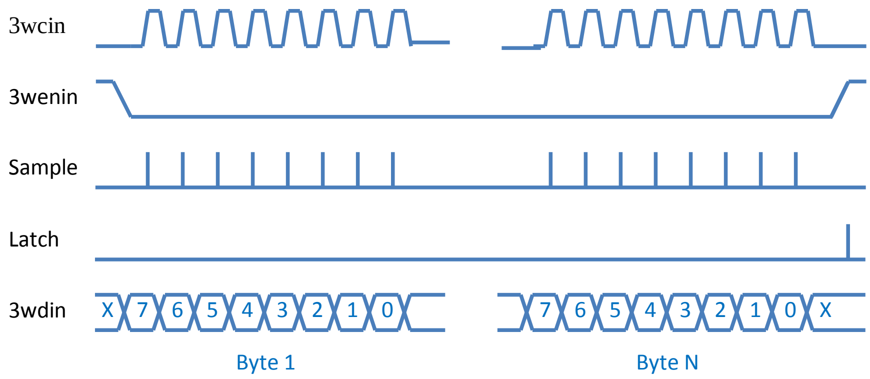

Fig. 3. SPI Load Order

POWER SUPPLY CONFIGURATION

The ASNT6104-PQB can operate with either a negative supply (vcc = 0.0*V* = ground and vee = -3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohms* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 3.3*V* and vee = 0*V* (external ground)

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.8	*V*
Power Consumption		2.1	*W*
Input Voltage Swing (SE)		1.0	*V*
Case Temperature*)		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dp	37	Input	CML differential data inputs with internal SE 50*Ohm* termination to vcc
dn	39		
ci	9	Input	SE full-rate clock input with internal 50*Ohm* termination to vcc_vco
msbp	25	Output	CML differential data outputs. Require external SE 50*Ohm* termination to vcc
msbn	23		
lsbp	29	Output	CML differential data outputs. Require external SE 50*Ohm* termination to vcc
lsbn	27		
co2p	35	Output	CML differential half-rate clock outputs. Require external SE 50*Ohm* termination to vcc
co2n	33		
Low-Speed I/Os			
3wenin	13	1.2*V* CMOS input	Enable input signal for 3-wire interface
3wcin	15		Clock input signal for 3-wire interface
3wdin	17		Data input signal for 3-wire interface
3wdo	19	1.2*V* CMOS output	Data output signal of 3-wire interface
Controls			
v1p2	3	I/O	Internally generated SPI supply voltage

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	2, 4, 6, 8, 10, 12, 14, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40
vcc_vco	Positive power supply for VCO (+3.3*V*)	11
vee	Negative power supply (GND or 0*V*)	1, 21, 31
n/used	Not used in this chip configuration	5, 7
nc	Not connected	16

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc and vcc_vco	+3.0	+3.3	+3.6	*V*	±9%
vee		0.0		*V*	
I_{vcc}		670		*mA*	
I_{vcc_vco}		45		*mA*	
Power Consumption		2.4		*W*	
Junction Temperature	-25	50	125	*°C*	
HS Input Data (dp/dn)					
Data Rate		16	17	*Gbaud*	PAM4
Swing p-p (Diff or SE)	0.05		0.6	*V*	
CM Voltage Level	vcc-0.8		vcc	*V*	
HS Input Clock (ci)					
Frequency		16	17	*GHz*	
Swing p-p (Diff or SE)	0.05		0.8		
CM Voltage Level	vcc-0.8		vcc		
HS Output Data (msbp/msbn, lsbp/lsbn)					
Data Rate		16	17	*Gbps*	
Logic “1” level		vcc		*V*	
Logic “0” level	vcc -0.66		vcc -0.6	*V*	
Jitter		3	5	*ps*	p-p
HS Output Half-Rate Clock (co2p/co2n)					
Clock Rate		8	8.5	*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level	vcc -0.66		vcc -0.6	*V*	
Jitter		2	4	*ps*	p-p
3-Wire Inputs (3wdin, 3wcin, 3wenin)					
High voltage level	vee+1.2		vee+1.4	*V*	
Low voltage level	vee		vee+0.35	*V*	
Clock speed		350	400	*MHz*	

PACKAGE INFORMATION

The chip is packaged in a standard 40-pin QFN package shown in Fig. 4. It is recommended that the center heat slug located on the back side of the package is soldered to ground to help dissipate heat generated by the chip during operation.

The part’s identification label is ASNT6104-PQB. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package’s manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

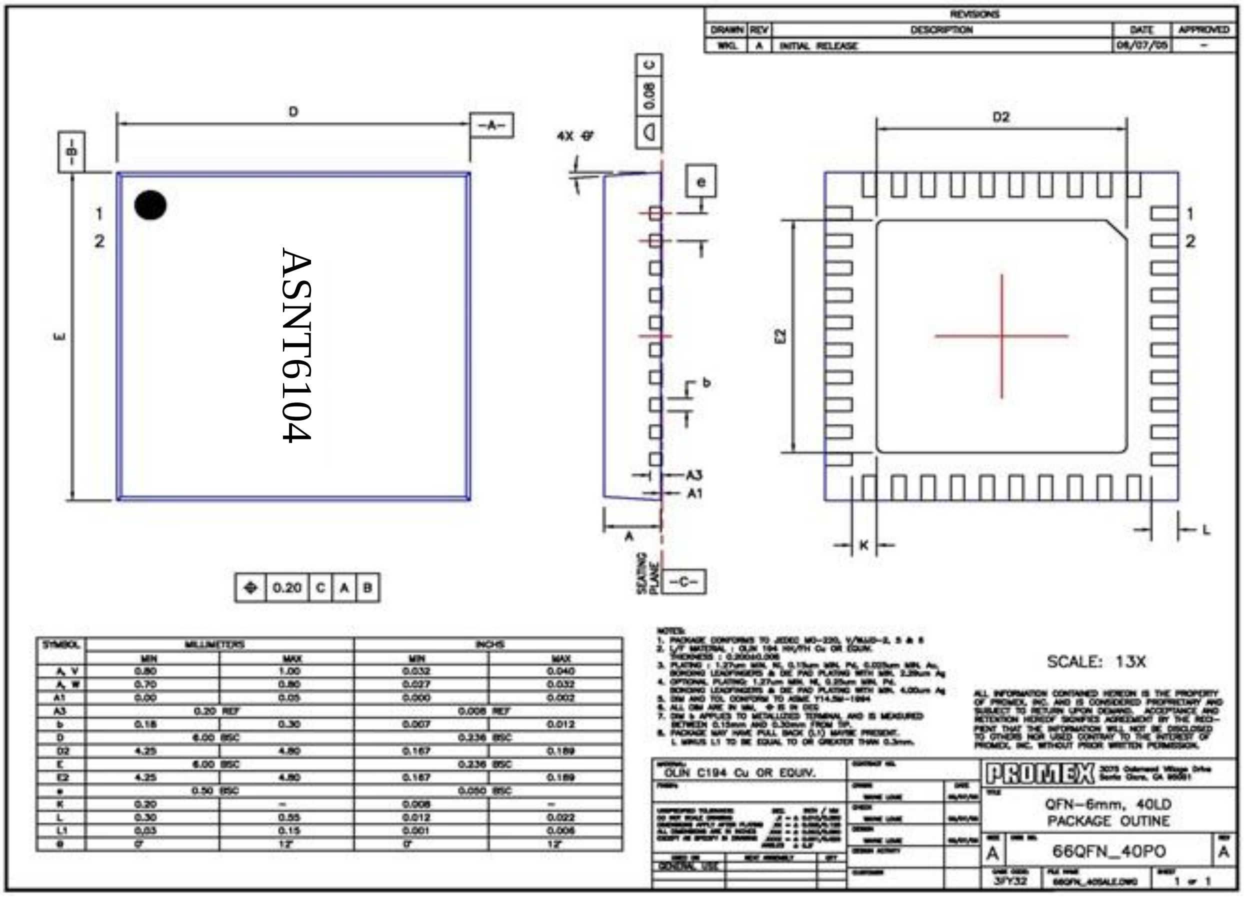

Fig. 4. QFN 40-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.0.2	01-2021	Corrected pin out diagram Corrected operational speed Corrected functional block diagram Removed CR description
0.2.2	12-2020	Corrected description of ci termination
0.1.2	09-2020	Pin out diagram corrected
0.0.2	09-2020	Preliminary release