ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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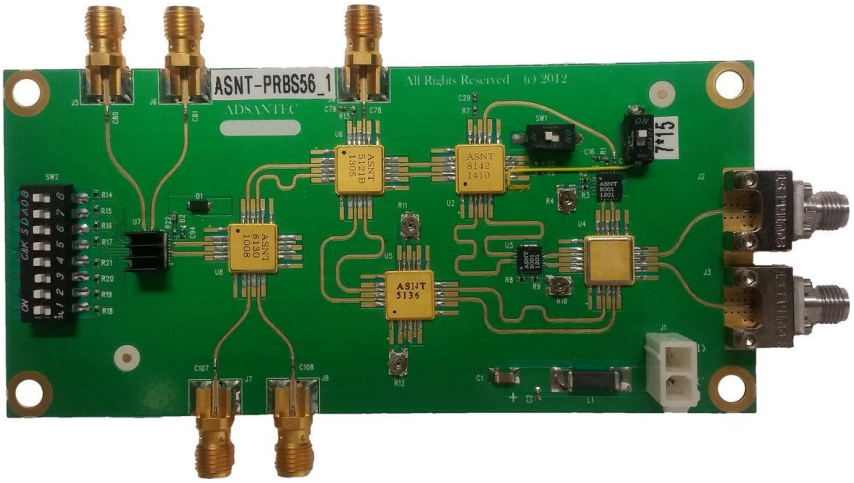
ASNT_PRBS56_1
4Gbps -52*Gbps* PRBS7/PRBS15 Generator with Sync Output

- Broadband frequency range 4*Gbps* – 52*Gbps*
- Adjustable clock duty cycle for MUX
- 2-512 divide differential sync output
- Static divide by four differential output
- AC coupled single-ended Clock Input
- Minimal insertion jitter
- Fast rise and fall times
- 50% duty cycle sync output on all divide ratios
- Single +3.3*V* supply



DESCRIPTION

The ASNT_PRBS56_1 is a broadband 2^7-1 or 2^{15}-1 PRBS generator intended for test, prototyping, microwave, and communication applications. A single-ended clock from 2*GHz* to 26*GHz* is used. This single-ended Clock Input feeds a static differential Divide by 4 Output, an adjustable differential divide by 2 to 512 Sync Output, a differential clock that supplies the multiplexer responsible for doubling the data rate up to 52*Gbps*, and a differential clock that triggers the PRBS generation. The Clock Input, Sync Output, and Divide by 4 Output are AC coupled on board. The PRBS Output is DC coupled operating with a common mode level above ground.

The ASNT_PRBS56_1 board contains five Emerson SMA connectors MFG PN: 142-0761-881, two Southwest 2.92mm (K-type) edge mount female connectors MFG PN: 1092-03A-5, 50*Ohm* transmission lines to the device, and power supply decoupling networks on the evaluation board. Power is supplied through a two-pin MOLEX connector P/N: 39-28-1023.

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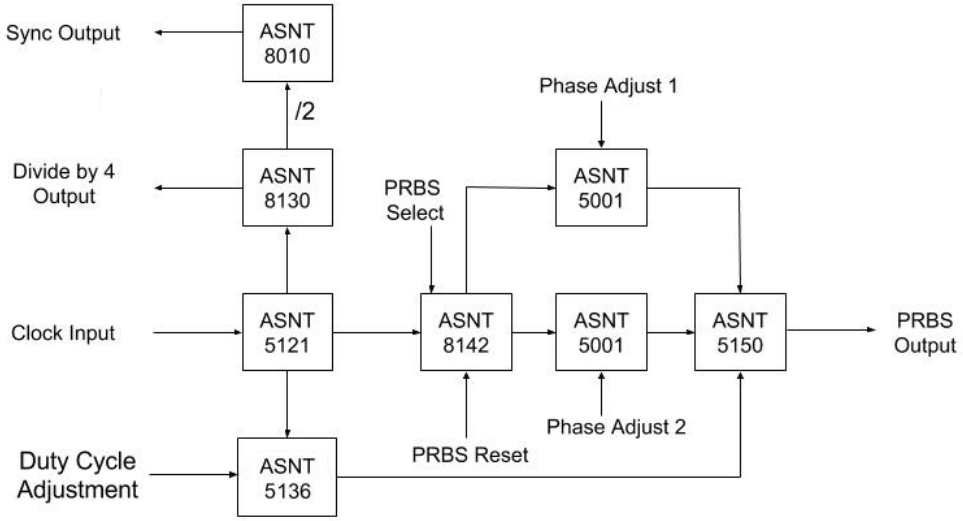
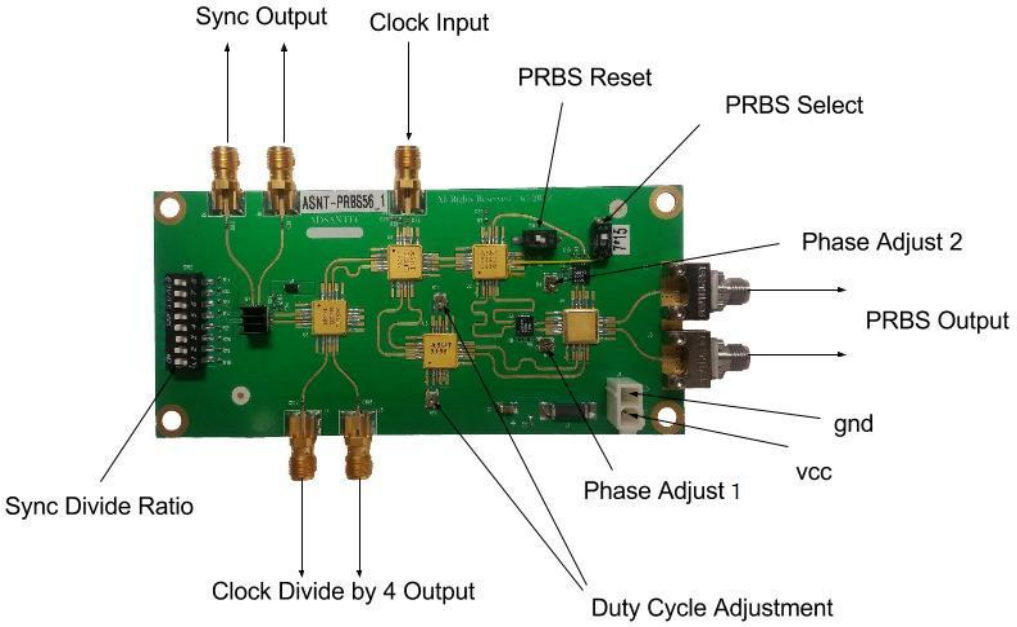
The data output's duty cycle is adjustable through two on-board potentiometers. Each phase shifter has an on-board potentiometer for adjusting the data entering the multiplexer. This adjustment capability ensures the best operating point for a specific frequency. PRBS7 or PRBS15 is selected through an on-board switch. An on-board PRBS reset switch is included to preset the generator to avoid the all zero state lock-up.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS



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PRBS Select

Move the switch to the ON position for PRBS15 data. Move the switch to the OFF position for PRBS7 data output. The PRBS Reset may need to be toggled to the ON position then OFF before a PRBS pattern is observed on the data output.

Sync Output

Using the Sync Output to trigger an oscilloscope will display an eye diagram or a PRBS7 pattern output for divide ratio of 254 or 508. It contains eight switches that represent 8 bits. The LSB starts at SW1 and the MSB ends at SW8. The binary value of zero gives a decimal n value of 512. Increasing binary values increases the decimal value n.

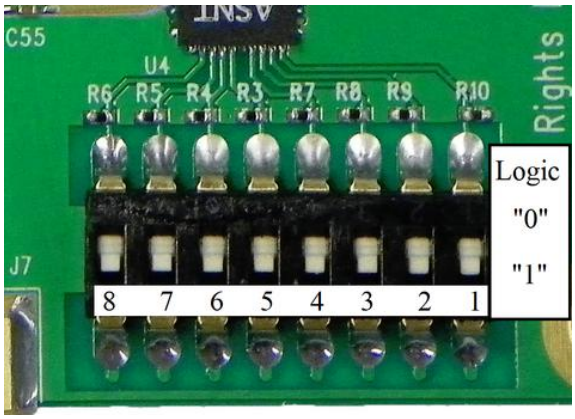

Table 1. Divide ratio

DIP SW # 8 7 6 5 4 3 2 1	n Divide Ratio	
0 0 0 0 0 0 0 1	2	
0 0 0 0 0 0 1 0	4	
0 0 0 1 0 0 0 0	32	Eye diagram
.		
0 1 1 1 1 1 1 1	254	pattern
1 1 1 1 1 1 1 0	508	pattern
0 0 0 0 0 0 0 0	512	

OPERATION

1. Set the PRBS Reset and PRBS Select switch to the OFF position.
2. Set the power supply to 0*V* and current limit it to 2.3*A*.
3. Connect the power supply to the board and slowly increase it to +3.3*V*.
4. Apply a DC coupled half-rate single-ended clock to the Clock Input. Note: The Clock Input is AC coupled on board.
5. Connect PRBS Output to a 50*Ohm* terminated oscilloscope single-ended/differentially AC coupled. Note: AC couple and 50*Ohm* terminate any unused outputs.
6. Connect Sync Output to the oscilloscope's trigger DC coupled. Note: Trigger outputs are AC coupled on board.
7. Set a divide ratio 254 or 508 ratio for the Sync Output.
8. Toggle the PRBS Reset switch to the ON position and then to the OFF position.
9. Scroll/Delay the 127 bit PRBS7 pattern on the oscilloscope until you observe a sequence of data close to 7 one's followed by 6 zero's. You may find a pattern shown below in **Figure 2**, which is incorrect.

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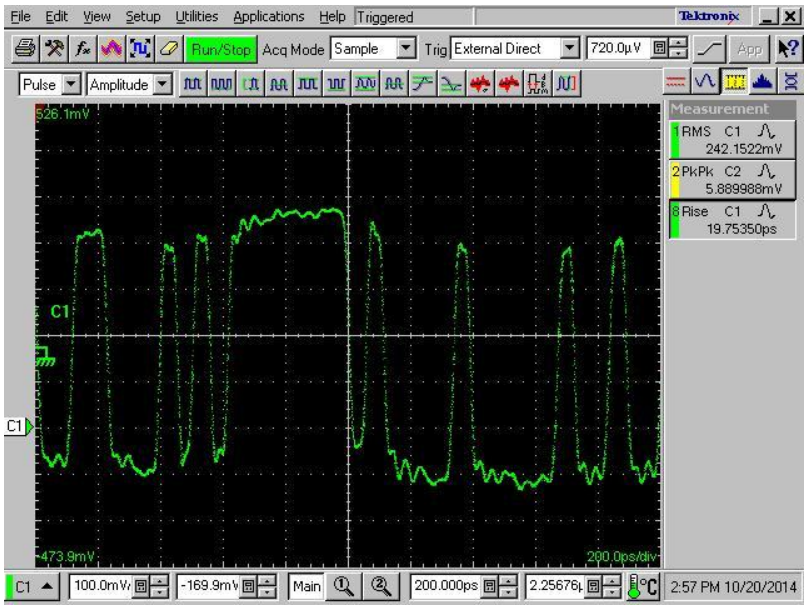

Figure 2. Incorrect PRBS7 pattern

10. Adjust Phase Adjust 1 and Phase Adjust 2 until the correct PRBS7 pattern is displayed as shown in **Figure 3**.

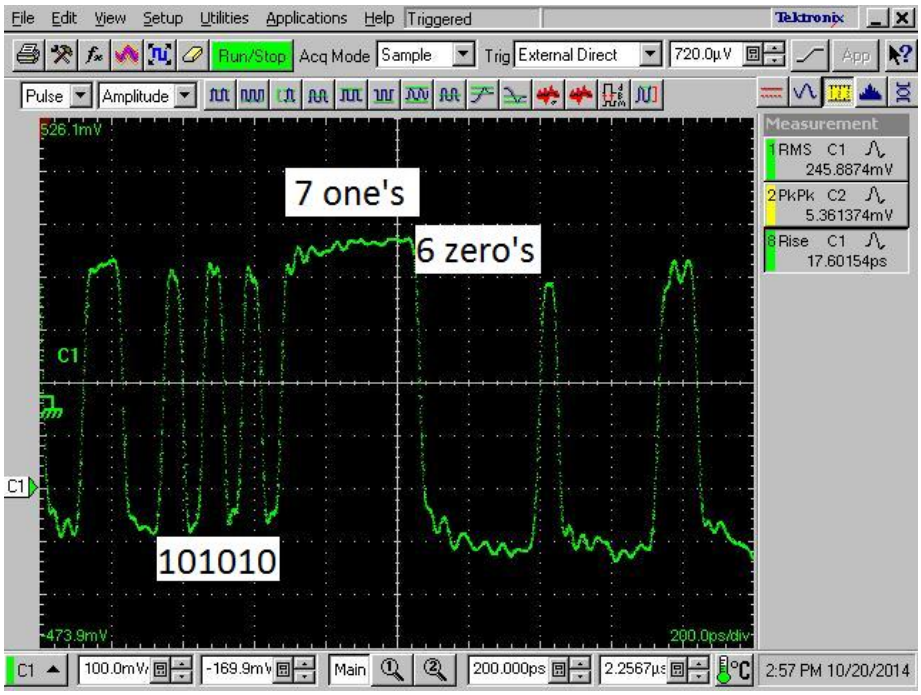

Figure 3. Correct PRBS7 pattern

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Alternatively, an error detector can be used instead of an oscilloscope to aid in adjusting Phase Adjust 1 and Phase Adjust 2 to provide the correct PRBS7 pattern.

11. Set a divide ratio other than 254 or 508 ratio for the Sync Output to view an eye diagram on the oscilloscope.
12. Adjust the two Duty Cycle Adjustment potentiometers to set a desired data output duty cycle.
13. The PRBS Select switch can be changed to PRBS15 and no further calibration will be needed to get the correct PRBS15 pattern.

    Note: If the data rate is changed, most likely all steps 7-12 will need to be repeated.
14. A Clock Divide by 4 output is AC coupled on-board and is available for general purpose use. Note: Terminate any unused outputs with 50*Ohm* loads.

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ELECTRICAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Comments
vee		0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	
I_{VCC}		2.12		*A*	
Power		7		*W*	
Operating Temperature	-25	50	85	*°C*	
Clock Input					
Frequency	2		26	*GHz*	
Single-Ended Swing	100	400	1000	*mV*	Peak-to-Peak
Duty Cycle	40	50	60	*%*	
Clock Divide by 4 Output					
Frequency	0.5		6.5	*GHz*	
Single-Ended Swing		300		*mV*	Peak-to-Peak
Duty Cycle	40	50	60	*%*	
Sync Output					
Frequency	0.0039		13	*GHz*	
Single-Ended Swing		600		*mV*	Peak-to-Peak
Rise/Fall Times	15	17	19	*ps*	20% to 80%
Duty Cycle		50		*%*	
PRBS7/PRBS15 Output					
Data rate	4		52	*Gbps*	
Single-Ended Swing		400		*mV*	Peak-to-Peak
Common Mode Level		3.1		*V*	
Duty Cycle	40	50	60	*%*	Adjustable
Rise/Fall Time	6	8	10	*ps*	20% to 80%

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MEASURED RESULTS

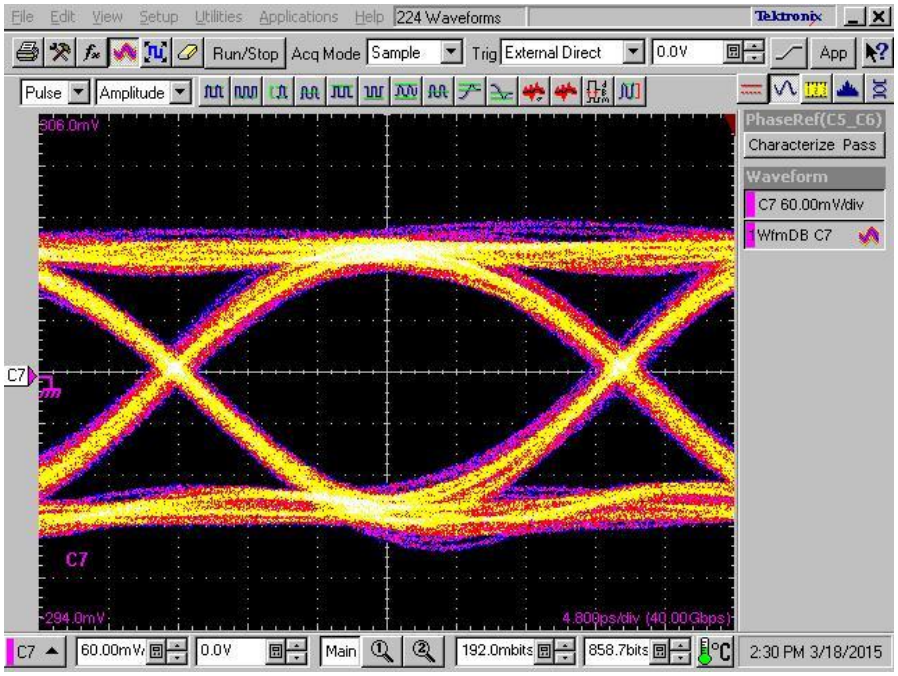

Figure 4. 32Gbps PRBS7 pattern
215fs Random Jitter
2.1ps Data Dependent Jitter

REVISION HISTORY

Revision	Date	Changes
1.2.2	07-2019	Updated Letterhead
1.2.1	04-2019	Added P/N of connectors to board description
1.1.1	04-2015	Updated board picture Added PRBS Select section Updated Operation section Revised Electrical Characteristics table Replaced Output eye section with Measured Results
1.0.1	04-2015	Initial release