CGA-6618

CGA-6618Z

RoHS Compliant & Green Package

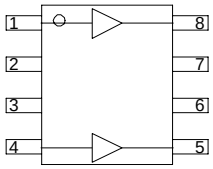
Dual CATV 1 MHz to 1000 MHz High Linearity GaAs HBT Amplifier

Product Description

Sirenza Microdevice's CGA-6618 is a high performance GaAs HBT MMIC Amplifier. Designed with the InGaP process technology for excellent reliability. A Darlington configuration is utilized for broadband performance. The heterojunction increases breakdown voltage and minimizes leakage current between junctions. The CGA-6618 contains two amplifiers for use in wideband Push-Pull CATV amplifiers requiring excellent second order performance. The second and third order non-linearities are greatly improved in the push pull configuration.

The matte tin finish on Sirenza's lead-free package utilizes a post annealing process to mitigate tin whisker formation and is RoHS compliant per EU Directive 2002/95. This package is also manufactured with green molding compounds that contain no antimony trioxide nor halogenated fire retardants.

Amplifier Configuration



Product Features

- **Now available in Lead Free, RoHS Compliant, & Green Packaging**
- **Excellent CSO/CTB/XMOD at +34 dBmV Output Power per Tone**
- **Dual Devices in each SOIC-8 Package simplify Push-Pull configuration PC board layout**
- **ESOP-8 Package**

Applications

- **CATV Head End Driver and Predriver Amplifier**
- **CATV Line Driver Amplifier**

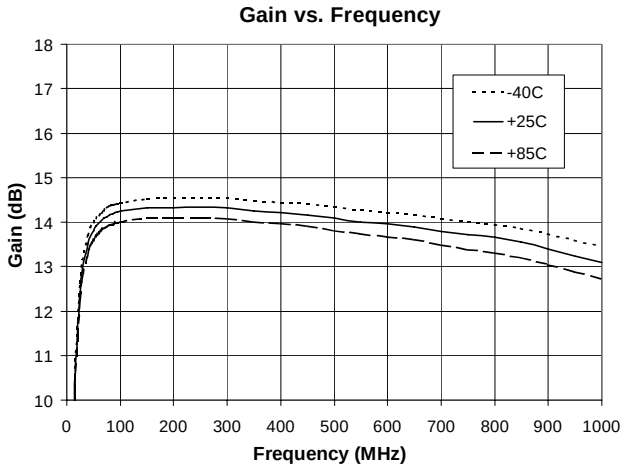
ELECTRICAL SPECIFICATIONS

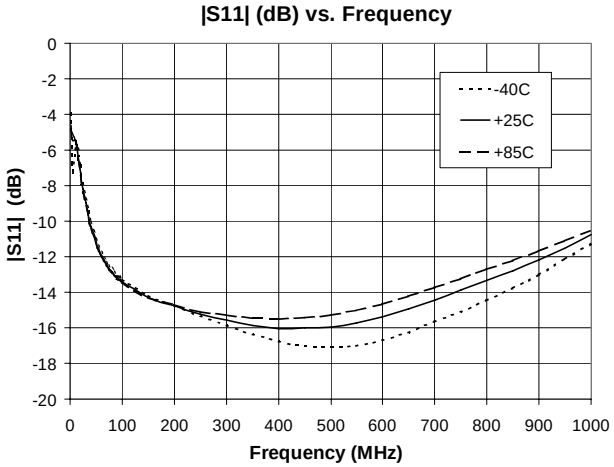
Symbol	Parameter	Freq.(MHz)	Min.	Typ.	Max.	Units
G	Small Signal Gain	50 500 870 1000	 12.4 12.0	13.8 14.1 13.4 13.0	 14.4 14.0	dB
OIP2	Output Second Order Intercept Point Tone Spacing = 1 MHz, Pout per tone = +6 dBm	50 250 500	 70.0	76.5 77.5 72.0		dBm
OIP3	Output Third Order Intercept Point Tone Spacing = 1 MHz, Pout per tone = +6 dBm	50 500 870	 38.0	38.0 39.0 40.0		dBm
P1dB	Output Power at 1dB Gain Compression	50 500 870	 19.5	20.0 21.0 21.5		dBm
IRL	Input Return Loss	500 100-870	 10	15.5		dB
ORL	Output Return Loss	500 100-870	 9.0	12.5		dB
NF	Noise Figure Balun Insertion Loss Included	50 500 870		5.3 5.4 5.6	 6.6	dB
CSO	Worst Case Over Band, 79 Ch., Flat, +34dBmV			81		dBc
CTB	Worst Case Over Band, 79 Ch., Flat, +34dBmV			70		dBc
XMOD	Worst Case Over Band, 79 Ch., Flat, +34dBmV			63		dBc
V_D	Device Operating Voltage		4.8	5.1	5.4	V
I_D	Device Operating Current		144	160	176	mA
$R_{TH(J-L)}$	Thermal Resistance (Junction to Lead)			35		°C/W

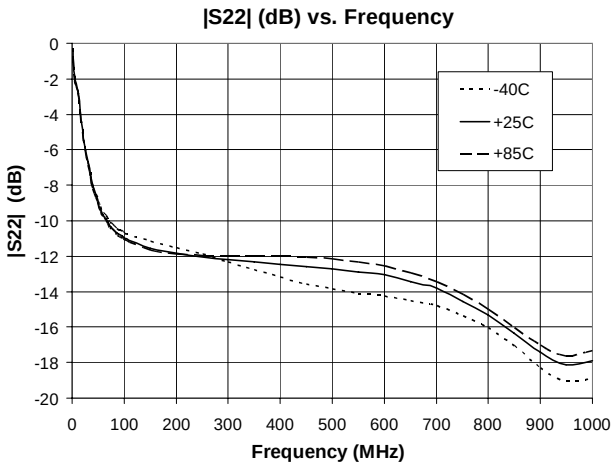
Test Conditions: V_S = 8 V I_D = 160 mA Typ. R_{BIAS} = 33 Ohms T_L = 25ºC $Z_S = Z_L$ = 75 Ohms Push Pull Application Circuit

Absolute Maximum Ratings	Parameter	Absolute Limit
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one. Bias Conditions should also satisfy the following expression: $I_D V_D < (T_J - T_L) / R_{TH, j-l}$	Max. Device Current (I_D)	240 mA
	Max. Device Voltage (V_D)	7 V
	Max. RF Input Power	+20 dBm
	Max. Junction Temp. (T_J)	+150°C
	Operating Temp. Range (T_L)	-40°C to +85°C
	Max. Storage Temp.	+150°C
	Min. Storage Temp.	-65°C

Typical RF Performance: V_S=8V, I_D=160mA @ T_L=+25°C, R_{BIAS}=33 Ohms, Push-Pull Config.



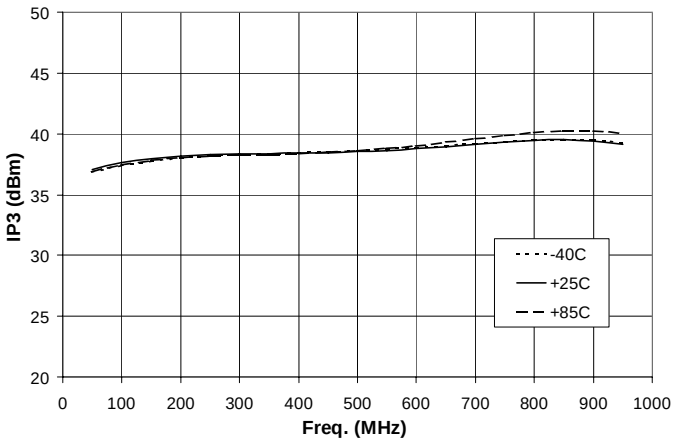




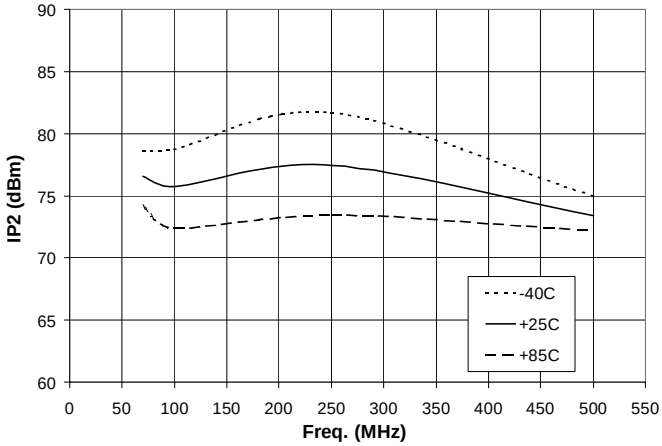
75 Ohm Push Pull S-parameters are available for download at *www.sirenza.com*

Typical RF Performance: V_S=8V, I_D=160mA @ T_L=+25°C, R_{BIAS}=33 Ohms, Push-Pull Config.

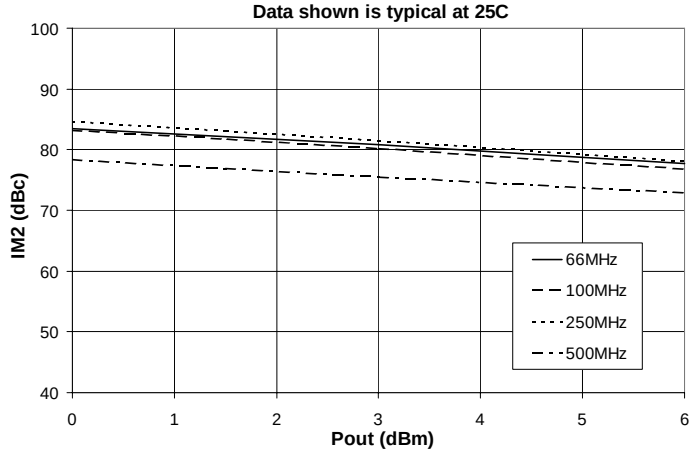
Third Order Intercept Point vs. Frequency over Temperature



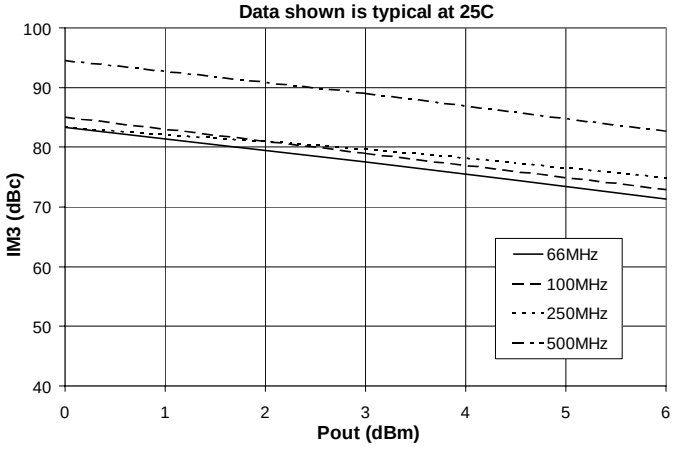
Second Order Intercept Point vs. Frequency over Temperature



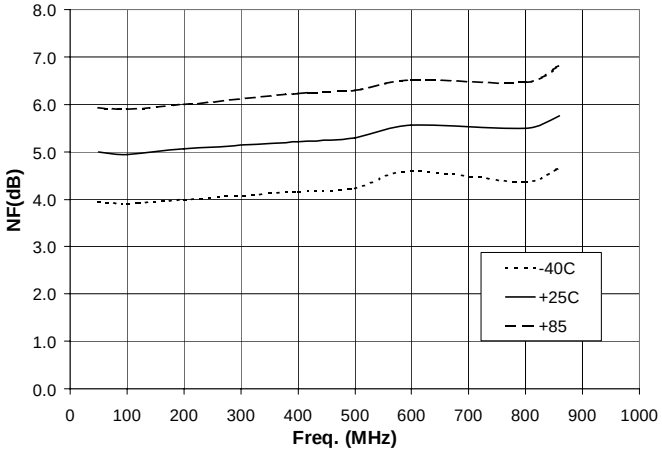
Second Harmonic vs. Pout and Freq.
Data shown is typical at 25C



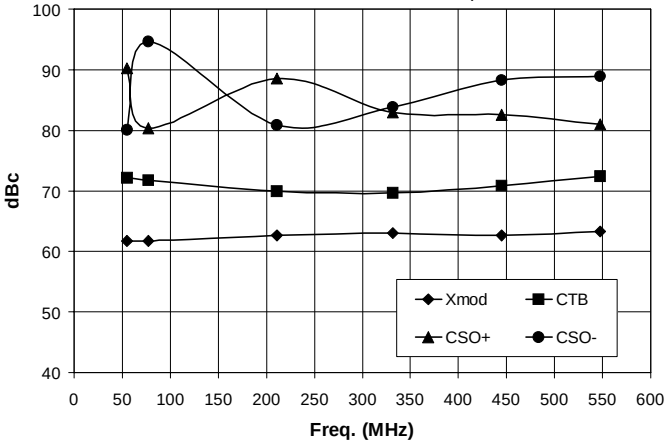
Third Harmonic vs. Pout and Freq.
Data shown is typical at 25C



Noise Figure vs. Frequency Over Temperature

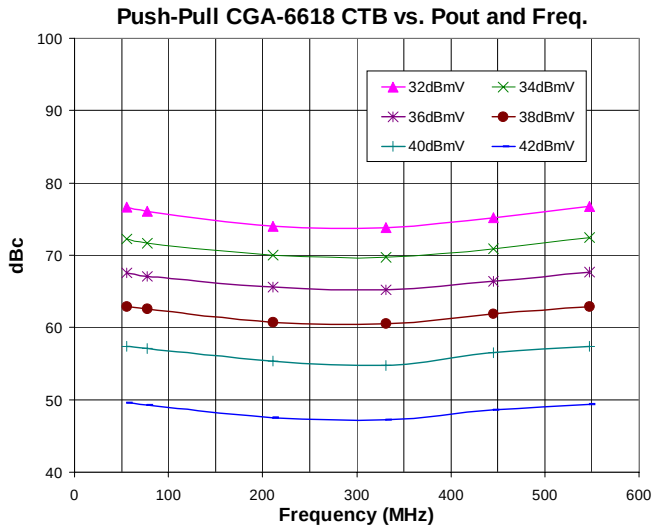


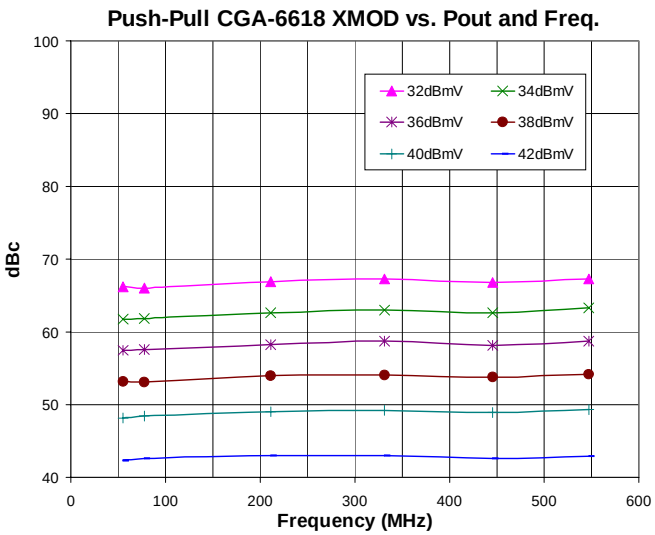
CTB/CSO/XMOD 34dBmV/Chan., Flat

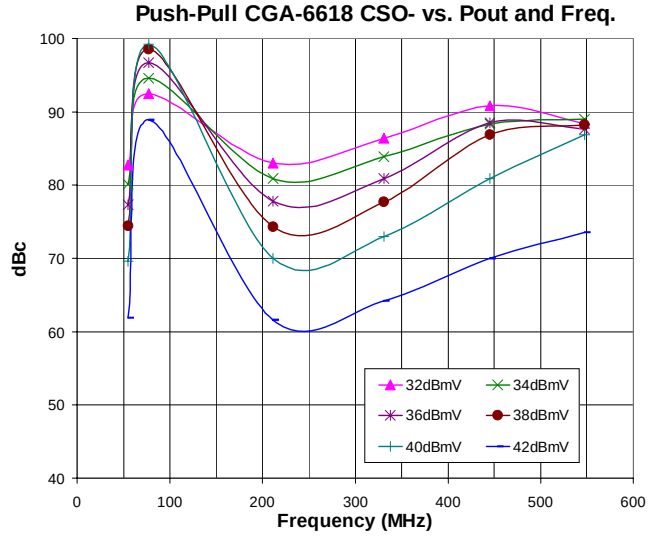


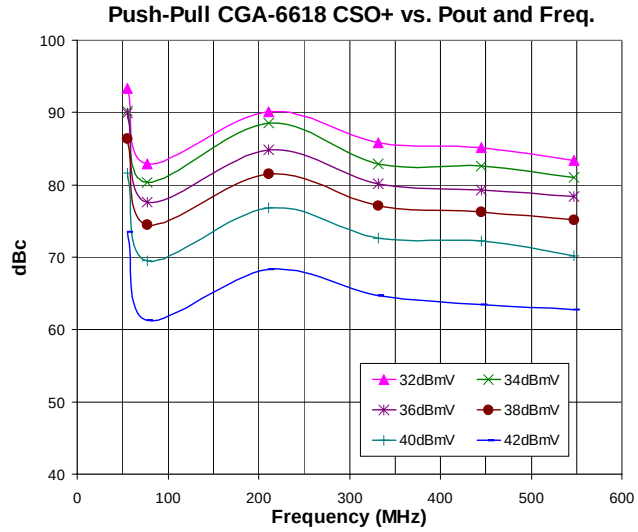
CSO/CTB/XMOD Performance:

V_S=8V, I_D=150mA @ T_L=+25°C, R_{BIAS}=39 Ohms, Push-Pull Config, 79 Ch. Flat Analog, No Digital Channels.





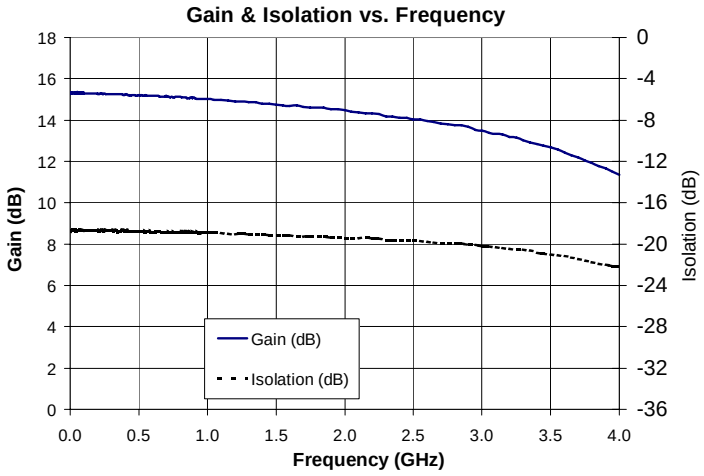


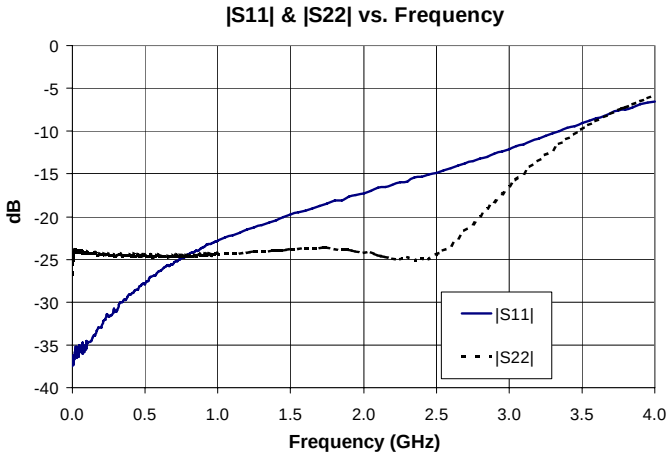


Note: CSO measurements > 85 dBc can be limited by system noise.

Typical RF Performance - Single Ended - 50 Ohm System

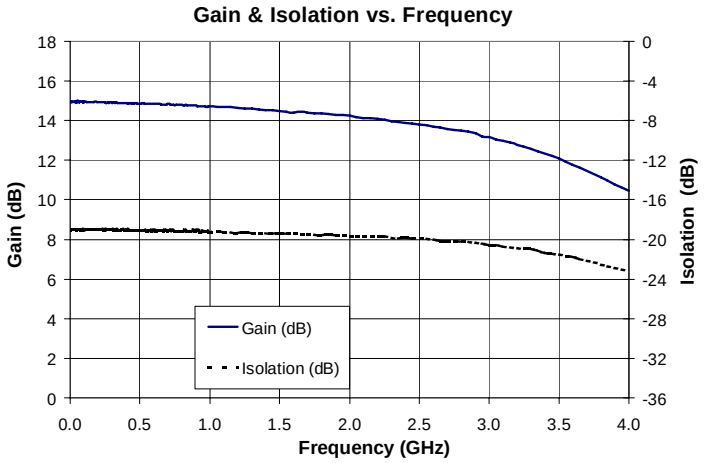
V_S=8V, I_D=80mA (one amp biased), T_L=+25°C, R_{BIAS}=33 Ohms

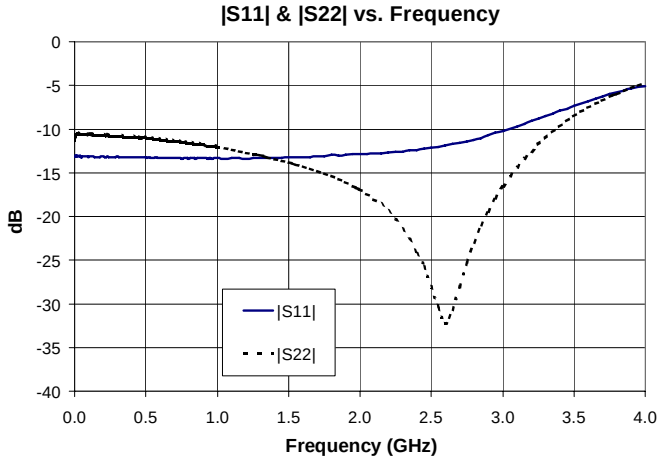




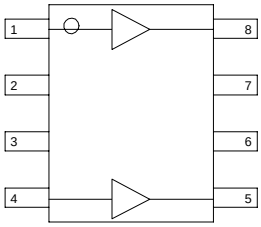
Typical RF Performance - Single Ended - 37.5 Ohm System

V_S=8V, I_D=80mA (one amp biased), T_L=+25°C, R_{BIAS}=33 Ohms

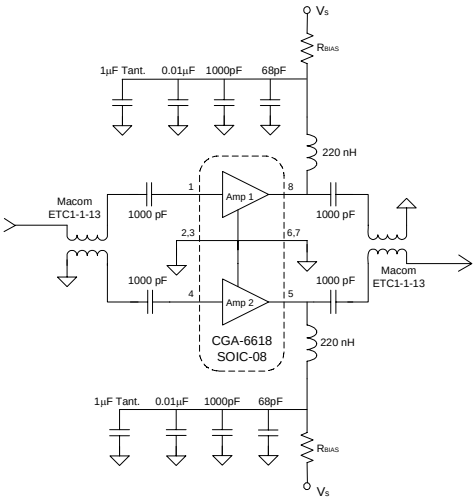




50 Ohm and 37.5 Ohm Single Ended S-parameter files are available for download at *www.sirenza.com*

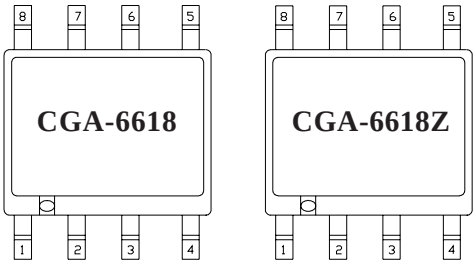
Pin #	Function	Description	Device Pin Out
1	RF IN Device 1	RF input pin. This pin requires the use of an external DC blocking capacitor as shown in the schematic.	
2,3,6,7	Ground	Connection to ground. Use via holes for best performance to reduce lead inductance as close to ground leads as possible.	
4	RF IN Device 2	Same as pin 1	
5	RF OUT / Vcc Device 2	RF output and bias pin. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed.	
8	RF OUT / Vcc Device 1	Same as pin 5	
EPAD	Ground	Exposed area on the bottom side of the package must be soldered to the ground plane of the board for proper thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern on page 5.	

Basic Application Schematic 50-870 MHz

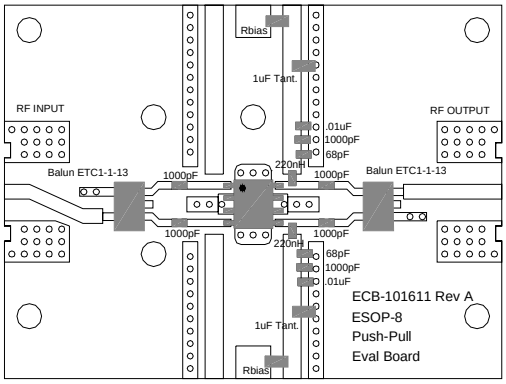


Recommended Bias Resistor Values for I_D=150mA $R_{BIAS}=2\ (V_S-V_D)\ /\ I_D$				
Supply Voltage(V_S)	8 V	9 V	12 V	15 V
R_{BIAS}	33 Ω	47 Ω	82 Ω	120 Ω
Note: R_{BIAS} provides DC bias stability over temperature.				

Part Identification Marking



Evaluation Board Layout 50-870 MHz



PCB Recommendations

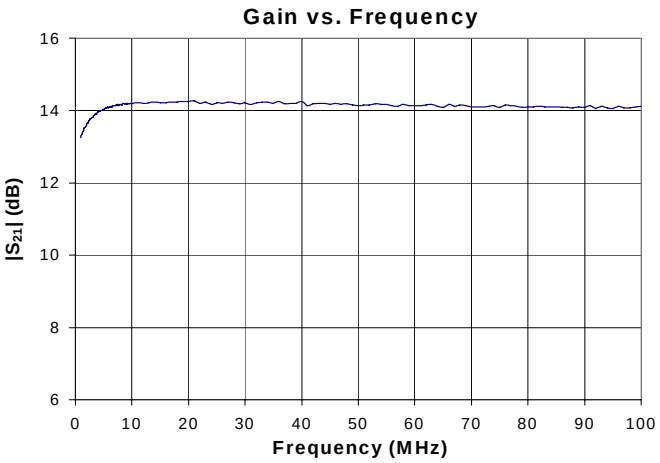
1. Solder the copper pad on the backside of the device package to the ground plane.
2. Use a large ground pad area with many plated through-holes as shown.
3. We recommend 1 or 2 ounce copper. Measurement for this data sheet were made on a 31 mil thick FR-4 board with 1 ounce copper on both sides.

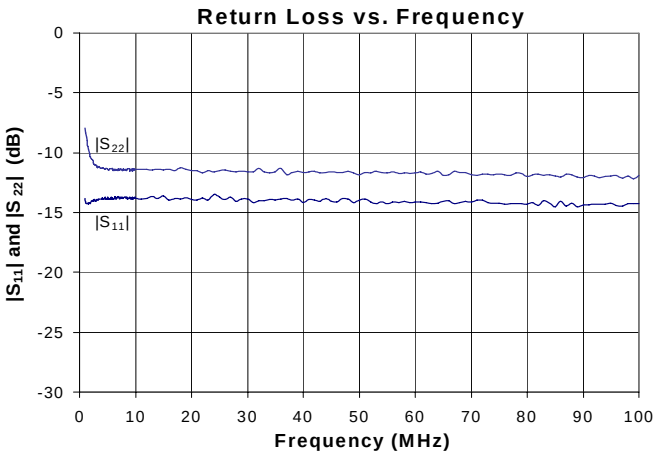
Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

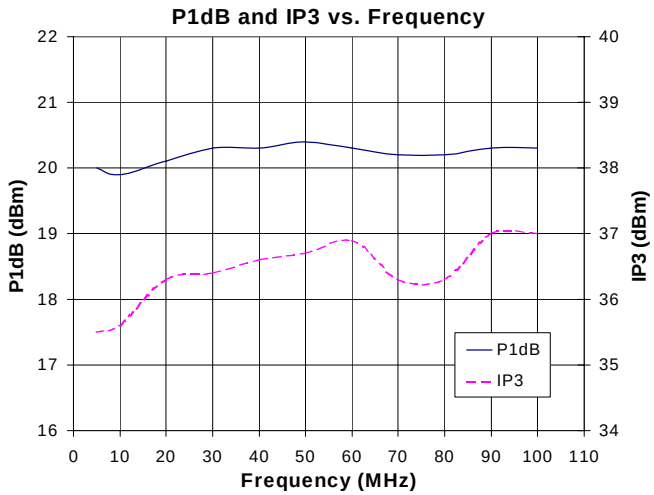
Part Number Ordering Information

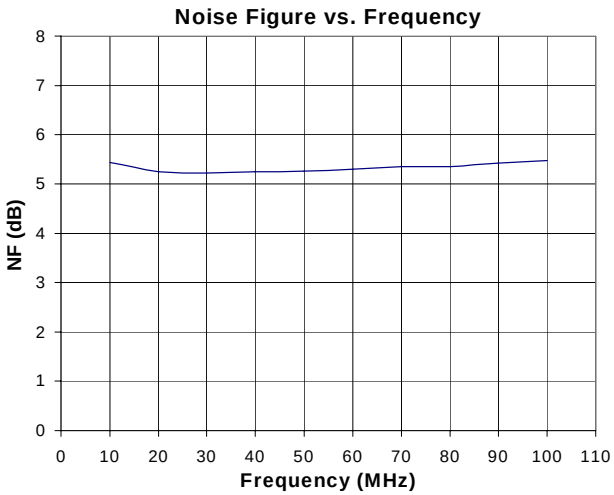
Part Number	Reel Size	Devices/Reel
CGA-6618	7"	500
CGA-6618Z	7"	500

5 - 100 MHz Application Circuit: V_S=8V, I_D=160mA @ T_L=+25°C, Push-Pull Config.

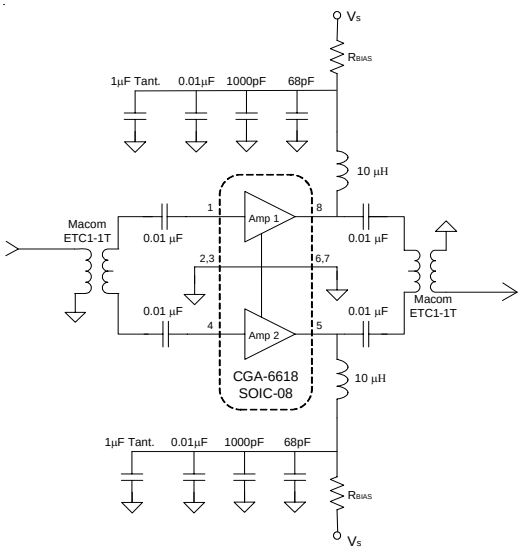




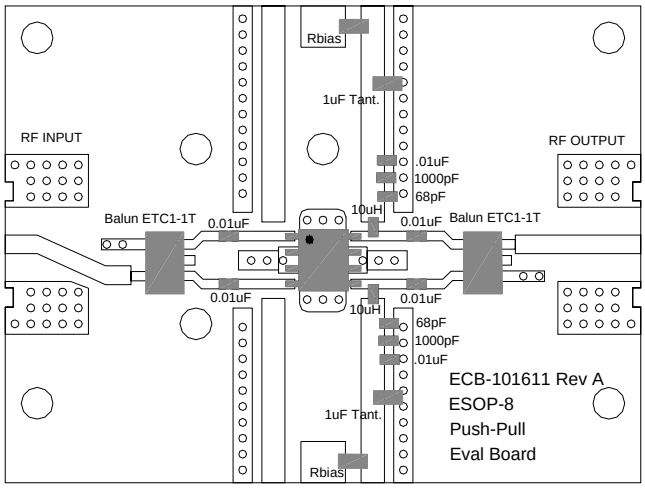




5-100 MHz Application Schematic

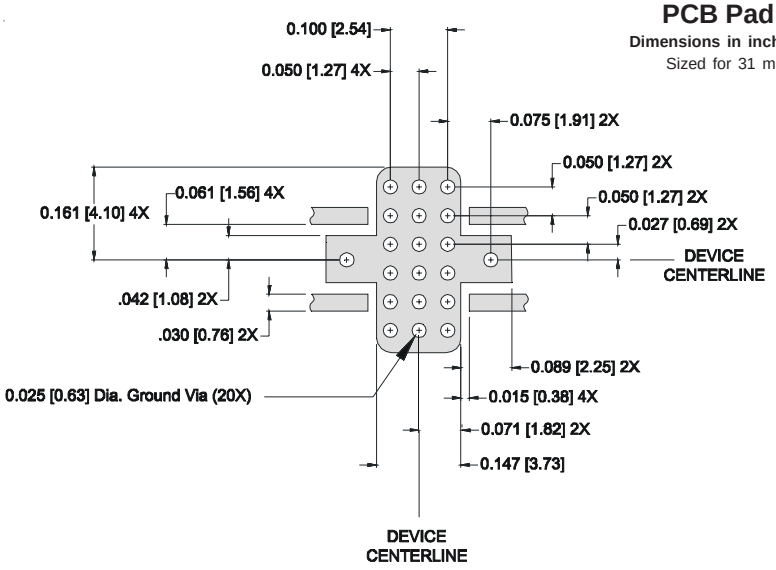


5-100 MHz Evaluation Board Layout



PCB Pad Layout

Dimensions in inches [millimeters]
Sized for 31 mil thick FR-4



Nominal Package Dimensions & Package Marking

Dimensions in inches [millimeters]
Refer to package drawing posted at *www.sirenza.com* for tolerances.

PACKAGE TYPE:
ESOP-8