

# LI5040SA

2/3 inch Diagonal 5.33MP CMOS Sensor on 180pin LGA with 3.4µm Square Pixels at 120fps.

## DESCRIPTION

LI5040SA is a CMOS type of solid-state image sensor with a 2/3 inch effective pixel array of 5.33M pixels. It uses a global shutter feature as a charge storage period control.

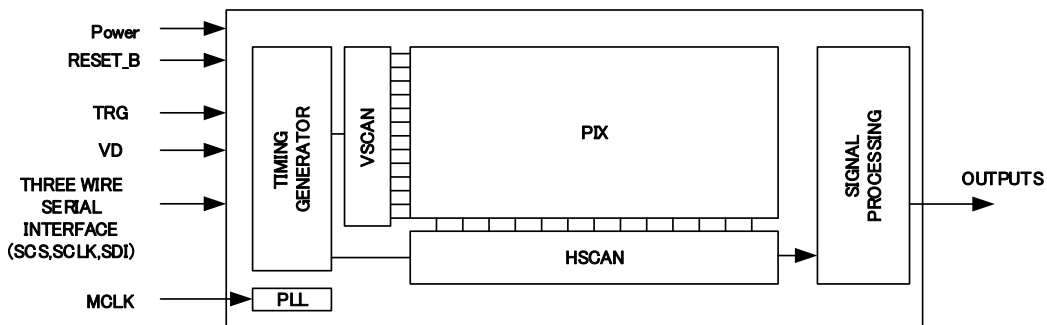
It can output an effective 2592 x 2056 pixels of video at 120 fps and 12bit via 12 channels of digital signal output.

\*LI5040SA series consists of LI5040SAC (color), LI5040SAM (monochrome) and LI5040SAI (RGBIR).

## FEATURES

- LI5040SAM: Monochrome sensor
- LI5040SAC: Color sensor (RGB on-chip color filter)
- LI5040SAI: RGBIR sensor (RGB IR on-chip color filter)
- Global shutter / Progressive scan
- Recording screen size: 2/3 inch equivalent (8.8 mm x 7.0 mm)
- Number of effective pixels: 2592 x 2056 (Horizontal x Vertical)
- Pixel size: 3.4 µm x 3.4 µm
- Number of output channels Data: 12 lanes, Clock: 2 lanes
- Main clock frequency: 36 MHz (recommended)
- Output format: LVDS output maximum 864 Mbps @12 bit
- Analog gain: 0 to 36 dB
- Digital gain: 0 to 24 dB
- Maximum of 8 areas (horizontal 8, vertical 8) of optional segmentation (ROI: Region Of Interest) feature
- Horizontal and vertical inverted output feature
- External trigger exposure control feature (Overlap trigger feature)
- Sensitivity (Green) of LI5040SAC: 30,000 e/lx/sec @Analog gain x1
- Sensitivity (Green) of LI5040SAI: 30,000 e/lx/sec @Analog gain x1
- Sensitivity of LI5040SAM: 54,000 e/lx/sec @Analog gain x1
- Saturation: 12,000 e @Analog gain x1, 60fps, Dynamic Range Priority Mode
- Saturation: 7,000 e @Analog gain x1, 120fps, Frame Rate Priority Mode
- Dark random noise: 2.6 e rms @Analog gain x1
- Dark current: 1.3 e/sec @Analog gain x1, room temperature
- Power consumption: 510 mW(Typ.) @using all pixels 120 fps
- Power consumption: 440 mW(Typ.) @using all pixels 42 fps
- Power supply voltages: 3.3 V, 1.2 V
- 180 pin ceramic LGA
- Package size: 18.96mm x 18.10mm x 2.51mm

## FUNCTIONAL BLOCK DIAGRAM



### 3. Pixel Arrangement

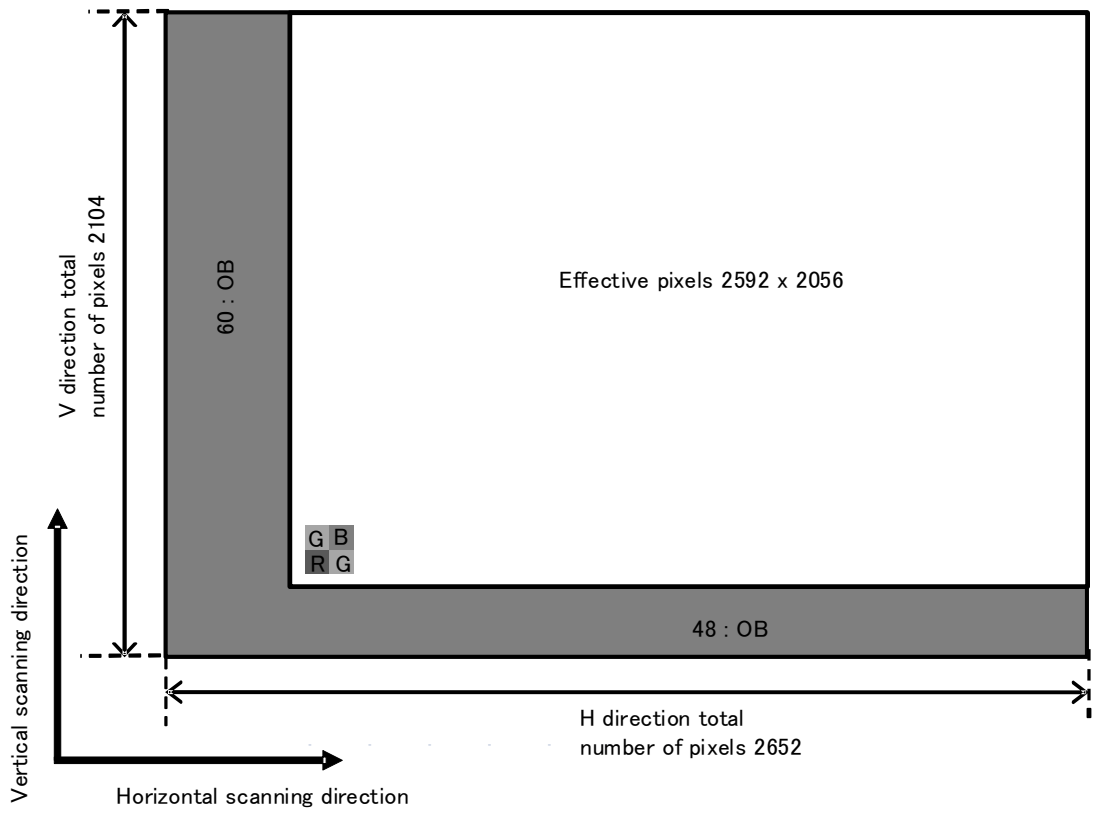


Figure 3-1. Pixel Data Format (Physical Arrangement)

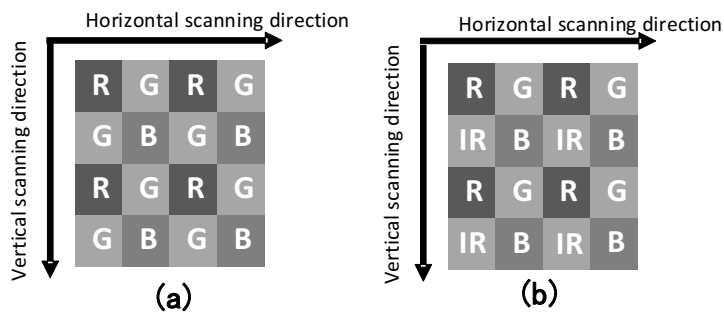


Figure 3-2. Pixel Color Filter Arrangement

\* Figure 3-2 (a) is color sensor (LI5040SAC) pixel pattern .  
Color filters are not installed in Monochrome sensor (LI5040SAM).  
Figure 3-2(b) is RGBIR sensor(LI5040SAI) pixel pattern.

## 4. Pin Specifications

Table 4-1. Pin Specifications 1

| Pin No. | Pin Name | Type | Content                                 | Remarks  |
|---------|----------|------|---|--|
| tA1     | DGND     | G    | Digital GND                             | -  |
| tA2     | DVDD     | P    | 1.2 V digital power supply              | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| tB1     | (NC)     | -    | -                                       | -  |
| tA3     | (NC)     | -    | -                                       | -  |
| tB2     | (NC)     | -    | -                                       | -  |
| tC1     | (NC)     | -    | -                                       | -  |
| tB3     | (NC)     | -    | -                                       | -  |
| tC2     | (NC)     | -    | -                                       | -  |
| tD1     | AGND1    | G    | Analog GND                              | -  |
| tC3     | SGND     | G    | Sensor GND                              | -  |
| tD2     | SVDD     | P    | 3.3 V sensor power supply               | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to SGND |
| tE1     | AVDDH1   | P    | 3.3 V analog power supply               | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to AGND |
| tD3     | (NC)     | -    | -                                       | -  |
| tE2     | VD       | I    | Digital signal (VD) input               | Logic input  |
| tF1     | CLK      | I    | Digital signal (Main CLK) input         | Logic input  |
| tE3     | TRG      | I    | Digital signal (external trigger) input | Logic input  |
| tF2     | DGND     | G    | Digital GND                             | -  |
| tG1     | DVDD     | P    | 1.2 V digital power supply              | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| tF3     | RESET_B  | I    | Digital signal (reset) input            | Asynchronous, Low active                                       |
| tG2     | TESTSIG1 | O    | Digital monitor output                  | Open. Connect to check pin if necessary                        |
| tH1     | (NC)     | -    | -                                       | -  |
| tG3     | (NC)     | -    | -                                       | -  |
| tH2     | AVDDH1   | P    | 3.3 V analog power supply               | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to AGND |
| tI1     | SVDD     | P    | 3.3 V sensor power supply               | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to SGND |
| tH3     | SGND     | G    | Sensor GND                              | -  |
| tI2     | AGND1    | G    | Analog GND                              | -  |
| tJ1     | AIN1_1   | I    | External signal input terminal          | AGND short circuit through 0 $\Omega$                          |
| tI3     | AIN1_2   | I    | External signal input terminal          | AGND short circuit through 0 $\Omega$                          |
| tJ2     | (NC)     | -    | -                                       | -  |
| tK1     | DVDD     | P    | 1.2 V digital power supply              | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| tJ3     | DGND     | G    | Digital GND                             | -  |
| tK2     | DVDDH    | P    | 3.3 V digital power supply              | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| tL1     | SGND     | G    | Sensor GND                              | -  |
| tK3     | DVDD     | P    | 1.2 V digital power supply              | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| tL2     | DGND     | G    | Digital GND                             | -  |

Type G: Ground, P: Power, I: Input, O: Output

Table 4-2. Pin Specifications 2

| Pin No. | Pin Name | Type | Content  | Remarks  |
|---------|----------|------|--|--|
| Gt1     | (NC)     | -    | -  | -  |
| Ht2     | (NC)     | -    | -  | -  |
| Ft1     | AOUT1    | O    | Analog Output                                  | Open   |
| Gt2     | AOUT2    | O    | Analog Output                                  | Open   |
| Ht3     | (NC)     | -    | -  | -  |
| Ft2     | (NC)     | -    | -  | -  |
| Gt3     | VINT01   | I/O  | Built-in power supply monitor / external input | 4.7 uF±10% relative to AGND                    |
| Ht4     | VINT02   | I/O  | Built-in power supply monitor / external input | 4.7 uF±10% relative to AGND                    |
| Ft3     | VINT03   | I/O  | Built-in power supply monitor / external input | 4.7 uF±10% relative to AGND                    |
| Gt4     | AVDDH2   | P    | 3.3 V analog power supply                      | Capacity 0.1 μF, 10 μF (±10%) relative to AGND |
| Ht5     | VINT04   | I/O  | Built-in power supply capacitance connection   | 10 uF±10% relative to AGND                     |
| Ft4     | VINT05   | I/O  | Built-in power supply capacitance connection   | 10 uF±10% relative to AGND                     |
| Gt5     | VINT06   | I/O  | Built-in power supply capacitance connection   | 4.7 uF±10% relative to AGND                    |
| Ht6     | AGND2    | G    | Analog GND                                     | -  |
| Ft5     | AGND2    | G    | Analog GND                                     | -  |
| Gt6     | AVDDH2   | P    | 3.3 V analog power supply                      | Capacity 0.1 μF, 10 μF (±10%) relative to AGND |
| Ht7     | RREF1    | I/O  | Ramp reference resistance connection           | 1 kΩ±1%, shielded by AGND                      |
| Ft6     | CR1      | I/O  | Ramp capacitance connection                    | 1000 pF±1% relative to AGND                    |
| Gt7     | CR2      | I/O  | Ramp capacitance connection                    | 1000 pF±1% relative to AGND                    |
| Ht8     | AGND2    | G    | Analog GND                                     | -  |
| Ft7     | VINT07   | I/O  | Built-in power supply capacitance connection   | 4.7 uF±10% relative to AGND                    |
| Gt8     | VINT08   | I/O  | Built-in power supply capacitance connection   | 10 uF±10% relative to AGND                     |
| Ht9     | VINT09   | I/O  | Built-in power supply capacitance connection   | 10 uF±10% relative to AGND                     |
| Ft8     | VINT10   | I/O  | Built-in power supply monitor / external input | 4.7 uF±10% relative to AGND                    |
| Gt9     | AVDDH2   | P    | 3.3 V analog power supply                      | Capacity 0.1 μF, 10 μF (±10%) relative to AGND |
| Ht10    | AGND2    | G    | Analog GND                                     | -  |
| Ft9     | RREF2    | I/O  | Current reference resistance connection        | 7.5 kΩ±1% relative to AGND, shielded by AGND   |
| Gt10    | AVDDH2   | P    | 3.3 V analog power supply                      | Capacity 0.1 μF, 10 μF (±10%) relative to AGND |
| Ht11    | (NC)     | -    | -  | -  |
| Ft10    | (NC)     | -    | -  | -  |
| Gt11    | AOUT4    | O    | Analog Output                                  | Open   |
| Ht12    | AOUT3    | O    | Analog Output                                  | Open   |
| Ft11    | (NC)     | -    | -  | -  |
| Gt12    | (NC)     | -    | -  | -  |

Type G: Ground, P: Power, I: Input, O: Output

Table 4-3. Pin Specifications 3

| Pin No. | Pin Name | Type | Content   | Remarks  |
|---------|----------|------|---|--|
| tM8     | DGND     | G    | Digital GND                                     | -  |
| tL7     | DVDD     | P    | 1.2 V digital power supply                      | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| tL8     | SGND     | G    | Sensor GND                                      | -  |
| tK6     | DVDDH    | P    | 3.3 V digital power supply                      | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| tK7     | DGND     | G    | Digital GND                                     | -  |
| tK8     | DVDD     | P    | 1.2 V digital power supply                      | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| tJ6     | (NC)     | -    | -   | -  |
| tJ7     | AIN2_2   | I    | External signal input terminal (for evaluation) | AGND short circuit through 0 $\Omega$                          |
| tJ8     | AIN2_1   | I    | External signal input terminal (for evaluation) | AGND short circuit through 0 $\Omega$                          |
| tI6     | AGND1    | G    | Analog GND                                      | -  |
| tI7     | SGND     | G    | Sensor GND                                      | -  |
| tI8     | SVDD     | P    | 3.3 V sensor power supply                       | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to SGND |
| tH6     | AVDDH1   | P    | 3.3 V analog power supply                       | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to AGND |
| tH7     | (NC)     | -    | -   | -  |
| tH8     | (NC)     | -    | -   | -  |
| tG6     | TESTSIG2 | O    | Digital monitor output                          | Open. Connect to check pin if necessary                        |
| tG7     | SCANTEST | I    | Scan test input                                 | DGND short circuit through 0 $\Omega$                          |
| tG8     | DVDD     | P    | 1.2 V digital power supply                      | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| tF6     | DGND     | G    | Digital GND                                     | -  |
| tF7     | SCS      | I    | Digital signal (3-wire serial) input            | -  |
| tF8     | SDI      | I    | Digital signal (3-wire serial) input            | -  |
| tE6     | SCLK     | I    | Digital signal (3-wire serial) input            | -  |
| tE7     | (NC)     | -    | -   | -  |
| tE8     | AVDDH1   | P    | 3.3 V analog power supply                       | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to AGND |
| tD6     | SVDD     | P    | 3.3 V sensor power supply                       | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to SGND |
| tD7     | SGND     | G    | Sensor GND                                      | -  |
| tD8     | AGND1    | G    | Analog GND                                      | -  |
| tC6     | (NC)     | -    | -   | -  |
| tC7     | (NC)     | -    | -   | -  |
| tC8     | (NC)     | -    | -   | -  |
| tB6     | (NC)     | -    | -   | -  |
| tB7     | (NC)     | -    | -   | -  |
| tB8     | (NC)     | -    | -   | -  |
| tA6     | DVDD     | P    | 1.2 V digital power supply                      | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| tA7     | DGND     | G    | Digital GND                                     | -  |

Type G: Ground, P: Power, I: Input, O: Output

Table 4-4. Pin Specifications 4

| Pin No. | Pin Name | Type | Content                    | Remarks  |
|---------|----------|------|----------------------------|--|
| Bt12    | DGND     | G    | Digital GND                | -  |
| At12    | DVDD     | P    | 1.2 V digital power supply | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| Ct11    | D33N     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| Bt11    | D33P     | O    | LVDS data output           |  |
| At11    | D32N     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| Ct10    | D32P     | O    | LVDS data output           |  |
| Bt10    | D31N     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| At10    | D31P     | O    | LVDS data output           |  |
| Ct9     | LVCK2N   | O    | LVDS clock output          | 100 $\Omega$ terminal  |
| Bt9     | LVCK2P   | O    | LVDS clock output          |  |
| At9     | D41N     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| Ct8     | D41P     | O    | LVDS data output           |  |
| Bt8     | D42N     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| At8     | D42P     | O    | LVDS data output           |  |
| Ct7     | D43N     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| Bt7     | D43P     | O    | LVDS data output           |  |
| At7     | DVDD     | P    | 1.2 V digital power supply | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| Ct6     | DGND     | G    | Digital GND                | -  |
| Bt6     | D23P     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| At6     | D23N     | O    | LVDS data output           |  |
| Ct5     | D22P     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| Bt5     | D22N     | O    | LVDS data output           |  |
| At5     | D21P     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| Ct4     | D21N     | O    | LVDS data output           |  |
| Bt4     | LVCK1P   | O    | LVDS clock output          | 100 $\Omega$ terminal  |
| At4     | LVCK1N   | O    | LVDS clock output          |  |
| Ct3     | D11P     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| Bt3     | D11N     | O    | LVDS data output           |  |
| At3     | D12P     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| Ct2     | D12N     | O    | LVDS data output           |  |
| Bt2     | D13P     | O    | LVDS data output           | 100 $\Omega$ terminal  |
| At2     | D13N     | O    | LVDS data output           |  |
| Ct1     | DVDD     | P    | 1.2 V digital power supply | Capacity 0.1 $\mu$ F, 10 $\mu$ F ( $\pm$ 10%) relative to DGND |
| Bt1     | DGND     | G    | Digital GND                | -  |

Type G: Ground, P: Power, I: Input, O: Output

\* Be sure to consider ESD when making system designs. Especially, Pin No. Ht5, Ft4, Gt5.

## 7. Absolute Maximum Ratings

**Table 7-1. Absolute Maximum Ratings**

| Item                         | Symbol                 | Min.     | Max.       | Unit | Notes                                 |
|------------------------------|------------------------|----------|------------|------|---------------------------------------|
| Power supply voltage 1.2 V   | DVDD                   | -        | 1.44       | V    | -                                     |
| Power Supply voltage 3.3V    | AVDDH<br>DVDDH<br>SVDD | -        | 3.9        |      | -                                     |
| Input voltage                | Digital Input          | GND -0.3 | DVDDH +0.3 |      | Do not exceed 3.9V                    |
| Output voltage 1.2V          | Digital Output         | GND -0.3 | DVDD       |      | Do not exceed 1.44V                   |
| Storage Temperature          | T <sub>str</sub>       | -30      | 105        | °C   | T <sub>a</sub> : ambient temperature  |
| Maximum Junction Temperature | T <sub>jmax</sub>      | -        | 100        | °C   | T <sub>j</sub> : Junction Temperature |

## 8. Recommended Operating Temperature

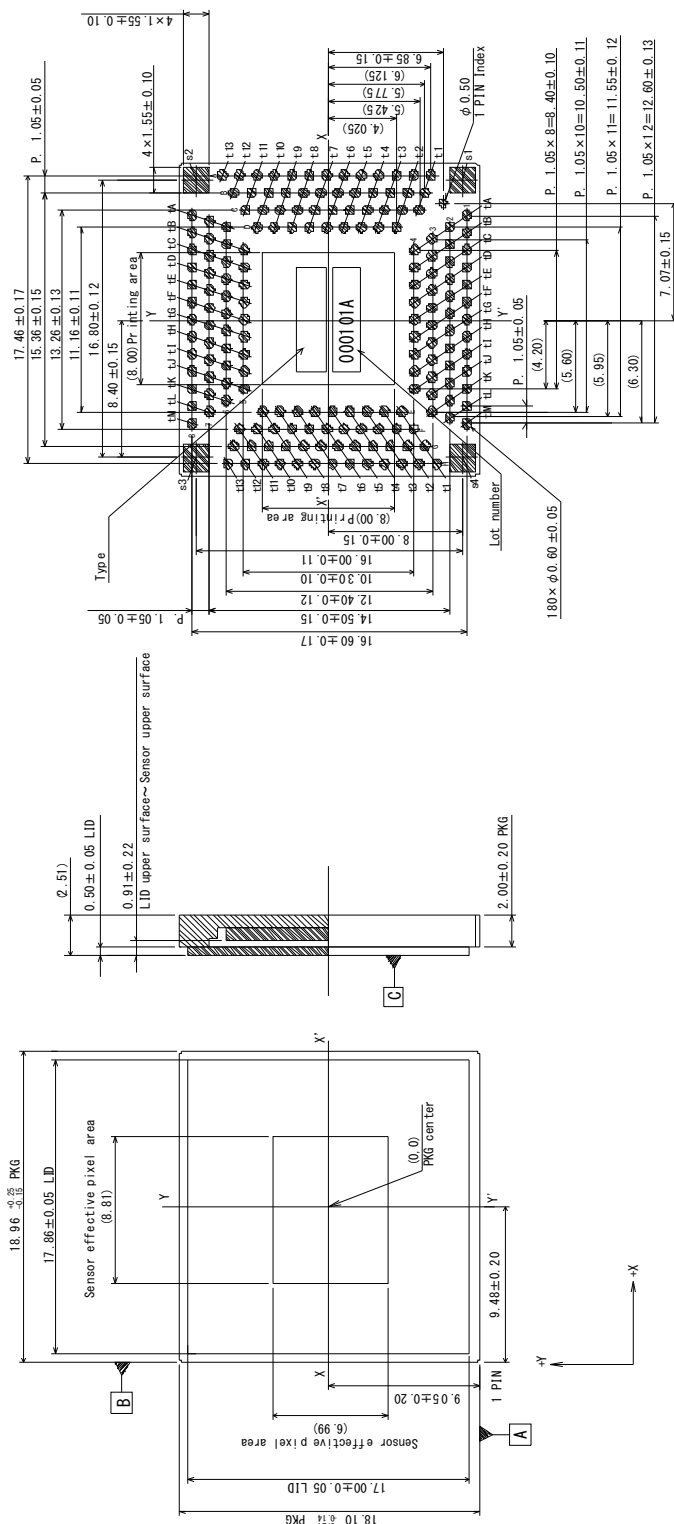
**Table 8-1. Recommended Operating Temperature**

| Item                  | Symbol    | Min. | Typ. | Max. | Unit | Notes                    |
|-----------------------|-----------|------|------|------|------|--------------------------|
| Operating Temperature | $T_{opr}$ | -20  | -    | 80   | °C   | Tj: Junction Temperature |

Typ.: Typical



# 15. Package Specification



Note

- 1) The PKG center (0.0) and the deviation of the effective pixel center (X, Y) = (-250μm, -13.6μm).
- 2) A, B and C indicate the reference plane.
- 3) Using the PKG center as a reference, the actual effective pixel area fits within the outer range of the relative position of the effective pixel area design +0.30mm. However, the rotational deviation is ±0.5° or less.
- 4) LID mounting accuracy: using the PKG center as a reference, X, Y ± 0.30mm.
- 5) Sensor effective pixel surface bending: 25μm or less.
- 6) Tilt between the sensor effective pixel surface and LID upper surface: 100μm or less.
- 7) LGA terminal plating process: electrolytic Au plating / electrolytic Ni plating.
- 8) PKG: multilayer ceramic LGA (LGA terminal: 180 pin + 4 pin reinforcement terminal = 184 pin).
- 9) LID material: glass (no AR coat).
- 10) PKG back surface LGA terminal coplanarity (including the reinforcement terminal): 0.10 mm or less.
- 11) The standard for resin extrusion of the PKG exterior is set as the PKG maximum external shape tolerance +0.2 mm.
- 12) All dimensions are in millimeters.

Figure 15-1. Package Specification