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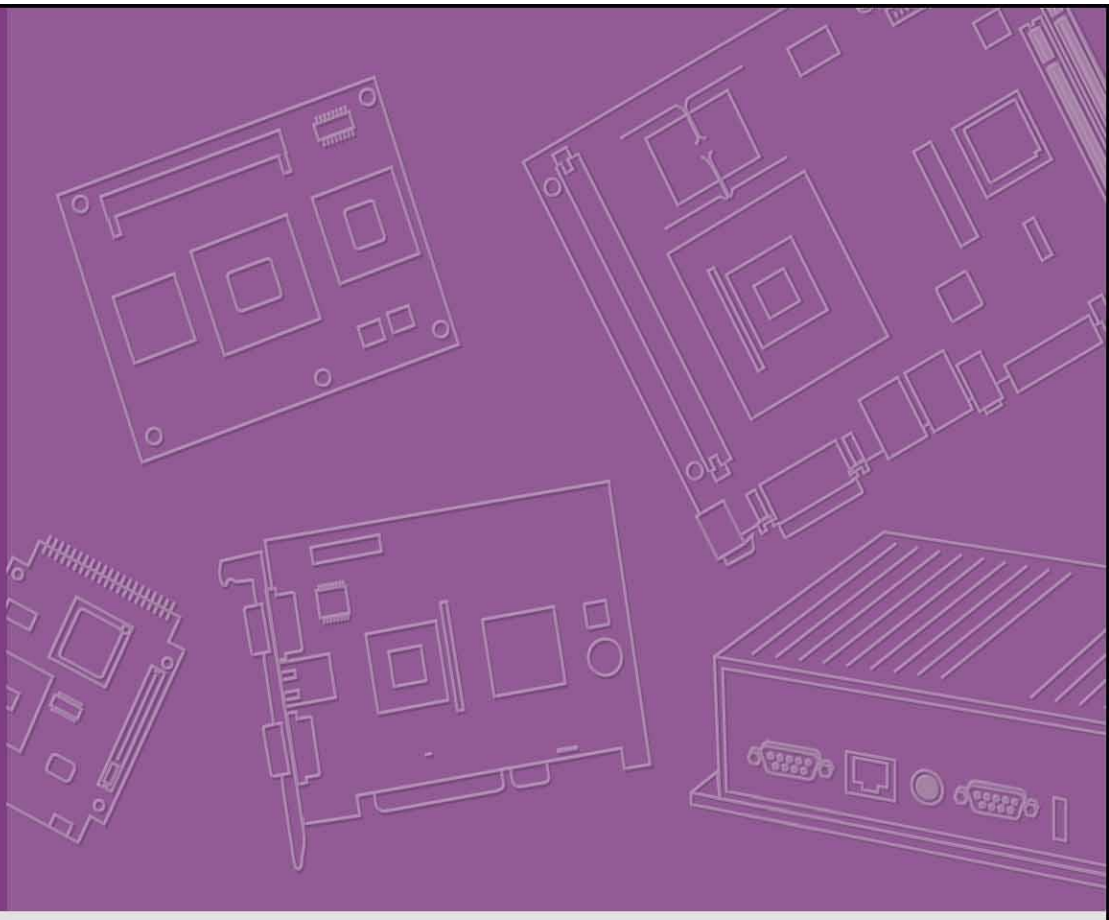

CarrierBoard Design Guide

QSEVEN

SOM-3567

R101 2018’05’03

ADVANTECH

Enabling an Intelligent Planet

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1. Introduction

1.1 About This Document

This document provides information for designing a custom system carrier board for Qseven® modules. It includes Signal Descriptions, Routing Guidelines and Trace Length Guidelines. The main purpose is designing Carrier Board for helping customers fast and easy using the module of Advantech to be designed.

1.2 Signal Table Terminology

Table 1 below describes the terminology used in this section for the Signal Description tables.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

The terms "Input" and "Output" and their abbreviations in Table 1 below refer to the Module's view, i.e. an input is an input for the Module and not for the Carrier-Board.

1.3 Terminology

Table 1: Conventions and Terminology

Terminology	*Description*
X86	The term x86 refers to a family of instruction set architectures based on the Intel 8086.
PCI Express (PCIe)	Peripheral Component Interface Express. Next-generation high speed serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for

	Receiver. Clocking information is embedded into the data stream.
x1, x2, x4	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4 link.
DDC	Display Data Channel is an I2C bus interface between a display and a graphics adapter.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
GBE	Gigabit Ethernet
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial interface standard for hard disks.
HDA	High Definition Audio
I2S	Integrated Interchip Sound (I2S) is an electrical serial bus interface standard used for connecting digital audio devices together.
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
DP eDP	(embedded) DisplayPort (DP/eDP) is a digital display interface developed by the Video Electronics Standards Association (VESA).
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
CAN	Controller Area Network
SPI	Serial Peripheral Interface
SDIO	Secure Digital Input Output
SMB	System Management Bus
LVDS	Low-Voltage Differential Signaling
ACPI	Advanced Control Programmable Interface
RoHS	Restriction on Hazardous Substances: The Directive on the Restriction of the Use of Certain Hazardous Substances in

	Electrical and Electronic Equipment 2002/95/EC.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined
EDID	Extended Display Identification Data
EDP	Embedded DisplayPort (eDP) is a digital display interface standard produced by the Video Electronics Standards Association (VESA) for digital interconnect of Audio and Video.
EEPROM	Electrically Erasable Programmable Read-Only Memory
EFT	Electrical Fast Transient
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ExpressCard	A PCMCIA standard built on the latest USB 2.0 and PCI Express buses.
FR4	A type of fiber-glass laminate commonly used for printed circuit boards.
GPI	General Purpose Input
GPIO	General Purpose Input Output
GPO	General Purpose Output
DE	Integrated Device Electronics – parallel interface for hard disk drives – also known as PATA
Legacy Device	Relics from the PC-AT computer that are not in use in contemporary PC systems: primarily the ISA bus, UART-based serial ports, parallel printer ports, PS-2 keyboards, and mice. Definitions vary as to what constitutes a legacy device. Some definitions include IDE as a legacy device.
LS	Least Significant
PCB	Printed Circuit Board
PD	Pull Down
PP	Push Pull
I	Input Pin
O	Output Pin
OD	Open Drain
P	Power Pin
PHY	Ethernet controller physical layer device
PEG	PCI Express Graphics
PS2	“Personal System 2” - an IBM trademark term used to refer to

PS2 Keyboard PS2 Mouse	Intel x86 based personal computers in the 1990s. The term survives as a reference to the style of mouse and keyboard interface that were introduced with the PS2 system.
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and dateas well as certain system setup parameters
S0, S1, S2, S3, S4, S5	Sleep States defined by the ACPI specificationS0 Full power, all devices powered S1Sleep State, all context maintained S2 Sleep State, CPU and Cache context lost S3 Suspend to RAM System context stored in RAM; RAM is in standby S4 Suspend to Disk System context stored on disk S5 Soft Off Main power rail off, only standby power rail present
TMDS	Transition Minimized Differential Signaling - a digital signaling protocol between the graphics subsystem and display. TMDS is used for the DVI digital signals. DC coupled
TPM	Trusted Platform Module, chip to enhance the security features of a computer system.
VESA	Video Electronics Standards Association
WDT	Watch Dog Timer

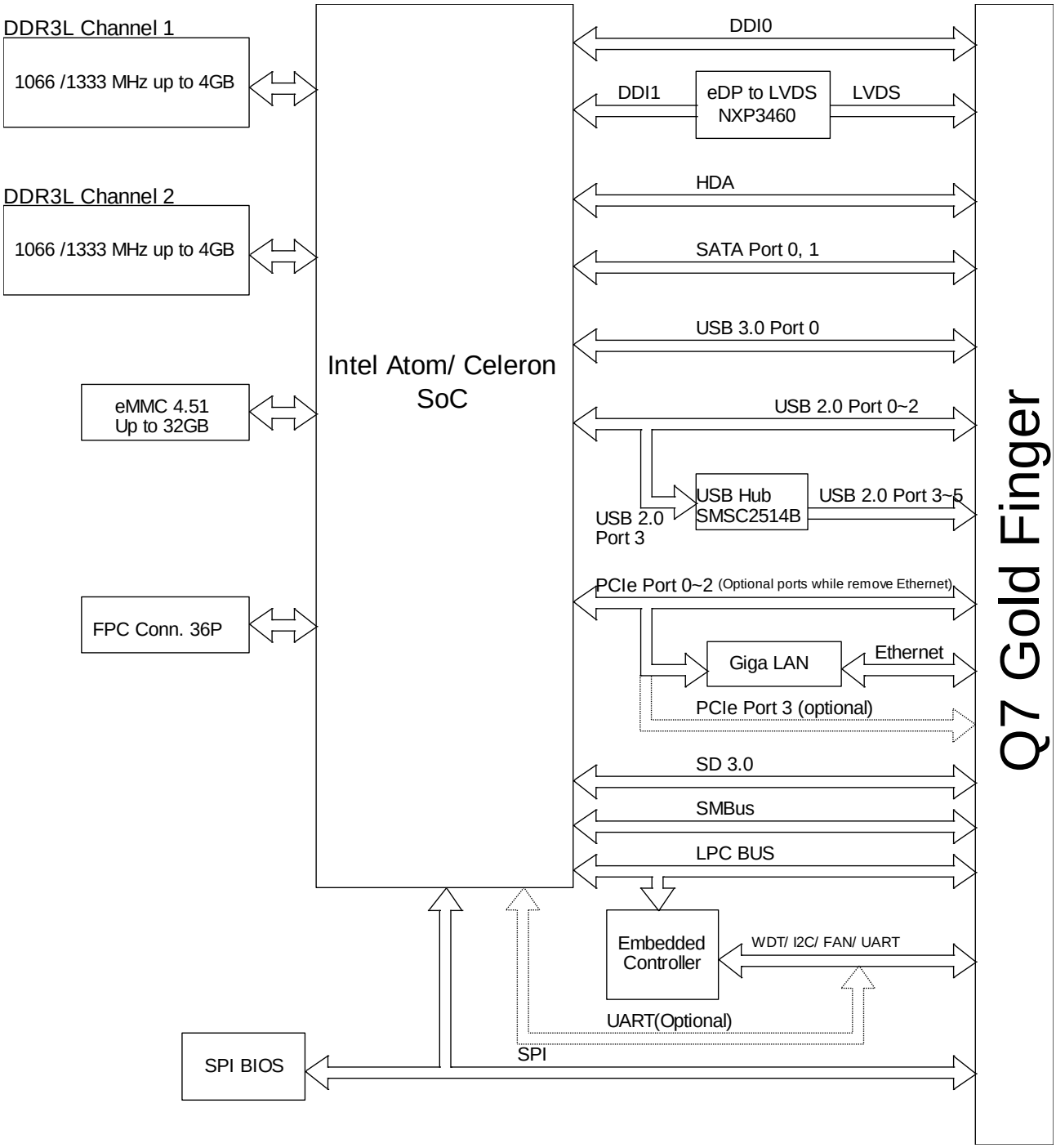
1.4 Reference Documents

Document
Qseven Design Guide Rev. 2.0
Qseven Specification 2.0 and Qseven Specification 2.1
Intel EDS Document
Intel Layout Guide Document
ATX12V Power Supply Design Guide Rev. 2.01

1.5 Revision History

Revision	Date	PCB Rev.	Changes
1.00	Oct 14, 2015	A101-2	SOM-3567 design for Q7 R2.0
1.10	May 03, 2018	A101-2	Update Table 18 LVDS impedance to 85

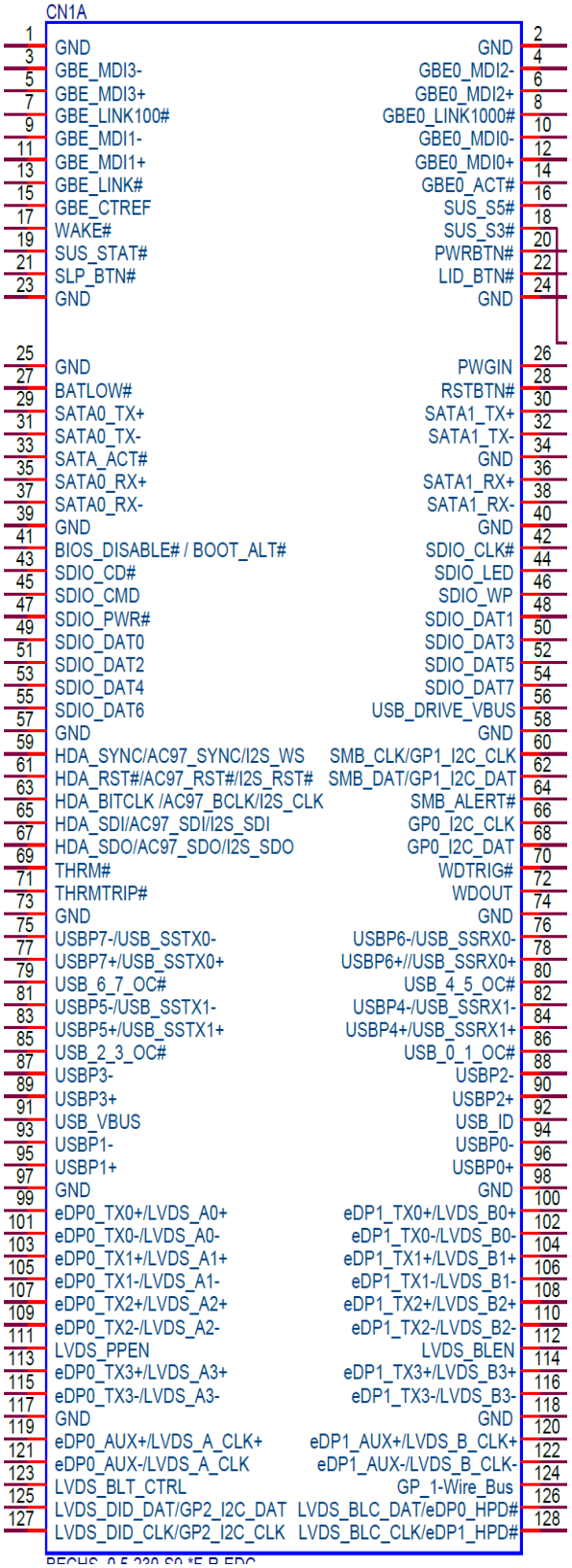
1.6 SOM-3567 Block Diagram

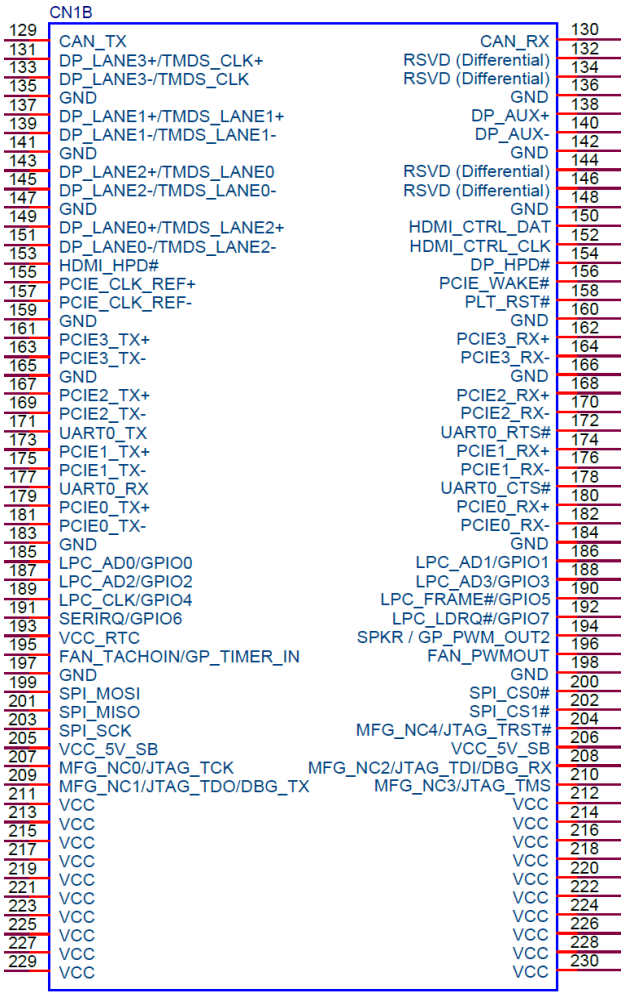


2. Qseven Interfaces

2.1 Qseven Connector Layout

Figure 1: Qseven Connector Layout


CN1A
1 GND
2 GND
3 GBE_MDI3-
4 GBE0_MDI2-
5 GBE_MDI3+
6 GBE0_MDI2+
7 GBE_LINK100#
8 GBE0_LINK1000#
9 GBE_MDI1-
10 GBE0_MDI0-
11 GBE_MDI1+
12 GBE0_MDI0+
13 GBE_LINK#
14 GBE0_ACT#
15 GBE_CTREF
16 SUS_S5#
17 WAKE#
18 SUS_S3#
19 SUS_STAT#
20 PWRBTN#
21 SLP_BTN#
22 LID_BTN#
23 GND
24 GND
25 GND
26 PWGIN
27 BATLOW#
28 RSTBTN#
29 SATA0_TX+
30 SATA1_TX+
31 SATA0_TX-
32 SATA1_TX-
33 SATA_ACT#
34 GND
35 SATA0_RX+
36 SATA1_RX+
37 SATA0_RX-
38 SATA1_RX-
39 GND
40 GND
41 BIOS_DISABLE# / BOOT_ALT#
42 SDIO_CLK#
43 SDIO_CD#
44 SDIO_LED
45 SDIO_CMD
46 SDIO_WP
47 SDIO_PWR#
48 SDIO_DAT1
49 SDIO_DAT0
50 SDIO_DAT3
51 SDIO_DAT2
52 SDIO_DAT5
53 SDIO_DAT4
54 SDIO_DAT7
55 SDIO_DAT6
56 USB_DRIVE_VBUS
57 GND
58 GND
59 HDA_SYNC/AC97_SYNC/I2S_WS
60 SMB_CLK/GP1_I2C_CLK
61 HDA_RST#/AC97_RST#/I2S_RST#
62 SMB_DAT/GP1_I2C_DAT
63 HDA_BITCLK /AC97_BCLK/I2S_CLK
64 SMB_ALERT#
65 HDA_SDI/AC97_SDI/I2S_SDI
66 GP0_I2C_CLK
67 HDA_SDO/AC97_SDO/I2S_SDO
68 GP0_I2C_DAT
69 THRM#
70 WDTRIG#
71 THRMTRIP#
72 WDOUT
73 GND
74 GND
75 USBP7-/USB_SSTX0-
76 USBP6-/USB_SSRX0-
77 USBP7+/USB_SSTX0+
78 USBP6+//USB_SSRX0+
79 USB_6_7_OC#
80 USB_4_5_OC#
81 USBP5-/USB_SSTX1-
82 USBP4-/USB_SSRX1-
83 USBP5+/USB_SSTX1+
84 USBP4+/USB_SSRX1+
85 USB_2_3_OC#
86 USB_0_1_OC#
87 USBP3-
88 USBP2-
89 USBP3+
90 USBP2+
91 USB_VBUS
92 USB_ID
93 USBP1-
94 USBP0-
95 USBP1+
96 USBP0+
97 GND
98 GND
99 eDP0_TX0+/LVDS_A0+
100 eDP1_TX0+/LVDS_B0+
101 eDP0_TX0-/LVDS_A0-
102 eDP1_TX0-/LVDS_B0-
103 eDP0_TX1+/LVDS_A1+
104 eDP1_TX1+/LVDS_B1+
105 eDP0_TX1-/LVDS_A1-
106 eDP1_TX1-/LVDS_B1-
107 eDP0_TX2+/LVDS_A2+
108 eDP1_TX2+/LVDS_B2+
109 eDP0_TX2-/LVDS_A2-
110 eDP1_TX2-/LVDS_B2-
111 LVDS_PPEN
112 LVDS_BLEN
113 eDP0_TX3+/LVDS_A3+
114 eDP1_TX3+/LVDS_B3+
115 eDP0_TX3-/LVDS_A3-
116 eDP1_TX3-/LVDS_B3-
117 GND
118 GND
119 eDP0_AUX+/LVDS_A_CLK+
120 eDP1_AUX+/LVDS_B_CLK+
121 eDP0_AUX-/LVDS_A_CLK
122 eDP1_AUX-/LVDS_B_CLK-
123 LVDS_BLT_CTRL
124 GP_1-Wire_Bus
125 LVDS_DID_DAT/GP2_I2C_DAT
126 LVDS_BLC_DAT/eDP0_HPD#
127 LVDS_DID_CLK/GP2_I2C_CLK
128 LVDS_BLC_CLK/eDP1_HPD#



2.2 Qseven 2.1 Connector Pin-out

Table 2: Qseven 2.1 Pin-out

Connector

Pin	Signal	Pin	Signal
1	GND	2	GND
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	GBE_LINK#	14	GBE_ACT#
15	GBE_CTREF	16	SUS_S5#
17	WAKE#	18	SUS_S3#
19	GPO0	20	PWRBTN#

21	SLP_BTN# / GPII1	22	LID_BTN# / GPII0
23	GND	24	GND
KEY		KEY	
25	GND	26	PWGIN
27	BATLOW# / GPII2	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	GND
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	GND	40	GND
41	BIOS_DISABLE# / BOOT_ALT#	42	SDIO_CLK#
43	SDIO_CD#	44	reserved
45	SDIO_CMD	46	SDIO_WP
47	SDIO_PWR#	48	SDIO_DAT1
49	SDIO_DAT0	50	SDIO_DAT3
51	SDIO_DAT2	52	reserved
53	reserved	54	reserved
55	reserved	56	USB_OTG_PEN
57	GND	58	GND
59	HDA_SYNC / I2S_WS	60	SMB_CLK / GP1_I2C_CLK
61	HDA_RST# / I2S_RST#	62	SMB_DAT / GP1_I2C_DAT
63	HDA_BITCLK / I2S_CLK	64	SMB_ALERT#

Pin	Signal	Pin	Signal
65	HDA_SDI / I2S_SDI	66	GP0_I2C_CLK
67	HDA_SDO / I2S_SDO	68	GP0_I2C_DAT
69	THRM#	70	WDTRIG#
71	THRMTRIP#	72	WDOUT
73	GND	74	GND
75	USB_P7- / USB_SSTX0-	76	USB_P6- / USB_SSRX0-
77	USB_P7+ / USB_SSTX0+	78	USB_P6+ / USB_SSRX0+
79	USB_6_7_OC#	80	USB_4_5_OC#
81	USB_P5- / USB_SSTX2-	82	USB_P4- / USB_SSRX2-
83	USB_P5+ / USB_SSTX2+	84	USB_P4+ / USB_SSRX2+

85	USB_2_3_OC#	86	USB_0_1_OC#
87	USB_P3-	88	USB_P2-
89	USB_P3+	90	USB_P2+
91	USB_VBUS	92	USB_ID
93	USB_P1-	94	USB_P0-
95	USB_P1+	96	USB_P0+
97	GND	98	GND
99	eDP0_TX0+ / LVDS_A0+	100	eDP1_TX0+ / LVDS_B0+
101	eDP0_TX0- / LVDS_A0-	102	eDP1_TX0- / LVDS_B0-
103	eDP0_TX1+ / LVDS_A1+	104	eDP1_TX1+ / LVDS_B1+
105	eDP0_TX1- / LVDS_A1-	106	eDP1_TX1- / LVDS_B1-
107	eDP0_TX2+ / LVDS_A2+	108	eDP1_TX2+ / LVDS_B2+
109	eDP0_TX2- / LVDS_A2-	110	eDP1_TX2- / LVDS_B2-
111	LVDS_PPEN	112	LVDS_BLEN
113	eDP0_TX3+ / LVDS_A3+	114	eDP1_TX3+ / LVDS_B3+
115	eDP0_TX3- / LVDS_A3-	116	eDP1_TX3- / LVDS_B3-
117	GND	118	GND
119	eDP0_AUX+ / LVDS_A_CLK+	120	eDP1_AUX+ / LVDS_B_CLK+
121	eDP0_AUX- / LVDS_A_CLK-	122	eDP1_AUX- / LVDS_B_CLK-
123	LVDS_BLT_CTRL / P_PWM_OUT0	124	GP_1-Wire_Bus / HDMI_CEC
125	GP2_I2C_DAT / LVDS_DID_DAT	126	eDP0_HPD# / LVDS_BLC_DAT
127	GP2_I2C_CLK / LVDS_DID_CLK	128	eDP1_HPD# / LVDS_BLC_CLK
129	CAN0_TX	130	CAN0_RX
131	DP_LANE3+ / TMDS_CLK+	132	USB_SSTX1-
133	DP_LANE3- / TMDS_CLK-	134	USB_SSTX1+
135	GND	136	GND

Pin	Signal	Pin	Signal
137	DP_LANE1+ / TMDS_LANE1+	138	DP_AUX+
139	DP_LANE1- / TMDS_LANE1-	140	DP_AUX-
141	GND	142	GND
143	DP_LANE2+ / TMDS_LANE0+	144	USB_SSRX1-

145	DP_LANE2- / TMDS_LANE0-	146	USB_SSRX1+
147	GND	148	GND
149	DP_LANE0+ / TMDS_LANE2+	150	HDMI_CTRL_DAT
151	DP_LANE0- / TMDS_LANE2-	152	HDMI_CTRL_CLK
153	HDMI_HPD#	154	DP_HPD#
155	PCIE_CLK_REF+	156	PCIE_WAKE#
157	PCIE_CLK_REF-	158	PCIE_RST#
159	GND	160	GND
161	PCIE3_TX+	162	PCIE3_RX+
163	PCIE3_TX-	164	PCIE3_RX-
165	GND	166	GND
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_TX-	170	PCIE2_RX-
171	UART0_TX	172	UART0_RTS#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_TX-	176	PCIE1_RX-
177	UART0_RX	178	UART0_CTS#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_TX-	182	PCIE0_RX-
183	GND	184	GND
185	LPC_AD0 / GPIO0	186	LPC_AD1 / GPIO1
187	LPC_AD2 / GPIO2	188	LPC_AD3 / GPIO3
189	LPC_CLK / GPIO4	190	LPC_FRAME# / GPIO5
191	SERIRQ / GPIO6	192	LPC_LDRQ# / GPIO7
193	VCC_RTC (3.3V)	194	SPKR / GP_PWM_OUT2
195	FAN_TACHOIN / GP_TIMER_IN	196	FAN_PWMOUT / GP_PWM_OUT1
197	GND	198	GND
199	SPI_MOSI	200	SPI_CS0#
201	SPI_MISO	202	SPI_CS1#
203	SPI_SCK	204	MFG_NC4
205	VCC_5V_SB (5V)	206	VCC_5V_SB (5V)

Pin	Signal	Pin	Signal
207	MFG_NC0	208	MFG_NC2
209	MFG_NC1	210	MFG_NC3

211	NC* / VCC (5V)	212	NC* / VCC (5V)
213	NC* / VCC (5V)	214	NC* / VCC (5V)
215	NC* / VCC (5V)	216	NC* / VCC (5V)
217	NC* / VCC (5V)	218	NC* / VCC (5V)
219	VCC (5V)	220	VCC (5V)
221	VCC (5V)	222	VCC (5V)
223	VCC (5V)	224	VCC (5V)
225	VCC (5V)	226	VCC (5V)
227	VCC (5V)	228	VCC (5V)
229	VCC (5V)	230	VCC (5V)

Notes:

1. Q7 R2.0 and Q7 R2.1 difference table

Pin	R2.0 Connector Pinout	R2.1 Connector Pinout	Pin	R2.0 Connector Pinout	R2.1 Connector Pinout
19	SUS_STAT#	GPO0	22	LID_BTN#	LID_BTN# / GPII0
21	SLP_BTN#	SLP_BTN# / GPII1	44	SDIO_LED	reserved
27	BATLOW#	BATLOW# / GPII2	52	SDIO_DAT5	reserved
53	SDIO_DAT4	reserved	54	SDIO_DAT7	reserved
55	SDIO_DAT6	reserved	56	USB_DRIVE_VBUS	USB_OTG_PEN
81	USB_P5- / USB_SSTX1-	USB_P5- / USB_SSTX2-	82	USB_P4- / USB_SSRX1-	USB_P4- / USB_SSRX2-
83	USB_P5+ / USB_SSTX1+	USB_P5+ / USB_SSTX2+	84	USB_P4+ / USB_SSRX1+	USB_P4+ / USB_SSRX2+
153	DP_HDMI_HPD#	HDMI_HPD#	124	GP_1-Wire_Bus	GP_1-Wire_Bus / HDMI_CEC
211	VCC	NC	132	RSVD	USB_SSTX1-
213	VCC	NC	134	RSVD	USB_SSTX1+
215	VCC	NC	144	RSVD	USB_SSRX1-
217	VCC	NC	146	RSVD	USB_SSRX1+
			212	VCC	NC
			214	VCC	NC
			216	VCC	NC
			218	VCC	NC

2.3 PCI Express

2.3.1 COM Express A-B Connector and C-D Connector PCIe Groups

PCI Express provides a scalable, high-speed, serial I/O point-to-point bus connection. A PCI Express lane consists of dual simplex channels, each implemented as a low-voltage differentially driven transmit pair and receive pair. They are used for simultaneous transmission in each direction. The bandwidth of a PCI Express link can be scaled by adding signal pairs to form multiple lanes between two devices. The Qseven modules can optionally provide configurations with x1 and x4 link widths. Each single lane has a raw data transfer rate of 2.5Gbps @ 1.25GHz.

The PCI Express interface of the Qseven module consists of a minimum of 0 [ARM] resp. 1 [x86] and up to 4 lanes, each with a receive and transmit differential signal pair designated from PCIE0_RX (+ and -) to PCIE3_RX (+ and -) and correspondingly from PCIE0_TX (+ and -) to PCIE3_TX (+ and -). According to the PCI Express specification, these four lanes can be configured as several PCI Express x1 links or to a combined x4 link. These configuration possibilities are based on the Qseven module's chipset capabilities. Refer to the vendor specific Qseven module documentation for the module that you are using for additional information about this subject.

2.3.2 General Purpose PCIe Signal Definitions

Table 3: General Purpose PCI Express Signal Descriptions

Signal	Pin#	Description	I/O	Note
PCIE0_RX+ PCIE0_RX-	180 182	PCIe channel 0. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near Qseven to PCIE0 x1 device PETp0. Slot - Connect to PCIE0 x1 Conn pin A16, A17 PERp0. N/C if not used.	I PCIE	
PCIE0_TX+ PCIE0_TX-	179 181	PCIe channel 0. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE0 x1 device PERp0.	O PCIE	

		Slot - Connect to PCIE0 x1 Conn pin B14, B15 PETp0. N/C if not used		

Signal	Pin#	Description	I/O	Note
PCIE1_RX+ PCIE1_RX-	174 176	PCIe channel 1. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near to PCIE1 x1 device PETp/n0. Slot - Connect to PCIE1 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	
PCIE1_TX+ PCIE1_TX-	173 175	PCIe channel 1. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE1 x1 device PERp/n0. Slot - Connect to PCIE1 x1 Conn pin B14, B15 PETp/n0. N/C if not used.	O PCIE	
PCIE2_RX+ PCIE2_RX-	168 170	PCIe channel 2. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near COME to PCIE2 x1 device PETp/n0. Slot - Connect to PCIE2 x1 Conn pin A16, A17 PERp/n0. N/C if not used.	I PCIE	
PCIE2_TX+	167	PCIe channel 2. Transmit Output	O PCIE	

PCIE2_TX-	169	differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE2 x1 device PERp/n0. Slot - Connect to PCIE2 x1 Conn pin B14, B15 PETp/n0. N/C if not used.		
PCIE3_RX+ PCIE3_RX-	162 164	PCIe channel 3. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near to PCIE3 x1 device PETp/n0. Slot - Connect to PCIE3 x1 Conn pin A16, A17 PERp/n0. N/C if not used. **Default** - N/C, LAN I210IT on the Module Alternative - PCIE (C235, C236 removed and R191,R193 added on the Module)	I PCIE	

Signal	Pin#	Description	I/O	Note
PCIE3_TX+ PCIE3_TX-	161 163	PCIe channel 3. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIE3 x1 device PERp/n0. Slot - Connect to PCIE3 x1 Conn pin B14, B15 PETp/n0. N/C if not used. **Default** - N/C, LAN I210IT on the Module Alternative - PCIE (C233,C234 removed and C237,C238 added on the	O PCIE	

		Module)		
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes. Carrier Board: Connect 0Ω in series to Device - PCIE device REFCLK+, REFCLK-. Slot - PCIE Conn pin A13 REFCLK+, A14 REFCLK-. *Connect to PCIE Clock Buffer input to provide PCIE clocks output for more than one PCIE devices or slots. N/C if not used.	O PCIE	2
WAKE0#	156	PCI Express wake up event signal. Module has integrated PU resistor to 3.3VDUAL Device - Connect to WAKE# pin of PCIE device. Slot - Connect to WAKE# pin B11 of PCIE slot. Express Card - Connect to WAKE# pin 11 of Express Card socket. N/C if not used.	I 3.3V Suspend CMOS	
PCIE_RST#	158	Reset output from Module to Carrier Board. Active low. Module has integrated 3.3V buffer and series resistor. Connect to reset pin of devices except PCI slots devices. N/C if not used.	O 3.3V CMOS Max. 1mA	3

Notes:

1. There are a maximum of 4 PCI Express TX and RX differential pairs supported on the Qseven module standard. Depending on the features supported by the Qseven module

and the core logic chipset used, these lines may be used to form x1 or x4 PCI Express links. The documentation for the Qseven module shall clearly identify, which PCI Express link configuration or configurations (in the case that these can be programmed in the core logic chipset) are supported.

2. PCI Express does not specify the external clock source for PCI Express devices. It only provides a 100MHz differential Serial Reference Clock (SRC), which can be used by the internal PLL of the PCI Express device to generate the required 1.25GHz clock. The corresponding Serial Reference Clock signals *'PCI_CLK_REF+'* and *'PCI_CLK_REF-'* can be found on the Qseven module connector on pins 155 and 157. In an application where more than one PCI Express slot or device is needed, the differential Serial Reference Clock signal must be replicated by using a buffer.

3. The Qseven module provides one PCI Express Reset signal on pin 158 of the Qseven connector(referenced as PLT_RST#) in the example schematics. It is recommended to use a buffer to replicate the Reset signal on the carrier board when more than one PCI Express slot or device is needed.

2.3.3 PCI Express* Trace Length Guidelines

Figure 2: Topology for PCI Express Slot Card.

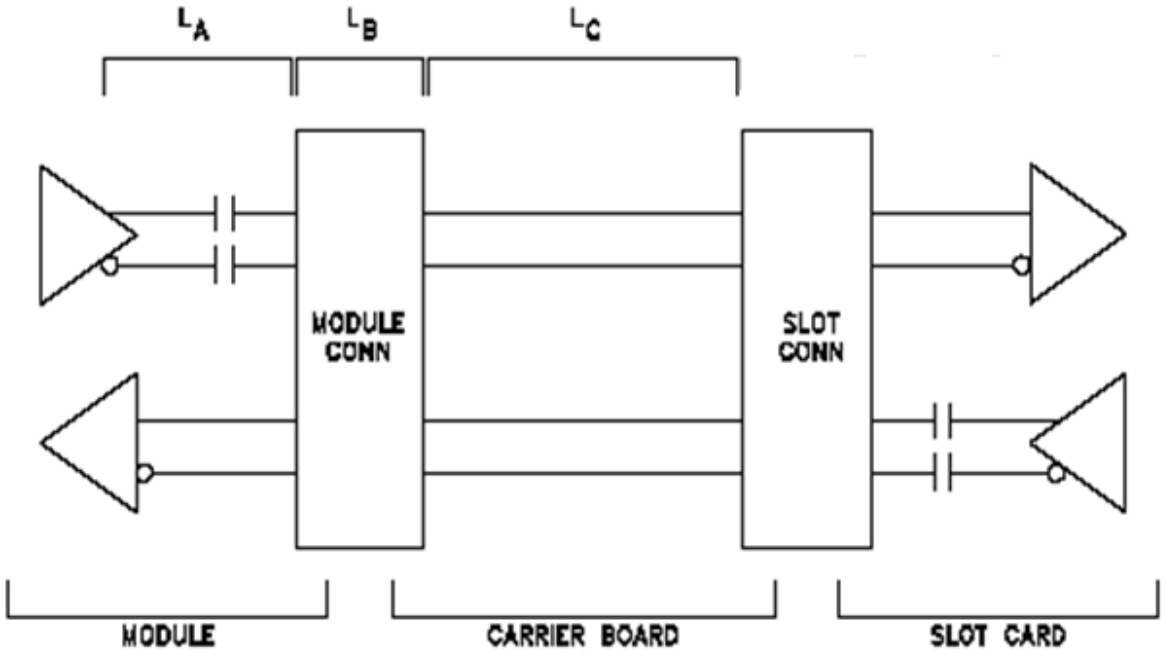


Figure 3: Topology for PCI Express Device Down.

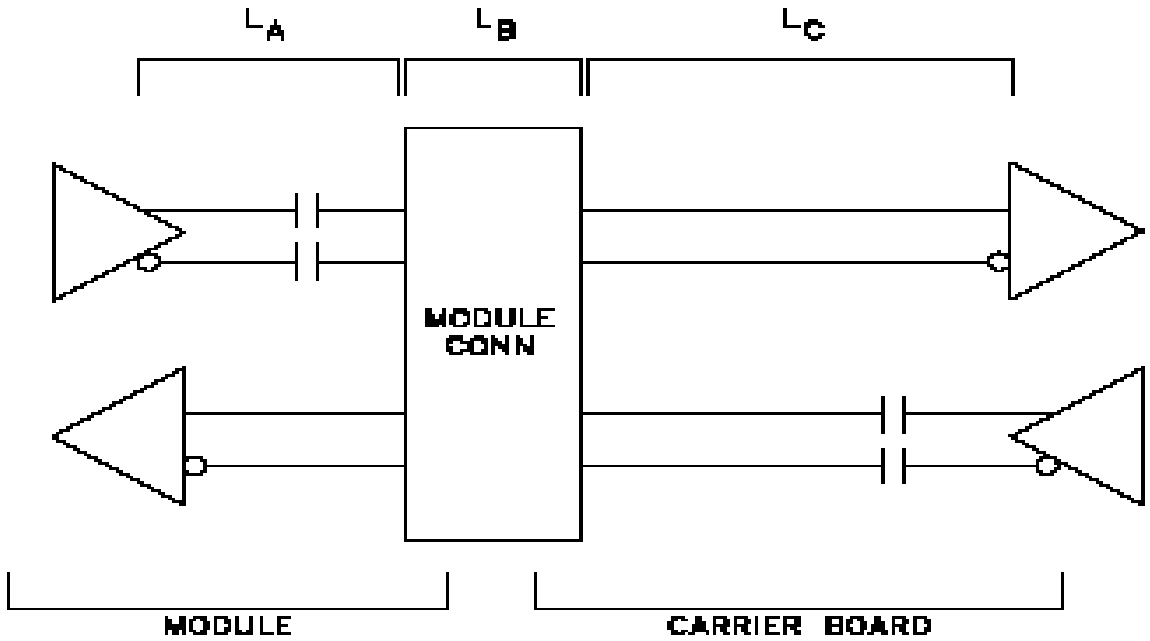


Table 4: PCI Express* Slot Card / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	PCI Express* expansion	
Differential Impedance Target	85Ω±10%	
Single End	55Ω±10%	
Isolation to equivalent pairs	20 mils (MS) and 15 mils (DS)	
Isolation to other signal groups	20 mils (MS) and 15 mils (DS)	
Tx/Rx Spacing	25 mils	
LA + LB	Please see the SOM-3567 Layout Checklist	
Lc	Carrier Board Length	
Max length of LA+LB+LC	Slot Card: 7.5” Device Down: 9”	
Length matching	Differential pairs (intra-pair): Max. ±10 mils REFCLK+ and REFCLK- (intra-pair):Max. ±10mils	
Reference Plane	GND referencing preferred Min 40-mil trace edge-to-major plane edge spacing GND stitching vias required next to signal vias if transitioning layers between GND layers Power referencing acceptable if stitching caps are used	
Carrier Board Via Usage	Max. 2 vias per TX trace, Max. 4 vias per RX trace	
AC coupling	The AC coupling capacitors for the TX lines are incorporated on the Qseven Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer Qseven Carrier Board. Capacitor type: X7R, 100nF ±10%, 16V, shape 0402.	1

Notes:

1. AC caps are recommended to be placed close to PCIe device side (avoid placing AC cpas on mid-bus).

2.4 LAN Interface

Qseven modules provide at least one 10/100/1000BaseT Gigabit Ethernet LAN port compliant with the IEEE 802.3ab specification.

2.4.1 LAN Signal Definitions

The LAN interface of the Qseven module consists of 4 pairs of low voltage differential pair signals designated from *'GBE_MDI0'* (+ and -) to *'GBE_MDI3'* (+ and -) plus additional control signals for link activity indicators. These signals can be used to connect a 10/100/1000BaseT RJ45 connector with integrated or external isolation magnetics to the carrier board.

Table 5: LAN Interface Signal Descriptions

Signal	Pin#	Description	I/O	Note
GBE0_MDI0+ GBE0_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI0+/- N/C if not used.	I/O GBE	
GBE0_MDI1+	11	Media Dependent Interface (MDI)	I/O	

GBE0_MDI1-	9	differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI0+/- N/C if not used	GBE	
GBE0_MDI2+ GBE0_MDI02	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI2+/- N/C if not used.	I/O GBE	

Signal	Pin#	Description	I/O	Note
GBE0_MDI3+ GBE0_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI3+/- N/C if not used	I/O GBE	
GBE0_CTREF	15	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should	REF	1

		be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less. Carrier Board: 0.1uF to ground. N/C if not used.		
GBE0_LINK#	13	Ethernet controller 0 link indicator, active low.	O 3.3V Suspend / 3.3V OD CMOS	
GBE0_LINK100#	7	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3V Suspend / 3.3V OD CMOS	
GBE0_LINK1000#	8	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3V Suspend / 3.3V OD CMO	
GBE0_ACT#	14	Ethernet controller 0 activity indicator, active low.	O 3.3V Suspend / 3.3V OD CMO	

Note:

1. SOM-3567 is NC.

2.4.2 LAN Implementation Guidelines

The most critical component in the LAN interface is the isolation magnetics connected directly to the MDI differential pair signals of the Qseven module. It should be carefully qualified for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection and Crosstalk Isolation to pass the IEEE conformance tests and EMI tests.

Even if a Qseven module complies with the basic specifications set forth for IEEE certification, it's still possible that the overall system could fail IEEE testing because of a

poor quality or unsuitable external isolation magnetics module and/or improper PCB layout of the carrier board.

2.4.3 LAN Magnetics Modules

1000Base-T Ethernet magnetics modules are similar to those designed solely for 10/100 BaseTx Ethernet, except that there are four MDI differential signal pairs instead of two. 1000Base-T magnetics modules have a center tap pin that is connected to the reference voltage output *'GBE_CTREF'* of the Qseven module, which biases the controller's output buffers. Magnetics with four center tap pins may have better characteristics than those with one or two center tap pins. Depending on the PHY manufacturer some PHYs may require, that each differential pair center tap pin is connected separately via a capacitor to ground. In this case the PHY center tap pins are not connected together.The isolation magnetics can be integrated in a RJ45 jack, which also provides activity and speed LED indicators. Alternatively, they can be designed as discrete magnetics modules, which will be connected to a pure RJ45 jack.

2.4.4 LAN Component Placement

When using RJ45 connectors without integrated magnetics, the discrete magnetics module has to be placed as close as possible to the RJ45 connector. The distance between the magnetics module and RJ45 connector must be less than 1 inch. This distance requirement must be observed during the carrier board layout when implementing LAN. Due to the insertion loss budget of Qseven, the overall trace length of the MDI signal pairs on the carrier board should be less than 4 inches. Signal attenuation could cause data transfer problems for traces longer than 4 inches.

2.4.5 LAN Ground Plane Separation

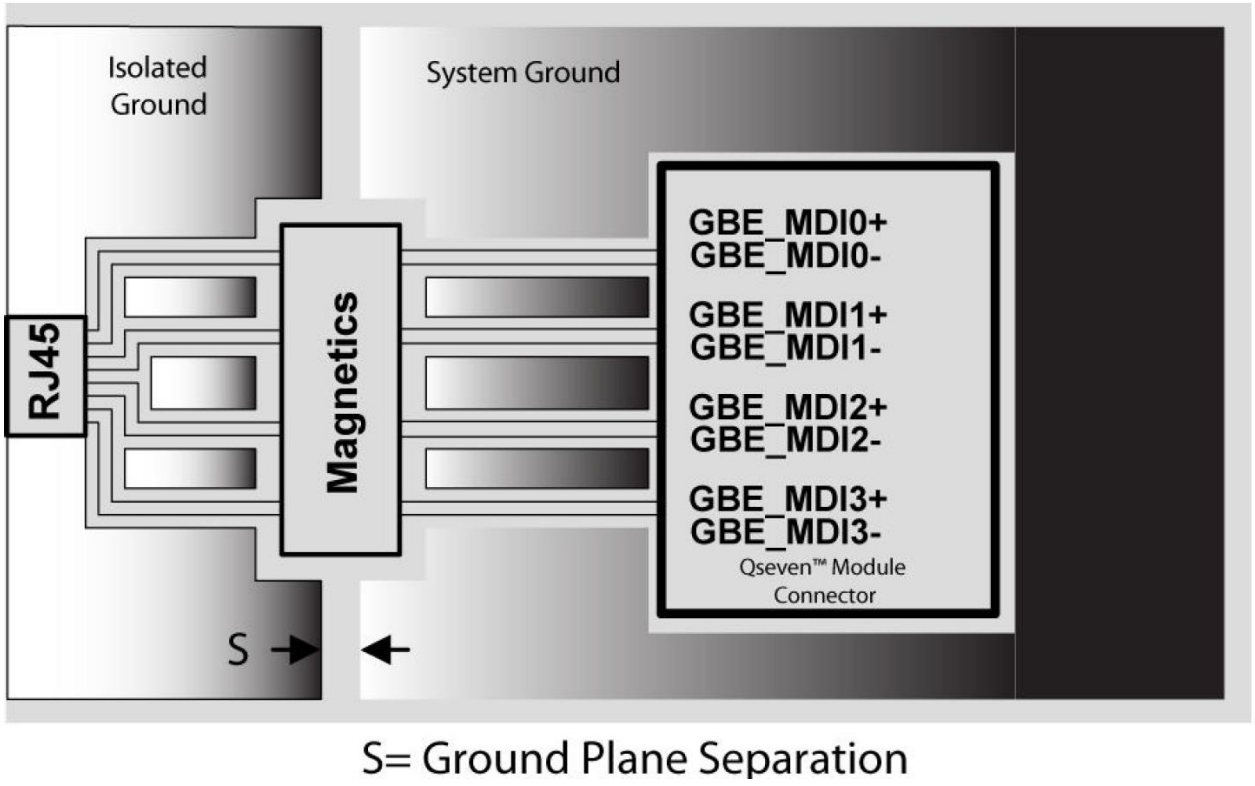
Isolated separation between the analog ground plane and digital ground plane is recommended. If this is not implemented properly then bad ground plane partitioning

could cause serious EMI emissions and degrade analog performance due to ground bounce noise.

The plane area underneath the magnetic module should be left empty. This free area is to keep transformer induced noise away from the power and system ground planes.

The isolated ground, also called chassis ground, connects directly to the fully shielded RJ45 connector. For better isolation it is also important to maintain a gap between chassis ground and system ground that is wider than 60mils. For ESD protection, a 3kV high voltage capability capacitor is recommended to connect to this chassis ground.

Figure 4: LAN Ground Plane Separation



2.4.6 LAN Link Activity and Speed LED

The Qseven module has four 3.3V push/pull outputs to directly drive activity, speed indication and link status LEDs. The 3.3V standby voltage should be used as LED supply voltage so that the link activity can be viewed during system standby state. Since LEDs are likely to be integrated into a RJ45 connector with integrated magnetics module, the LED traces need to be routed away from potential sources of EMI noise. Consider adding a filtering capacitor per LED for extremely noisy situations. The suggested value for this capacitor is 470pF.

2.4.7 LAN Trace Length Guidelines

Figure 5: Topology for Ethernet Jack

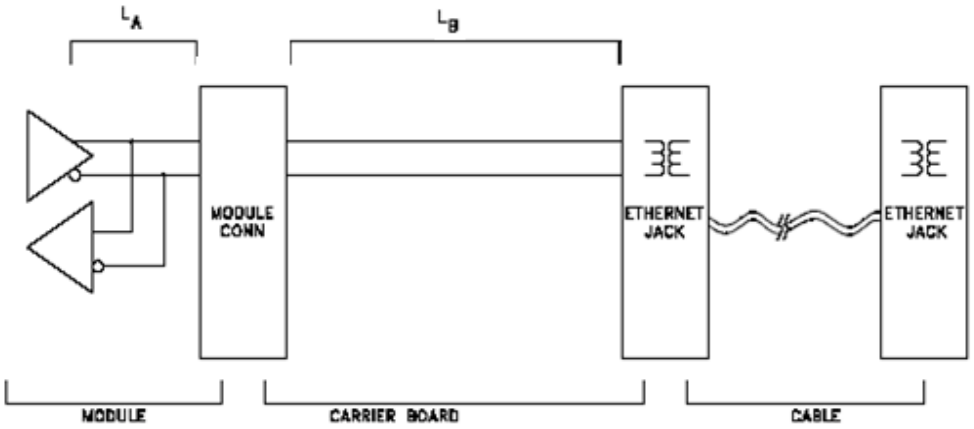


Table 6: Ethernet Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	GBE0_MDIx+, GBE0_MDIx-	
Differential Impedance Target	95 Ω ±10%	
Single End	55Ω ±10%	
Spacing between RX and TX pairs (inter-pair) (s)	Min. 50mils	
Spacing between differential pairs and high-speed periodic signals	Min. 100mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 50mils	
Spacing between digital ground and analog ground plane (between the magnetics Module and RJ45 connector)	Min. 100mils	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	Qeven Module to the magnetics Module - 5.0 inches. Magnetics Module to RJ45 connector - Max. 1.0 inches.	
Length matching	Differential pairs (intra-pair): Max. ±2.5 mils	

	RX and TX pairs (inter-pair) - Max. ±15mils	
Reference Plane	GND referencing preferred..	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Max. 2 vias.	

Notes:

2.4.8 Reference Ground Isolation and Coupling

The Carrier Board should maintain a well-designed analog ground plane around the components on the primary side of the transformer between the transformer and the RJ-45 receptacle. The analog ground plane is bonded to the shield of the external cable through the RJ-45 connector housing.

The analog ground plane should be coupled to the carrier's digital logic ground plane using a capacitive coupling circuit that meets the ground plane isolation requirements defined in the 802.3-2005 specification. It is recommended that the Carrier Board PCB design maintain a minimum 30 mil gap between the digital logic ground plane and the analog ground plane.

It's recommended to place an optional GND to SHIELDGND connection near the RJ-45 connector to improve EMI and ESD capabilities.

2.5 SATA

Serial ATA (SATA) is a serial interface for connecting storage devices (mainly hard disks) and was defined to replace the old parallel ATA interface. Serial ATA uses a point-to-point serial connection between the system and the storage device. The first generation of standard Serial ATA provides a maximum effective data transfer rate of 150MB/s per port. With the second generation SATA II, an effective transfer rate of up to 300MB/s per port is possible. Serial ATA is completely software transparent to the IDE interface while providing a lower pin count and higher performance.

2.5.1 SATA Signal Definitions

Qseven modules can provide up to 2 Serial ATA channels, each with a receive and transmit differential signal pair designated from *'SATA0_RX'* (+ and -) to *'SATA1_RX'* (+ and -) and correspondingly from *'SATA0_TX'* (+ and -) to *'SATA1_TX'* (+ and -). The appropriate signals can be found on the Qseven module connector.

Table 7: SATA Signal Definitions

Signal	Pin#	Description	I/O	Note
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive input differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA0 Conn pin 6 RX+ Connect to SATA0 Conn pin 5 RX- N/C if not used.	I SATA	
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit output differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA0 Conn pin 2 TX+	O SATA	

		Connect to SATA0 Conn pin 3 TX- N/C if not used.		
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive input differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA1 Conn pin 6 RX+ Connect to SATA1 Conn pin 5 RX- N/C if not used.	I SATA	
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit output differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA1 Conn pin 2 TX+ Connect to SATA1 Conn pin 3 TX- N/C if not used.	O SATA	
SATA_ACT#	33	Serial ATA activity LED. Open collector output pin driven during SATA command activity. Module has integrated PU resistor Carrier Board: Connect to LED and current limiting resistors 250 to 330 Ω to 3.3V N/C if not used.	O 3.3V CMOS OC	Able to drive 10 mA

Notes:

2.5.2 SATA Routing Guidelines

2.5.2.1 General SATA Routing Guidelines

Use the following general routing and placement guidelines when laying out a new design.

- SATA signals must be ground referenced. If changing reference plane is completely unavoidable (that is, ground reference to power reference), proper placement of stitching caps can minimize the adverse effects of EMI and signal quality performance caused by reference plane change. Stitching capacitors are small valued capacitors (1 µF or lower in value) that bridge the power and ground planes close to where a high-speed signal changes layers. Stitching caps provide a high frequency current return path between different reference planes. They minimize the impedance discontinuity and current loop area that crossing different reference planes created. The maximum number allowed for SATA to change reference plane is one.
- Route all traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane can cause signal reflections and should be avoided.
- Minimize layer changes. If a layer change is necessary, ensure that trace matching for either transmit or receive pair occurs within the same layer. Intel recommends to use SATA vias as seldom as possible.
- **DO NOT** route SATA traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- **DO NOT** place stubs, test points, test vias on the route to minimize reflection. Utilize vias and connector pads as test points instead.

- For testability, route the TX and RX pairs for a given port on the same layer and close to each other to help ensure that the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of RX pair layout quality can be approximated by using the results from actively testing the TX pair's signal quality.
- Length matching rules are required on SATA differential signals for optimum timing margins, preventing common-mode signals and EMI. Each net within a differential pair should be length matched on a segment-by-segment basis at the point of discontinuity. Total length mismatch must not be more than 20 mils (0.508 mm). Examples of segments might include breakout areas, routes running between two vias, routes between an AC coupling capacitor and a connector pin, etc. The points of discontinuity would be the via, the capacitor pad, or the connector pin. Matching of TX and RX within the same port and between SATA TX and RX pairs from differential ports is not required. When length matching compensation occurs, it should be made as close as possible to the point where the variation occurs.
- **DO NOT** serpentine to match RX and TX traces; there is **NO** requirement to match RX and TX traces. In addition, **DO NOT** serpentine to meet minimum length guidelines on RX and TX traces.
- Recommend keeping SATA traces 20 mils (0.508 mm) from any vias on the motherboard whenever possible.

2.5.3 SATA Trace Length Guidelines

Figure 6: Topology for SATA

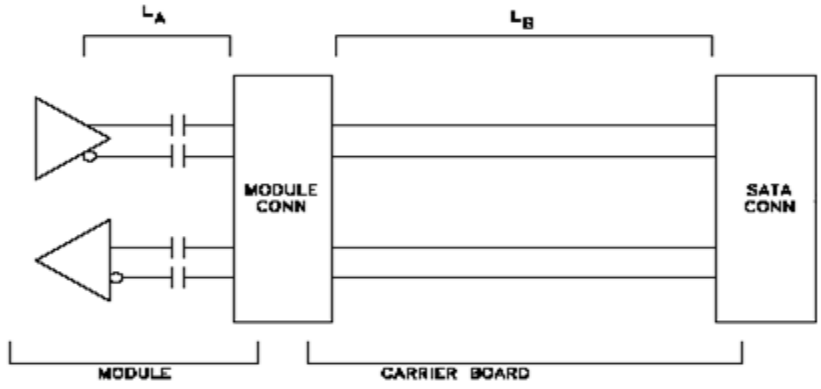


Table 8: SATA Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SATA	
Differential Impedance Target	85 Ω ±10%	

Single End	50Ω ±10%	
Signal length available for the COM Express Carrier Board	3 inches, a redriver may be necessary for GEN3 signaling rates	
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20 mils	
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	8”	
Length matching	Differential pairs (intra-pair): Max. ±5 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	A maximum of 2 vias is recommended.	
AC Coupling capacitors	The AC coupling capacitors for the TX and RX lines are implemented on the Qseven module.	

Notes:

2.6 USB2.0 Ports

The Universal Serial Bus interface of the Qseven module is compliant to USB 1.1 as well as USB 2.0 and USB 3.0 specification. Qseven specifies a minimum configuration of 3 USB 2.0 host ports for ARM architectures respectively 4 USB 2.0 ports for Intel architectures up to a maximum of 8 ports on both platforms. The number of USB 3.0 ports may vary from 0 to 2 ports on both platforms.

Note:

Depending on the Qseven module' used, some USB ports may not support USB 1.1 , USB 2.0 or USB 3.0.

2.6.1 USB2.0 Signal Definitions

Table 9: USB Signal Descriptions

Signal	Pin#	Description	I/O	Note
USB_P0+ USB_P0-	96 94	USB Port 0, data + or D+ USB Port 0, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB_P1+ USB_P1-	95 93	USB Port 1, data + or D+ USB Port 1, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB_P2+ USB_P2-	90 88	USB Port 2, data + or D+ USB Port 2, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	

Signal	Pin#	Description	I/O	Note
USB_P3+	89	USB Port 3, data + or D+	I/O USB	

USB_P3-	87	USB Port 3, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used		
USB_P4+ USB_P4- / USB_SSRX1+ USB_SSRX1- for R2.0 USB_SSRX2+ USB_SSRX2- for R2.1	84 82	USB Port 4, data + or D+ USB Port 4, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB_P5+ USB_P5- / USB_SSTX1+ USB_SSRX1- for R2.0 USB_SSTX2+ USB_SSTX2- for R2.1	83 81	USB Port 5, data + or D+ USB Port 5, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	
USB_P6+ USB_P6- / USB_SSRX0+ USB_SSRX0-	78 76	USB Port 6, data + or D+ USB Port 6, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	1
USB_P7+ USB_P7- / USB_SSTX0+ USB_SSTX0-	77 75	USB Port 7, data + or D+ USB Port 7, data + or D- Carrier Board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB	1

Signal	Pin #	Description	I/O	Note
USB_0_1_OC#	86	USB over-current sense, USB ports 0 and 1. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I 3.3V CMOS ≥ 5 mA	
USB_2_3_OC#	85	USB over-current sense, USB ports 2 and 3. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I 3.3V CMOS ≥ 5 mA	
USB_4_5_OC#	80	USB over-current sense, USB ports 4 and 5. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I 3.3V CMOS ≥ 5 mA	
USB_6_7_OC#	79	USB over-current sense, USB ports 6 and 7. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I 3.3V CMOS ≥ 5 mA	2
USB_ID	92	USB ID pin. Configures the mode of the USB Port 1. The resistance of this pin measured to ground is used to determine whether USB Port 1 is going to be used as USB Client to enable/ disable USB Client support. Please check the USB-OTG Reference of your chip manufacturer for further details. Carrier Board: Client - PU 100KΩ to 3.3VSB Host - PD 100KΩ to GND	O Analogue	2
USB_DRIVE_VBUS for R2.0 / USB_OTG_PEN for R2.1	56	USB Power enable pin for USB Port 1 Enables the Power for the USB-OTG port on the carrier board.	I 3.3V COMS	2
USB_VBUS	91		I 5V COMS	2

Notes:

1. SOM-3567 is use USB3.0, please see chapter 2.7 USB 3.0

2. SON-3567 is NC.

2.6.1.1 USB Over-Current Protection (USB_x_y_OC#)

The USB Specification describes power distribution over the USB port, which supplies power for USB devices that are directly connected to the Carrier Board. Therefore, the host must implement over-current protection on the ports for safety reasons. Should the aggregate current drawn by the downstream ports exceed a permitted value, the over-current protection circuit removes power from all affected downstream ports. The over-current limiting mechanism must be resettable without user mechanical intervention. For more detailed information about this subject, refer to the 'Universal Serial Bus Specifications Revision 2.0', which can be found on the website http://www.usb.org.

Over-current protection for USB ports can be implemented by using power distribution switches on the Carrier Board that monitor the USB port power lines. Power distribution switches usually have a soft-start circuitry that minimizes inrush current in applications where highly capacitive loads are employed. Transient faults are internally filtered.

Additionally, they offer a fault status output that is asserted during over-current and thermal shutdown conditions. These outputs should be connected to the corresponding Qseven USB over-current sense signals. Fault status signaling is an option at the USB specification. If you don't need the popup message in your OS you may leave the signals USB_0_1_OC#, USB_2_3_OC#, USB_4_5_OC# and USB_6_7_OC# unconnected.

Simple resettable PolySwitch devices are capable of fulfilling the requirements of USB overcurrent protection and therefore can be used as a replacement for power distribution switches.
Fault status signals are connected by a pullup resistor to VCC_3V3_SBY on COM Express Module. Please check your tolerance on a USB port with VCC_5V supply.

2.6.1.2 Powering USB devices during S5

The power distribution switches and the ESD protection shown in the schematics can be powered from Main Power or Suspend Power (VCC_5V_SBY). Ports powered by Suspend Power are powered during the S3 and S5 system states. This provides the ability for the Qseven to generate system wake-up events over the USB interface.

2.6.2 USB2.0 Routing Guidelines

2.6.2.1 USB 2.0 General Design Considerations and Optimization

Use the following general routing and placement guidelines when laying out a new design. These guidelines help minimize signal quality and EMI problems.

- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Separate signal traces into similar categories, and route similar signal traces together (such as routing differential-pairs together).
- Keep USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
- Follow the 20 x h rule by keeping traces at least [20 x (height above the plane)] mils away from the edge of the plane (VCC or GND). For an example stackup, the height above the plane is 4.5 mils (0.114 mm). This calculates to a 90-mil (2.286-mm) spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.
- Avoid stubs on high-speed USB signals because stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils (5.08 mm).

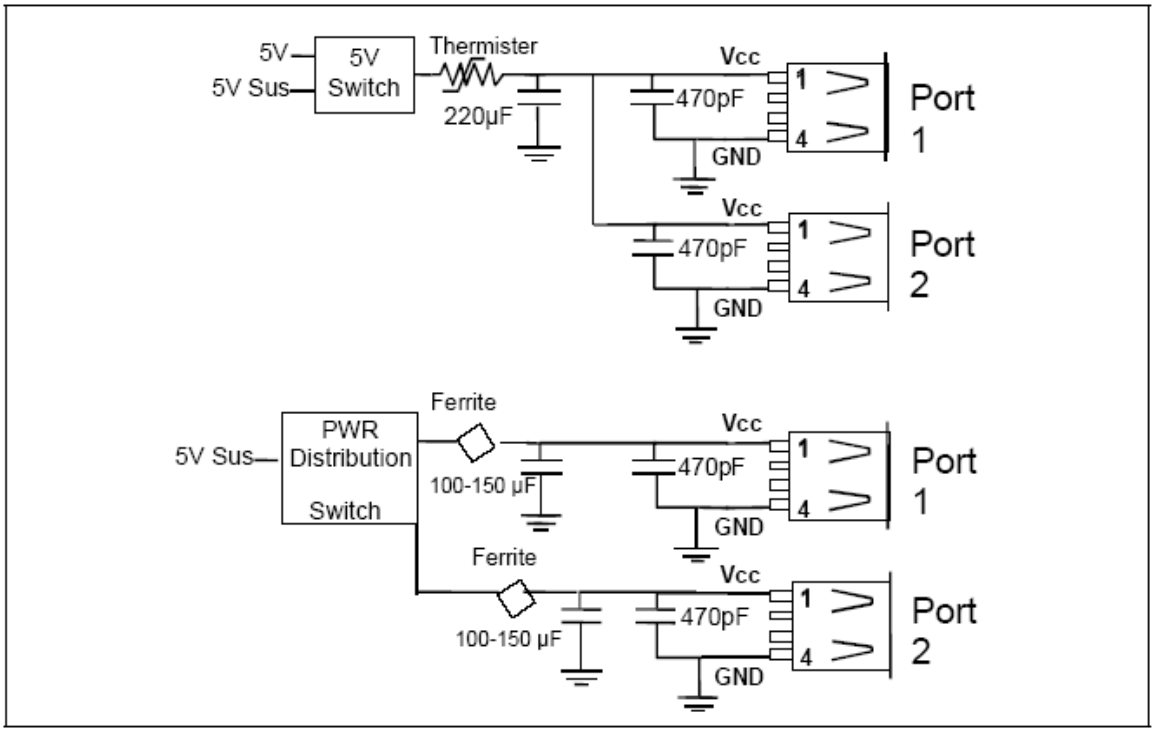
2.6.2.2 USB 2.0 Port Power Delivery

The following is a suggested topology for power distribution of VBUS to USB ports. These circuits provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach fly back protection. These two types require both bulk capacitance (droop) and filtering capacitance (for dynamic detach fly back voltage filtering). Intel recommends the following:

- Minimize the inductance and resistance between the coupling capacitors and the USB ports.
- Place capacitors as close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane.

• Make the power-carrying traces wide enough that the system fuse blows on an over current event. If the system fuse is rated at 1 A, then the power-carrying traces should be wide enough to carry at least 1.5 A.

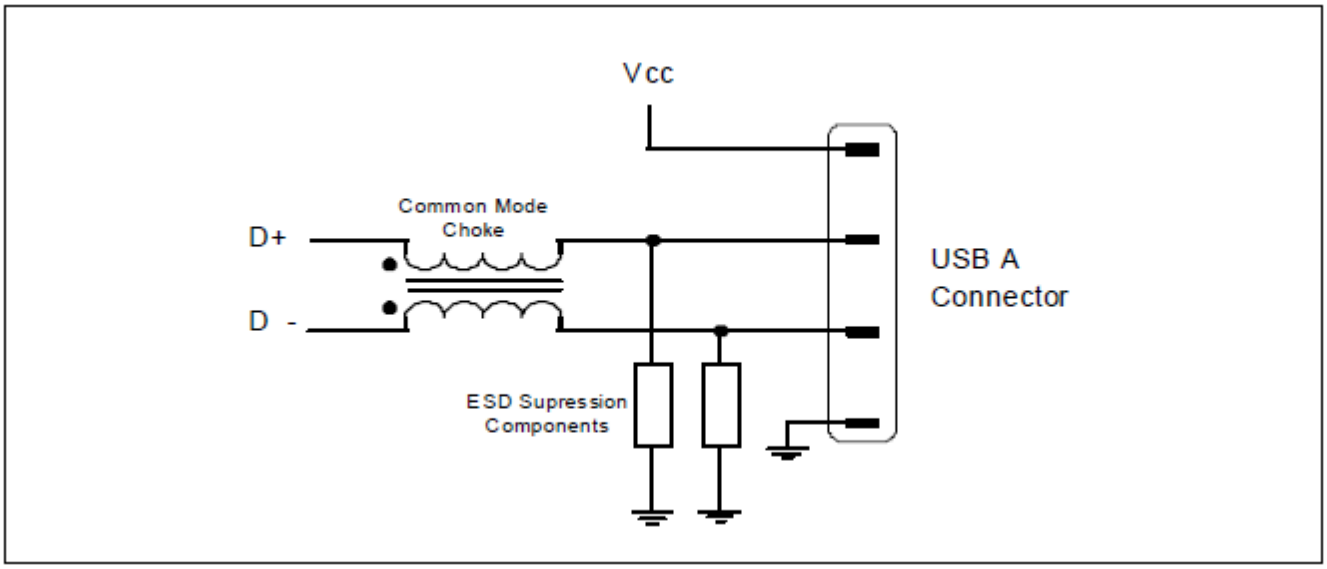
Figure 7: USB 2.0 Good Downstream Power Connection



2.6.2.3 USB 2.0 Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design should include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. Below figure shows the schematic of a typical common mode choke and ESD suppression components. Place the choke as close as possible to the USB connector signal pins.

Figure 8: USB 2.0 A Common Mode Choke



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases the distortion increases, therefore test the effects of the common mode choke on full speed and high-speed signal quality. Common mode chokes with a target impedance of 80 Ω to 90 Ω, at 100 MHz, generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process:

1. Choose a part with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that should be suppressed.
2. After obtaining a part that gives passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed, and highspeed USB operation.

Further common mode choke information can be found on the high-speed USB Platform Design Guides available at www.usb.org.

2.6.2.4 EMI / ESD Protection

To improve the EMI behavior of the USB interface, a design should include common

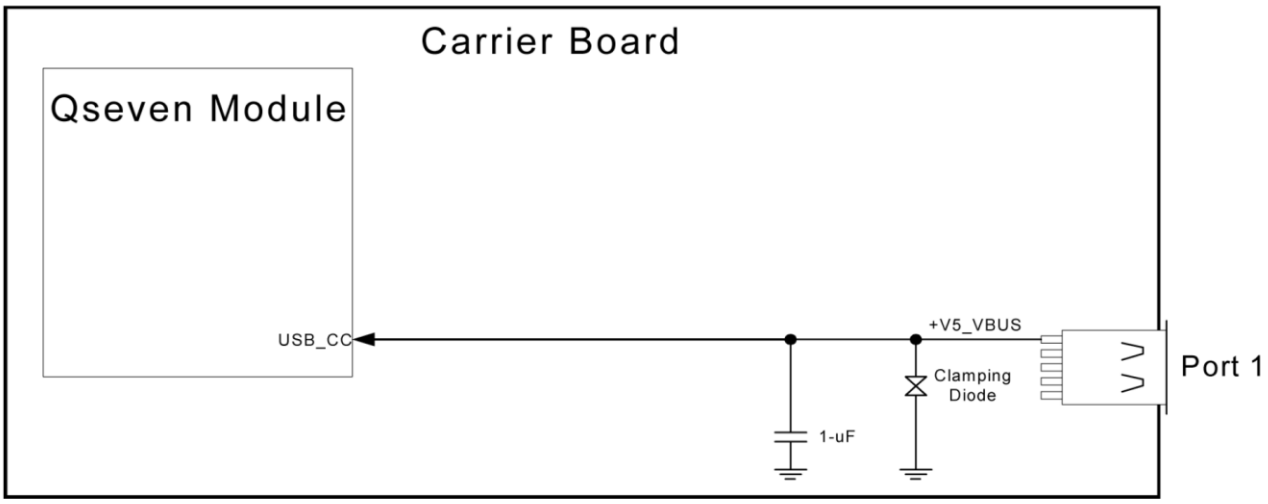
mode chokes, which have to be placed as close as possible to the USB connector signal pins.
Common mode chokes can provide required noise attenuation but they also distort the signal quality of full-speed and high-speed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the Carrier Board design.

To protect the USB host interface of the Module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes have to be implemented on the Carrier Board design.

2.6.2.5 USB Client Considerations

Precautions at the carrier board level must be taken to protect against voltage spikes and ESD to ensure robust operation of the host detection circuitry after multiple connect/disconnect events. A clamping diode may be used to minimize ESD, and a bulk capacitor should be placed on +5V USB client rail to avoid excessive voltage spikes.
Level Shifter removed for Qseven Specification 2.0 – please check for compatibility with old 1.2 designs

Figure 9: USB Client Connect Protection



Note:

In the errata sheet 1 for the Qseven Specification Rev 2.0 the USB_CC signal is redefined to be the USB_VBUS signal. So there is no level shifter circuit needed on the USB_CC signal. The module's USB_VBUS input is directly connected to the +5V Vbus Signal on the connector on the carrier board.

2.6.3 USB2.0 Trace Length Guidelines

Figure 10: Topology for USB2.0

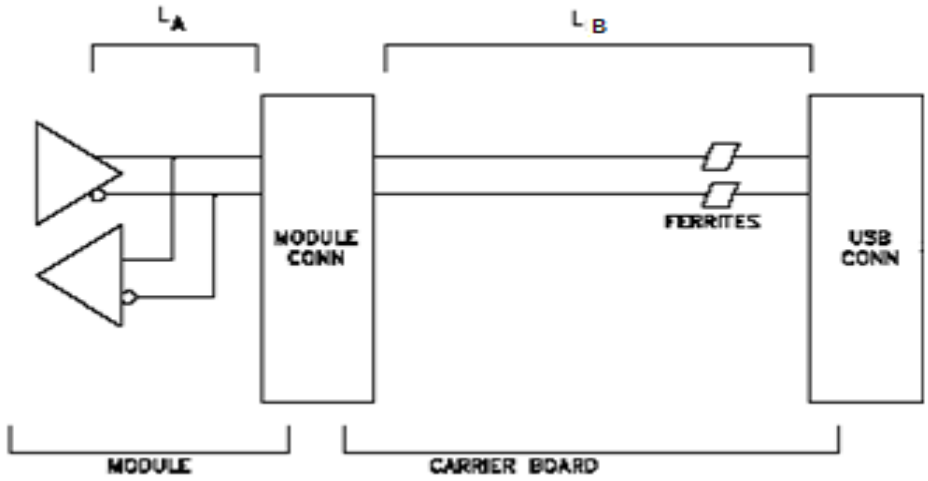


Table 10: USB2.0 Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	USB[7:0]+, USB[7:0]-	1
Differential Impedance Target	90 Ω ±10%	
Single End	45Ω ±10%	
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20 mils	
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	14”	
Length matching	Differential pairs (intra-pair): Max. ±5 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Try to minimize number of vias	

Notes:

1. There are 6 USB ports on the SOM-3567.

2.7 USB3.0

USB 3.0 is the third major revision of the Universal Serial Bus (USB) standard for computer connectivity. It adds a new transfer speed called SuperSpeed (SS) to the already existing LowSpeed (LS), FullSpeed (FS) and HighSpeed (HS).

USB 3.0 leverages the existing USB 2.0 infrastructure by adding two additional data pair lines to allow a transmission speed up to 5 Gbit/s, which is 10 times faster than USB 2.0 with 480 Mbit/s.

The additional data lines are unidirectional instead of the bidirectional USB 2.0 data lines. USB 3.0 is fully backward compatible to USB 2.0. USB 3.0 connectors are different from USB 2.0 connectors. The USB 3.0 connector is a super set of a USB 2.0 connector, with 4 additional pins that are invisible to USB 2.0 connectors. A USB 2.0 Type A plug may be used in a USB 3.0 Type A receptacle, but the USB 3.0 SuperSpeed functions will not be available.

2.7.1 USB3.0 Signal Definitions

Table 11: USB3.0 Signal Definitions

Signal	Pin#	Description	I/O	Note
USB_P4+ USB_P4- / USB_SSRX1+ USB_SSRX1- For R2.0 USB_SSRX2+ USB_SSRX2- For R2.1	84 82	USB Port 1, SuperSpeed RX + USB Port 1, SuperSpeed RX – Carrier Board: Device - Connect AC Coupling Capacitors 100nF near COME to StdA_SSTX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 6 StdA_SSRX+ / Pin 5 StdA_SSRX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	I USB Super Speed	1
USB_P5+ USB_P5- / USB_SSTX1+ USB_SSTX1- For R2.0	83 81	USB Port 1, SuperSpeed TX + USB Port 1, SuperSpeed TX – Module has integrated AC Coupling Capacitors Carrier Board: Device - Connect to StdA_SSRX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and	O USB Super Speed	1

USB_SSTX2+ USB_SSTX2- For R2.1		USB3.0 ESD suppressors to GND to Pin 9 StdA_SSTX+ / Pin 8 StdA_SSTX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used		

Signal	Pin#	Description	I/O	Note
USB_P6+ USB_P6- / USB_SSRX0+ USB_SSRX0-	78 76	USB Port 0, SuperSpeed RX + USB Port 0, SuperSpeed RX – Carrier Board: Device - Connect AC Coupling Capacitors 100nF near COME to StdA_SSTX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 6 StdA_SSRX+ / Pin 5 StdA_SSRX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	I USB Super Speed	2
USB_P7+ USB_P7- / USB_SSTX0+ USB_SSTX0-	77 75	USB Port 0, SuperSpeed TX + USB Port 0, SuperSpeed TX – Module has integrated AC Coupling Capacitors Carrier Board: Device - Connect to StdA_SSRX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 9 StdA_SSTX+ / Pin 8 StdA_SSTX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	O USB Super Speed	2
USB_SSTX1+ USB_SSTX1- For R2.1	134 132	USB Port 1, SuperSpeed TX + USB Port 1, SuperSpeed TX – Module has integrated AC Coupling Capacitors Carrier Board: Device - Connect to StdA_SSRX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 9 StdA_SSTX+ / Pin 8 StdA_SSTX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	O USB Super Speed	3
USB_SSRX1+ USB_SSRX1- For R2.1	146 144	USB Port 1, SuperSpeed RX + USB Port 1, SuperSpeed RX – Carrier Board:	I USB Super	3

		Device - Connect AC Coupling Capacitors 100nF near COME to StdA_SSTX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 6 StdA_SSRX+ / Pin 5 StdA_SSRX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	Speed	

Notes:

1. USB 2.0 Port 4 and Port 5 are used on SOM-3567.
2. SOM-3567 is only support USB3.0 Port 0.
3. SOM-3567 is NC.

2.7.1.1 USB Over-Current Protection (USB_x_y_OC#)

The USB Specification describes power distribution over the USB port, which supplies power for
USB devices that are directly connected to the Carrier Board. Therefore, the host must implement over-current protection on the ports for safety reasons. Should the aggregate current drawn by the downstream ports exceed a permitted value, the over-current protection circuit removes power from all affected downstream ports. The over-current limiting mechanism must be resettable without user mechanical intervention. For more detailed information about this subject, refer to the 'Universal Serial Bus Specifications Revision 2.0', which can be found on the website http://www.usb.org.

Over-current protection for USB ports can be implemented by using power distribution switches on the Carrier Board that monitor the USB port power lines. Power distribution switches usually have a soft-start circuitry that minimizes inrush current in applications where highly capacitive loads are employed. Transient faults are internally filtered.

Additionally, they offer a fault status output that is asserted during over-current and thermal shutdown conditions. These outputs should be connected to the corresponding COM Express Modules USB over-current sense signals. Fault status signaling is an option at the USB specification. If you don't need the popup message in your OS you may leave the signals USB_0_1_OC#, USB_2_3_OC#, USB_4_5_OC# and USB_6_7_OC# unconnected.

Fault status signals are connected by a pullup resistor to VCC_3V3_SBY on COM Express Module. Please check your tolerance on a USB port with VCC_5V supply.

USB 2.0 port's VCC current limit should be set to 500mA. For USB 3.0 implementations, the VCC current limit is raised to 1A. A different, USB 3.0 compatible, power switch is used.

2.7.1.2 EMI / ESD Protection

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins.

Common mode chokes can provide required noise attenuation but they also distort the signal quality of FullSpeed, HighSpeed and SuperSpeed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the Carrier Board design.

To protect the USB host interface of the Module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes have to be implemented on the Carrier Board design.

2.7.2 USB3.0 Trace Length Guidelines

Figure 11: Topology for USB3.0

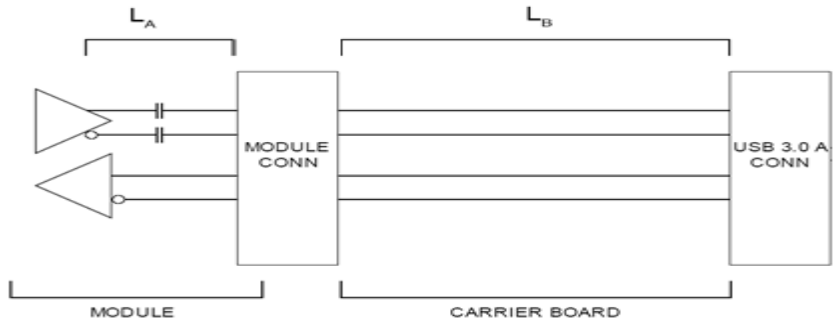


Table 12: USB3.0 Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	USB3.0	
Differential Impedance Target	85 Ω ±10%	

Single End	50Ω ±10%	
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20 mils	
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	9”	
Length matching	Differential pairs (intra-pair): Max. ±5 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Max. 2 vias per differential signal trace	

Notes:

2.8 SDIO Interface

SDIO (Secure Digital I/O) provides an easy to implement solution for high-speed data I/O combined with low power consumption. SDIO cards are fully compatible with SD memory cards. This includes mechanical, electrical, power, signaling and software compatibility. SDIO hosts are able to drive SD cards and MMC (MultiMediaCards) as well as SDIO cards that provide functions such as Ethernet or WLAN, GPS receivers, Bluetooth, modems etc.

The Qseven specification defines one optional 8-bit SDIO interface on the module.

2.8.1 SDIO Signal Definitions

SDIO stands for Secure Digital Input Output. Devices that support SDIO can use small devices such as SD-Card or MMC-Card flash memories.

Table 13: Signal Definition SDIO

Signal	Pin#	Description	I/O	Notes
SDIO_CD#	43	SDIO Card Detect. This signal indicates	I/O 3.3V	

		when a SDIO/MMC card is present. Carrier Board: Connect to CD# of SDIO/MMC device or card N/C if not used	CMOS	
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz Carrier Board: Connect to CLK of SDIO/MMC device or card N/C if not used	O 3.3V CMOS	
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Carrier Board: Connect to CMD of SDIO/MMC device or card N/C if not used	I/O 3.3V CMOS	
SDIO_LED for R2.0 / Reserved for R2.1	44	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus. Carrier Board: Connect to inverter circuit to LED and current limiting resistors 250 to 330 Ω to 3.3V N/C if not used.	O 3.3V CMOS Max 1mA	2
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. Carrier Board: Connect to WP of SDIO/MMC device or card	I/O 3.3V CMOS	

		N/C if not used		
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device. Carrier Board: Connect to power enable of power distribution switch (with short circuit and thermal protection) N/C if not used	O 3.3V CMOS	
SDIO_DAT0-7 For R2.0	48 to 55	SDIO Data lines. These signals operate in push-pull mode. Carrier Board: Connect to DATA0-7 of SDIO/MMC device or card N/C if not used	I/O 3.3V CMOS PP	3
Reserved For R2.1	52 to 55	Reserved. Do not connect.		

Note:

1. *If the SDIO presence LED is located on the carrier board a pulldown resistor is required on the carrier board.*
2. SOM-3567 is NC.
3. DAT4-7 pins are NC on the SOM-3567.

2.8.2 SDIO Interface Routing Guidelines

Figure 12: Topology for SDIO

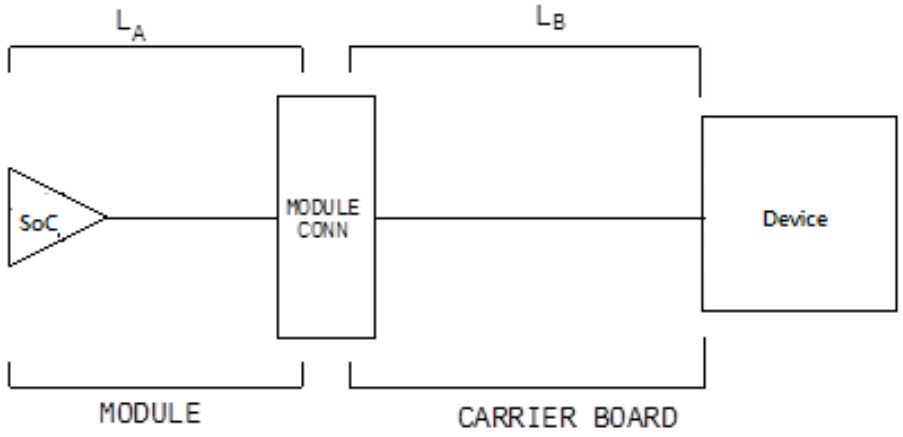


Table 14: SDIO Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SDIO	
Single End	50Ω ±10%	
DATA to CLK Maximum Pin to Pin Length Mismatch	500 mils	
Main Route segment for CMD/Data/CD#	Minimum Trace Spacing Between Other SD Card and Interface Signals 5 mils	
Main Route segment for CLK)	Minimum Trace Spacing Between Other SD Card and Interface Signals 15mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	5”	
Length matching	Data to Clock must be matched within 500mils	
Reference Plane	GND referencing preferred. Min 20-mil trace edge-to-major plane edge spacing.	

Notes:

2.9 High Definition Audio / AC97 / I?S Audio Signals

Since Version 2.0Qseven modules support either High Definition Audio (HDA), AC'97 or I²S for implementing audio functionality.

2.9.1 Audio Codec Signal Descriptions

Table 15: Audio Codec Signal Descriptions

Signal	Pin#	Description	I/O	Note
AC/HDA_RST#	61	HD Audio/AC'97/I²S Codec Reset. Carrier Board: AC97 - Connect 0 Ω in series to CODEC pin 11 RESET# HDA - Connect 0 Ω in series to CODEC pin 11 RESET# N/C if not used	O 3.3V CMOS	
AC/HDA_SYNC	59	Serial Sample Rate Synchronization. Carrier Board: AC97 - Connect 0 Ω in series to CODEC pin 10 SYNC HDA - Connect 0 Ω in series to CODEC pin 10 SYNC N/C if not used	O 3.3V CMOS	
AC/HDA_BITCLK	63	Serial Bit Clock for HDA CODEC. Carrier Board: AC97 - Connect 33-47 Ω in series to CODEC pin 6 BIT_CLK HDA - Module has integrated series resistor. Connect 0 Ω in series to CODEC pin 6 BIT_CLK N/C if not used	O 3.3V CMOS	
AC/HDA_SDO	67	Audio Serial Data Output Stream. Carrier Board: AC97 - Connect 33-47 Ω in series to CODEC pin 8 SDATA_IN HDA - Connect 33-47 Ω in series and PD 10KΩ(NL) to CODEC pin 8 SDATA_IN N/C if not used	O 3.3V CMOS	

AC/HDA_SDI	65	Audio Serial Data Input Stream from CODEC. Carrier Board: AC97 - Connect 33-47 Ω in series to CODEC pin 8 SDATA_IN HDA - Connect 33-47 Ω in series and PD 10KΩ(NL) to CODEC pin 8 SDATA_IN N/C if not used	I 3.3V CMOS	

Note:

1. *I/O Orientation: Input denotes a signal flow to the module and output denotes a signal flow from the module.*
2. *The High Definition Audio interface found on the Qseven* module complies with Intel High Definition Audio Specification 1.0.
3. *HD Audio is primarily intended for use with x86 products.*

2.9.2 Audio Routing Guidelines

The implementation of proper component placement and routing techniques will help to ensure that the maximum performance available from the codec is achieved. Routing techniques that should be observed include properly isolating the codec, associated audio circuitry, analog power supplies and analog ground planes from the rest of the Carrier Board. This includes split planes and the proper routing of signals not associated with the audio section.

The following is a list of basic recommendations:

Traces must be routed with a target impedance of 50Ω with an allowed tolerance of ± 15%.

Ground return paths for the analog signals must be given special consideration.

Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Locate the analog and digital signals as far as possible from each other.

Partition the Carrier Board with all analog components grouped together in one area and all digital components in another.

Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.

Provide separate analog and digital ground planes with the digital components over the digital ground plane, and the analog components, including the analog power regulators,

over the analog ground plane. The split between the planes must be a minimum of 0.05 inch wide.

Route analog power and signal traces over the analog ground plane.

Route digital power and signal traces over the digital ground plane.

Position the bypassing and decoupling capacitors close to the IC pins with wide traces to reduce impedance.

Place the crystal or oscillator (depending on the codec used) as close as possible to the codec.

(HDA implementations generally do not require a crystal at the codec)

Do not completely isolate the analog/audio ground plane from the rest of the Carrier Board ground plane. Provide a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between the planes must be a minimum of 0.05 inch wide.

Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main Carrier Board ground. That is, no signal should cross the split/gap between the ground planes, because this would cause a ground loop, which in turn would greatly increase EMI emissions and degrade the analog and digital signal quality.

2.9.3 Audio Trace Length Guidelines

Figure 13: Topology for Audio

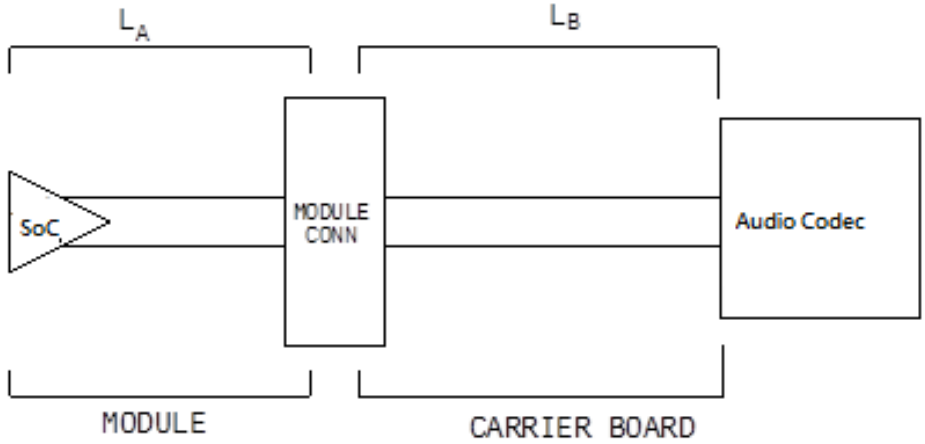


Table 16: Audio Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	Audio	
Single End	50Ω ±15%	
Nominal Trace Space within Audio Signal Group	Min. 15mils	
Spacing to Other Signal	Min. 20mils	

Group		
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	9”	
Length matching	Data to Clock must be matched within 500mils	
Reference Plane	GND referencing preferred. Min 20-mil trace edge-to-major plane edge spacing.	

Notes:

2.10 LVDS

The Qseven 2.0 specification defines a LVDS flat panel interface that optionally supports up to two 24-bit LVDS channels. It permits dual pixel, two channel data transmission between the host and flat panel display. Each LVDS channel consists of up to five LVDS signal pairs transmitting a serial bit stream directly to a LVDS flat panel or to an external LVDS receiver. Additional control signals, as well as a dedicated I²C bus interface, are specified to control flat panel attributes. This dedicated I²C bus can be used to connect an external I²C EEPROM containing the specific timing data of the flat panel display.

2.10.1 Signal Definitions

Table 17: LVDS Signal Definitions

Signal	Pin#	Description	I/O	Note
LVDS_A0+ LVDS_A0-	99 101	LVDS channel A differential signal pair 0 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever - RXinO0+/- with 100Ω termination	O LVDS	

		Conn. - RXinO0+/- N/C if not used		
LVDS_A1+ LVDS_A1-	103 105	LVDS channel A differential signal pair 1 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinO1+/- with 100Ω termination Conn. – RxinO1+/- N/C if not used	O LVDS	
LVDS_A2+ LVDS_A2-	107 109	LVDS channel A differential signal pair 2 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinO2+/- with 100Ω termination Conn. – RxinO2+/- N/C if not used	O LVDS	
LVDS_A3+ LVDS_A3-	113 115	LVDS channel A differential signal pair 3 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinO3+/- with 100Ω termination Conn. – RxinO3+/- N/C if not used	O LVDS	

Signal	Pin#	Description	I/O	Note
LVDS_A_CK+ LVDS_A_CK-	119 121	LVDS channel A differential clock pair Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever - RXOC+/- with 100Ω termination Conn. - RXOC+/- N/C if not use	O LVDS	
LVDS_B0+ LVDS_B0-	100 102	LVDS channel B differential signal pair 0 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever - RXinE0+/- with 100Ω termination Conn. - RXinE0+/- N/C if not used	O LVDS	

LVDS_B1+ LVDS_B1-	104 106	LVDS channel B differential signal pair 1 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinE1+/- with 100Ω termination Conn. – RxinE1+/- N/C if not used	O LVDS	
LVDS_B2+ LVDS_B2-	108 110	LVDS channel B differential signal pair 2 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinE2+/- with 100Ω termination Conn. – RxinE2+/- N/C if not used	O LVDS	
LVDS_B3+ LVDS_B3-	114 116	LVDS channel B differential signal pair 3 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinE3+/- with 100Ω termination Conn. – RxinE3+/- N/C if not used	O LVDS	
LVDS_B_CK+ LVDS_B_CK-	120 122	LVDS channel B differential clock pair Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever - RXEC+/- with 100Ω termination Conn. - RXEC+/- N/C if not used	O LVDS	

Signal	Pin#	Description	I/O	Note
LVDS_PPEN	111	LVDS flat panel power enable. Carrier Board: Connect to enable control of LVDS panel power circuit. N/C if not used	O 3.3V, CMOS	
LVDS_BKLEN	112	LVDS flat panel backlight enable high active signal Carrier Board:	O 3.3V, CMOS	

		Connect to enable control of LVDS panel backlight power circuit. N/C if not used		
LVDS_BLT_CTRL	123	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this purpose it can be used as General Purpose PWM Output. Carrier Board: Connect to brightness control of LVDS panel backlight power circuit. N/C if not used	O 3.3V, CMOS	
LVDS_DID_CLK / GP_I2C_CLK	127	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used it can be used as General Purpose I²C bus clock line. Carrier Board: Connect to DDC clock of LVDS panel N/C if not used	O 3.3V, OD CMOS	
LVDS_DID_DAT / GP_I2C_DAT	125	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be used as General Purpose I²C bus data line. Carrier Board: Connect to DDC data of LVDS panel N/C if not used	I/O 3.3V, OD CMOS	

Signal	Pin#	Description	I/O	Note
LVDS_BLC_CLK	128	Control clock signal for external SSC clock chip. Carrier Board: Connect to SSC clock of external clock chip N/C if not used	I/O 3.3V, OD CMOS	1
LVDS_BLC_DAT	126	Control data signal for external SSC clock chip. Carrier Board:	I/O 3.3V, OD	1

		Connect to SSC data of external clock chip N/C if not used	CMOS	

Note:

1. SOM-3567 is NC.

2.10.1.1 Display Timing Configuration

The graphic controller needs to be configured to match the timing parameters of the attached flat panel display. To properly configure the controller, there needs to be some method to determine the display parameters. Different Module vendors provide differing ways to access display timing parameters. Some vendors store the data in non-volatile memory with the BIOS setup screen as the method for entering the data, other vendors might use a Module or Carrier based EEPROM. Some vendors might hard code the information into the BIOS, and other vendors might support panel located timing via the signals LVDS_I2C_CLK and LVDS_I2C_DAT with an EEPROM strapped to 1010 000x. Regardless of the method used to store the panel timing parameters, the video BIOS will need to have the ability to access and decode the parameters. Given the number of variables it is recommended that Carrier designers contact Module suppliers to determine the recommend method to store and retrieve the display timing parameters.

The Video Electronics Standards Association (VESA) recently released DisplayID, a second generation display identification standard that can replace EDID and other proprietary methods for storing flat panel timing data. DisplayID defines a data structure which contains information such as display model, identification information, colorimetry, feature support, and supported timings and formats. The DisplayID data allows the video controller to be configured for optimal support for the attached display without user intervention. The basic data structure is a variable length block up to 256 bytes with additional 256 byte extensions as required. The DisplayID data is typically stored in a serial EPROM connected to the LVDS_I2C bus. The EPROM can reside on the display or Carrier. DisplayID is not backwards compatible with EDID. Contact VESA (www.vesa.org) for more information.

2.10.1.2 Backlight Control

Backlight inverters are either voltage, PWM or resistor controlled. The Qseven specification provides two methods for controlling the brightness. One method is to use the backlight control and enable signals from the CPU chipset. These signals are brought on Qseven LVDS_BKLEN and LVDS_BLT_CTRL. LVDS_BLT_CTRL is a Pulse Width Modulated (PWM) output that can be connected to display inverters that accept a PWM input. The second method it to use the LVDS I2C bus to control an LVDS I2C DAC. The output of the DAC can be used to support voltage controlled inverters. The DAC can be used driving the backlight voltage control input pin of the inverter.

2.10.2 LVDS Routing Guidelines

Route LVDS signals as differential pairs (excluding the five single-ended support signals), with a 100-Ω differential impedance and a 55-Ω, single-ended impedance. Ideally, a LVDS pair is routed on a single layer adjacent to a ground plane. LVDS pairs should not cross plane splits. Keep layer transitions to a minimum. Reference LVDS pairs to a power plane if necessary. The power plane should be well-bypassed.

Length-matching between the two lines that make up an LVDS pair (“intra-pair”) and between different LVDS pairs (“inter-pair”) is required. Intra-pair matching is tighter than the inter-pair matching.
All LVDS pairs should have the same environment, including the same reference plane and the same number of vias.

2.10.3 LVDS Trace Length Guidelines

Figure 14: Topology for LVDS

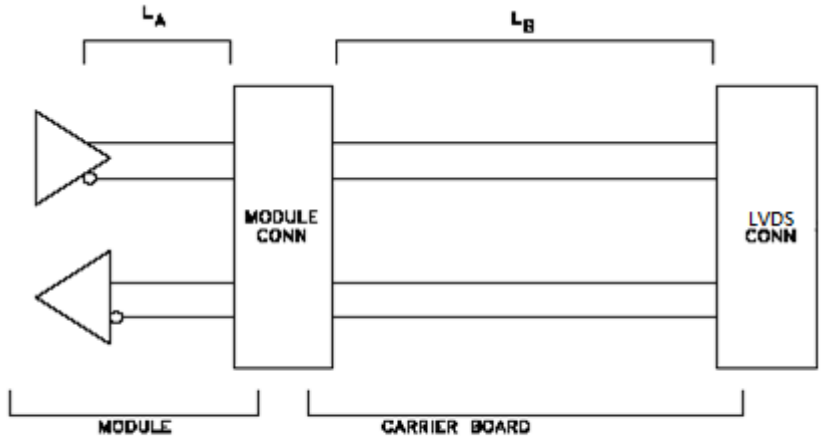


Table 18: LVDS Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	LVDS	
Differential Impedance Target	85 Ω ±10%	
Single End	55Ω ±10%	
Signal length to the LVDS connector available for the COM Express Carrier Board	6.75”	
Spacing between pair to pairs (inter-pair) (s)	Min. 20 mils	
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-3867 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	8.75”	

Length matching	Differential pairs (intra-pair): Max. ±20 mils Clock and data pairs (intra-pair): Max. ±20 mils data pairs (inter-pair) : Max. ±40 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Max. of 2 vias per line.	

Notes:

2.11 Embedded DisplayPort (eDP) *SOM-3567 is not support

Qseven Rev 2.0 modules optionally support up to two Embedded DisplayPort (eDP) Version 1.2 interfaces. These interfaces are shared with LVDS signals.

eDP is an open, industry standard digital display interface that is under development within the Video Electronics Standards Association (VESA). The eDP specification defines a scalable digital display interface. It defines a license-free, royalty-free, state-of-the-art digital video interconnect intended to be used primarily between a computer and its internal display(s). The eDP interface supports 1, 2, or 4 data pairs that carry the video signal and embeds the clock in the data signal. The eDP interface is designed to replace LVDS as an internal Graphics interface in the coming years. Benefits are embedded clock, higher data rates and less data lines than with LVDS. EDP support is offered by ARM and x86 processor based platforms, depending on the selected processor. AC coupling is provided on the module. If the eDP display interface of the Qseven module is not implemented, all signals associated with this interface should be left open.

2.11.1 eDP Signal Definitions

Table 19: eDP Signal Definitions

Signal	Pin#	Description	I/O	Note
eDP0_TX0+ eDP0_TX0-	99 101	eDP0 lane 0, TX +/- Carrier Board: N/C if not used	O PCIe	1
eDP0_TX1+ eDP0_TX1-	103 105	eDP0 lane 1, TX +/- Carrier Board: N/C if not used	O PCIe	1
eDP0_TX2+	107	eDP0 lane 2, TX +/-	O PCIe	1

eDP0_TX2-	109	Carrier Board: N/C if not used		
eDP0_TX3+ eDP0_TX3-	113 115	eDP0 lane 3, TX +/- Carrier Board: N/C if not used	O PCIe	1
eDP0_AUX+ eDP0_AUX-	119 121	eDP0 auxiliary lane +/- Carrier Board: Connect to device or eDP connector. N/C if not used.	I/O PCIe	1
eDP0_HPD	126	eDP0 Detection of Hot Plug / Unplug and notification of the link layer Carrier Board: Connector to device or eDP connector HP pin.	I CMOS OD	1

Signal	Pin#	Description	I/O	Note
eDP1_TX0+ eDP1_TX0-	100 102	eDP1 lane 0, TX +/- Carrier Board: N/C if not used	O PCIe	1
eDP1_TX1+ eDP1_TX1-	104 106	eDP1 lane 1, TX +/- Carrier Board: N/C if not used	O PCIe	1
eDP1_TX2+ eDP1_TX2-	108 110	eDP1 lane 2, TX +/- Carrier Board: N/C if not used	O PCIe	1
eDP1_TX3+ eDP1_TX3-	114 116	eDP1 lane 3, TX +/- Carrier Board: N/C if not used	O PCIe	1
eDP1_AUX+ eDP1_AUX-	120 122	eDP1 auxiliary lane +/- Carrier Board: Connect to device or eDP connector. N/C if not used.	I/O PCIe	1
eDP1_HPD	128	eDP1 Detection of Hot Plug / Unplug and notification of the link layer Carrier Board: Connector to device or eDP connector HP pin.	I CMOS OD	1
eDP_PPEN	111	eDP power enable Carrier Board:	O CMOS	1

		Connect to enable control of eDP panel power circuit. N/C if not used		
eDP_BLEN	112	eDP backlight enable Carrier Board: Connect to enable control of eDP panel backlight power circuit. N/C if not used	O CMOS	1
eDP_BLT_CTRL	123	eDP backlight brightness control Carrier Board: Connect to brightness control of eDP panel backlight power circuit. N/C if not used	O CMOS	1

Notes:

1. SOM-3567 is not support eDP interface.

2.11.2 eDP Implementation Guidelines

Many carrier board designs do not need the full range of eDP performance offered by Qseven modules. It depends on the flat panel configuration of the Qseven module, as well as the carrier board design, as to how many eDP lanes are supported. In this case all unused eDP signal lanes should be left open on the carrier board. If the eDP display interface of the Qseven module is not implemented at all, non-shared signals associated with this interface should be left open.

2.11.3 eDP Trace Length Guidelines

Figure 15: Topology for eDP

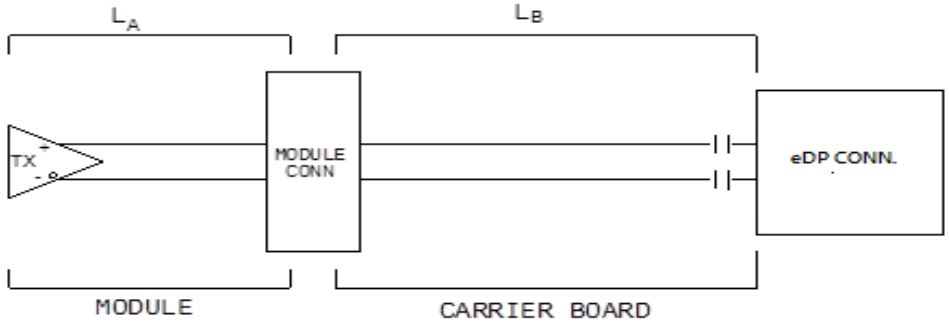


Table 20: DisplayPort Connector / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes

Signal Group	eDP	1
Differential Impedance Target	85 Ω ±10%	1
Single End	55Ω ±10%	1
Isolation to equivalent pairs	20 mils (MS) and 15 mils (DS)	1
Isolation to other signal groups	20 mils (MS) and 15 mils (DS)	1
LA	SOM-3567 is not support.	1
LB	Carrier Board Length	1
Max length of LA+LB	eDP differential pairs to eDP connector: AUX channel:	1
Length matching	Differential pairs (intra-pair): Max. ±5 mils For each channel, match the lengths of the differential pairs (Inter-Pair) to be within a 1-inch window (max length – min length < 1 inch (2.54 cm)).	1
Reference Plane	GND referencing preferred. Min 40-mil trace edge-to-major plane edge spacing.	1
Carrier Board Via Usage	Max. 2 vias.	1

Notes:

1. SOM-3567 is not support eDP interface.

2.12 DisplayPort Interfaces

2.12.1 DisplayPort Interface Signals (from Module)

Qseven Rev 2.0 modules optionally support one DisplayPort Version 1.2 interface. This interface is shared with TMDS signals.

DisplayPort is an open, industry standard digital display interface that is under development within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect intended to be used primarily between a computer and its display monitor.

The DisplayPort interface supports 1, 2, or 4 data pairs that carry the video signal, clock and optional audio signals. The video signal of the DisplayPort interface is not compatible with DVI or HDMI but a DisplayPort connector can pass these signals through. While DVI

and HDMI require separate clock signals, DisplayPort embeds the clock in the data signal. Unlike the separate DVI/HDMI and LVDS standards, DisplayPort supports both external (monitor) or internal (LCD panel) display connections.

Display Port++ (also known as dual-mode DisplayPort) output signals can easily provide the lower voltages required for Display Port using a passive adapter. This enables cost-efficient direct support for single-link HDMI and DVI signals. Dual-mode chipsets are able to detect when a DVI or HDMI passive adapter is connected and then switch to DVI/HDMI mode using the 4-lane main DisplayPort link and the AUX channel link to transmit 3 TMDS signals, clock and display data channel Data and Clock. Dual-mode compatible devices are recognizable by the DP++ logo.

Note:

1. AC coupling is provided on the module for the main link, auxiliary channel needs AC coupling on the carrier board.

2. DP/DP++ use the same (shared) pins as TMDS to transmit the DP/DP++ graphics signals (see Table21).

Table 21: Signal Definition DisplayPort

Signal	Shared With	Pin#	Description	I/O	Notes
DP_LANE3- DP_LANE3+	TMDS_CLK- TMDS_CLK+	133 131	DisplayPort differential pair lines lane 3. Carrier Board: Device - Connect to DisplayPort0 receiver ML_Lane 3(p), ML_Lane 3(n). DisplayPort - Connect to DisplayPort0 Conn pin 10 ML_Lane 3(p), pin 12 ML_Lane 3(n) and ESD protection N/C if not used.	O PCIE	

DP_LANE2- DP_LANE2+	TMDS_LANE0- TMDS_LANE0+	145 143	DisplayPort differential pair lines lane 2. Carrier Board: Device - Connect to DisplayPort0 receiver ML_Lane 2(p), ML_Lane 2(n). DisplayPort - Connect to DisplayPort0 Conn pin 7 ML_Lane 2(p), pin 9 ML_Lane 2(n) and ESD protection N/C if not used.	O PCIE	
DP_LANE1- DP_LANE1+	TMDS_LANE1- TMDS_LANE1+	139 137	DisplayPort differential pair lines lane 1. Carrier Board: Device - Connect to DisplayPort0 receiver ML_Lane 1(p), ML_Lane 1(n). DisplayPort - Connect to DisplayPort0 Conn pin 4 ML_Lane 1(p), pin 6 ML_Lane 1(n) and ESD protection N/C if not used.	O PCIE	
DP_LANE0- DP_LANE0+	TMDS_LANE2- TMDS_LANE2+	151 149	DisplayPort differential pair lines lane 0. Carrier Board: Device - Connect to DisplayPort0 receiver ML_Lane 0(p), ML_Lane 0(n). DisplayPort - Connect to DisplayPort0 Conn pin 1 ML_Lane 0(p), pin 3 ML_Lane 0(n) and ESD protection N/C if not used.	O PCIE	
	GP_1-Wire_Bus / HDMI_CEC for R2.1	124	General Purpose 1-Wire bus interface. Can be used for consumer electronics control bus (CEC) of HDMI	IO 3.3V COMS	1

Signal	Pin#	Description	I/O	Notes
DP_AUX- DP_AUX+	140 138	Auxiliary channel used for link management and device control. Differential pair lines. Carrier Board: Device - Connect AC Coupling cap 0.1uF in series to DisplayPort0 receiver AUX CH(p) and AUX CH(n). DisplayPort - Connect AC Coupling cap 0.1uF in series	I/O PCIE	

		to DisplayPort0 Conn pin 15 AUX CH(p), PD 100KΩ to GND and ESD protection Connect AC Coupling cap 0.1uF in series to DisplayPort0 Conn pin 17 AUX CH(n), PU 100KΩ to 2.5V~3.3V and ESD protection N/C if not used.		
DP_HDMI_HPD# for R2.0 HDMI_HPD# for R2.1	153	Hot plug detection signal that serves as an interrupt request. Carrier Board: Module has integrated current blocking circuit or Logic inversion and PD resistor to GND Connect to Device - TMDS device TMDS_HPD DVI - DVI Conn pin 16 Hot Plug Detect HDMI - HDMI Conn pin 19 Hot Plug Detect N/C if not used.	I 3.3V COMS	
DP_HPD#	154	Hot plug detection signal that serves as an interrupt request. Carrier Board: Device - Connect to DisplayPort0 device Hot Plug Detect DisplayPort - Connect to DisplayPort0 Conn pin 18 Hot Plug Detect N/C if not used.	I 3.3V COMS	1

Notes:

1. SOM-3567 is NC.

2.12.2 DisplayPort Interfaces Routing Guidelines

2.12.2.1 DisplayPort Routing Guidelines

Carriers that support DisplayPort (DisplayPort only or dual mode):

- DC blocking capacitors shall be placed on the Carrier for the DP_PAIR[0:3] signals.
- The Carrier shall include a blocking FET on DP_HPD to prevent back-drive current from damaging the Module.

When implementing DisplayPort on the Carrier Board, the DP_AUX+ line shall have a pulldown resistor to GND. The resistor value should be 100kΩ. The DP_AUX- line shall have a pull-up resistor to 2.5V. The resistor value should be 100kΩ. The DP_HPD signal shall include a blocking FET to prevent back-drive current damage. The DP_HPD signal shall be pulled-down to GND with a 110kΩ resistor.

The DP signals can be used to support a variety of video interfaces. The circuits required to realize the different video interfaces will be determined by a future Qseven Carrier Design Guide subcommittee. At this time, they only requirement placed on Modules for the DP signals is the maximum trace length specified.

Figure 16: Topology for DisplayPort

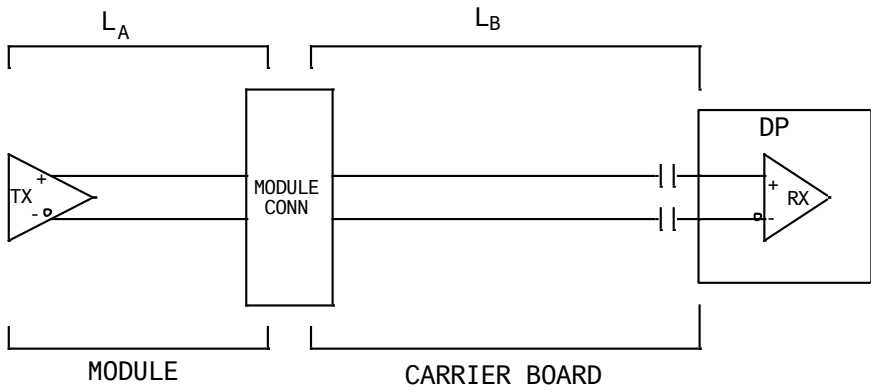


Table 22: DisplayPort Connector / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	DisplayPort	
Differential Impedance Target	85 Ω ±10%	
Single End	55Ω ±10%	
Spacing between pairs-to-pair	Min. 20mil	
Spacing between differential pairs and high-speed periodic signals	Min. 50mil	
Spacing between differential pairs and low-speed non periodic signals	Min. 20mil	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	DDI differential pairs to DP connector: 6.5” DDI differential pairs to Device Down: 6.5” AUX channel: 13”	
Length matching	Differential pairs (intra-pair): Max. ±5 mils For each channel, match the lengths of the differential pairs (Inter-Pair) to be within a 1-inch window (max length – min length < 1 inch (2.54 cm)).	
Reference Plane	GND referencing preferred. Min 40-mil trace edge-to-major plane edge spacing.	
Carrier Board Via Usage	Max. 2 vias.	
AC coupling capacitors (if required)	Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.	

Notes:

2.12.2.2 HDMI / DVI Routing Guidelines

High-Definition Multimedia Interface (HDMI) is a licenseable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is fully backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video. Additionally, HDMI adds the ability to send up to 8 separate channels of uncompressed digital audio and auxiliary control data during the horizontal and vertical blanking intervals of the TMDS video stream.

The Qseven specification defines a single-link HDMI interface with a pixel clock rate of up to 165 MHz. The appropriate TMDS receive and transmit differential signal pair, as well as additional control signals, can be found on the Qseven module edge connector. This interface is shared with the DisplayPort signals.

Figure 17: Topology for HDMI / DVI

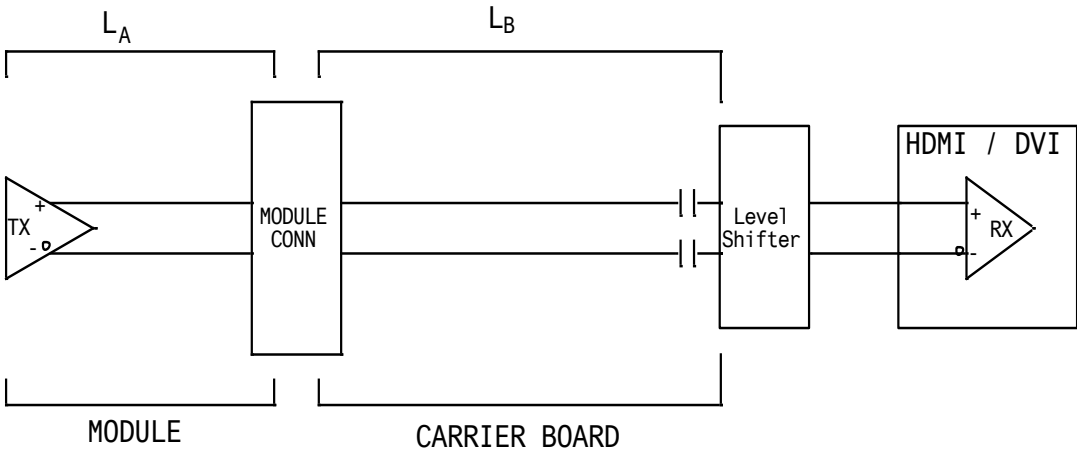


Table 23: HDMI / DVI Connector / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	HDMI / DVI (TMDS)	
Differential Impedance Target	85 Ω ±10%	
Single End	55Ω ±10%	
Spacing between pairs-to-pair	Min. 20mil	

Spacing between differential pairs and high-speed periodic signals	Min. 50mil	
Spacing between differential pairs and low-speed non periodic signals	Min. 20mil	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	DDI differential pairs to HDMI/DVI connector: 7.5” DDI differential pairs to Device Down: 7.5” AUX channel: 12.5”	
Length matching	Differential pairs (intra-pair): Max. ±5 mils For each channel, match the lengths of the differential pairs (Inter-Pair) to be within a 1-inch window (max length – min length < 1 inch (2.54 cm)). CTRDATA - CTRCLK < 1000	
Reference Plane	GND referencing preferred. Min 40-mil trace edge-to-major plane edge spacing.	
Carrier Board Via Usage	Max. 2 vias.	
AC coupling capacitors (if required)	Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.	

Notes:

2.12.3 HDMI / DVI Level Shifter Requirements

The HDMI specification requires the receiver to be terminated to AVCC (nominally 3.3 V) through Rt (nominally 50 Ω). The HDMI receiver requirements require the native HDMI signals from the SOC to be level shifted. This prevents electrical overstress of the driver and ensure that the receiver is operational within the receiver specifications defined in the *High Definition Multimedia Interface Specification 1.4a*.

2.12.4 ESD Protection

HDMI signals are subjected to ESD strikes due to plugging in of the devices through the HDMI cable and frequent human contact that can destroy both the HDMI host and devices on the platform. Therefore these ports need to be protected.

There are a wide variety of ESD protection devices and ESD suppressors readily available in the market such as Metal Oxide Varistors (MOVs), Zener Diode, Transient Voltage Suppressor (TVS), Polymer devices and ESD diode arrays. With 1.65 Gbps of data rate, HDMI is very sensitive to parasitic capacitance. Excessive parasitic capacitance can severely degrade the signal integrity and lead to a compliance or operational failure. To maintain signal integrity, Intel recommends to use ESD suppressors or diode arrays having a low junction capacitance.

Recommended characteristics of an ideal ESD Protection Diode for HDMI:

- Able to withstand at least 8 kV of ESD strikes.
- Low capacitance <1 pF to minimize signal distortion at high data rates as higher capacitance degrade the HDMI signal quality.
- Fast response/rise time to protect from the fast rise time of ESD surge pulses.
- Low-leakage current to minimize static power consumption.
- Ensure the selected ESD solution will not violate HDMI Voff spec. In a low power state a power rail ESD diode can become forward biased as a result on the HDMI sink (panel) termination of 50 Ω to 3.3 V
- Some ESD devices may impact the trace impedance. Care should be taken while choosing such devices so that the differential-impedance target in the *HDMI 1.4 Specification* is not violated.

The *HDMI 1.4a Specification* requires that 8 kV of ESD strikes be tolerated.

The ESD protection devices should be placed as close to the HDMI connector as possible so that when ESD strikes occur, the discharges can be quickly absorbed or diverted to the ground/power plane before it is coupled to another signal path nearby.
Footprints for ESD components or diode arrays can be provided on board with no stubs and no more than 750 mils (19.05 mm) from the connector. The ESD components can be stuffed depending on the requirement.

2.13 LPC Bus – Low Pin Count Interface

The Low Pin Count Interface was defined by Intel Corporation to facilitate the industry's transition towards legacy free systems. It allows the integration of low-bandwidth legacy I/O components within the system, which are typically provided by a Super I/O controller. Furthermore, it can be used to interface firmware hubs, Trusted Platform Module (TPM) devices and embedded controller solutions. Data transfer on the LPC bus is implemented over a 4 bit serialized data interface, which uses a 33MHz LPC bus clock. For more information about LPC bus refer to the 'Intel Low Pin Count Interface Specification Revision 1.1'.

Since Qseven is designed to be a legacy free standard for embedded modules, it does not support legacy functionality such as PS/2 keyboard/mouse, serial and parallel ports. Instead it provides an LPC interface that can be used to add peripheral devices to the carrier board design. The reduced pin count of the LPC interface makes it easy to implement such devices. All corresponding signals can be found on the module

connector.

2.13.1 LPC Signal Definition

Table 24: LPC Interface Signal Definition

Signal	Pin#	Description	I/O	Note
SERIRQ	191	LPC serialized IRQ. Carrier Board: Connect to LPC - SERIRQ N/C if not use	I/O 3.3V CMOS	
LPC_FRAME#	190	LPC frame indicates start of a new cycle or termination of a broken cycle. Carrier Board: LPC - LFRAME# FWH - Pin 23 LFRAME# N/C if not used	O 3.3V CMOS	
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	185 186 187 188	LPC multiplexed command, address and data. Carrier Board: Connect to LPC - LAD0 , LAD1, LAD2, LAD3 FWH - Pin 13 LAD0, Pin 14 LAD1, Pin 15 LAD2, Pin 17 LAD3 N/C if not used	I/O 3.3V CMOS	

Signal	Pin#	Description	I/O	Note
LPC_DRQ#	192	LPC encoded DMA/Bus master request. Carrier Board: Connect to LPC - LDRQ0#, LDRQ1# N/C if not used	I 3.3V CMOS	3
LPC_CLK	189	LPC clock output 33MHz. Carrier Board: Connect to LPC - LCLK	O 3.3V CMOS	

		FWH - Pin 31 LCLK N/C if not used		

Note:

1. While LPC interface is useful in x86 systems for backward compatibility it is not relevant at all for ARM systems.
2. Implementing external LPC devices on the Qseven carrier board always requires customization of the Qseven module's BIOS in order to support basic initialization for the LPC device. Otherwise the functionality of LPC device will not be supported by a Plug&Play or ACPI capable system.

3. SOM-3567 is NC.

2.13.2 LPC Routing Guidelines

2.13.2.1 General Signals

LPC signals are similar to PCI signals and may be treated similarly. Route the LPC bus as 50 Ω, single-ended signals. The bus may be referenced to ground (preferred), or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is preferred, although stubs up to 1.5 inches may be acceptable. Length-matching among LPC_AD[3:0], LPC_FRAME# are needed

2.13.2.2 Bus Clock Routing

Route the LPC clock as a single-ended, 50 Ω trace with generous clearance to other traces and to itself. A continuous ground-plane reference is recommended. Routing the clock on a single ground referenced internal layer is preferred to reduce EMI.

The LPC clock implementation should follow the routing guidelines for the PCI clock defined in the 'PCI Local Bus Specification Revision 2.3'.

Qseven specifies a single LPC reference clock signal called *'LPC_CLK'* on the modules connector on pin 189. If more than one LPC clock signal is required on the carrier board to supply several LPC devices, a zero delay buffer must be used to expand the number of LPC clock lines.

2.13.3 LPC Trace Length Guidelines

Figure 18: Topology for LPC

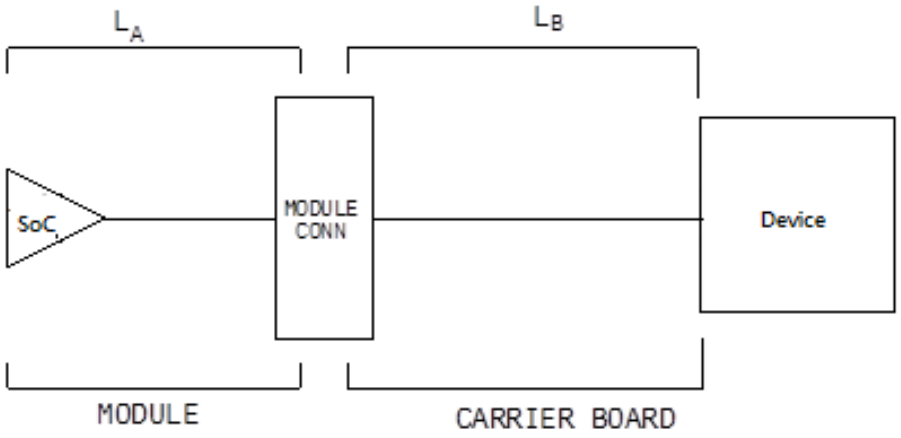


Table 25: LPC Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	LPC	
Single End	50Ω ±15%	
Nominal Trace Space within LPC Signal Group	Min. 15mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	16.5”	
Length matching between single ended signals	Max. 200mils	
Length matching between clock signals	Max. 200mils	
Reference Plane	GND referencing preferred.	
Via Usage	Try to minimize number of vias	

Notes:

2.14. CAN Interface *SOM-3567 is not support CAN Interface.

Controller Area Network (CAN or CAN-bus) is a message based protocol designed specifically for automotive applications but now is also used in other areas such as industrial automation and medical equipment.

Starting with Qseven Specification revision 1.20, Qseven modules can optionally support one CAN bus.

2.14.1 CAN interface Signal Definitions

Table 26: CAN interface Signal Definitions

Signal	Pin#	Description	I/O	Note
CAN0_TX	129	Transmit Line for CAN Carrier Board: Connect to CAN Bus transceiver transmit data input TXD pin N/C if not used	O CMOS	1
CAN0_RX	130	Receive Line for CAN Carrier Board: Connect to CAN Bus transceiver receive data output RXD pin N/C if not used	I CMOS	1

Note:

1. SOM-3567 is not support CAN Interface.

2.14.2 CAN interface Routing Guidelines

It should be routed as a differential pair signal with 120 Ohm differential impedance. The end points of CAN bus should be terminated with 120 Ohms or with 60 Ohms from the CAN_H line and 60 Ohms from the CAN_L line to the CAN Bus reference voltage. Check your CAN transceiver application notes for further details on termination.

2.14.3 CAN interface Trace Length Guidelines

Figure 19: Topology for CAN interface

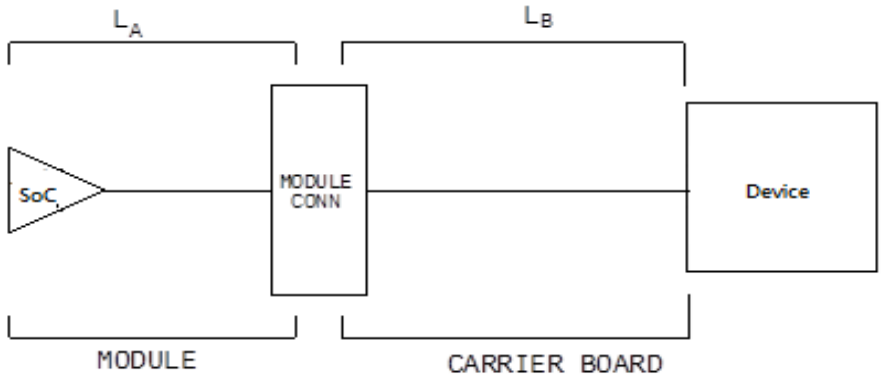


Table 27: CAN interface Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	CAN interface	1
Single End	NA	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	SOM-3567 is not support CAN Interface	
LB	Carrier Board Length	
Max length of LA+LB	NA	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

1. SOM-3567 is not support CAN Interface

2.15 SPI – Serial Peripheral Interface Bus

The Serial Peripheral Interface (SPI) is a 4-pin interface that provides a potentially lower-cost alternative for system devices such as EEPROM and flash components. Starting with Qseven Specification revision 1.20, Qseven modules can optionally support one SPI interface. Check module vendor's user guide whether general purpose SPI can be used.

2.15.1 SPI Signal Definition

Table 28: SPI Interface Signal Definition

Signal	Pin#	Description	I/O	Note
SPI_CS0#	200	SPI chip select 0 output. Carrier Board: Connect to SPI Flash - Chip Select pin 1 Device - Chip Select pin N/C if not used	O CMOS – 3.3V Suspend	
SPI_CS1#	202	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used. Carrier Board: Connect to SPI Flash - Chip Select pin 1 Device - Chip Select pin N/C if not used	O CMOS – 3.3V Suspend	
SPI_MISO	201	Data in to Module from Carrier SPI Carrier Board: Connect to SPI Flash - Serial Data Out pin 2 Device - Serial Data Out pin N/C if not used	I CMOS – 3.3V Suspend	

SPI_MOSI	199	Data out from Module to Carrier SPI Carrier Board: Connect to SPI Flash - Serial Data In pin 5 Device - Serial Data In pin N/C if not usE	O CMOS – 3.3V Suspend	
SPI_CLK	203	Clock from Module to Carrier SPI Connect to SPI Flash - Series Clock pin 6 Device - Series Clock N/C if not used	O CMOS – 3.3V Suspend	

2.15.2 SPI Routing Guidelines

NA

2.15.3 SPI Trace Length Guidelines

Figure 20: Topology for SPI

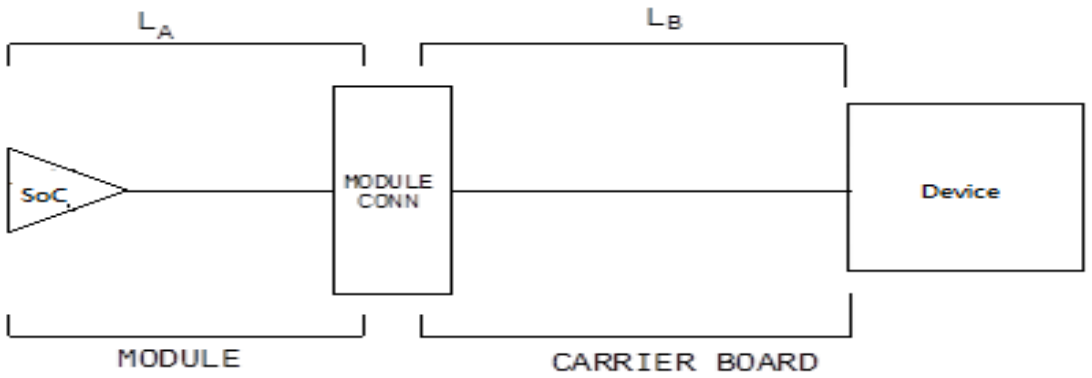


Table 29: SPI Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SPI	
Single End	50Ω ±15%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	8”	

DATA to CLK Maximum Pin to Pin Length Mismatch	Max. 500mils	
Via Usage	Try to minimize number of vias	

Notes:

2.16 General Purpose I2C Bus Interface

The I2C (Inter-Integrated Circuit) bus is a two-wire serial bus originally defined by Philips. The bus is used for low-speed (up to 400kbps) communication between system ICs. The bus is often used to access small serial EEPROM memories and to set up IC registers. The Qseven Specification defines several I2C interfaces that are brought to the Module connector for use on the Carrier. Some of these interfaces are for very specific functions (LVDS and DDIX), one interface is the SMBus used primarily for management and one other interface is a general purpose I2C interface. Since Qseven this interface should support multi-master operation. This capability will allow a Carrier to read an optional Module EEPROM before powering up the Module.

Revision 1.0 of the specification placed the I2C interface on the non-standby power domain. With this connection, the I2C interface can only be used when the Module is powered on. Since the I2C interface is used to connect to an optional Carrier EEPROM and since it is desirable to allow a Module based board controller access to the optional Carrier EEPROM before the Module is powered on, revision 2.0 of this specification changes the power domain of the I2C interface to standby-power allowing access during power down and suspend states. There is a possible leakage issue that can arise when using a R2.0 Module with a R1.0 Carrier that supports I2C devices. The R1.0 Carrier will power any I2C devices from the non-standby power rail. A R2.0 Module will pull-up the I2C clock and data lines to the standby-rail through a 2.2K resistor. The difference in the

power domains on the Module and Carrier can provide a leakage path from the standby power rail to the non-standby power rail.

Vendor interoperability is given via EAPI – Embedded Application Programming Interface, which allows and easier interoperability of Qseven Modules.

2.16.1 Signal Definitions

Required termination (pullup and/or pulldown resistors) is on the module unless otherwise noted.

These signals are NOT powered by the suspend rail.

The I²C Bus of the Qseven module can be accessed and programmed by using the API (Application Program Interface) called Embedded Application Programming Interface (EAPI). For more details about EAPI, refer to the Qseven specification and the module vendor's EAPI Programmers Guide.

Starting with specification Rev. 1.20, Qseven modules offer a second General Purpose I²C Bus. This I²C Bus is available on the Qseven connector pins 125 (GP_I2C_DAT) and 127 (GP_I2C_CLK) and is multiplexed with the LVDS flat panel detection signals LVDS_DID_DAT and LVDS_DID_CLK.

Table 30: General Purpose I2C Interface Signal Descriptions

Signal	Pin#	Description	I/O	Pwr Rail	Note
I2C_CLK	66	General Purpose I2C Clock output Carrier Board: Connect to SDA of I2C device N/C if not used	I/O OD CMOS	3.3V Suspend	
I2C_DAT	68	General Purpose I2C data I/O line. Carrier Board: Connect to SMBCLK of SMBus device. N/C if not used	I/O OD CMOS	3.3V Suspend	

2.16.2 I2C Routing Guidelines

2.16.3 I2C Trace Length Guidelines

Figure 21: Topology for I2C

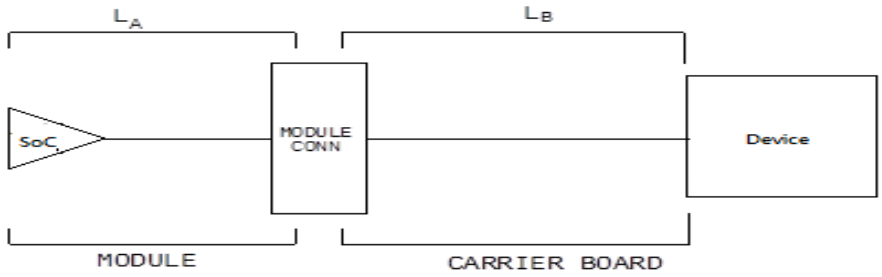


Table 31: I2C Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	I2C	
Single End	50Ω ±15%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	13”	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

2.16.4 Connectivity Considerations

The maximum amount of capacitance allowed on the Carrier General Purpose I2C bus lines (I2C_DAT, I2C_CK) is specified by Advantech’s Module. The Carrier designer is responsible for ensuring that the maximum amount of capacitance is not exceeded and the rise/fall times of the signals meet the I2C bus specification. As a general guideline, an IC input has 8pF of capacitance, and a PCB trace has 3.8pF per inch of trace length.

2.17 System Management Bus (SMBus)

The SMBus is primarily used as an interface to manage peripherals such as serial presence detect (SPD) on RAM, thermal sensors, PCI/PCIe devices, smart battery, etc. The devices that can connect to the SMBus can be located on the Module and Carrier. Designers need to take note of several implementation issues to ensure reliable SMBus interface operation. The SMBus is similar to I2C. I2C devices have the potential to lock up the data line while sending information and require a power cycle to clear the fault condition. SMBus devices contain a timeout to monitor for and correct this condition.

Designers are urged to use SMBus devices when possible over standard I2C devices. Qseven Modules are required to power SMBus devices from Early Power in order to have control during system states S0-S5. The devices on the Carrier Board using the SMBus are normally powered by the 3.3V main power. To avoid current leakage between the main power of the Carrier Board and the Suspend power of the Module, the SMBus on the Carrier Board must be separated by a bus switch from the SMBus of the Module. However, if the Carrier Board also uses Suspend powered SMBus devices that are designed to operate during system states S3-S5, then these devices must be connected to the Suspend powered side of the SMBus, i. e. between the Qseven Module and the bus switch. Since the SMBus is used by the Module and Carrier, care must be taken to ensure that Carrier based devices do not overlap the address space of Module based devices. Typical Module located SMBus devices and their addresses include memory SPD (serial presence detect 1010 000x, 1010 001x), programmable clock synthesizes (1101 001x), clock buffers (1101 110x), thermal sensors (1001 000x), and management controllers (vendor defined address). Contact Advantech for information on the SMBus addresses used.

2.17.1 SMB Signal Definitions

Table 32: SMB Signal Definitions

Signal	Pin#	Description	I/O	Pwr Rail	Note
SMB_CK	60	Clock line of System Management Bus. Carrier Board: Connect to SMBCLK of SMBus device. N/C if not used	I/O OD CMOS	3.3V Suspend rail	
SMB_DAT	62	Data line of System Management Bus. Carrier Board: Connect to SMBDAT of SMBus device. N/C if not used.	I/O OD CMOS	3.3V Suspend rail	
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus. Carrier Board: Connect to SMBALERT# of SMBus device. N/C if not used	I CMOS	3.3V Suspend Rail	

Note:

2.17.2 SMB Routing Guidelines

The SMBus should be connected to all or none of the PCIe/PCI devices and slots. A

general recommendation is to not connect these devices to the SMBus.

The maximum load of SMBus lines is limited to 3 external devices. Please contact Advantech if more devices are required.

Do not connect Non-Suspend powered devices to the SMBus unless a bus switch is used to prevent back feeding of voltage from the Suspend rail to other supplies.

Contact Advantech for a list of SMBus addresses used on the Module. Do not use the same address for Carrier located devices.

2.17.3 SMB Trace Length Guidelines

Figure 22: Topology for LPC

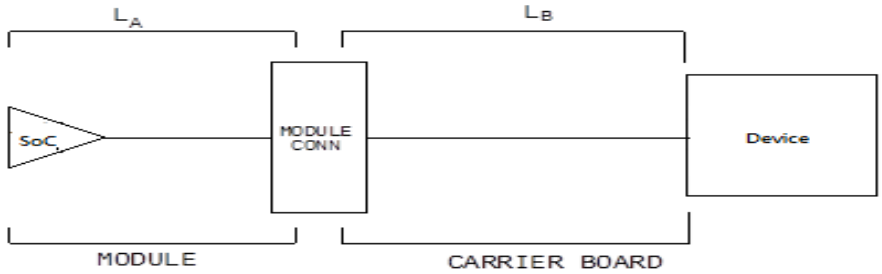


Table 33: SMB Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SMB	
Single End	50Ω ±15%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	13”	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

2.18 UART

2.18.1 UART interface Signal Definitions

Table 34: Serial interface Signal Definitions

Signal	Pin#	Description	I/O	Note
UART0_TX	171	Serial Data Transmitter	O 3.3V CMOS Max 1mA	
UART0_RX	177	Serial Data Receiver	I 3.3V CMOS ≥ 5 mA	
UART0_CTS#	178	Handshake signal, ready to send data	I 3.3V CMOS ≥ 5 mA	
UART0_RTS#	172	Handshake signal, ready to receive data	O 3.3V CMOS Max 1mA	

Note:

2.18.2 Serial interface Routing Guidelines

NA

2.18.3 Serial interface Trace Length Guidelines

Figure 23: Topology for Serial interface

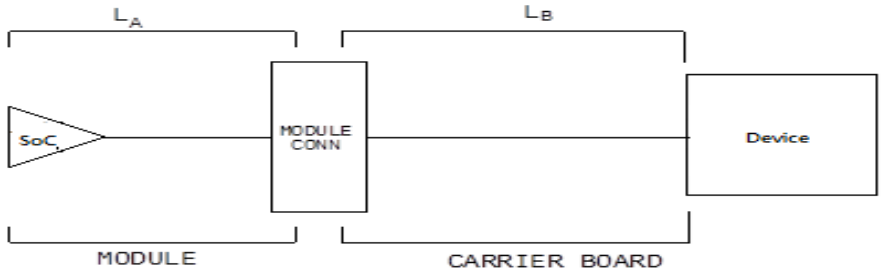


Table 35: Serial interface Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	Serial interface	
Single End	50Ω ±15%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-3567 Layout Checklist	
LB	Carrier Board Length	

Max length of LA+LB	NA	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

2.19 Miscellaneous Signals

2.19.1 Miscellaneous Signals

Table 36: Miscellaneous Signal Definitions

Signal	Pin#	Description	I/O	Note
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse. Carrier Board: Connect to trigger output of Watchdog device. N/C if not used	I 3.3V CMOS ≥ 10 mA	
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down. Carrier Board: Connect to trigger input of Watchdog device. N/C if not used	O 3.3V CMOS Max 5mA	
SPKR /GP_PWM_OUT2	194	Primary functionality is output for audio enunciator, the “speaker” in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output. Carrier Board: Connect to Speaker circuit. N/C if not used	O 3.3V CMOS	
BIOS_DISABLE# /BOOT_ALT#	41	Module BIOS disable input signal. Pull low to disable module's on-board BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example	I 3.3V CMOS	

		a bootloader. Carrier Board: PD 0Ω to GND or connect 0Ω in series to pin 28 of FWH to disable Module BIOS N/C if not used		

Signal	Pin#	Description	I/O	Note
MFG_NC0 MFG_NC1 MFG_NC2 MFG_NC3 MFG_NC4	207 209 208 210 204	Do not connect on the carrier board. These pins are reserved for manufacturing purposes.	NA	1

Note:

1. On SOM-3567, Pin 204 is JTAG_UART_SEL, Pin 207 is UART1_CTS#, Pin 208 is UART1_RX,
   Pin 209 is UART1_TX, Pin 210 is UART1_RTS#.

2.19.1.1 Watchdog Control Signals

The Watchdog on Qseven modules can be initialized and controlled by the API (Application Program Interface) called Embedded Application Programming Interface (EAPI). For more details about EAPI, refer to the Qseven specification and the module vendor's EAPI Programmers Guide.

In addition to the software trigger available via EAPI, the Watchdog on a Qseven module can be hardware-triggered by an external control circuitry. When generating a low level pulse on the Qseven module's *'WDTRIG#'* (Watchdog trigger signal) signal, the Watchdog timer will be reset and restarted.

If the Watchdog timer has expired without a software or hardware trigger occurrence, the Qseven module will signal this with a high level output on the *'WDOUT'* (Watchdog event indicator) signal.

2.19.1.2 PC Speaker Output

The Qseven module provides a speaker output signal called *'SPKR',* which is intended to drive an external FET or a logic gate to connect a PC speaker. The *'SPKR'* signal can be found on the module's pin 194.

The *'SPKR'* signal is often used as a configuration strap for the module's chipset. It should not be connected to a pull-up or pull-down resistor, which could overwrite the internal chipset configuration and result in a malfunction of the module.

2.19.2 Miscellaneous Signals Routing Guidelines

NA

2.19.3 Miscellaneous Signals Trace Length Guidelines

NA

2.20 Thermal Signals

2.20.1 Thermal Interface

Qseven modules provide the *'THRM#'* and *'THRMTRIP#'* signals, which are used for system thermal management. In most current system platforms, thermal management is closely associated with system power management. For more detailed information about the thermal management capabilities of the Qseven module refer to the module's user's guide.

Table 37: Thermal Management Signal Definitions

Signal	Pin#	Description	I/O	Note
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling. Carrier Board: Connect to THRM# output of Hardware Monitor. N/C if not used.	I 3.3V CMOS	
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off). Carrier Board: Connect to THERMTRIP# input of devices. N/C if not used.	O 3.3V CMOS	

Note:

2.20.2 Thermal Signals Routing Guidelines

NA

2.20.3 Thermal Signals Trace Length Guidelines

NA

2.21 Fan Control Implementation

2.21.1 Fan Control Interface

Qseven modules provide additional support for fan speed control through the use of two signals named *'FAN_TACHOIN'* and *'FAN_PWMOUT'*. In order to easily implement fan speed control in customer specific application software, there is a software API (Application Program Interface) called Embedded Application Programming Interface (EAPI). For more information about EAPI, refer to the Qseven specification and the Module vendor's EAPI Programmers Guide.

Table 38: Fan Control Signal Definitions

Signal	Pin #	Description	I/O	Note
FAN_PWMOUT / GP_PWM_OUT1	196	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output. Carrier Board: 4-Wire PWM Fan - Connect 3.3V to 5V level shift to fan connector pin 4 CONTROL with bypass 470pF to GND.	O 3.3V CMOS OC	

		3-Wire PWM Fan - Connect 3.3V to 12V level shift to fan connector pin 2 PWR with bypass 470pF/10uF to GND. N/C if not used.		
FAN_TACHOIN / GP_TIMER_IN	195	Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input. Carrier Board: 4-Wire PWM Fan - Connect to diode anode and diode cathode connects to fan connector pin 3 SENSE with bypass 470pF to GND. 3-Wire PWM Fan - Connect to diode anode and diode cathode connects to fan connector pin 3 TACHO with bypass 470pF to GND. N/C if not used.	I 3.3V CMOS	

Note:

2.21.2 Fan Control Signals Routing Guidelines

NA

2.21.3 Fan Control Signals Trace Length Guidelines

NA

3. Power

3.1 General Power requirements

Qseven modules are designed to be driven with a single +5V input power rail. Additionally, two optional power rails are specified by Qseven to provide a +5V standby voltage (5V-Always) on the Qseven module as well as a +3V Real Time Clock (RTC) supply voltage, which is provided by a battery cell located on the carrier board.

If the carrier board does not require standby functionality, then the +5V standby power rail can be omitted. In this case the VCC_5V_SB pins shall be connected to the +5V input power rail. The same applies to the +3V RTC battery voltage rail. If no RTC/CMOS backup functionality is required by the system during power-off, then the +3V RTC supply battery voltage can be omitted. During standby and power-on the RTC/CMOS should be supplied by the 3.3V standby rail on the carrier board. Please refer to the Qseven specification for the power up and power down power rail sequencing.

The following practices should be implemented in order to prevent possible damage to the customized carrier board and/or injury to the operator.

Over-current Protection

For safety reasons, the main power supply path should be fused. There should be a fuse placed between the system's power supply output and the customized carrier board's power supply input. This fuse may be a standard fuse or could also be a poly fuse. Either one is sufficient. The maximum current must be tested and determined by the carrier board designer.

3.1.1 Power Management Signals

Table 39: Power Management Signal Definitions

Signal	Pin#	Description	I/O	Note
PWGIN	26	High active input for the Qseven module indicates that power from the power supply is ready. Carrier Board: Connect to power good pin of main power supply ATX - Connect to PW-OK pin 8 of ATX power connector. AT - Connect to PW-OK pin 1 of AT power connector. Other - Connect to power good of 5V and 5VSB N/C if not used.	I 3.3V / 5V CMOS ≥ 4 mA	
PWRBTN#	20	Power Button: Low active power button input. This	I 3.3V	

		signal is triggered on the falling edge. Carrier Board: ATX - Connect to Power Button or SIO Power Button Out pin (Active low) AT - N/C N/C if not use	Suspend CMOS OD ≥ 10 mA	
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module. Carrier Board: Connect to Reset button N/C if not used	I 3.3V CMOS ≥ 10 mA	
BATLOW# for R2.0 BATLOW# / GPII2 for R2.0	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event. Carrier Board: Connect to BATLOW# of Smart Battery N/C if not used.	I 3.3V Suspend CMOS ≥ 10 mA	1
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event. Carrier Board: Connect to PME# of SIO N/C if not used.	I 3.3V Suspend CMOS ≥ 10 mA	

Signal	Pin#	Description	I/O	Note
SUS_STAT# for R2.0 GPO0 for R2.1	19	Suspend Status: indicates that the system will be entering a low power state soon. Carrier Board: Connect to LPCPD# of LPC device. N/C if not used.	O 3.3V Suspend CMOS max. 1 mA	1
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to RAM), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	O 3.3V Suspend CMOS max. 1 mA	

		Carrier Board: Connect to SLP_S3# (Suspend To RAM) of LPC device or SIO. N/C if not used.		
SUS_S5#	16	S5 Sleep Control signal indicating that the system resides in S5 State (Soft Off). Carrier Board: Connect to SLP_S5# (Soft Off) of LPC device or SIO. N/C if not used.	O 3.3V Suspend CMOS max. 1 mA	
SLP_BTN# for R2.0 SLP_BTN# / GPII1 for R2.1	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge. Carrier Board: Connect to Sleep button N/C if not used	I 3.3V Suspend CMOS ≥ 10 mA	1
LID_BTN# for R2.0 LID_BTN# / GPII0 for R2.1	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. TBD: Open/Close state.. Carrier Board: Connect to LID button N/C if not used	I 3.3V Suspend CMOS ≥ 10 mA	1

Note:

1. BATLOW#, SUS_STAT#, SLP_BTN# and LID_BTN# are used on SOM-3567.

3.2 Power Up Control

The power up control is responsible for switching the Qseven V2.0 reference carrier board on or off when a power-up or a power-down event occurs. A power event can be generated by pressing the power button or by another system event, which can originate from or be detected by the Qseven module's chipset.

The native system power-up support of Qseven modules utilize the *'SUS_S3#'* signal to control the *'PSON'* signal, which is used to switch the supply rails on or off. When using the *SUS_S3#'* signal, Qseven modules are capable of supporting Suspend to RAM (S3). When the system goes to Suspend to RAM (S3) or Soft Off (S5), the *'SUS_S3#'* signal is asserted by the chipset of the module. Through this behavior the signal can be used to

drive 'PSON' and switches off the power rails of the carrier. Vice versa, if the system is in a power-down system state, any system wake-up event invokes the module's chipset to dessert the *'SUS_S3#'* signal and transfers the system to Full-On (S0) state.

3.2.1 ATX and AT Power Sequencing Diagrams

The power up control is responsible for switching the ATX power supply on or off when a power-up or a power-down event occurs. A power event can be generated by pressing the power button or by another system event, which can originate from or be detected by the Qseven module's chipset.

The native system power-up support of Qseven modules utilize the *'SUS_S3#'* signal to control the *'PS_ON#'* signal, which is used to switch the ATX power supply on or off. When using the *SUS_S3#'* signal, Qseven modules are capable of supporting Suspend to RAM (S3).

When the system goes to Suspend to RAM (S3) or Soft Off (S5), the *'SUS_S3#'* signal is asserted by the chipset of the module. Through the use of an inverter, the low active *'PS_ON#'* signal goes high and switches off the ATX power supply. Vice versa, if the system resides in a power-down system state, any system wake-up event invokes the chipset of the module to deassert the *'SUS_S3#'* signal. This results in a system transition to Full-On (S0).

The way Suspend to RAM is implemented on a Qseven module may differ depending on the module manufacturer. For this reason it is recommended that a hardware jumper be implemented on the carrier board in order to provide the ability to choose if the *'PS_ON#'* signal should be controlled either by the *'SUS_S3#'* signal or '*SUS_S5#'* signal.

A sequence diagram for an ATX style boot from a soft-off state (S5), initiated by a power button press, is shown in Figure 24 below.

A sequence diagram for an AT style boot from the mechanical off state (G3) is shown in Figure 25 below .

In both cases, the VCC_12V, VCC_5V and VCC_3V3 power lines should rise together in a monotonic ramp with a positive slope only, and their rise time should be limited. Please refer to the ATX specification for more details.

Figure 24: ATX Style Power Up Boot – Controlled by Power Button

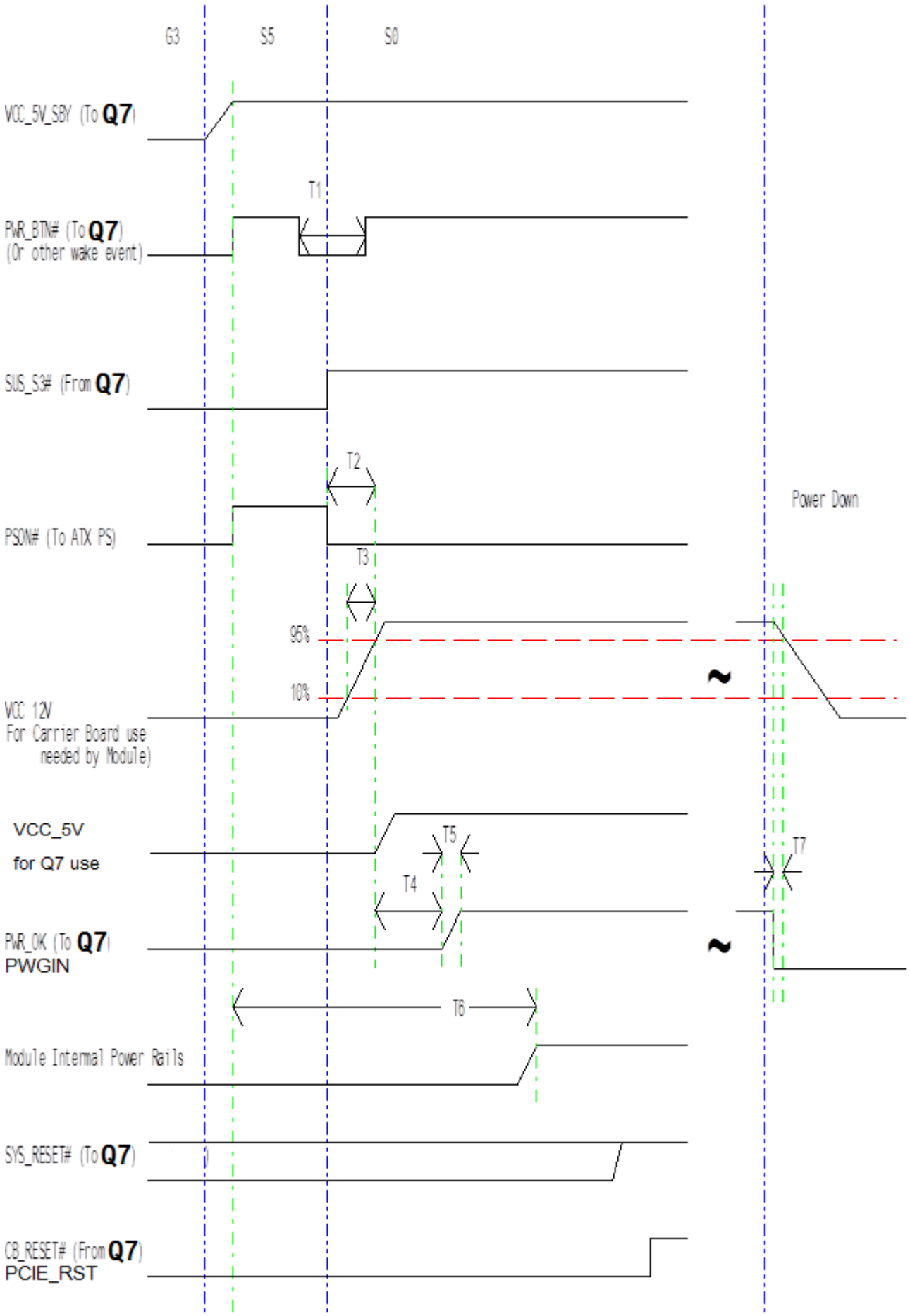

G3
S5
S0
VCC_5V_SBY (To Q7)
T1
PWR_BTN# (To Q7)
(Or other wake event)
SUS_S3# (From Q7)
T2
Power Down
PSON# (To ATX PS)
T3
95%
10%
VCC 12V
For Carrier Board use
needed by Module)
VCC_5V
for Q7 use
T5
T7
T4
PWR_OK (To Q7)
PWGIN
T6
Module Internal Power Rails
SYS_RESET# (To Q7)
CB_RESET# (From Q7)
PCIE_RST

Figure 25: AT Style Power Up Boot

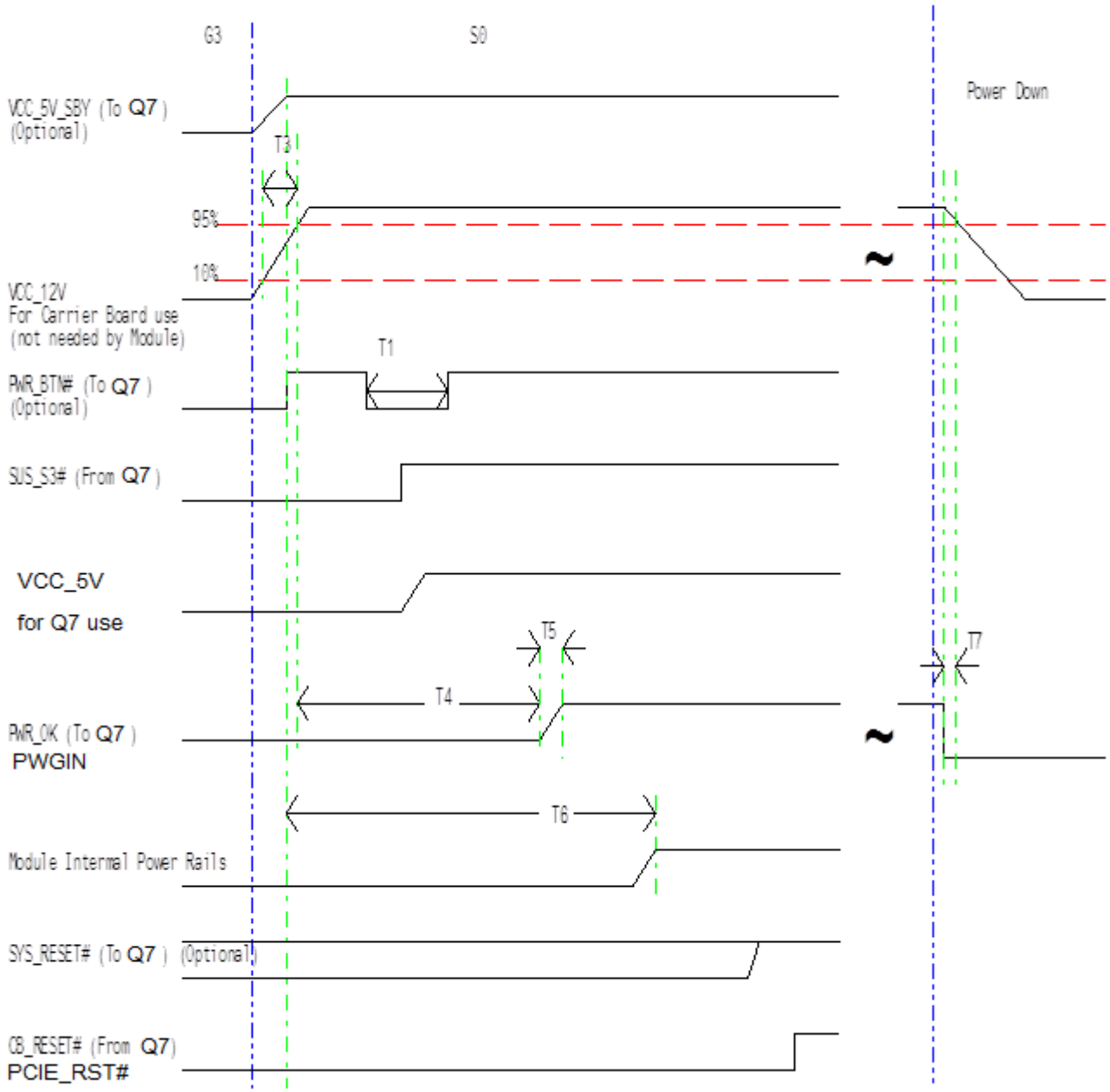


Table 40: Power Management Timings

Sym	Description	Min	Max
T1	Power Button	16ms	
T2	The power-on time is defined as the time from when PS_ON# is pulled low to when the VCC_12V and VCC_5V.		500ms
T3	VCC_12V rise time from 10% to 95%	0.1ms	20ms
T4	PWR_OK delay	100ms	
T5	PWR_OK rise time		10ms
T6	Module Internal Power Rails		

T7	Power-down warning	1ms	

Note:

3.3 RTC Battery

The Real Time Clock (RTC) is responsible for maintaining the time and date even when the Qseven module is not connected to a main power supply. Usually a +3V lithium battery cell is used to supply the internal RTC of the module. The Qseven specification defines an extra power pin *'VCC_RTC',* which connects the RTC of the module to the external battery. The specified input voltage range of the battery is defined between +2.4V and +3.3V. The signal *'VCC_RTC'* can be found on the module's connector pin 193.

3.3.1 RTC Battery Lifetime

The RTC battery lifetime determines the time interval between system battery replacement cycles. Current leakage from the RTC battery circuitry on the carrier board is a serious issue and must be considered during the system design phase. The current leakage will influence the RTC battery lifetime and must be factored in when a specific life expectancy of the system battery is being defined.

In order to accurately measure the value of the RTC current it should be measured when the complete system is disconnected from AC power.

The RTC power plane is normally ored with the 3V3 Voltage on the module, so it may not be necessary to perform this on the carrier board. Please consult the module vendor's documentation.

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Table 41: Absolute Maximum Ratings

SOM-3567		MIN	MAX	UNIT
Power	VIN	4.75 (5-5%)	5.25 (5+5%)	V
	VSB	4.75 (5-5%)	5.25 (5+5%)	V
	RTC Battery	2.3	3.3	V

4.2. DC Characteristics

Table 42: DC Current Characteristics1

Intel(R)Atom(TM)CPU E3845 @1.9GHz							
Power Plane	Maximum Power Consumption						
Symbol	S0				S3	S5	G3
+VIN (+5V)	TAT CPU+GPU 100%	TAT CPU 100%	Burn-in	Idle	--	--	--
	11.896W	9.217W	7.486W	3.238W			
+V5SB_CB	0.061W	0.046W	0.046W	0.046W	0.652W	0.554W	--
RTC Battery	--				--	1.44uA	4.07uA

4.3. Inrush Current

Table 43: Inrush Current

Power Plane	Maximum	
Symbol	G3 to S5	S5 to S0
+V5SB_CB	0.45647 A	-----
+VIN (+5V)	-----	3.1843 A