TLE9271...74QX(V33)
High-End DC/DC System Basis Chip Family

Referenced datasheets

- Infineon-TLE9271QX_DS_v01_50-EN
- Infineon-TLE9271QXV33_DS_v01_50-EN
- Infineon-TLE9272QX_DS_v01_50-EN
- Infineon-TLE9272QXV33_DS_v01_50-EN
- Infineon-TLE9273QX_DS_v01_50-EN
- Infineon-TLE9273QXV33_DS_v01_50-EN
- Infineon-TLE9274QX_DS_v01_50-EN
- Infineon-TLE9274QXV33_DS_v01_50-EN

Overview

This document lists the errata of the High-End DC/DC System Basis Chip Family.

It is strongly recommended that the device behavior and proposed workarounds are considered for the application.

Affected Products

Product	OPN
TLE9271QX	TLE9271QXXUMA1
TLE9271QX V33	TLE9271QXV33XUMA1
TLE9272QX	TLE9272QXXUMA1
TLE9272QX V33	TLE9272QXV33XUMA1
TLE9273QX	TLE9273QXXUMA1
TLE9273QX V33	TLE9273QXV33XUMA1
TLE9274QX	TLE9274QXXUMA2
TLE9274QX V33	TLE9274QXV33XUMA1

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1 CAN dominant pulse on RXDCAN when switching off CAN receiver

Whenever the CAN receiver is deactivated and VCC1 is available, a short dominant puls on RXDCAN line is visible.

1.1 Description of behavior and occurrence

Necessary conditions 1:

- SBC is in SBC normal mode AND
- CAN transceiver is switched via SPI command from {CAN normal mode or CAN receive only mode} to {CAN wake capable mode or CAN OFF mode} (see orange arrows in **Figure 1**).

or

Necessary conditions 2:

- CAN transceiver is switched automatically from {CAN normal mode or CAN receive only mode} to CAN wake capable mode via SBC mode transition (see green arrows in **Figure 1**).

Unexpected device behavior:

If above conditions apply, then a typ. 1 us dominant pulse is visibile on RXDCAN. See timing diagram in **Figure 2**.

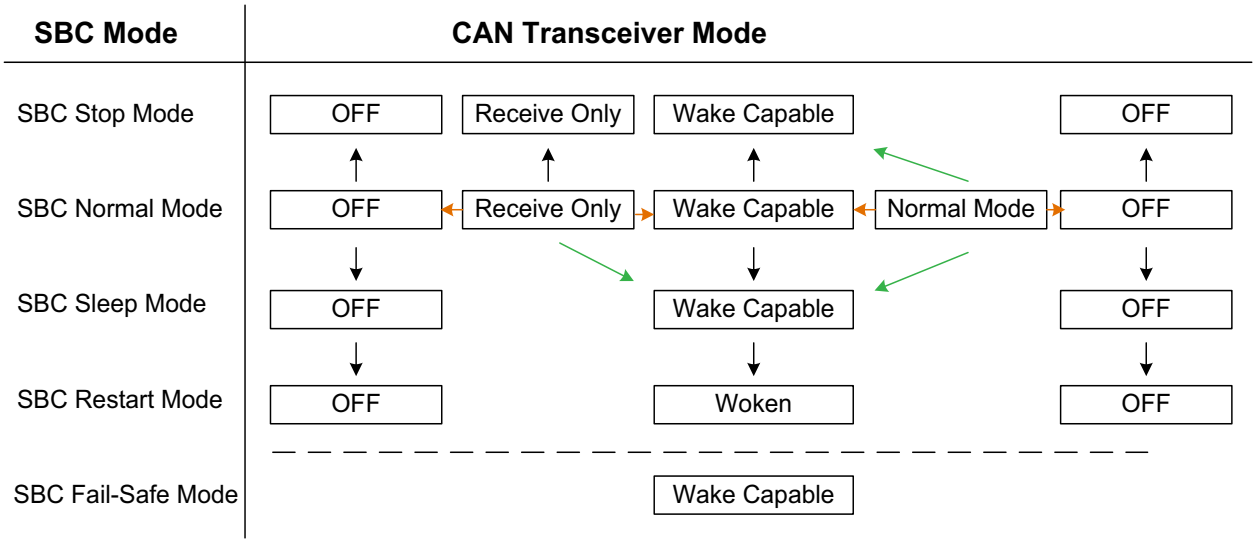

Figure 1 Affected mode transition in orange and green

Note: Automatic transitions from {CAN normal mode or CAN receive only mode} because of SBC mode transition to SBC Fail-Safe mode are also affected by this behaviour. But as RO is low in SBC Fail-Safe mode reseting the microcontroller and VCC1 is switched off, this scenario is not described within this errata.

1.2 Possible impact

This unexpected pulse could wake up the microcontroller which is in or on the way to low power mode. Only this applications are affected which are listening for wake-up on the RXDCAN pin.

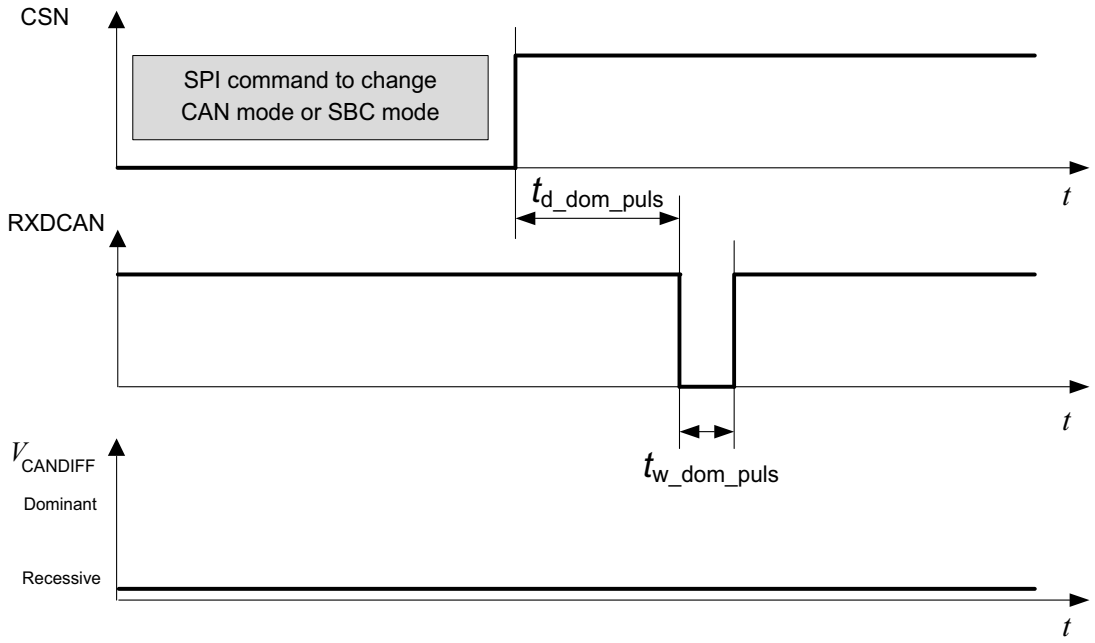

Figure 2 Timing diagram for the RXDCAN dominant pulse

1.3 Proposed workaround

In order to avoid the application unintendendly to wake up from low power mode or to cancel the transition to low power mode, the software implementation for the microcontroller must consider one of the following options.

- Software may not use the RXDCAN pin of the SBC to receive a wake event on bus, but use the INT pin.
- Software need to mask this dominant pulse, which may lead to an additional delay during the shutdown sequence of the ECU.

Table 1 RXDCAN dominant pulse parameter

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Delay time for RXDCAN dominant pulse	$t_{d\_dom\_puls}$	-	-	3	µs	1)
Width of RXDCAN dominant pulse	$t_{w\_dom\_puls}$	-	1	-	µs	1) min and max values correlated with the oscillator frequency tolerance as specified in the datasheet parameter P_13.9.24 (f_{CLKSBC})

1) Not subject to production test. Specified by design.

2 Revision history

Revision	Date	Changes
1.30	2021-04-07	• Released errata about “CAN dominant pulse on RXDCAN when switching off CAN receiver” • Remove errata about “Unintended stuck in PFM operation mode during the initiation of PFM-PWM transition of the buck converter”
1.20	2019-12-17	• Released errata about “Unintended stuck in PFM operation mode during the initiation of PFM-PWM transition of the buck converter” • Remove errata about “Unintended CAN dominant pulse when entering SBC Sleep or Fail-Safe Mode while in CAN Normal Mode” because corrective action implemented with datasheet rev. 1.40
1.10	2018-04-23	• Released errata about “Unintended CAN dominant pulse when entering SBC Sleep or Fail-Safe Mode while in CAN Normal Mode”

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Do you have a question about any aspect of this document?
Email: erratum@infineon.com

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