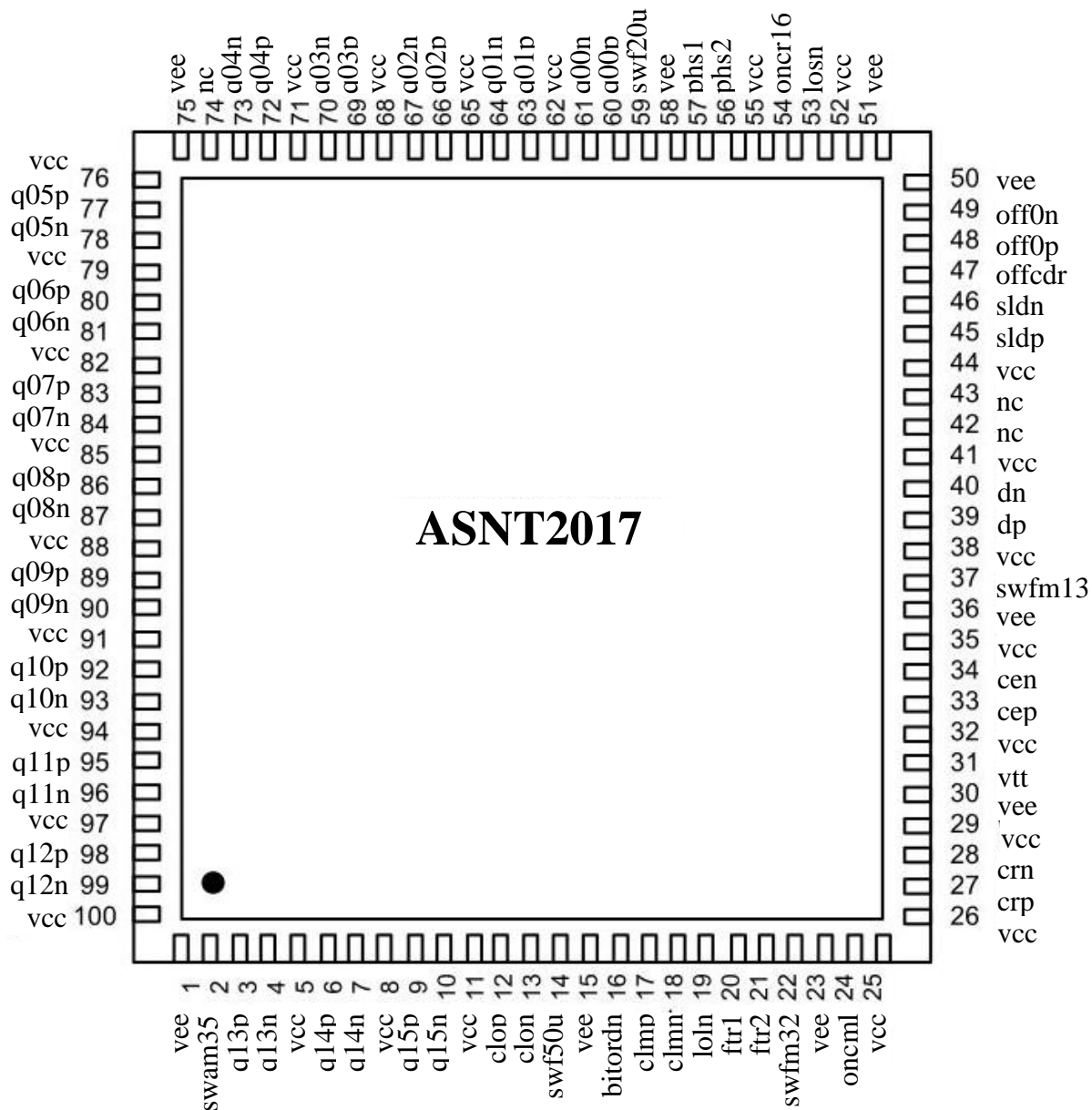# ASNT2017-PQA
Programmable CDR/Digital DMUX 1:16

- 1-to-16 demultiplexer (DMUX) with integrated full rate CDR
- Supports data rates from 12.5*Gb/s* to 13.6*Gb/s* in CDR mode
- Supports data rates from DC to 17*Gb/s* in the optional digital mode
- Proprietary low-power LVDS output buffers for data and clock-divided-by-16
- Supports divided by 16 or by 64 input reference clocks in CDR mode
- Single +3.3*V* power supply
- Industrial temperature range
- Low power consumption of 890*mW* at maximum speed
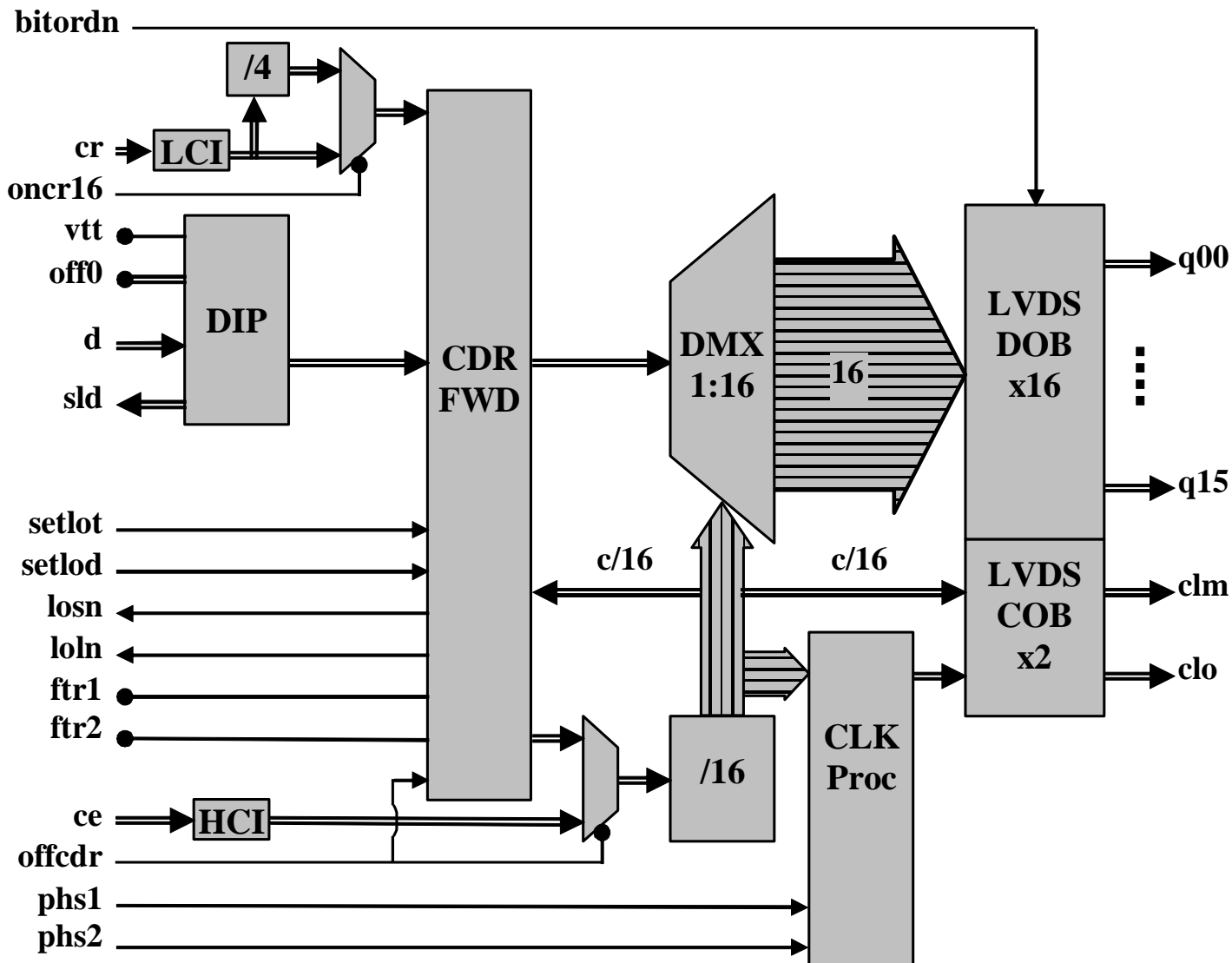- Standard 100-pin QFN package (12*mm* x 12*mm*)

DESCRIPTION

Fig. 1. Functional Block Diagram

ASNT2017-PQA is a user-programmable 1:16 deserializer (DMUX) with a full-rate integrated clock and data recovery unit (CDR) that incorporates a frequency window detector (FWD). The main function of the chip shown in Fig. 1 is to demultiplex a serial input data signal d running at a bit rate of f_{bit} into 16-bit wide parallel data words q00-q15 running at a bit rate of $f_{bit}/16$. The DMUX can operate in one of two main modes: CDR mode that utilizes on-chip full-rate VCO with a central frequency of f_{bit}, or broadband digital mode that requires application of an external full-rate clock ce with the same frequency to the inputs of a high speed CML clock input buffer (HS CIB). Selection of the operational mode is made through control pin offcdr.

The high sensitivity CDR FWD block incorporates phase and frequency acquisition loops to ensure accurate recovery of clock and data for an NRZ input data stream. For the correct operation of the block, off-chip passive filter components should be connected to pins ftr1 and ftr2. CDR FWD also requires an external reference clock running at 1/16 or 1/64 the VCO's frequency to be applied to the input cr. The acceptable frequency of the reference clock is defined by the oncr16 control signal. If the 1/16 mode is selected, the input clock with

frequency of $f_{bit}/16$ is applied to CDR FWD after an additional divider by 4 (/4). The reference clock input buffer supports LVDS or CML interfaces as defined by the oncml control signal. The recovered clock is used for sampling the input data bits before they are demultiplexed and is also sent to the internal divider (/16). CDR FWD also provides active-low alarm indicators for loss of input signal (losn) and loss of lock (loln).

The high-speed CML data and clock input buffers provide on-chip $50Ohm$ termination and are designed to be driven by devices with $50Ohm$ source impedance. The data input buffer sets its termination voltage internally, but the vtt pin can be used to externally adjust it if desired. Pin off0 control the offset voltage between data inputs dp and dn allowing the user to change the slicing or threshold level at the serial data input. A peak detector is incorporated in Data IB to monitor the amplitude of the incoming data stream with its output made available through differential pins sld.

The reconstructed serial input data is latched into the demultiplexer (DMX1:16) and is subsequently deserialized and delivered to the demultiplexer's output as 16-bit wide low-speed parallel words. Sixteen proprietary low-power LVDS output data buffers (LVDS DOBx16) are used to deliver the 16 data output signals q00-q15, while a similar dual LVDS clock output buffer (LVDS COBx2) outputs the two copies clm and clo of the low-speed clock signal. The buffers satisfy all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 standards. The phase of the clo clock signal can be selected with a 90° increment by utilizing control pins phs1 and phs2.

Utilizing control pin bitordn, the deserializer can designate either q00 or q15 as the MSB (first input serial bit), thus simplifying the interface between the demultiplexer chip and a following ASIC.

The chip uses a single $+3.3V$ power supply and is characterized for operation from $-25°C$ to $125°C$ of junction temperature.

DIP

The Data Input Processor (DIP) can process differential or single-ended CML signals with bit rates from DC to f_{bit}. The data inputs utilize on-chip single-ended $50Ohm$ termination to vtt=$2.5V$ (default) for each input line where vtt can be also adjusted externally. A single-ended data signal can be applied to one of the differential input pins either directly (DC coupling) or through a capacitor (AC coupling). In case of DC coupling, a threshold voltage must be set on the other pin. In case of AC coupling, the unused input pin must be terminated to vtt. In any case, the duty cycle of the received signal can be adjusted using control inputs off0n or off0p with input impedances of $250Ohm$.

Additionally, DIP includes an input signal peak detector that generates two DC signals sldp and sldn shown in Fig. 2a. The value of sldn represents the input data common mode voltage as shown in Fig. 2b. The difference between sldp and sldn represents the input SE peak-to-peak swing as shown in Fig. 2c. Each single-ended output of the peak detector has a $3.1KOhm$ impedance value in relation to vcc.
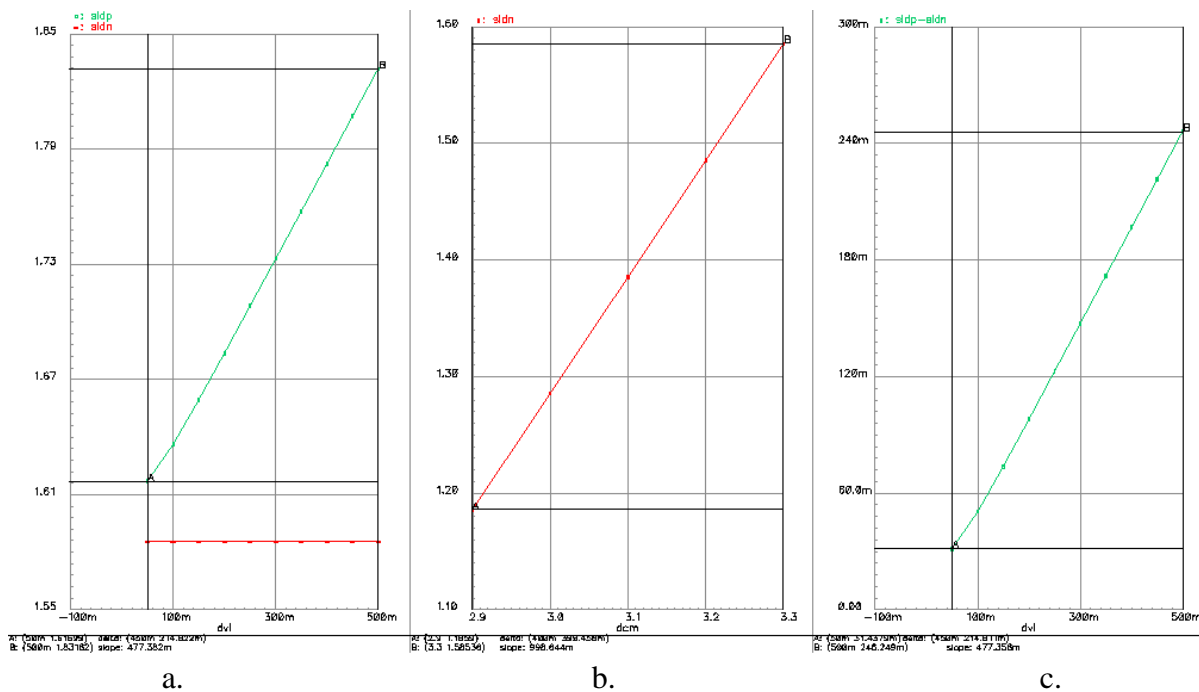
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a.   b.   c.

Fig. 2. Simulated Peak Detector Output Signals: (a) – sldp and sldn vs. SE input swing (p-p) at vcc=3.3V, (b) – sldn vs. input common mode voltage at vcc=3.3V, (c) – sldp-sldn vs. SE input swing (p-p) at vcc=3.3V

LCI

The Low-Speed Clock Input Buffer (LCI) is a proprietary universal input buffer (UIB) that can run at a frequency up to 1.0*GHz*. The input termination impedance is controlled by the CMOS signal offecl and is set to 100*Ohm* differential if offecl="1" (true LVDS mode, default state) or 50*Ohm* single-ended to vecl if offecl="0" (CML mode). The value of vecl should be equal to vcc in CML mode or to vcc-2*V* in PECL mode. In PECL mode, the corresponding termination voltage source should be able to both sink and source up to 20*mA* of current. Possible input clock application schemes are detailed in Table 1, where *V*cm is the common-mode voltage of the clock signal. As can be seen, UIB is designed to accept differential signals with common mode DC voltages between negative (vee) and positive (vcc) supply rails, as well as AC common mode noise with a frequency up to 5*MHz* and voltage levels from vee to vee+2.4*V*. It can also receive single-ended signals with a threshold voltage between vee and vcc applied to the unused pin of the differential input port.

Table 1. LS Input Clock Application Schemes

Interface type	Clock type	cep signal			cen signal		
		Swing, *mV*	**Connection**	***Vcm, V***	**Swing, *mV***	**Connection**	***Vcm, V***
LVDS (offecl ="1")	Diff.	70-to-500	DC	1.2±1.0	70-to-500	DC	1.2±1.0
	SE	140-to-900	AC	-	Threshold	DC	vee-to-vcc
		Threshold	DC	vee-to-vcc	140-to-900	AC	-
CML or PECL (offecl ="0")	Diff.	70-to-500	DC	vcc-Swing/2	70-to-500	DC	vcc-Swing/2
			AC	-		AC	-
	SE	140-to-900	AC	-	-	Not connected	-
		140-to-900	AC	-	Threshold	DC	vcc
		-	Not connected	-	140-to-900	AC	-
		Threshold	DC	vcc	140-to-900	AC	-

/4

The divider by 4 (/4) is used to adjust the external reference clock cr if its frequency is selected to be equal to 1/16 of the active VCO's frequency. The divider is activated by the oncr16 control signal (oncr16=vcc) and delivers a standard divided-by-64 reference clock to CDR FWD. In case of oncr16=vee, the reference clock is delivered to CDR FWD, bypassing /4.

HCI

The high-speed clock input buffer (HCI) can accept external CML clock signals and provides on-chip single-ended termination of $50 Ohm$ to vcc for each input line cep or cen. A single-ended clock can be applied to one of the differential input pins either directly (DC coupling) or through a capacitor (AC coupling). In case of DC coupling, a threshold voltage must be set on the other pin. In case of AC coupling, the unused input pin must be terminated to vcc.

CDR FWD

The clock and data recovery block with frequency window detector (CDR FWD) contains both phase and frequency acquisition loops. It requires an off-chip filter shown in Fig. 3. The main function of CDR FWD is to lock the frequency of the on-chip VCO to that of the input data signal (clock recovery) while adjusting the VCO's clock phase to latch in the incoming data with minimal error (data recovery). The recovered clock is also utilized by the internal divider (/16) to generate all internal timing signals.
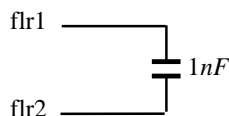

Fig. 3. External Filter Schematic

CDR FWD assigns the $3.3V$ CMOS loss-of-signal flag losn="0" when the input data's transition density is not enough or too much. The similar loss-of-lock flag loln="0" is generated by CDR FWD when the frequency difference between the reference clock and the internal clock divided-by-64 exceeds $\pm 1000 ppm$.

/16

The divider-by-16 (/16) includes four divide-by-2 circuits connected in series. The high-speed clock delivered by CDR FWD is fed into the first divide-by-2 where its output is routed internally to the next divide-by-2 circuit and outside of the block to DMX1:16 through a buffering circuit. Other divided down clock signals are also buffered and routed to DMX1:16 in a similar fashion. The clock divided-by-16 c/16 is passed on to one LVDS OB and to CLK Proc for additional phase adjustment.

DMX1:16

The 1-to-16 demultiplexer (DMX1:16) utilizes a tree-type architecture which latches in the data stream from CDR FWD on both edges of the half-rate clock signal that is supplied by the divider /16. The high speed data signal is subsequently demultiplexed down and delivered to LVDS data output buffers (LVDS DOBx16) as16-bit wide parallel words.

CLK Proc

By utilizing the $3.3V$ CMOS control pins phs1 and phs2, the phase of the main low-speed clock output signal clo can be selected in accordance with the table below.

Table 2. Clock Phase Selection

phs1	phs2	C16 phase
vee (default)	vee (default)	270°
vee	vcc	180°
vcc	vee	90°
vcc	vcc	0°

LVDS DOBx16

LVDS data output buffers (LVDS DOBx16) accept 16-bit wide words from DMX1:16 and convert them into sixteen LVDS output signals. Each proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at bit rates up to 2*Gb/s* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. The block also provides a bit order selection under control of the external 3.3*V* CMOS signal bitordn. The first input serial bit (MSB) is assigned to q15 at bitordn="0" (default) or to q00 at bitordn="1".

LVDS COB x2

The dual LVDS clock output buffer (LVDS COBx2) utilizes the same proprietary output buffers as in DOBx16. It receives two clock signals and converts them into LVDS output signals clo and clm. The phase of clo can be adjusted as described above.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.6	*V*
Power Consumption		1.0	*W*
RF Input Voltage Swing (SE)		1.2	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	5, 8, 11, 25, 26, 29, 32, 35, 38, 41, 44, 52, 55, 62, 65, 68, 71, 76, 79, 82, 85, 88, 91, 94, 97, 100
vee	Negative power supply (GND or 0*V*)	1, 15, 23, 30, 36, 50, 51, 58, 75
nc	Unconnected pin	42, 43, 74

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
dp	39	Input	CML differential data inputs with internal SE 50*Ohm* termination to vtt
dn	40		
cep	33	Input	CML differential clock inputs with internal SE 50*Ohm* termination to vcc
cen	34		
Controls			
bitordn	16	LS In., CMOS	Output bit order selection (default: low, the first serial bit (MSB) is q15; active: high, MSB is q00)
loln	19	LS Out, CMOS	CDR FWD lock indicator (high: locked; low: no lock)
ftr1	20	I/O	External CDR FWD filter connections
ftr2	21		
oncml	24	LS In., CMOS	Low-speed input clock termination selection: (default: low, LVDS; active: high, CML)
vtt	31	DC In.	Adjustable termination voltage for DIP (default: 2.5*V*)
swam35	2	LS In., CMOS	Charge pump current selection (apd current, off by default)
swf50u	14	LS In., CMOS	Charge pump current selection (fwd current, off by default)
swfm32	22		
swfm13	37		
swf20u	59		
offcdr	47	LS In., CMOS	Selects CDR or Digital mode of operation (default: low, CDR; active: high, Digital)
off0p	48	DC In.,	DATA IB thresholding
off0n	49		
losn	53	LS Out, CMOS	Input data signal quality indicator (high: good; low: not good)
oncr16	54	LS In., CMOS	cr16 frequency selection (default: low, cr=C/64, active: high, cr=C/16)
phs1	57	LS In., CMOS	Low-speed output clock clo phase selection (default: both low)
phs2	56		

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
**Low-Speed I/Os**			
crp	27	Input	LVDS or CML reference clock inputs for CDR FWD. Can correspond to either C/16 or C/64
crn	28		
q15n	10	Output	LVDS data outputs
q15p	9		
q14n	7		
q14p	6		
q13n	4		
q13p	3		
q12n	99		
q12p	98		
q11n	96		
q11p	95		
q10n	93		
q10p	92		
q09n	90		
q09p	89		
q08n	87		
q08p	86		
q07n	84		
q07p	83		
q06n	81		
q06p	80		
q05n	78		
q05p	77		
q04n	73		
q04p	72		
q03n	70		
q03p	69		
q02n	67		
q02p	66		
q01n	64		
q01p	63		
q00n	61		
q00p	60		
clop	12	Output	LVDS clock outputs. Can transmit four different clock phases as defined in Table 2
clon	13		
clmp	17	Output	LVDS clock outputs
clmn	18		
sldp	45	Output	Peak detector outputs
sldn	46		

ELECTRICAL CHARACTERISTICS

| PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.14	+3.3	+3.47	*V*	±5%
vee		0.0		*V*	External ground
*I*vcc		270		*mA*	
Power consumption		890		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (dp/dn)					
Data Rate	12.5		13.6	*Gbps*	In CDR mode
	0.0		17	*Gbps*	In digital mode
Swing (Diff or SE)	0.02		1.2	*V*	Peak-to-peak
CM Voltage Level	vcc-0.8		vcc	*V*	
HS Input Clock (cep/cen)					
Frequency	0.0		17	*GHz*	
Swing (Diff or SE)	0.2		1.2	*V*	Peak-to-peak
CM Voltage Level	vcc -0.8		vcc	*V*	
Duty Cycle	40	50	60	*%*	
LS Input Reference Clock (crp/crn)					
Frequency	781		850	*MHz*	C/16 reference
	195		213	*MHz*	C/64 reference
Swing (Diff or SE)	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	vee		vcc	*V*	
Duty Cycle	40	50	60	*%*	
LS Output Data (q00p/q00n-q15p/q15n)					
Data Rate	DC		1063	*Mbps*	
Interface		LVDS			Meets IEEE Std. 1596.3-1996
LS Output Clocks (clmp/clmn, clop/clon)					
Frequency	DC		1063	*MHz*	
Interface		LVDS			Meets IEEE Std. 1596.3-1996
Output of Peak Detector (sldp/sldn)					
Swing (Diff)	0		0.6	*V*	Peak-to-peak over full input range
CM Voltage Level		vcc -2.5		*V*	
CMOS Control Inputs/Outputs					
Logic "1" level	vcc -0.4			*V*	
Logic "0" level			vee +0.4	*V*	
Timing Parameters					
clm and clo to q0-q15 delay variation		±2.5		*%*	Over the full temperature range

PACKAGE INFORMATION
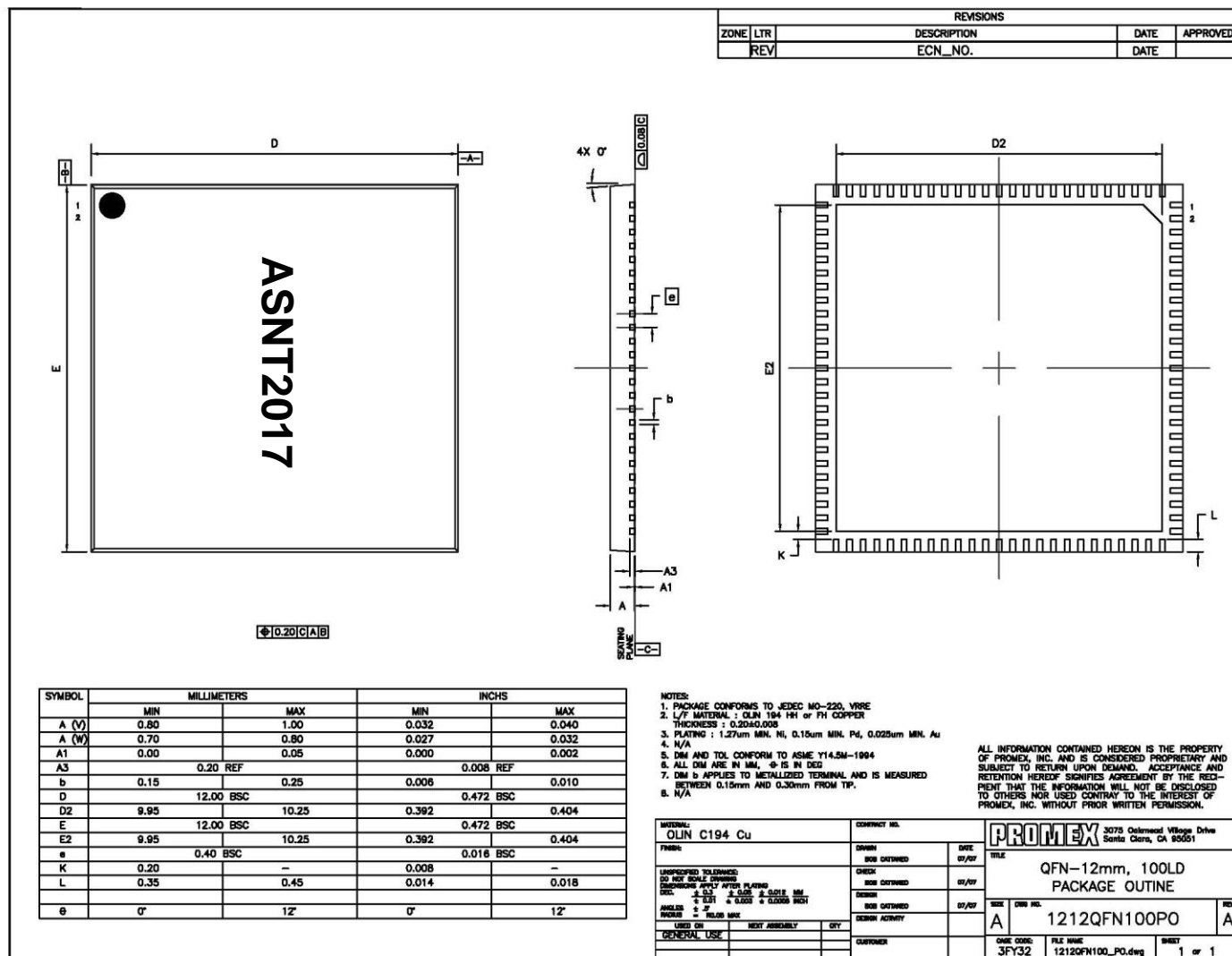
Fig. 4. Package Drawing

The chip die is housed in a custom 100-pin CQFP package shown in Fig. 4. Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the **vee** plain that is ground for the positive supply.

The part's identification label is ASNT2017-PQA. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

Ultra High-Speed Mixed Signal ASICs

REVISION HISTORY

Revision	Date	Changes
2.0.2	05-2020	Updated Package Information
1.9.2	07-2019	Updated Letterhead
1.9.1	06-2014	Corrected frequency of operation in CDR mode
		Corrected electrical characteristics
1.8.1	01-2014	Corrected description
		Corrected electrical characteristics
		Revised package information
1.7.1	07-2013	Corrected format
1.6.1	01-2013	Corrected LS output data rate and output clock frequency
1.5.1	12-2012	Corrected Electrical Specifications
1.4.1	10-2012	Corrected Data/Clock Input frequency
1.3.1	07-2012	Added Peak Detector description
1.2.1	06-2012	Corrected LCI description
		Added loop filter schematic
		Corrected formatting
1.1	06-2012	Added package pin out drawing
		Corrected pin out information
		Added Absolute Maximum Ratings
		Revised Package Information section
1.0	03-2011	First release