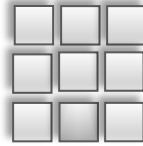


LSI/CSI



LS7190

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Digital Potentiometer/Rheostat with Incremental Encoder and SPI Interface

FEATURES:

- 64 position wiper control
- Direct interface with Incremental Encoders
- Adjustable debounce for mechanical encoder/switch
- Configurable to operate with non-quadrature clock
- SPI interface for host MCU controllers
- Supply voltage: 3 to 5 volts
- Available in 20K, 50K and 100K versions
- Qualifies for automotive temperature range
- Available in SOIC-8, SOIC-14 and TSSOP-14

APPLICATIONS:

- Replacement for mechanical potentiometer
- Potentiometer adjustment with mechanical Incremental encoder
- Remote adjustment of instrumentation for gain, offset, time constant, line impedance matching, audio equipment volume control etc.

GENERAL DESCRIPTION:

LS7190, LS7191, 7192, LS7193, LS7194 and LS7195 are versions of a three terminal digital potentiometer. Quadrature clocks from an incremental encoder or non-quadrature up and down clocks are applied to the A and B inputs. The clocks drive an internal 6-bit up/down counter with a count N ranging between 0 and 63 to correspond to 64 wiper-tap positions of a resistor chain consisting of 64 equal resistors. Each count equals to incremental resistance change of $R/64$ between the wiper terminal, Tw and either terminal Ta or Tb. For example, incremental resistance for 20K is $20K/64 = 312.5\Omega$, for 50K is $50K/64 = 781\Omega$ and for 100K is $100K/64 = 1.6K$. For 20K resistor count $N = 1$ corresponds to Tw to Tb resistance = $(20K/64) \times 1 = 312.5\Omega$ and Tw to Ta resistance = $(20K/64) \times (64 - 1) = 19.688K$. For $N = 63$ Tw to Tb resistance is $(20K/64) \times 63 = 19.688K$ and Tw to Ta resistance = $(20K/64) \times (64 - 63) = 312.5\Omega$.

LS7190 and LS7193 interfaces with quadrature clocks from incremental encoders and LS7191/92 and LS7194/95 interfaces with non-quadrature up (A) and down (B) clocks. A and B inputs for LS7190/91 and LS7193/94 are debounced allowing these signals to be sourced from mechanical encoders or push-button switches. A and B inputs for LS7192 and LS7195 are not debounced so that fast clocks from electronic clock sources can be used. Following is a summary of the main functional differences among different models:

- LS7190 and LS7193: A/B inputs quadrature mode, A/B inputs debounced.
- LS7191 and LS7194: A/B inputs non-quadrature mode, A/B inputs debounced.
- LS7192 and LS7195: A/B inputs non-quadrature mode, A/B inputs non-debounced

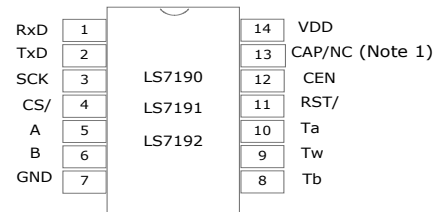


Fig 1A (SOIC-14 and TSSOP-14)

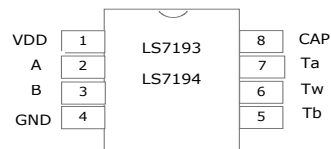


Fig 1B (SOIC-8)

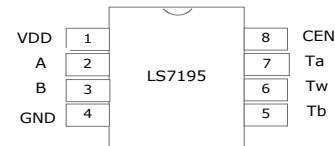


Fig 1C (SOIC-8)

Note 1. Pin 13 is "No Connection" in LS7192

Inputs RxD, TxD, SCK and CS/ together constitute the SPI bus for communicating with a host MCU. The SPI bus interface is available in LS7190, LS7191 and LS7192. T... MCU can preset the counter for a specific tap position in... se devices or read their current tap positions and save the data in external non-volatile memory.

The counter in all these devices can be enabled or disabled for counting with the CEN input or preset with the RST/ input to $N = 32$ to correspond to the potentiometer mid-point for the wiper terminal, Tw. Upon power-up Tw is set to $N = 32$

INPUTS/OUTPUTS:

RxD (pin 1). Receive Data input. Data is received on this input from the host MCU in SPI mode 0 protocol. (See fig 5). This input has a soft internal pull-up.

TxD (pin 2). Transmit data output. Data is sent on this output to the host MCU in SPI mode 0 protocol. (See fig 5). The TxD output goes into high impedance state when CS/ input is high or when device is not transmitting.

SCK (pin 3). Shift clock input for shifting SPI data in and out of the selected device. The clock must be supplied by the host controller. This input has a soft internal pull-up.

CS/ (pin 4). Chip Select input in SPI mode 0 protocol (See fig 5) for enabling the LS7190/91/92 for data receive or transmit. This input has a soft internal pull-up.

A (pin 5, pin 2), **B** (pin 6, pin 3): Count Inputs. In quadrature mode A and B inputs together constitute the quadrature clocks to increment or decrement the counter. When A leads B the counter increments, when A lags B the counter decrements. LS7190 and LS7193 operate in quadrature mode.

In non-quadrature mode, input A functions as UP count input and input B functions as the DOWN count input. The counter advances at positive transition of A and B. LS7191, LS7192, LS7194 and LS7195 operate in non-quadrature mode. For either quadrature and non-quadrature mode the counter does not roll over but freezes at maximum (63) or minimum (1) until the count direction is reversed.

GND (pin 7, pin 4). Supply ground, to be connected to the power supply negative terminal.

Tb (pin 8, pin 5). Potentiometer terminal B

Tw (pin 9, pin 6). Potentiometer wiper terminal.

Ta (pin 10, pin 7). Potentiometer terminal A.

RST/ (pin 11, pin 8). Reset input. A low at this input presets the counter to N=32 which corresponds to the potentiometer mid-point for the wiper tap. The RST/ input has an internal pull-up.

CEN (pin12). Count enable Input. A logic high at the CEN input enables the device for counting; a logic low at the CEN input disables the device from counting. The input has an internal pull-up. In LS7193 and LS7194 counting is enabled all the time.

CAP (pin8, pin13). A capacitor at this pin sets the debounce oscillator frequency for the A and B inputs for the applicable devices. The oscillator period is set as follows:

$T_{OSC} = 39E3xC @ Vdd = 3V$

$T_{OSC} = 33E3xC @ Vdd = 5V$

Where C is the capacitor at CAP pin.

A and B inputs debounce delay is $T_{DB} = 10xT_{OSC}$

VDD (pin 14, pin 1): Supply voltage positive terminal

ABSOLUTE MAXIMUM RATINGS:

(All voltages are referenced to GND; $T_A = +25^{\circ}C$ unless otherwise specified)

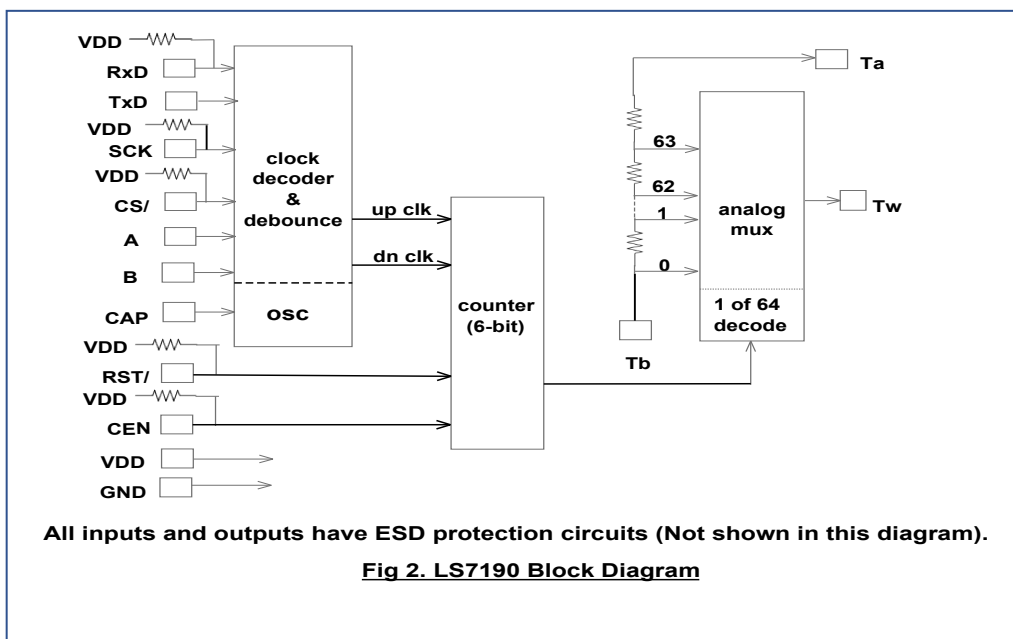
Supply Voltage.....	-0.3V min, +7V max
Ta, Tw, Tb voltages.....	-0.3V min, VDD+0.3V max
Current Ta-Tw, Tb-Tw, Ta-Tb.....	20mA for 20K versions
Current Ta-Tw, Tb-Tw, Ta-Tb	8ma for 50K versions
Current Ta-Tw, Tb-Tw, Ta-Tb	4ma for 100K versions
Input voltages (all inputs).....	-0.3V min, VDD+0.3V max
Operating temperature.....	-40°C to +125°C
Storage temperature.....	-65°C to +150°C

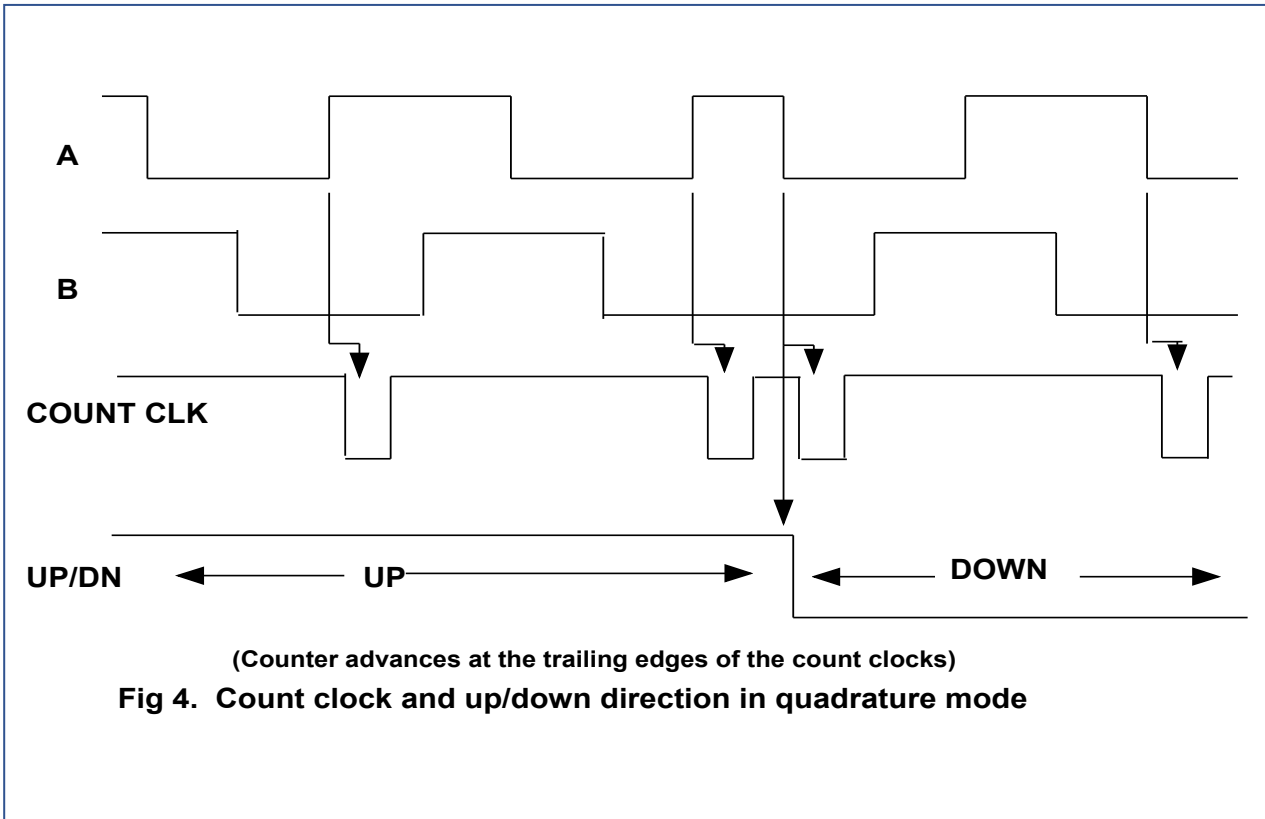
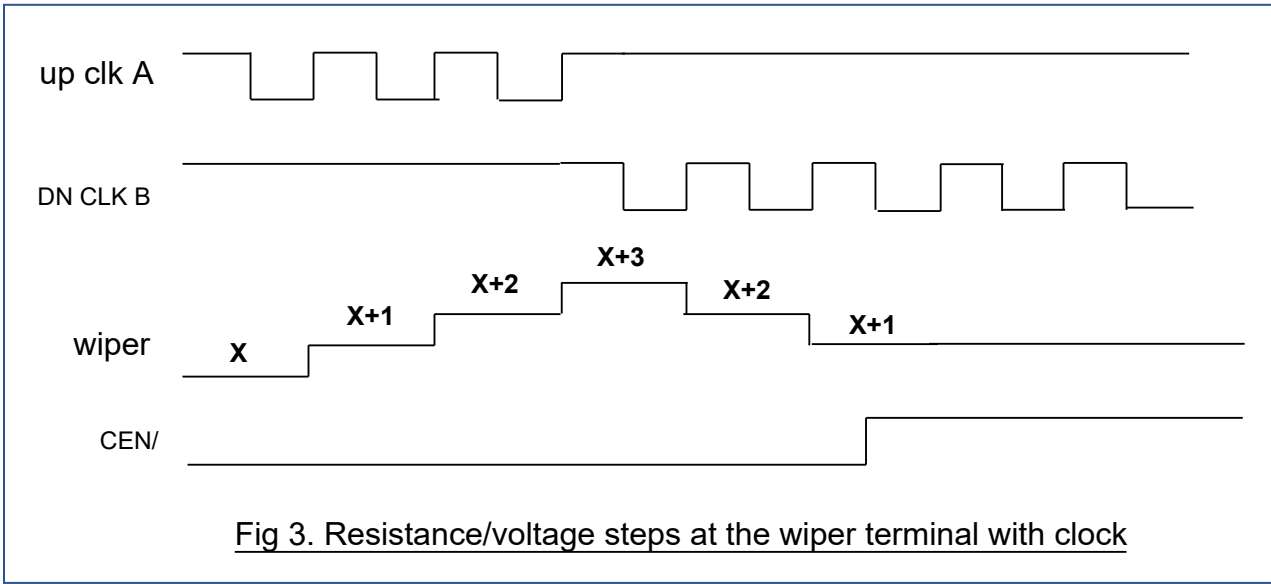
The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, or for any infringements of patent rights of others which may result from its use

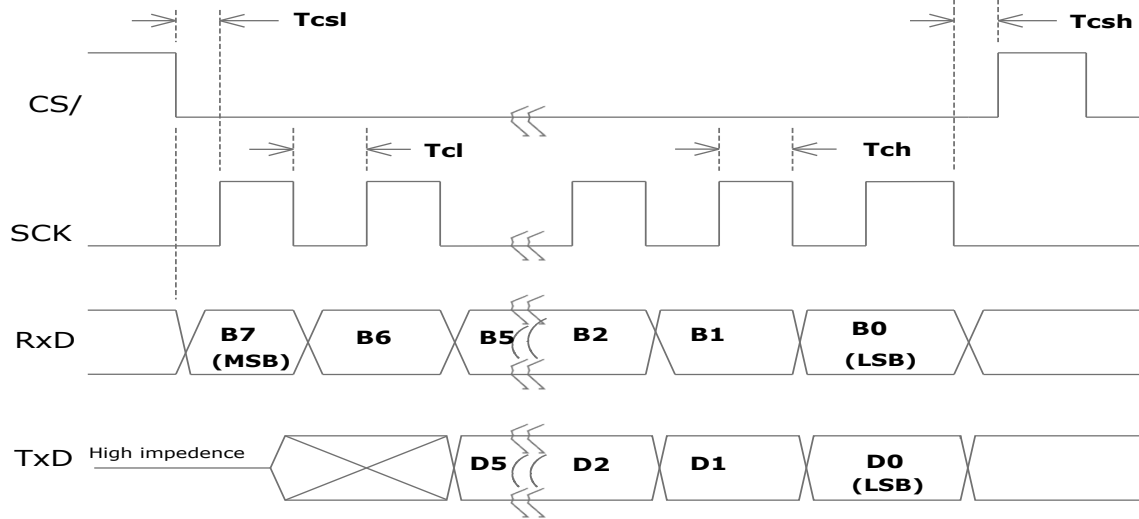
ELECTRICAL/TRANSIENT CHARACTERISTICS; VDD = 3V to 5V, TA = -40°C to +85°C unless specified otherwise						
Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	VDD	3.0	-	5.0	Volt	
Supply Current	IDD	-	7/18	-	uA	VDD = 3V/5V, debounce osc off
		-	76/238	-	uA	VDD= 3V/5V, debounce osc on
Inputs A, B, RxD, SCK and CS/ high	Vsih	-	1.9/3.1	2.2/3.3	Volt	VDD = 3V/5V
Inputs A, B, RxD, SCK and CS/ low	Vsil	0.8/1.5	0.9/1.6	-	Volt	VDD = 3V/5V
Inputs A, B, RxD, SCK and CS/ hysteresis	Vsihs	-	0.79/1.18	-	Volt	VDD = 3V/5V
Input Logic high (All other inputs)	Vih	-	0.5VDD	0.7VDD	Volt	
Input Logic low (All other inputs)	Vil	0.1VDD	0.3VDD	-	Volt	
Input current, all inputs high	I1h	-	50	-	nA	Leakage current
Input current A, B low	I1l	-	-50	-	uA	Leakage current
Input current RxD, CS/, SCK low	I2l	-3	-6	-10	uA	Vi = 0.1V
Input current, CEN, RST/ low	I3l	-7	-14	-25	uA	Vi = 0.1V
TxD output current sink	Iosnk	1.3/3.8	3.0/4.8	-	mA	Vo = 0.5V, VDD = 3.0V/5.0V
TxD output current source	Iosrc	- 1.5/-2.4	-2.5/-4.8	-	mA	Vo = 2.0V/4.0V, VDD = 3.0V/5.0V
Input voltage Ta, Tb, Tw	Vtrm	0	-	VDD	Volt	
Current between terminals Ta-Tb, Ta-Tw, Tb-Tw	Itrm	-	-	4.0	mA	See absolute maximum ratings on page 2.
Resistor tolerance	ΔR	-20	-	20	%	TA = 27°C
Resistor temperature coefficient	Rtc	-50	-200	-350	ppm/°C	
Wiper resistance	Rw	34	46	64	Ω	VDD = 5V
Debounce clock Period	Tosc	-	(39E3)xC	-	S	VDD = 3V, C = capacitor on CAP pin
		-	(33E3)xC	-	S	VDD=5V, C = capacitor on CAP pin
A, B debounce delay (Note 1)	Tdb	-	10xTosc	-	S	
A, B frequency (Note 2)	fab	-	-	3/10	MHz	VDD = 3V/5V, TA = 27°C
SCK high pulse width	Tch	120/100	-	-	nS	VDD= 3V/5V
SCK low pulse width	Tcl	120/100	-	-	nS	VDD= 3V/5V
CS/ set up time	Tcsl	120/100	-	-	nS	VDD= 3V/5V
CS/ hold up time	Tcsh	120/100	-	-	nS	VDD= 3V/5V
CS/ high between commands	Tich	120/100	-	-	nS	VDD= 3V/5V

Note 1. For LS7190, LS7191, LS7193 and LS7194

Note 2. For LS7192, LS7195



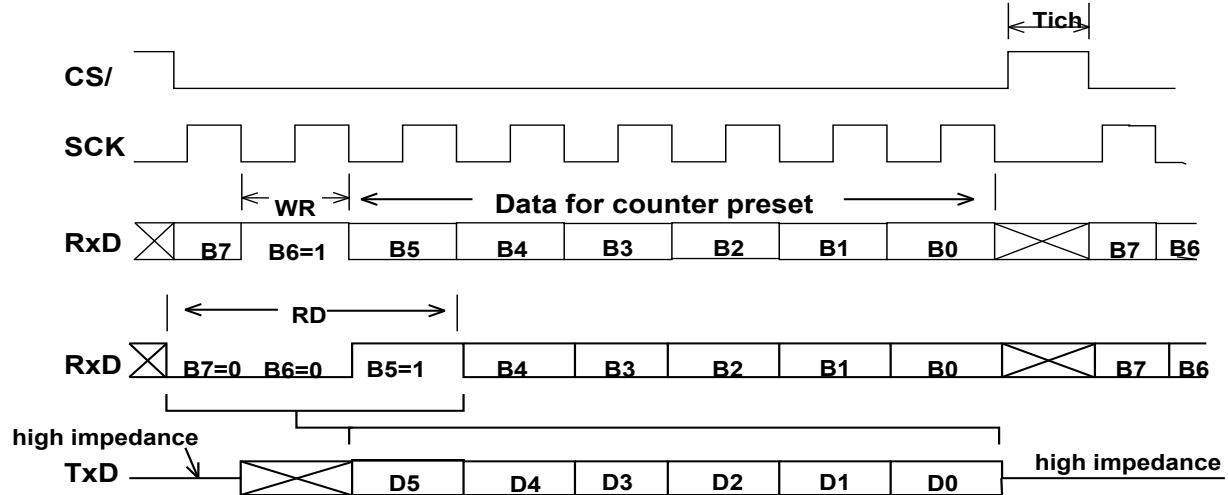




Note. The SPI port of the host MCU must be set up in Mode0 as follows:

1. MCU in Master mode
2. SCK idle state = low
3. SCK clock edge for RxD data shift = high to low
4. SCK clock edge for input data (TxD) sample by the MCU = low to high

Fig 5. SPI bus protocol in Mode 0



Note1. In RD (read) operation received data (RxD) B7 and B4 through B0 are irrelevant
 Note2. TxD data D5 through D0 represent the counter value.
 Note3. In WR (write) operation TxD stays in high impedance state throughout RxD data shift

Fig 6. SPI Read and Write

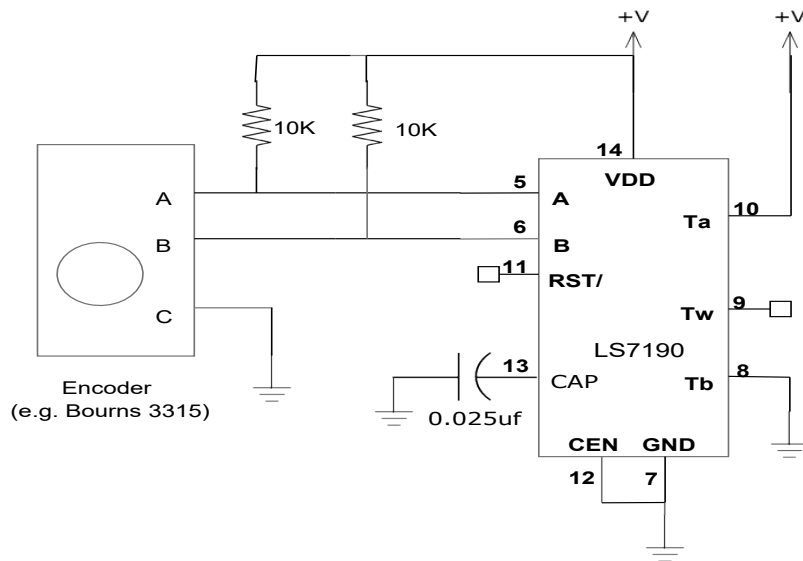


Fig 7. Mechanical encoder interface with 8ms A/B debounce

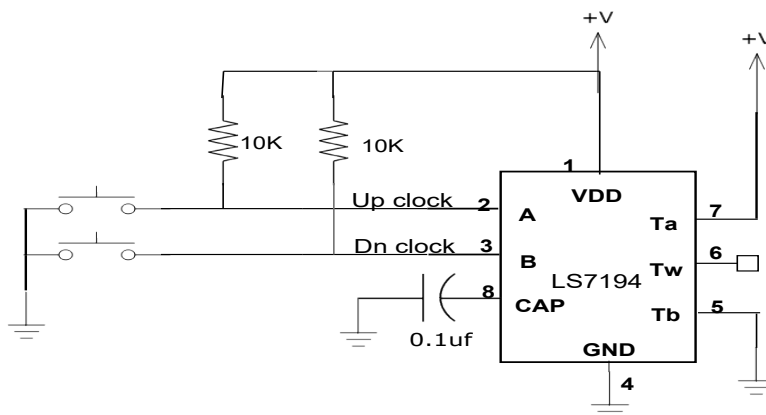


Fig 8. Push-button clock interface with 33ms A/B debounce

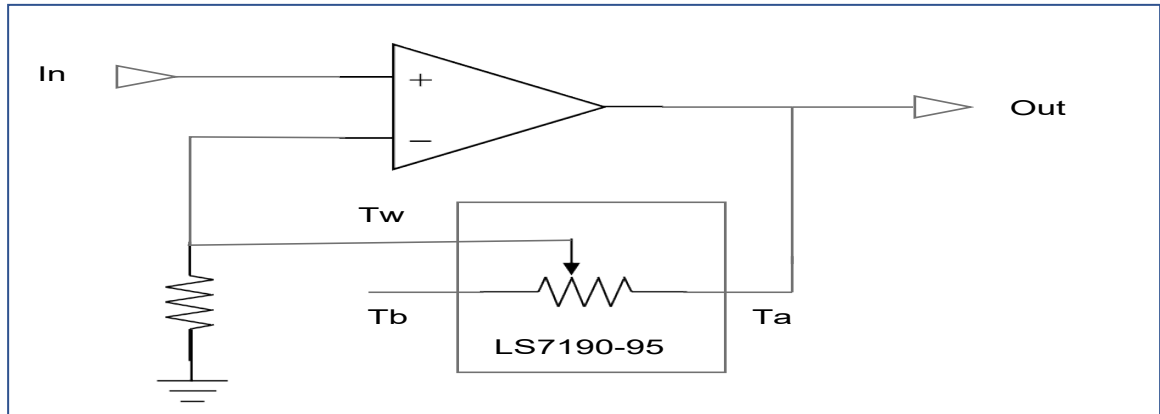


Fig 8. Rheostat mode for variable gain amplifier application

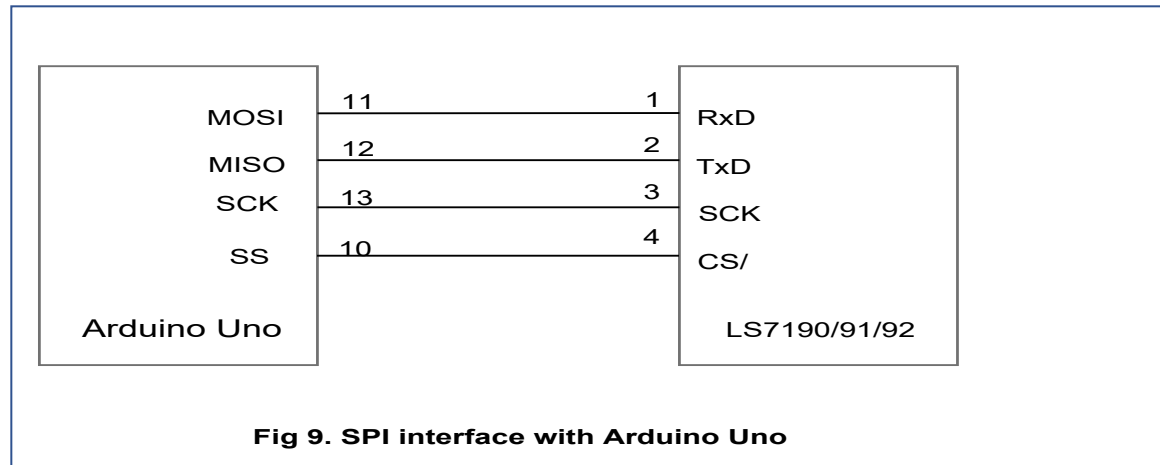


Fig 9. SPI interface with Arduino Uno

```

/*****
This program is implemented on Arduino Uno for communicating with LS7190-93 via SPI.
The program displays the current wiper tap position in LS7190-93 on the serial monitor
and allows for selecting a new tap position with keyboard entry. Any new tap position entry is
automatically stored in the Arduino Uno EEPROM and displayed.
*****/
#include <SPI.h>
#include <EEPROM.h>

/*****parameters definition*****/
const int slaveSelectPin = 10;
const int bit_mask = 0x3f; //mask for recovering wiper address from received data
const int wr_op = 0x40; //opcode for write = 0x40
int wr_tap; //wiper tap 2-digit address
int wipertap; //address and WR opcode combined
int wiperAddress; //current wiper tap address
int tapPoint; //wiper tap address stored in EEPROM
/*****End parameters*****/

/*****Set up SPI protocol*****/
void setup() {
  pinMode(slaveSelectPin, OUTPUT); //set the slaveSelectPin as an output

  //set the SPI mode=0, sck speed=4MHz and MSB first
  SPI.beginTransaction(SPISettings(4000000,MSBFIRST,SPI_MODE0));

  SPI.begin(); // initialize SPI
  Serial.begin(9600);
}

/*****End SPI setup*****/

/*****Main loop*****/
void loop()
{
  delay(1000);

  RD(); //Read, store and display current wiper tap point

  Serial.print( "Current Wiper tap in device = ");
  Serial.print( tapPoint);
  Serial.print("\n");
  Serial.print( "Wiper tap saved in EEPROM = ");
  Serial.print( wr_tap);
  Serial.print("\n");

  Serial.print("Enter between 00 and 63 for new tap selection: ");
  Serial.print("\n");

  start: delay(100);

  while (Serial.available() == 0){

    wr_tap = Serial.parseInt();
    if (wr_tap > 63)
      {wr_tap = 63;} //truncate invalid entry to 63 max

    wipertap = (wr_op | wr_tap); //address and WR opcode combined
    digitalWrite(slaveSelectPin, LOW); //select chip for write

    delay(10);

    SPI.transfer(wipertap); //send opcode plus wiper address to chip
    digitalWrite(slaveSelectPin, HIGH); //de-select chip
    EEPROM.write(0,wr_tap); //save the wiper address in memory
  }
}

```



```

Serial.print("Brightness level selected = ");
Serial.print( wr_tap);
Serial.print("\n" "\n");

return;

}

/*****End main loop*****/

/*****LS7190-93 read function*****/

int RD(){

digitalWrite(slaveSelectPin, LOW); //Select chip for read
delay(10); //send in the write code and value via SPI
wiperAdress = SPI.transfer(0x20);
delay(10);

digitalWrite(slaveSelectPin, HIGH); //take the SS pin high to de-select the chip

tapPoint = (wiperAdress & bit_mask); //Recover 6-bit wiper address from from 8-bit data
return tapPoint;

}

/*****End read and store*****/

/*****End Program*****/

```

Ordering information:

For ordering, the part numbers are designated in the format: LS71XX-PP-RR

where,

XX (Device ID) = 90, 91, 92, 93, 94 or 95

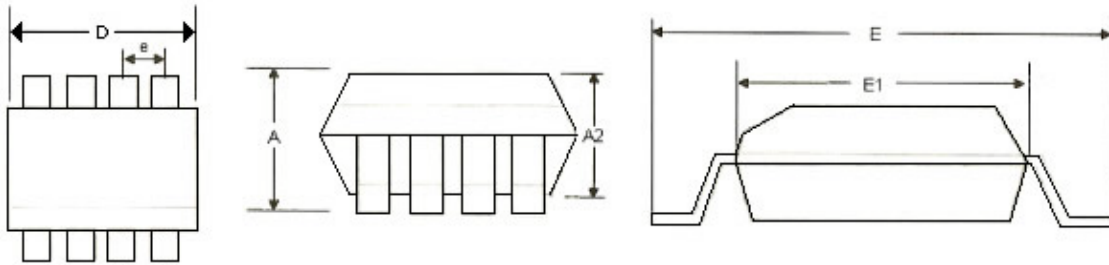
PP (Package ID), S = SOIC, TS = TSSOP

RR (Resistor Size), 02 = 20K, 05 = 50K, 10 = 100K

Example: LS7193TS05 stands for LS7193, TSSOP package, 50K resistor version

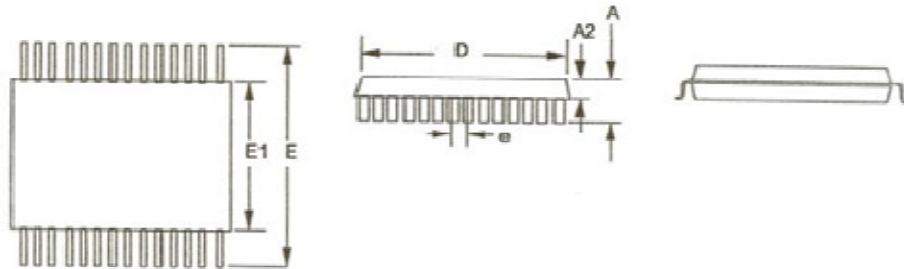
For parts to be delivered on Tape and Reel the above example is modified to: LS7193TS05-TR
(Part number designations without -TR are delivered in tubes)

SOIC PACKAGE DRAWING



Inches						
	e	E1	D	E	A	A2
SOIC-8	0.050 BSC	0.153	0.193	0.236	0.069	0.049
SOIC-14	0.050 BSC	0.153	0.340	0.236	0.069	0.049
mm						
SOIC-8	1.27 BSC	3.90 BSC	4.90	6.00	1.75 max	1.25 max
SOIC-14	1.27 BSC	3.90 BSC	8.65	6.00	1.75 max	1.25 max

TSSOP PACKAGE OUTLINE DRAWINGS



Inches						
	e	E1	D	E	A	A2
TSSOP-14	0.0256 BSC	0.173	0.196	0.252	0.047	0.039
mm						
TSSOP-14	0.65 BSC	4.40	5.0	6.4	1.20 max	1.0