600 W half bridge LLC eval board with 600 V CoolMOS™ C7 and digital control by XMC™

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Application Note

About this document

Scope and purpose

This note will describe the design and performance of a 600 W HB LLC evaluation board intended for use in the HV DC-DC stage of a switch mode power supply for server applications. This is a high performance example with a complete Infineon solution, including HV & LV power MOSFETs, controllers, and drivers, demonstrating a very effective way to design the isolated HV DC-DC stage of a server PSU fulfilling the 80Plus® Titanium Standard.

Key Infineon products used to achieve this performance level include:

- 600 V CoolMOS™ C7 superjunction MOSFET
- XMC4200 microcontroller
- HB gate drive 2EDL05N06PF
- Advanced dual channel gate drive 2EDN7524
- Bias QR flyback controller ICE2QR2280Z
- SyncRec MOSFETs OptiMOS™ BSC010N04LS

As well as design information and documentation of the LLC converter, the reader will receive additional information on how the 600 V CoolMOS™ C7 behaves in this LLC board and the benefits that will be achieved, how the high performance magnetics design can be approached (built for this board by partner company Kaschke Components GmbH), plus insights on how to develop LLC converters in similar power ranges adapted to your own requirements.

Intended audience

This document is intended for design engineers who wish to evaluate high performance alternative topologies for medium to high power SMPS converters, and develop an understanding of the design process and how to apply the somewhat complex LLC design methods to their own system applications.

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1 Introduction

The reduction of size in power converters by increasing switching frequency and reducing magnetics component size is a goal that has been persued for decades. The development of resonant converters with Zero Voltage Switching (ZVS) has been a cornerstone of this effort. It has at times been rightly said that resonant converters are a way to make good power from mediocre semiconductors. With the advent of CoolMOS™ high performance silicon switches based on the superjunction concept, the improvements in Figure of Merit (FoM) lessened the need for resonant topologies for many years. Now, the industry requirements for high efficiency in converter performance, which drove a trend towards resonant switching square wave converters such as the phase shift full bridge converter, are creating the need for a closer look at the somewhat more difficult to design multiresonant LLC converter. Fundametal to practical density improvement is efficiency optimization, with the attendant reduction of thermal dissipation.

Classically, fully resonant converters have had a nominal disadvantage in conduction losses compared with soft switching square wave converters like the Phase Shift Full Bridge(FSFB), due to the difference in peak versus RMS current for sinusoidal current waveforms versus trapezoidal. However, with the advent of the multi-resonant converter, and its boost mode of operation, it is possible with modern MOSFETs and their excellent FoM to achieve highly optimized results with the LLC converter. This is largely due to the fact that the square wave converter is optimized at maximum duty cycle, which is only achieved at low line condition. Hence, to provide operational capability with typical PFC front ends, and some converter hold up time capability, they will typically need to be optimized for DC input as low as 325 V or 300 V, wherein they will normally operate at 380 V with a less favorable crest factor and higher net RMS current.

In contrast, an LLC converter can be optimized for the nominal DC input voltage, and use the boost mode below the main resonance to achieve low line regulation, with proper design. As these operational conditions are transistory, usually only for tens of milliseconds, the efficiency and thermal impact of higher RMS losses are minimal. Combine this with a favorable silicon BOM situation compared with a Phase Shift Full Bridge (PSFB) for the mid power range, and the proper design approach, and a high performance converter is readily in reach.

The main benefits of the LLC are due to its full resonant behavior allowing soft voltage and current transitions, which intrinsically help to minimize losses in both the power devices and magnetic components.

Figure 1 is a summary of the main differences between the two most popular soft switching topologies in server SMPS arena, the HB LLC (red bars) and the ZVS PSFB (blue bars). The FoMs are assigned based on common practical rules well known to SMPS designers.

The selection of the most suitable topologiy is always a trade–off between the performance target and personal preference/experience: according to Figure 1, the overall average FOM is higher for the HB LLC than the ZVS PSFB.

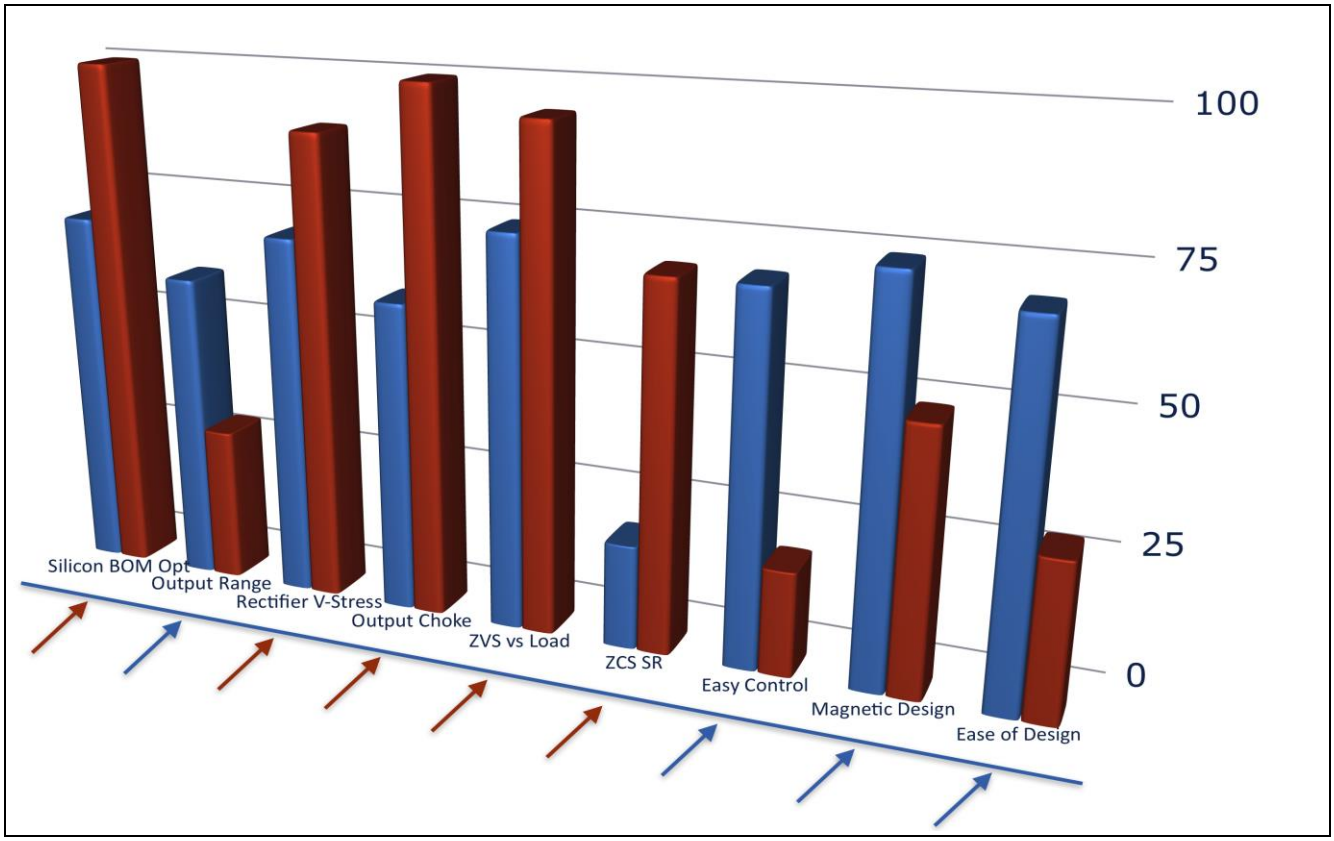

Figure 1 Comparison of several Figure of Merit(FoM) metrics based on cost and performance between the ZVS PSFB converter (blue) and the LLC HB (red).

This application note will describe the design of an LLC isolated DC-DC stage designed to be part of an 80+ Titanium converter, with an efficiency of 97.5% at 50% load or higher. When configured with a high performance PFC stage operating at 230 V_{AC} with efficiency of 98.5% or more (no more than 9 W loss), this combination will meet the 80+ Titanium requirements at half load.

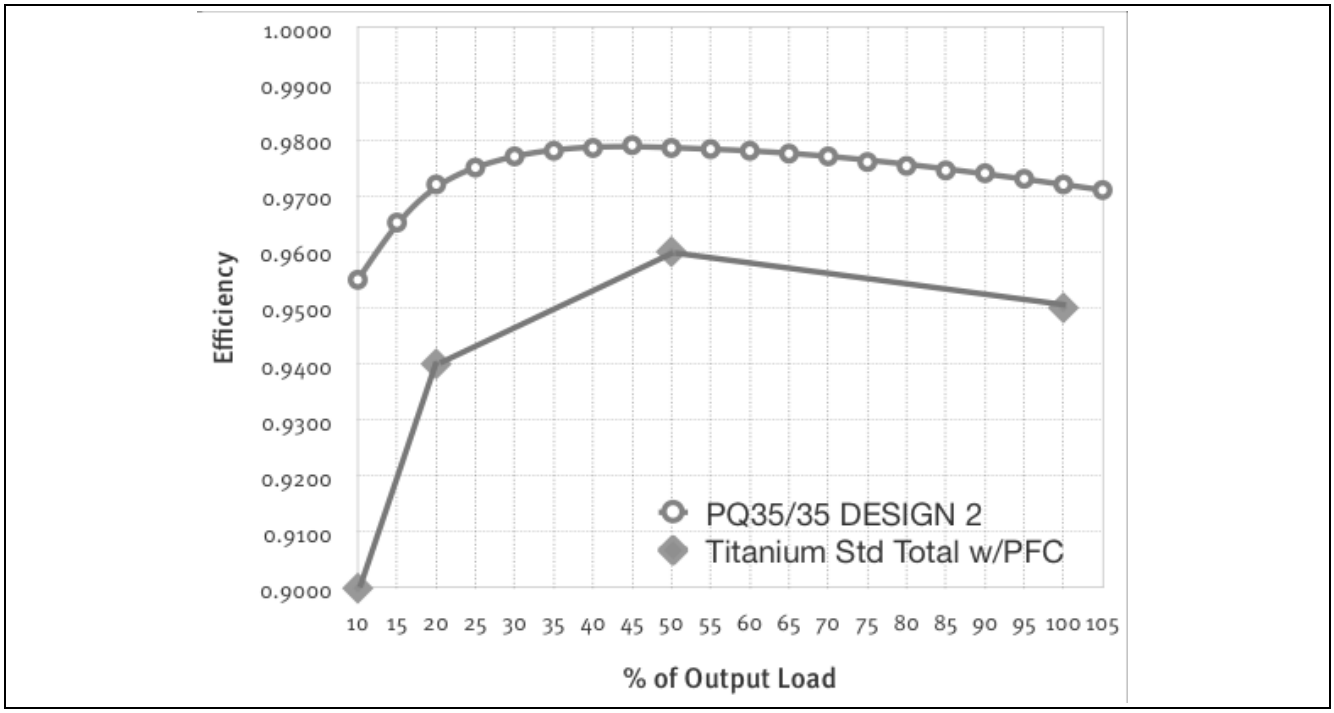

Figure 2 LLC converter efficiency and target limits for complete Titanium Std. converter (incl. PFC)

In the next section the principles of operation for the LLC converter will be examined, and the main tank design concepts reviewed. This will be followed by a brief overview of the design methodologies using both First Harmonic Approximation (FHA), and supplemented by an alternative design path using simulation based nomagraphs and component analysis. A variety of issues will be explored, including minimization of losses through optimum transformer design and operating frequency selection. Then, the 600 W evaluation board circuitry and component BOM will be described in detail.

This document will describe an analog controlled 600 W half bridge (HB) LLC converter fully designed using Infineon products.

The evaluation board can be ordered on line (ISAR) using the following ordering code:

EVAL_600W_12V_LLC_C7_d

2 HB LLC converter principles of operation

In this chapter the most common modes of operation of the LLC converter will be discussed, using an initial description of the concept behind First Harmonic Approximation (FHA). The reasoning behind the basic configuration of the resonant tank will be detailed, along with some special considerations to reduce problems with capacitive mode at startup and during burst mode. Also, the concepts and challenges for implementing synchronous rectification successfully will be outlined.

2.1 Tank configuration and operational modes

The principle schematic of a half bridge LLC converter is shown in Figure 3.

C_r, L_r and L_m represent the “resonant tank”: together with the main transformer they are the key components in the LLC design.

The primary half bridge and the output rectification are the other two stages to be defined.

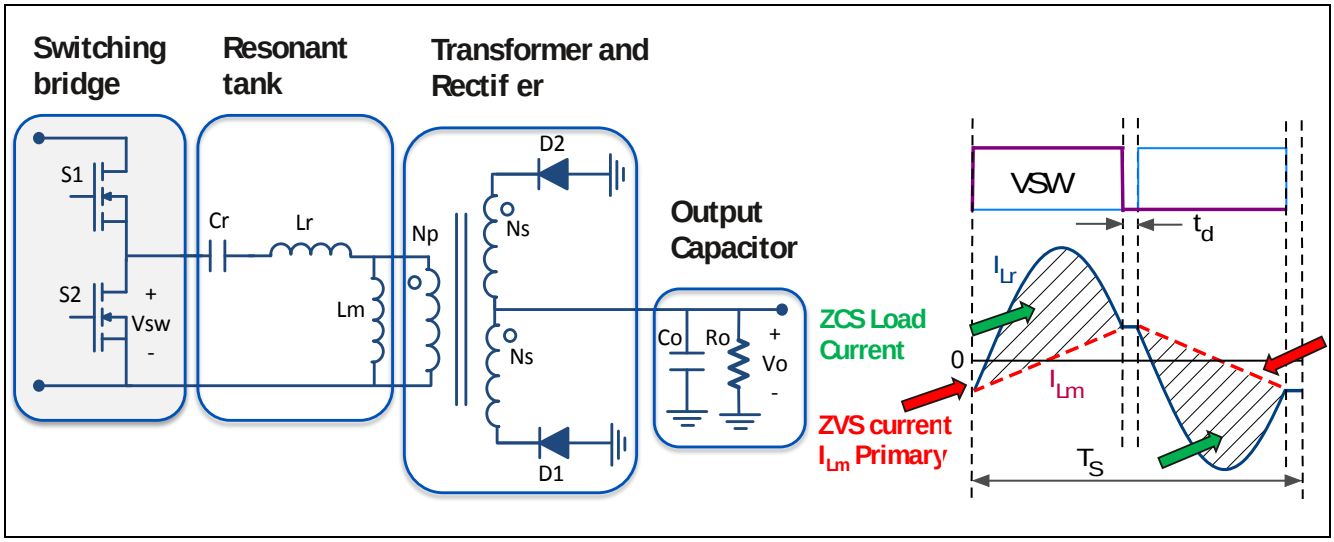

Figure 3 Principle schematic of a half bridge LLC converter

The LLC is a resonant converter - that means it operates with frequency modulation, instead of Pulse Width Modulation (PWM) - the traditional approach to power conversion. The LLC is a multi-resonant converter in that there are two resonant modes that impact the overall voltage gain. One is the series resonant combination formed by C_r and L_r; the other is a resonant mode at a lower frequency in which the inductive component is the combination of L_r and L_m, the magnetizing inductance of the isolation transformer. The overall transfer function gain “G” is defined by:

$$G = \frac{V_O}{V_{in}} = \frac{1}{2} \cdot K\left(Q, Ln, Fx\right) \cdot \frac{N_S}{N_P} \quad (1)$$

Where the gain factor is modified by ½ for a half bridge configuration, and 1 for a Full Bridge, and $K(Q,L_n,F_x)$ is a function defining the tank gain as a function of the Q of the tank and the reflected output load, L_n is the ratio of L_r to L_m, and F_x is the normalized frequency, being 1 at the series tank resonance.

When operating at the primary resonance (fo) of the series resonant tank components L_r and C_r, the highest efficiency can be achieved because load current (I_Lr in Figure 4) can be switched under ZCS conditions, optimizing for lowest switching losses at turn-off for the LLC primary side switches, S1 and S2. Furthermore, the magnetizing current of the transformer primary, L_m, can be sized so that it provides resonant ZVS

transitions for the LLC switchs S1 and S2, largely eliminating turn-on losses except for Epassive losses in the MOSFET epitaxial and edge structure, which may be thought of as an equivalent series resistance connected with C_{oss}.

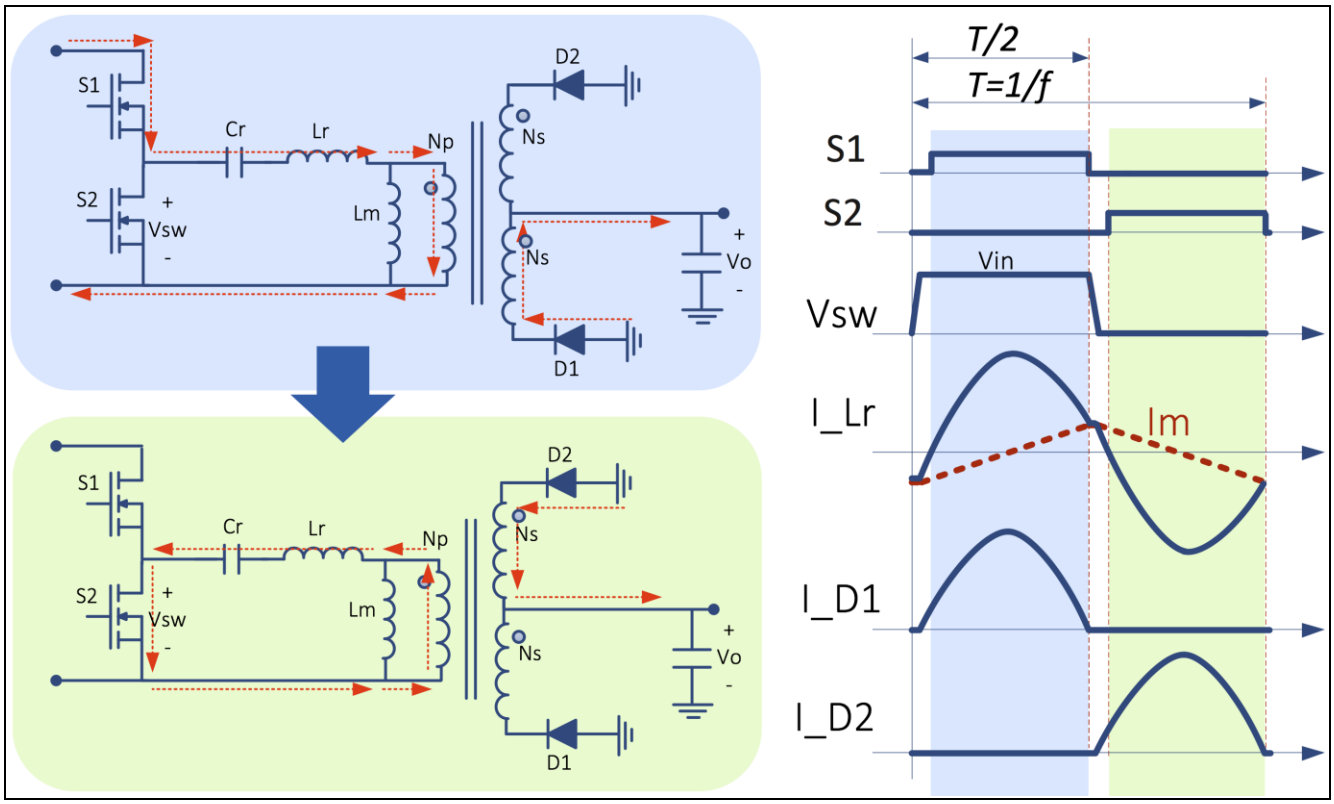

Figure 4 Fully resonant operating mode, at the resonant point for C_r and L_r, with near ZCS turn-off of the primary side MOSFETs.

Two other operating regions exist for the LLC/tank behavior;

- Over resonance, when the switching frequency is above fo, and the converter is operating in buck mode (Figure 5)
- Under resonant mode, or DCM boost mode, when the converter is operating with resonance between C_r and L_r plus L_m (Figure 5 & 6).

Over resonant mode results in buck operation, or reduction of the output voltage, to a degree dependent on the resonant circuit components, the Ln ratio, and the degree of output loading. Turn-off switching is no longer ZCS, and losses increase in this mode depending upon the switching point on the primary resonant current.

Under resonant mode results in boost operation until the resonant frequency is reached, based on the tank components C_r, L_r + L_m, and R_{eff}, the effective loading reflected to the primary side. Boost gain comes in this mode, but the primary to secondary current transfer is discontinuous (Fig. 6, 7). Additionally, operating at the lower frequency increases the I-L_m current value, and as this current is not transferred to the output, it only contributes to increased conduction losses. Lower I-L_m results in a lower increase in conduction loss, but also lower boost up gain.

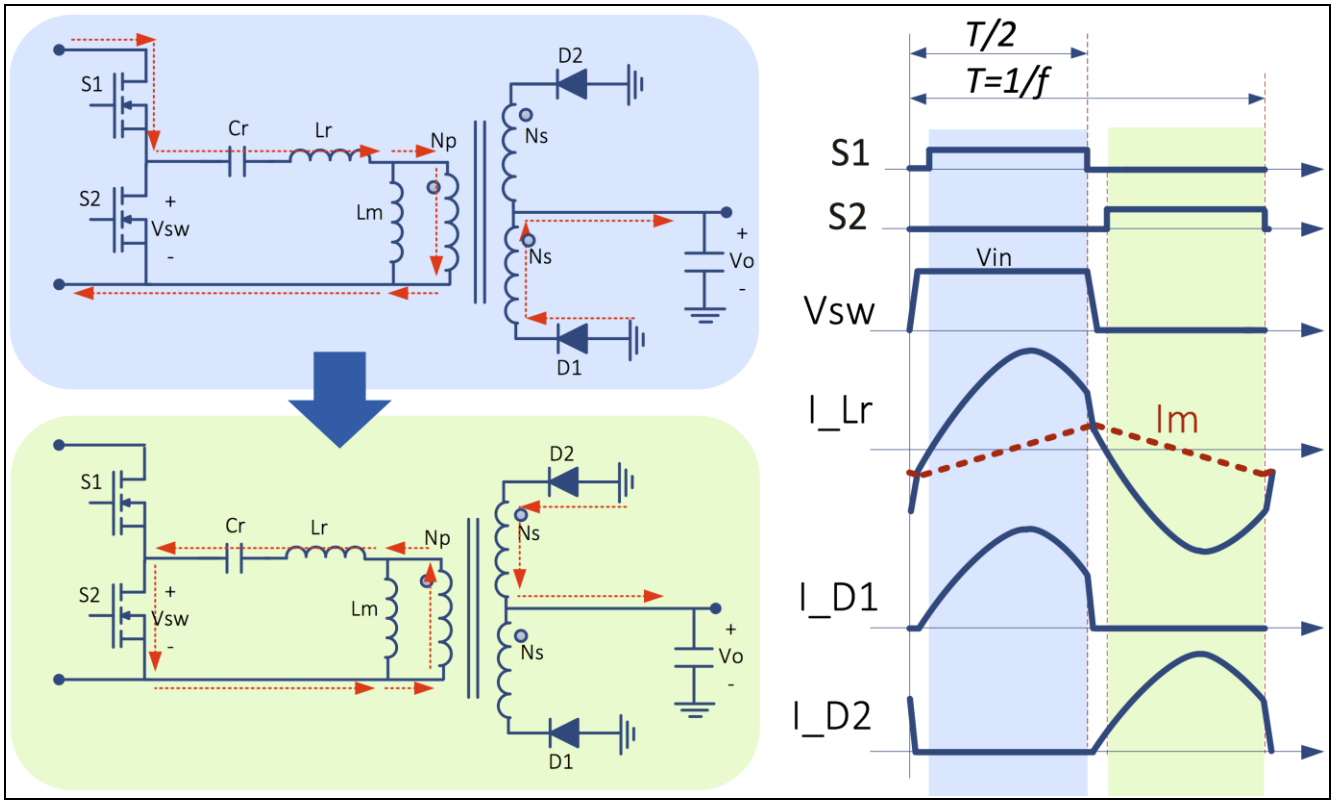

Figure 5 Over resonant operation, above C_r-L_r resonance, for both half cycles, showing tank current waveforms and non-ZCS turnoff of the primary side MOSFETs

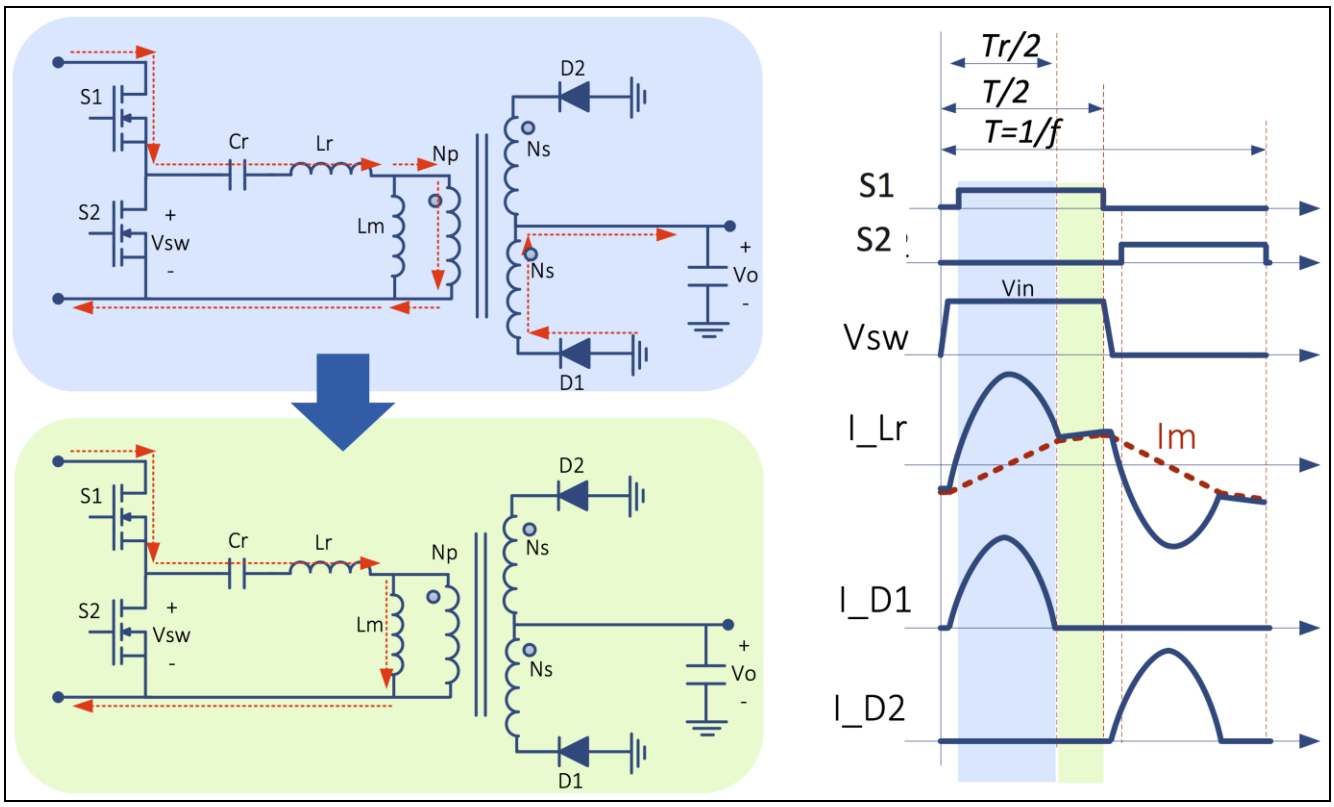

Figure 6 Under resonant DCM operation, (between resonant point of C_r and L_r, versus resonant point of C_r and L_r+L_m) half cycle 1

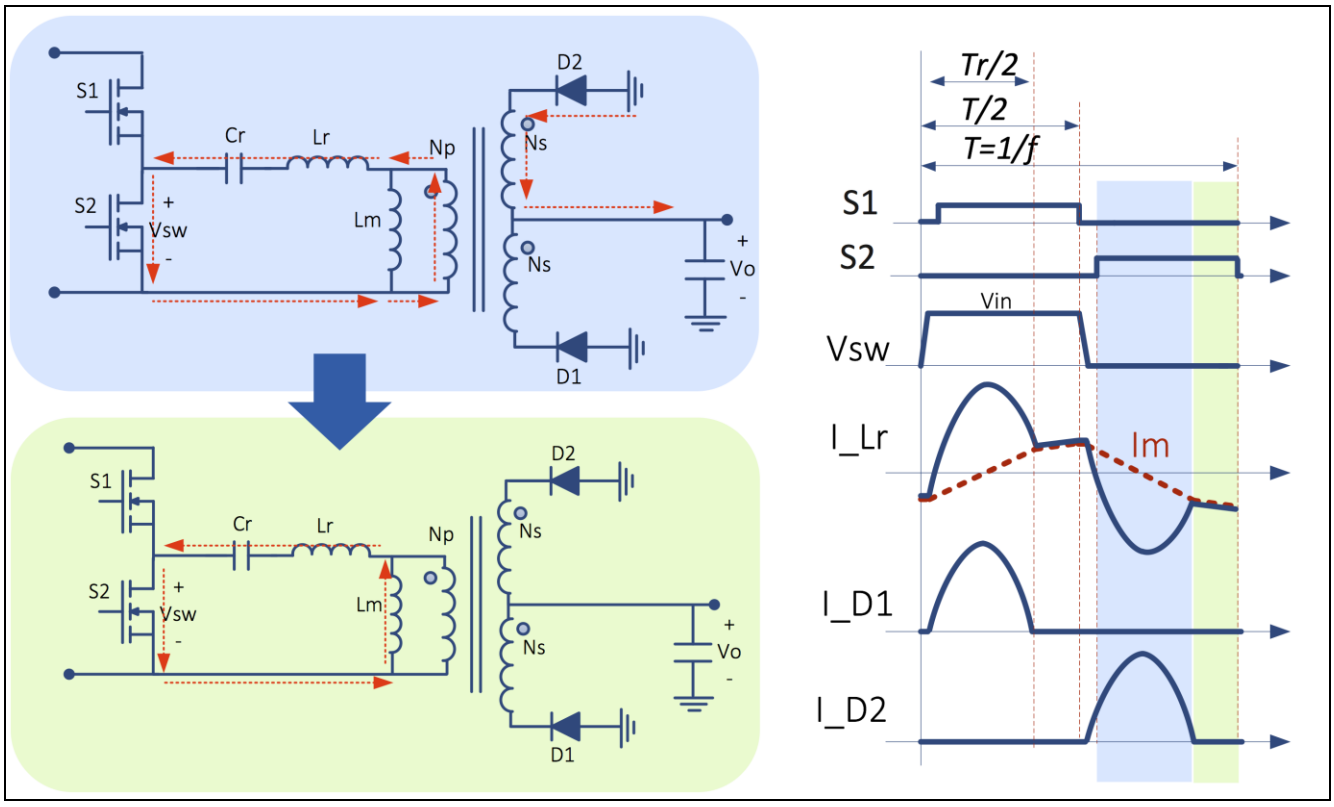

Figure 7 Under resonant DCM mode operation, (between resonant point of C_r and L_r, versus resonant point of C_r and L_r+L_m) 2nd half cycle

2.2 Analysis of the basic tank characteristics using the FHA method

The starting point in a resonant converter design is the definition of an energy transfer function, which can be seen as a voltage gain function. In other words, a mathematical relationship between the input and output voltage of the converter. Trying to get this function in an “exact” way involves several nonlinear circuit behaviors governed by complex equations requiring difficult mathematical techniques for closed form solutions [2, 3]. However, under the assumption that the LLC operates in the vicinity of the series resonant frequency some important simplifications can be introduced.

In fact, under this assumption, the current circulating in the resonant tank can be considered purely sinusoidal, ignoring all of the higher order harmonics: this is the so called First Harmonic Approximation method (FHA), which is the most common approach to the design of an LLC converter. This approach is quite valid for high Q factors with substantial loading, near the primary resonance, but falls off in accuracy at lower Q factors and lighter loading, and away from the primary resonance.

Using the FHA method the voltage gain is calculated with reference to the following equivalent resonant circuit, shown in Figure 8, with an assumed drive based on sine wave excitation; i.e. the first harmonic. This is a transformation of the circuit of Figure 8, in which the output transformer and rectifier + filter are replaced with an equivalent load R_{ac} effective, which is the output loading of the converter transformed back thorugh the converter transformer.

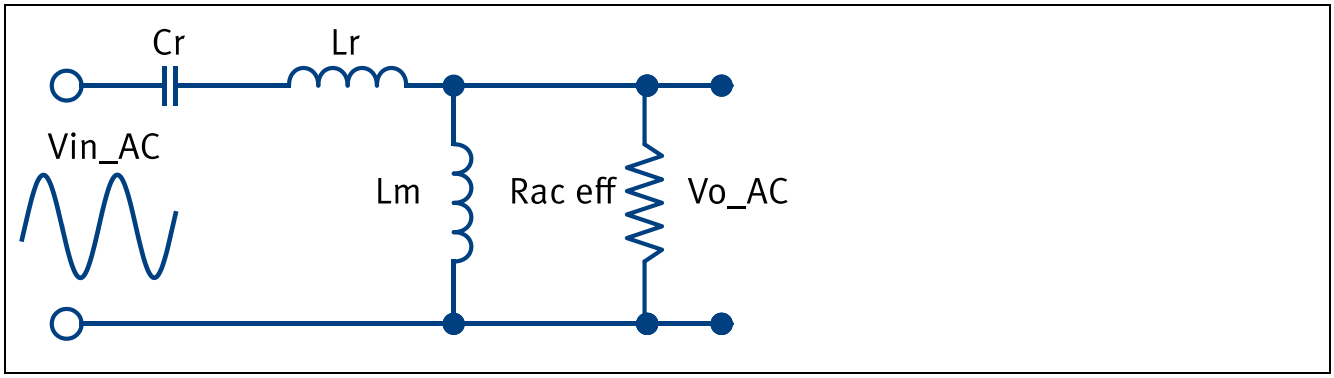

Figure 8 First harmonic approximation equivalent resonant circuit

The mathematical expression of the gain K is given in terms of a normalized resonant frequency F_x:

$$K\left(Q,Ln,Fx\right)=\frac{Fx^2\left(Ln-1\right)}{\sqrt{\left(Ln\cdot Fx^2-1\right)^2+Fx^2\cdot\left(Fx^2-1\right)^2\cdot\left(Ln-1\right)^2\cdot Q^2}} \quad (2)$$

where:

$$L_n=\frac{L_r+L_m}{L_r};\qquad f_r=\frac{1}{\sqrt{L_r\cdot C_r}};\qquad Fx=\frac{f_s}{f_r};\qquad Rac=\frac{8}{\pi^2}\cdot\frac{Np^2}{Ns^2}\cdot Ro;\qquad Q=\frac{\sqrt{L_r/C_r}}{Rac}; \quad (3)$$

Using this method, families of curves can be calculated by modeling the variation in the Q on the primary side derived from the reflected AC load, or R_{ac}, derived from the output load R_o.

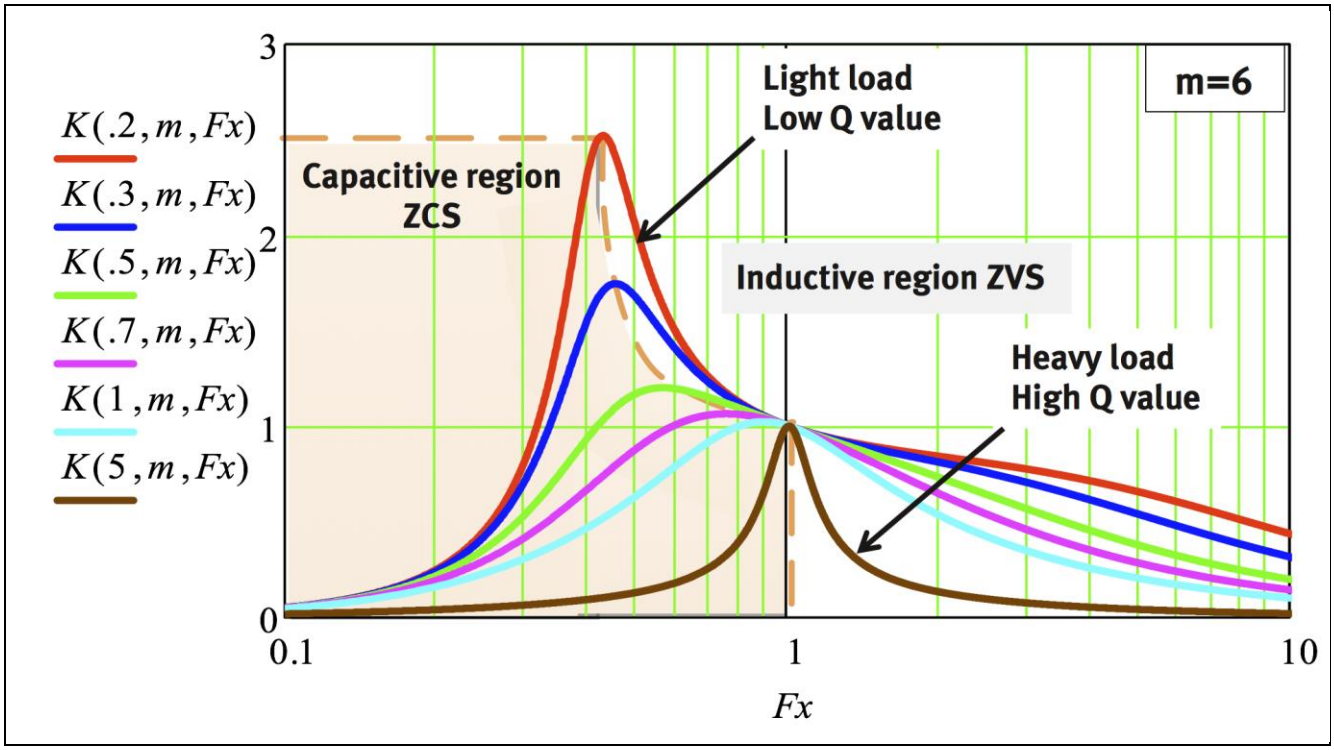

Figure 9 Family of Q curves for a fixed m inductance ratio of 6

2.3 Tank Q values and m inductance ratio: system implications

The resonant tank gain K can be plotted as a function of the normalized driving frequency f_x for different values of the quality factor Q and any single value of the inductance ratio factor m. Note; in various papers, different terminology may be encountered for both the gain definition and the inductance ratio; L_n and $_m$ are both used for the ratio of L_r to L_m.

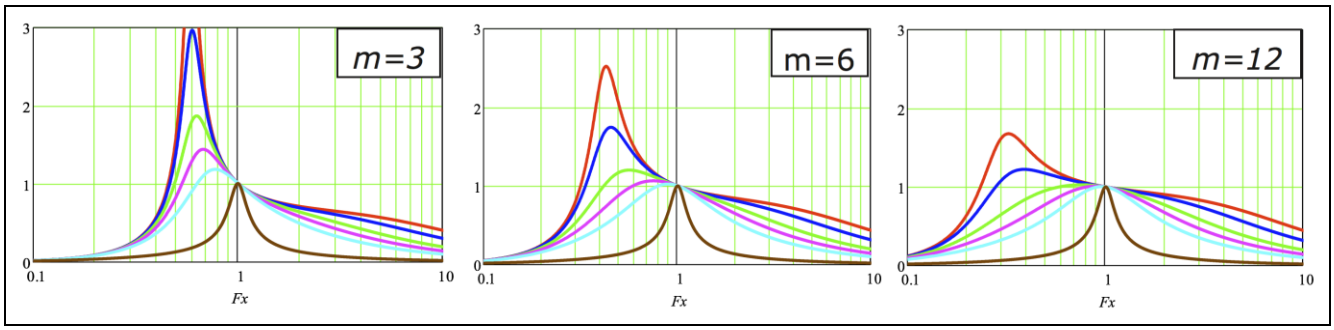

Figure 10 Family of Q curves for m inductance ratios of 3, 6, and 12

FHA can be very useful for visualizing trends and understanding the basic operating concepts in a format that is adaptable to calculation using math programs or spreadsheets. Due to the approximations used, FHA has some accuracy issues, which are greatest in the Q factor range where power supplies are typically designed, from 0.5 and below. [1, 2, 3]. Exact form calculations are quite difficult, and so there is a trend towards using simulation with a tool such as SIMPLIS. The POP (Periodic Operating Point) analysis and variable stepping make detailed simulation investigation of LLC peak gain curves in an exact sense reasonably feasible. A detailed explanation on the usage of FHA is presented in [4], and is not duplicated here. An alternative design process based on SIMPLIS generated peak gain curves in nomagraph [5] will be described.

3 A LLC design methodology for specifc application requirements starting from component technologies

3.1 Design flow

The proposed working design flow is shown in Figure 11. The goal with this approach is to, as much as possible, find a flow that minimizes iterative and repetitive steps for finding solutions, and simplifies the types of calculations required, while focusing on developing a solution based on available or realizable components. To that end, this requires executing the design tasks in a different sequence than is often used.

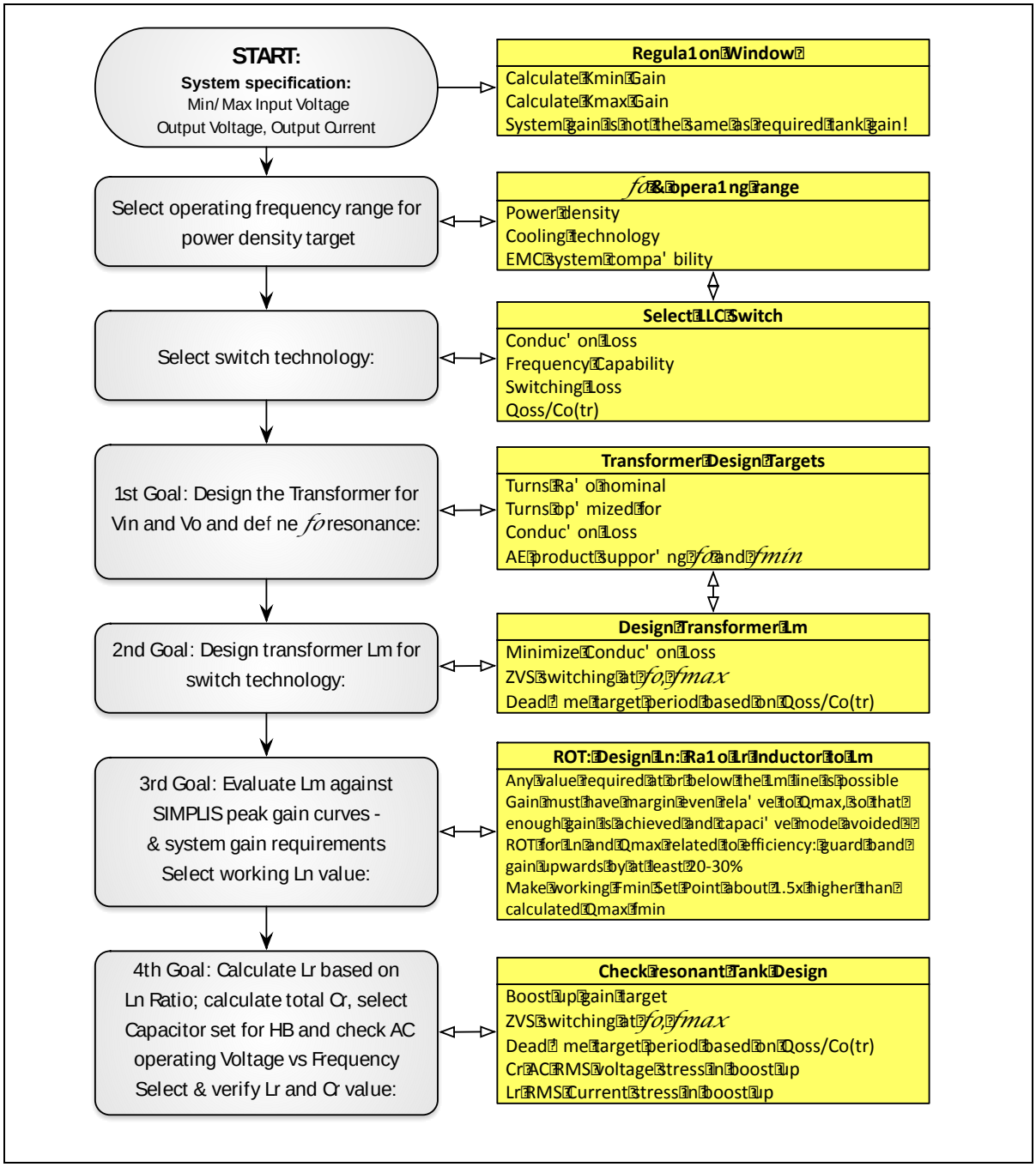

Figure 11 Design flow

3.1.1 Input design data

In Table 1 an overview of the major design parameter is displayed.

Table 1 Design parameters

Description	Minimum	Nominal	Maximum
Input voltage	350 V_{DC}	380 V_{DC}	410 V_{DC}
Output voltage	11.9 V_{DC}	12.0 V_{DC}	12.1 V_{DC}
Output power			600 W
Efficiency at 50% P_{max}	97.5% *		
Switching frequency	90 kHz	150 kHz	250 kHz
Dynamic output voltage regulation (0-90% Load step)			Max. overshoot = 0.1 V Max. undershoot = 0.3 V
V_{out_ripple}			150 mV_{pk-pk}

*80+ Titanium non-redundant for a complete SMPS is 96% at 50% load; this allows 1.5% efficiency loss for a high performance PFC stage coupled with the DC input LLC converter to configure a complete AC powered SMPS.

A compact high performance 800 W PFC Infineon reference design meeting Platinum standards at 230 V_{AC} is available [1]; this uses a conventional bridge rectifier with boost converter. Titanium standard PFC must use a quasi-bridgeless or bridgeless type design to achieve 98.5% efficiency.

From the table above, the first important design parameters can be derived:

Main transformer turn ratio

$$n = \frac{N_p}{N_s} = \frac{V_{in\_nom}}{2 \cdot V_{out\_nom}} \approx 16 \quad (4)$$

Minimum required gain

$$K_{\min}(Q, m, F_x) = \frac{n \cdot V_{o\_\min}}{V_{in\_\max}/2} \approx 0.95 \quad (5)$$

Maximum required gain

$$K_{\max}(Q, m, F_x) = \frac{n \cdot V_{o\_\max}}{V_{in\_\min}/2} \approx 1.08 \quad (6)$$

3.1.2 Select operating frequency range for design targets

While this seems a superficially easy parameter to specify, in practice it has considerable bearing on other design targets and component characteristics. Published LLC designs have fo operating ranges all the way from 40 kHz to 1 MHz and more - a separate paper could be written about the challenges and advantages to different approaches, especially considering whether the target is purely maximizing efficiency, or whether power density (which still must rely on efficiency even with forced air cooling) is the main target.

Key points to consider include:

- Power density target – how much useful improvement is possible through shrinking the size of the magnetic components? At what point is conduction efficiency compromised?
- Cooling technology – heat must be removed, and high density high frequency designs can make this more difficult
- Transformer design, which tends to move in stepped parameter groups, due to granularity of options such as core sizes, and practical turns winding steps due to steep turns ratio for low voltage outputs
- Semiconductor technology - there is a range of performance capability within the families of super-junction MOSFETs, and new technologies such as SiC and GaN switches will open additional possibilities in the near future. Here, the output Q_{oss} is a limiting factor with regards to the energy required for ZVS transitions, followed by switching turn-off losses and turn-on Epassive losses. In particular, fo operation may not be a problem, but assuring safe and adequately efficient operation at the resulting f_{max} for protection, no load, and soft start requires some evaluation.
- EMC compatibility – traditional SMPS design usually strives to keep the fundamental frequency below the 150 kHz lower measurement for conducted EMI, but the low harmonic signature of a well designed LLC converter gives some latitude for selecting a higher operating frequency

With superjunction MOSFET types suited to LLC applications, a reasonable initial range to consider for the target power range of 600 W is 100 – 160 kHz. A lower switching frequency range might permit incremental improvement of the efficiency, but probably only with larger core designs than would be cost effective.

3.1.3 Select LLC primary switch based on system requirements and technology trade-offs

First, the choice of LLC switch is based on the electrical characteristics that influence switching behavior under normal conditions operating at fo. Key device parameters include Q_{oss}, which describes the output charge needed to transition the drain to source voltage passively (when the MOSEFET is not turned on) and describes the behavior during ZVS switching. Q_{oss} is not usually given in high voltage MOSFET data sheets, but the parameter for time related output capacitance $C_{o(tr)}$ is given, and is derived from Q_{oss}. The lower the value of the effective $C_{o(tr)}$, the less current is required for a given drain to source transition time, and the this allows a higher value of magnetizing inductance for the transformer, which in turn lowers parasitic losses on the primary side. Also important are Q_{gd}, which describes the charge required for gate to drain switching, and R_g, which describes the limiting internal gate resistance. Combined, these two parameters give an indication of turn-off capability and losses, and hence the maximum operating frequency.

The LLC converter has two operating modes that impose particular stresses on the primary side power MOSFETs. One is always present, operating at higher switching frequencies up to $fmax$, as a result of regulation requirements, initial soft start, and over current protection. The main requirement under these conditions is assuring that sufficient $I\text{-}Lm$ current is available to complete ZVS turn-on transitions in the allocated dead time t_d, and that the turn-off behavior is sufficiently fast so that losses are not excessive when turning off under non-ZCS conditions, and that turn-off time is accomplished quickly within the total period allocated for dead time.

The other challenging operating condition is capacitive region operation in the boost mode below fo, which in a properly designed LLC converter should be avoided at all times, yet in a few conditions may be unavoidable, albeit briefly. In this operating mode, the MOSFET body diode will be conducting current and then hard commutated when the other MOSFET on the primary side of the LLC converter turns on. Hard commutation leads to high di/dt and high dV/dt through the primary side loop, which as well as stressing the body diode and parasitic bipolar transistor of the MOSFET, may lead to hard avalanche operation simultaneously. Device characteristics affecting this mode include the reverse recovery charge Q_{rr} (the lower, the better), and the maximum allowable diode commutation speed, which is a measure of the MOSFET robustness under this operating condition.

Three current Infineon MOSFET technologies may be considered most suitable for the LLC application, but even here there is a spread of characteristics that should be considered, taking into account the parameters that may be most important for a particular design implementation.

Table 2 Key primary side MOSFET parameters for LLC

Parameter		IPP65R190CFD	IPP60R190P6	IPP60R180C7
Effective output capacitance, time related	$C_{o(tr)}$	336 pF	264 pF	349 pF
Gate to drain charge	Q_{gd}	37	13 nC	8 nC
Internal gate resistance	R_g	1.0 Ω	3.4 Ω	0.85 Ω
Reverse recovery charge	Q_{rr}	0.5 µC	4 µC	2.6 µC
Maximum diode commutation speed	di_f/dt	900 A/µs	500 A/µs	350 A/µs

CFD2 650 V is a MOSFET technology using a platinum doping lifetime killing process derived from CoolMOS™ C6, but with a number of enhancements, including a gate threshold range of 3.5 to 4.5 V optimized for bridge topology applications, and a much lower internal gate resistance. The lifetime killing process reduces reverse recovery charge by about 10:1, that dramatically improves T_{rr} and lowers the peak I_{rrm} in hard commutated applications. OTOH, the Q_{gd} charge is fairly high, which contributes to stable control in hard commutation in conventional bridge converters, but which drawback for the high operating frequency of an LLC. Effective output capacitance is moderately high, but with no abrupt corner region, so ZVS dV/dt, while slower, is well controlled. This may be the component to choose if the target design is known to have parameters leading to capacitive mode operation, as it will be the most robust choice under those conditions.

P6 600 V is also derived from C6, but with a focus on higher switching frequency SMPS applications. The super-junction structure and cell structure were optimized more for high frequency switching applications, though keeping the same overall pitch geometry, and much of the diode robustness of the C6 series. The

gate threshold voltage range of 3.5 to 4.5 V is also better suited to bridge applications than standard MOSFETs (to avoid CdV/dt turn-on when in the off state). It uses substantially lowered Q_{gd}, which is only about 35% of the CFD2 technology, which speeds drain to source switching time. The diode characteristics are conventional as regards Q_{rr}, but robust as regards the high safe diode commutation speed that is permissible. Due to the internal Rg, switching speed is not quite as fast as C7, but the robustness of diode technology and low Q_{gd} places it well in the midrange for performance.

C7 600 V is derived from the best in class 650 V C7, but with emphasis on further improvements in FoM as regards gate charge and output capacitance relative to $R_{DS[on]}$, and further lowering both hard switching and soft switching turn-on losses. Body diode robustness has been substantially improved, raising the maximum diode commutation speed from 55 A/µs to 350 A/µs, allowing some capacitive mode capbility. $C_{o(tr)}$ is even slightly higher than for CFD2, but this is a tricky issue, due to the difference in the shape of the capacitance versus drain to source voltage. Figure 12 compares the capacitance characteristics of all three technologies for 190/180 mΩ class parts. Note that the X-axis and Y-axis are not the same for each graph. C7 600 V has the lowest capacitance above 50 V, but the highest overall under 50 V.

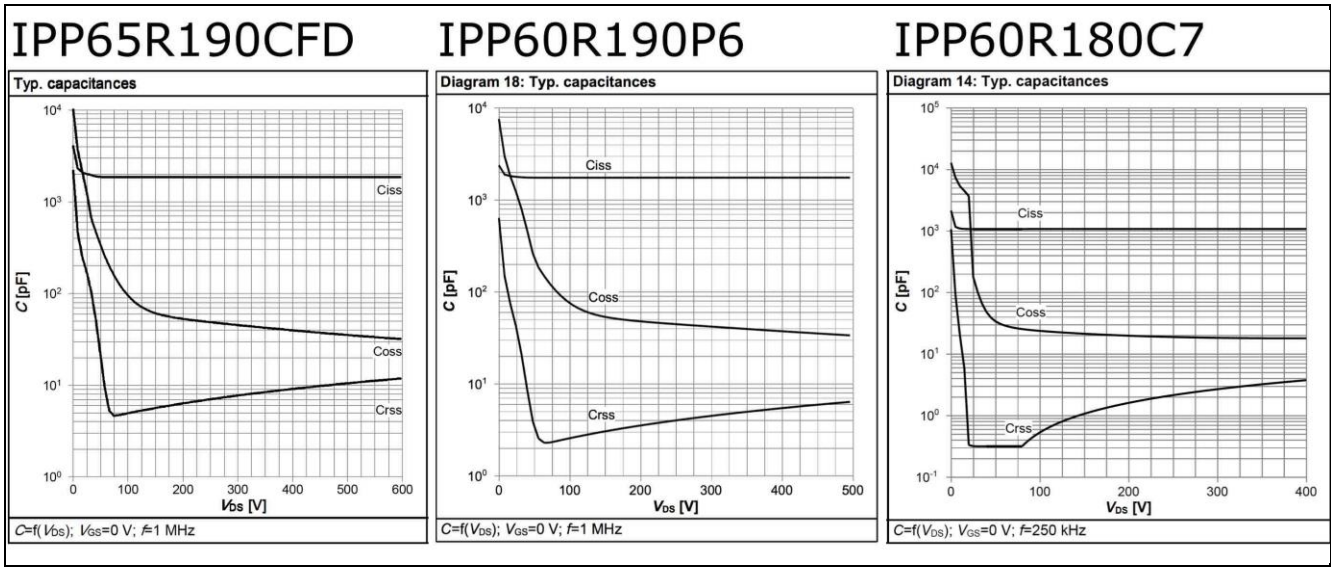

Figure 12 Key capacitance comparison for IPP65R190CFD, IPP60R190P6, and IPP60R180C7

This has a decided impact on the ZVS turn-on behavior and dV/dt, as can be seen in this SIMetrix simulation comparing the 65R190CFD, the 60R190P6, and the 60R180C7 (Figure 13). The greater turn-off delay of the 65R190CFD and higher zero voltage C_{oss} delays the onset of the ZVS transition, and higher C_{oss} reduces the dV/dt of the mid region transistion. Note that both simulations and measurements must be evaluated carefully, because normal production tolerances can result in 20% or more difference for some device capacitances from lot to lot.

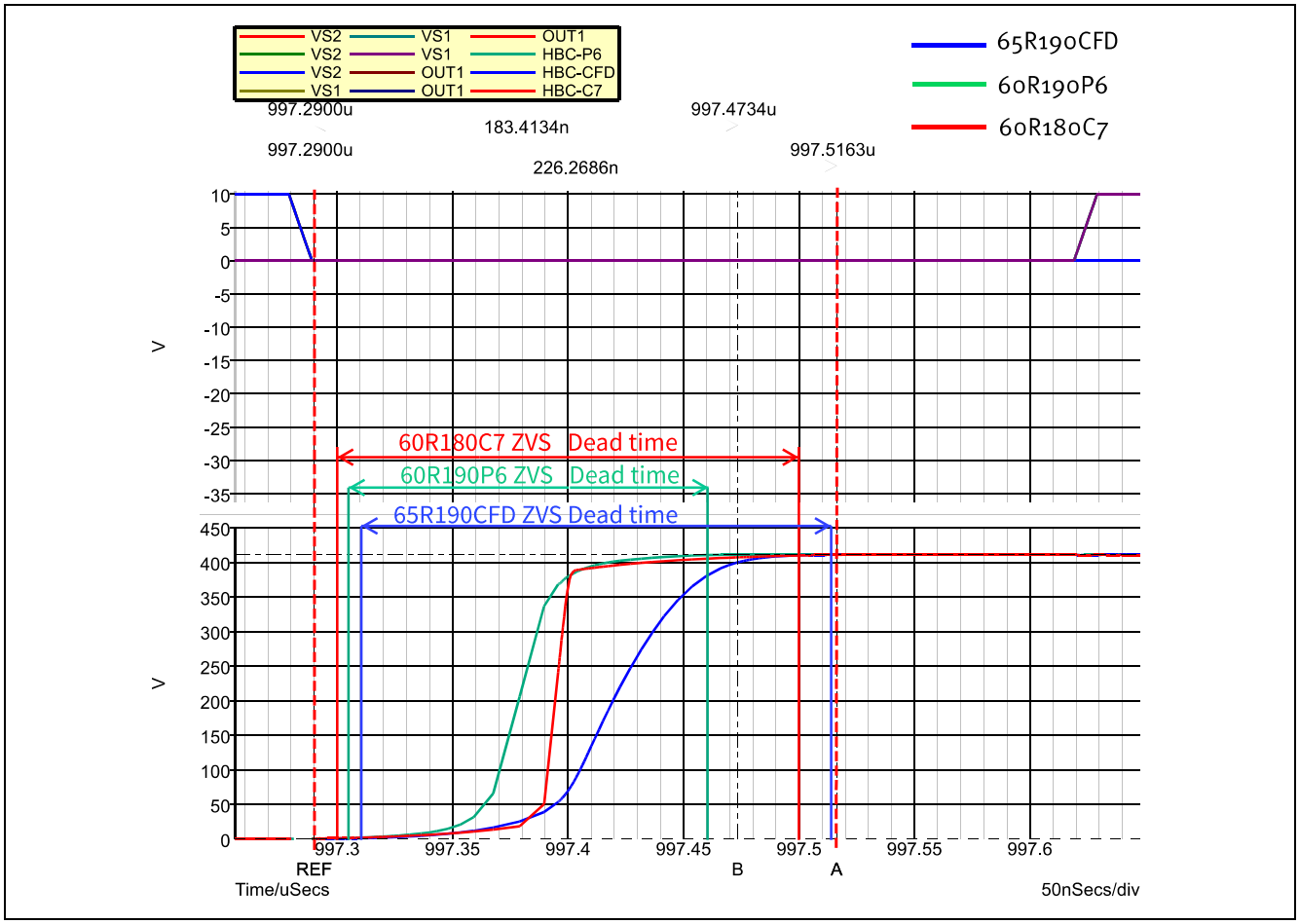

Figure 13 Comparison of dead time ZVS transition simulation at peak I-L_m of 1.4 A

Also, as expected due to the low C_{oss} above 50 V, the dV/dt in the mid voltage region between 50 and 350 V with C7 is much higher than the other two technologies. Apart from capacitively coupled common mode EMC, this is also a potential concern depending on the driver technology used. A sufficiently high CMTR capability should exist in the driver for peak $\boldsymbol{I\text{-}L_m}$ at $\boldsymbol{fo}$ and below, when $\boldsymbol{I\text{-}L_m}$ will be highest, along with the dV/dt. If needed, this may be counteracted using low value capacitors in the range of 47 to 180 pF connected from drain to source with each C7 MOSFET.

This document will describe the performance of a 600 W HB LLC evaluation board using CoolMOS™ C7 600 V technology.

3.1.4 1st goal: design the isolation transformer for V_{in} and V_o for efficiency targets at target f_o operating point

The target efficiency of this design is fixed by the 80+ Titanium standard; that means fixing certain minimum requirements for the HV DC-DC stage at 10%, 20%, 50%, 100% load conditions.

The most critical condition for the main transformer is the full load, mainly due to thermal reasons. The selection of the core size and material is performed according to this condition along with the power density (thus switching frequency) target and the available airflow.

Keeping due margin room in the design, the minimum efficiency requirement at full load is fixed for the HB LLC converter to 97%, which means the goal is to keep the total dissipated power in that condition below 18 W.

In order to guarantee a balanced spread of power and heating, a good rule of thumb in the design of the LLC converter is to keep the total power dissipated in the main transformer below 1/6 of the total dissipated power, which means the maximum dissipated power shall be 3 W. This is our first important design input.

$$P_{trafo\_MAX} = 3W \quad (7)$$

The max operating temperature is 55°C, as is common in typical server applications. Due to transformer safety insulation approvals, the max operating temperatiure of the transformer must be lower than 110°C, so:

$$\Delta T_{trafo\_MAX} = \left(110 - 55\right)^{\circ} C = 55^{\circ} C \quad (8)$$

From (7) and (8) the required max thermal resistance of the core shape can easily be derived:

$$Rth\_trafo\_\max = \frac{\Delta T_{trafo\_Max}}{P_{trafo\_Max}} = \frac{55^{\circ}}{3} C/W = 18.3^{\circ} C/W \quad (9)$$

So, the selected core shape must have thermal resistence lower than 18.3°C/W.

This requrement can be fulfilled with different choices: the preferred method will allow maximizing the ratio between available winding area and effective volume, of course compatibilty with eq. (18).

Also considering the power density target (in the range of 20 W/in^3), the most suitable selection is

PQ 35/35, shown in Figure 4, as the PQ40 offers little benefit with the increase in size.

The related coil former shows a minimum winding area of 1.58 cm^2 and a thermal resistence of 16.5°C/W, so lower than (18) and thus able to dissipate up to 3.33 W by keeping the ΔT_{MAX} <55°C.

Once verified that the thermal equations are fulfilled, we can proceed with the design of the primary and secondary windings and the core material selection, with some important goals:

- Fitting the geometry/overall dimensions of the core
- Fulfilling the condition (7)
- Try to split the losses as equally as possible between core and windings: ideally “fifty-fifty” should be achieved at full load, but any percentage close to it would be acceptable.

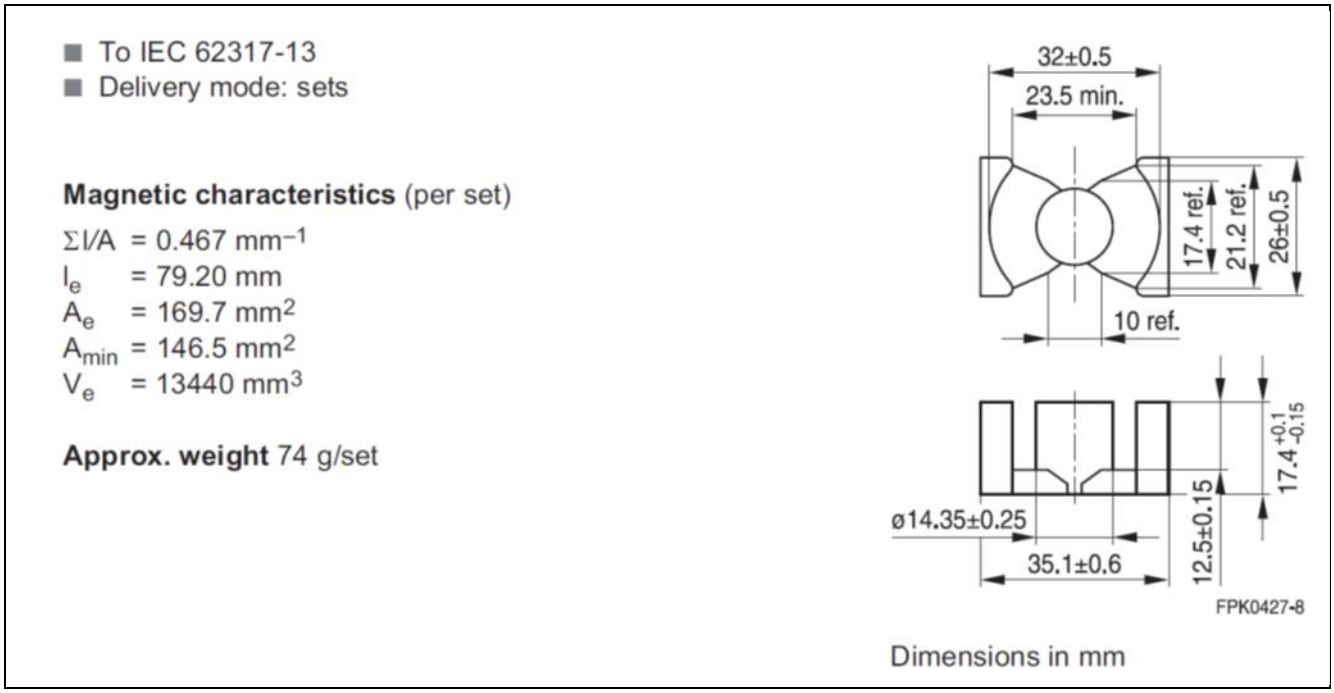

Figure 14 TDK-Epcos PQ35/35 core

The selected core material is the ferrite TDK PC95, showing a very interesting plot of core losses (PCV) vs. flux density vs. frequency (see Figure 14 below):

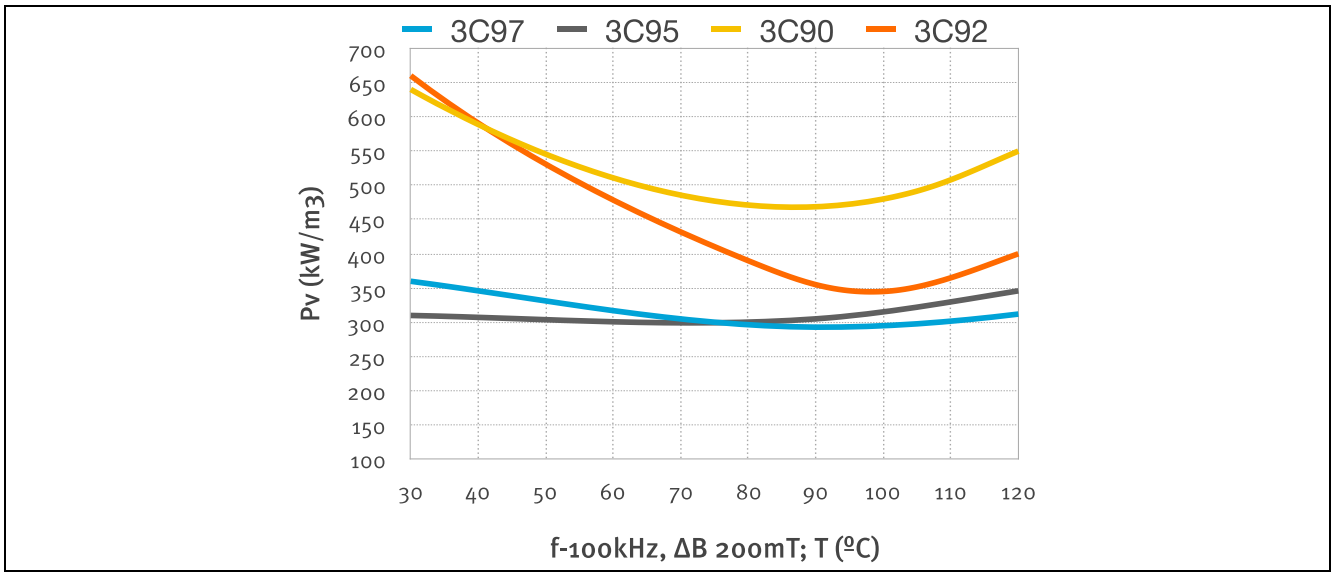

Figure 15 Ferrite core material TDK PC95/3C95

3C92 is an improved type when compared with 3C90, offering steadily improving core loss at high temperature up to 90-95°C. For efficiency over a wide temperature range, 3C95 and 3C97 offer the flattest temperature vs core loss curves, with PC95/3C95 being the best at temperatures below 85°C, typically found in server and telecom applications.

Interaction of *fr* frequency selection and transformer design

There are two necessary and sometimes conflicting goals for optimizing the LLC transformer design- keeping core loss at a low level, and reducing winding conduction loss, both DC and AC, to the lowest

possible value. Other factors such as the influence of fringing flux must be considered also, but are secondary or tertiary effects.

Two design examples will be shown, along with the influence design choices will have for the chosen operating frequency.

First, we will consider an initially conservative approach with regards to material selection, core loss, and operating frequency. By this, we will first target an operating frequency in the range of 100 kHz or slightly more, and the use of well established and relatively low cost core material, such as 3C90 or Magnetics Inc. type R, for the selected PQ35 core type. This is based on the early prototype developed for this project.

Core physical parameters Ferroxcube PQ3535 (vendors vary slightly in specified parameters):

$$Ae = 1.9 \times 10^{-4};\ l_m = 0.088;\ Ve = 1.63 \times 10^{-5};\ l_n = 1.52 \times 10^{-4};\ MLT = 0.075 \quad (10)$$

For this version, the chosen transformer turns ratio n=15, the tank resonant frequency fr = 115 kHz, and the primary magnetizing inductance target was 180 uH. The voltage in regulation on the primary side is established from the output voltage, rectifier drop, and turns ratio n:

$$V_P = n \times \left(V_O + V_f\right) = 15 \times \left(12 + 0.2\right) = 183V \quad (11)$$

The actual minimum operating frequency is determined by relationship to fr:

$$fmin = F_{\min} \times fr = 69kHz \quad (12)$$

Using a targeted ΔB we can calculate the minimum turns required:

$$N_{P\_min} = \frac{n \times \left(V_O + V_f\right)}{2 \times fmin \times Ae \times \Delta B} = 23.265 \quad (13)$$

Given the desired turns ratio of 15, and the necessity for whole turns on the secondary, this results in a primary winding of 30T and a secondary of 2T.

Using this configuration the working ΔB can be established, and the approximate core loss estimated for the fr working point using the Steinmetz coefficients for this core material at 100 – 200 kHz:

$$\Delta B = \frac{1}{N_p \times Ae} \times \left(V_O \times n \times \frac{0.5}{fr}\right) = 0.138T \quad (14)$$

$$P_{core} = a \times \left(\frac{fr}{10^3}\right)^c \times \left(\frac{DB \times 10}{2}\right)^d \times Ve \times \frac{10^{-3}}{10^{-6}} = 0.513W \quad (15)$$

The next step is to do a first cut estimation for winding losses, based on splitting the available winding window (An) between one primary winding and two secondary windings, using a realistic k fill factor for copper winding allocation, and estimating the conductor resistance based on conductor length and area derived from the available winding area and MLT (mean length turn) for this core/bobbin type.

$$l_{wire.pri} = MLT \times N_P = 2.25 \quad (16)$$

$$l_{wire.sec} = MLT \times N_S = 0.15 \quad (17)$$

Winding area:

$$A_{n\_p} = A_n \times \frac{k}{2} = 7.6 \times 10^{-6} \quad (18)$$

$$A_{n\_s} = A_n \times \frac{k}{2 \times N_{sec}} = 3.8 \times 10^{-6} \quad (19)$$

Conductor cross section area:

$$A_{wire.pri} = \frac{A_{n\_p}}{N_P} = 2.533 \times 10^{-7} \quad (20)$$

$$A_{wire.sec} = \frac{A_{n\_s}}{N_S} = 1.9 \times 10^{-6} \quad (21)$$

Estimated DC winding resistance (not considering yet the number of conductor strands or form factor needed to target the equivalent AC winding resistance):

$$R_{dc\_pri} = \frac{r \times l_{wire.pri}}{A_{wire.pri}} = 0.153\Omega \quad (22)$$

$$R_{dc\_sec} = \frac{r \times l_{wire.sec}}{A_{wire.pri}} = 1.361 \times 10^{-3}\Omega$$

From the basic analysis of the converter, and knowing the sum of the primary magnetizing current and the primary side load current, the winding conduction losses can be calculated, and the total transformer loss estimated:

$$Pri_{Loss} = I_{Pri}^{\ 2} \times R_{dc\_pri} = 2.701W \quad (24)$$

$$Sec_{Loss} = I_{Sec}^{2} \times R_{dc\_sec} = 3.4W \quad (25)$$

$$Total_{Loss\_Est} = Pcore + Pri_{Loss} + Sec_{Loss} = 6.617W \quad (26)$$

From this we can see that there is a real problem with the winding loss and the total power dissipation in the transformer considering the Rth of this core. With sufficient forced-air cooling the design can work, but it will fall short of the efficiency target.

There is not a smooth granularity of design options – given the turns ratio ***n*** and the need for complete windings on the secondary, the only option (besides a larger core and larger window area to increase the copper cross section area) is to reduce the number of turns (from 2 to 1) on the secondary, and adjust the operating frequency to a range which this core geometry can support with reasonable losses. It is likely that this will require a better core material. We will now review that for the final design, retaining the PQ35 core form factor.

The proposed alternative design raises the switching frequency to 155 kHz. It also adjusts the turns ratio ***n*** = 16, so that the converter operating point is better optimized at the nominal DC input of 380 V. This results in primary turns of 16, which increases the ΔB core losses at the minimum operating frequency.

Repeating some of the calculations, the primary voltage in regulation is now:

$$V_P = n \times \left(V_O + V_f\right) = 15 \times \left(12 + 0.2\right) = 195V \quad (27)$$

The minimum operating frequency in the boost up region is:

$$fmin = F_{\min} \times fr = 90kHz \quad (28)$$

And the minimum turns at maximum desired ΔB is:

$$N_{P\_min} = \frac{n \times \left(V_O + V_f\right)}{2 \times fmin \times Ae \times \Delta B} = 15.4 \quad (29)$$

At ***fr***, the calculated core loss for the 3C90 material is almost 2.5 W with this low turns primary. For this reason, a higher performance material such as PC95 or 3C95 is needed. Then the calculated core loss at ***fr*** is reduced to about 1.3 W. This is still substantially higher than the original design, so lets look at the estimated winding loss next.

The available winding area is the same, but the number of turns is about half in each case, which both cuts the winding length in half and allows roughly doubling the working conductor cross section. As a result, the winding resistance drops substantially:

$$R_{dc\_pri} = \frac{r \times l_{wire.pri}}{A_{wire.pri}} = 0.044\text{W} \quad (30)$$

$$R_{dc\_sec} = \frac{r \times l_{wire.sec}}{A_{wire.pri}} = 0.34 \times 10^{-3}\text{W} \quad (31)$$

As does the calculated conduction loss:

$$Pri_{Loss} = I_{Pri}^{2\prime} R_{dc\_pri} = 0.768W \quad (32)$$

$$Sec_{Loss} = I_{Sec}^{2\prime} R_{dc\_sec} = 0.851W \quad (33)$$

$$Total_{Loss\_Est} = Pcore + Pri_{Loss} + Sec_{Loss} = 2.925W \quad (34)$$

Though these loss estimates do not include possible issues with AC winding resistance and fringing flux, known design techniques can keep these effects down to reasonable levels. From this, it appears that it is possible to meet the target loss goals for the transformer design.

So the primary is realized in a “sandwich” technique using 16 turns of 4 layers of Litz wire with 45 strands of 0.1mm diameter. This minimizes the AC losses due to skin and proximity effects. The secondary uses a copper band of 20x0.5 mm.

The final structure of the main transformer is shown in Figure 16 below. This has been developed in cooperation with the partner company ICE Transformers s.r.l., Loreto Aprutino (PE) – Italy.

With the calculated turns ratio, there are only two likely possibilities for the turns structure. For any given core, if two turns are used on the secondary instead of one, this will roughly quadruple the DC losses on the secondary. A factor of two results because of double the MLT (mean length of turns) and another factor of two results because the wire cross-section must be halved in order to fit in the available window area.

A number of popular core types are capable of supporting the possible frequency range and volt seconds required, such as the PQ3230, ETD39, ETD33, PQ35 and PQ40. The winding window ends up being the deciding factor for achieving low I^2R losses. In all cases there is an optimum gap range whether using a 32:2 winding or 16:1 winding. The choice is based on the minimum between core losses dominating for small air gap dimensions (lower frequency) and higher proximity losses for large gap lengths.

With the 16:1 winding structure, the PQ35 and PQ40 show the lowest losses by 20-25% overall, due to the window area and lowest core loss, with an optimum operating frequency range between 150 and 250 kHz. With a 32:2 winding structure, the PQ40 core will return the best performance by about 10%, at an optimum frequency in the range of 50-75 kHz, but will be approximately 10% higher in losses than the PQ35 or PQ40 in the 150-200 kHz range with a optimized 16:1 winding structure.

With this choice, at full load condition the total copper losses will be (primary + secondary, DC+AC components) 1.1 W, the core losses are 1.8 W, so overall:

$$P_{trafo} = P_{copper} + P_{core} = 2.9W < P_{trafo\_Max} \quad (35)$$

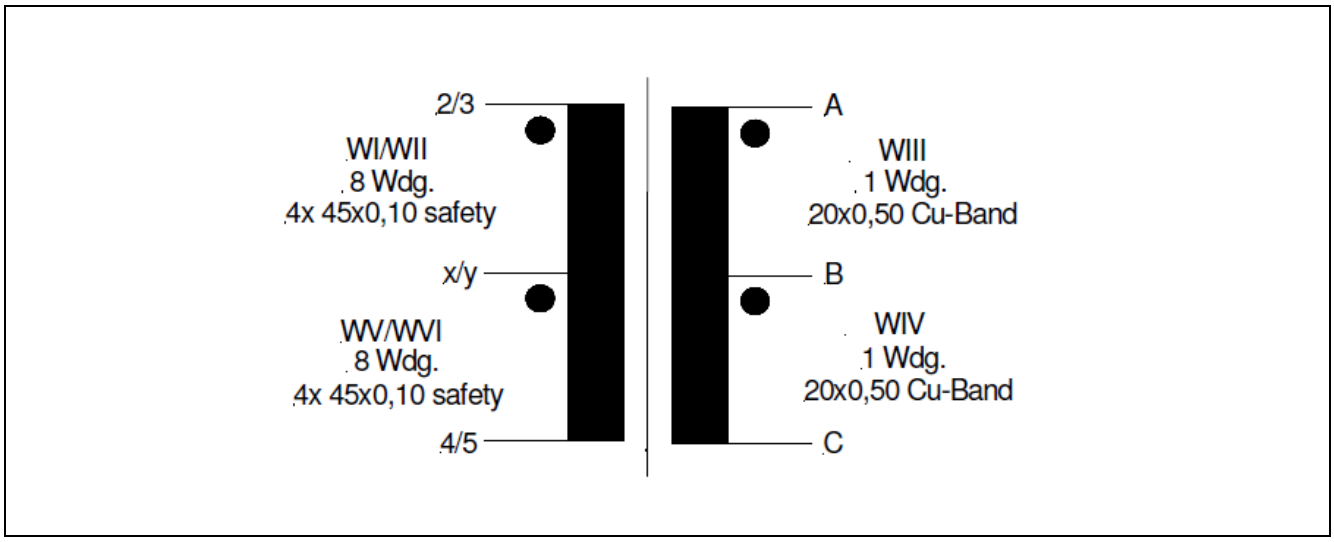

Figure 16 Winding structure of the PQ 35/35 LLC transformer (ICE Transformers s.r.l.)

An important transformer parameter in an LLC design is the primary or magnetizing inductance L_m. This value is obtained with a distributed air-gap on the side legs of the PQ core: this construction is preferred since it minimizes the effect of the (so called) “fringing flux” whch generates additional losses in the windings close to the inner limb.

3.1.5 2nd goal: design the transformer L_m for the selected switch technology

Given a target for minimum switching frequency for the PQ35 design in the range of 150-160 kHz, the desired magnetizing inductance Lm must be determined next. This also has a significant interaction with the transformer design relating to the operating gap and core losses, at the target operating frequency fo. Once again, all three possible Infineon MOSFET technologies will be examined, in the interest of producing a result with broad applicability.

The available current from magnetizing inductance is defined by:

$$I_{Lmp} = \frac{V_{IN}}{L_m} \cdot \frac{T_S}{4} \quad (36)$$

The nominal switching period from 160 kHz: fo = 160 kHz; $T_S = 1/fo$ = 6.37 µs

The target fmax will be defined as 250 kHz: $fmax$ = 250 kHz; $T_{S2} = 1/fmax$ = 4µs

For the fo switching period T_s, it is suggested to use a dead time interval in the range of 1/18 to 1/20 of the overall period; longer deadtime intervals will start to compromise the fo efficiency by raising the RMS loss for a given transferred power. Using these criteria, it is suggested to set the dead time t_d to 350 ns.

For a given switching period T_S and desired dead time t_d, the needed L_m is:

$$L_m = \frac{T_S \cdot t_d}{16 C_{o(tr)}} \quad (37)$$

Given that MOSFET capacitance and magnetic components have some variability in production, a guard band should be employed to assure ZVS switching for components in a production environment. Experience or rule-of-thumb suggests a total guard band of 30% be applied. Calculating for all three Infineon MOSFET technologies,

$$Lm_{fmax}CFD = \frac{T_{S2} \times t_d}{16 \times Cotr_{CFD} \times 1.3} = 200.32\,mH \quad (38)$$

$$Lm_{fmax}P6 = \frac{T_{S2} \times t_d}{16 \times Cotr_{P6} \times 1.3} = 255\,mH \quad (39)$$

$$Lm_{fmax}C7 = \frac{T_{S2} \times t_d}{16 \times Cotr_{C7} \times 1.3} = 192\,mH \quad (40)$$

Based on these calculations, a suggested value for L_m lies in the range of 190 to 200 mH.

The next step for L_m determination is to check back against the starting transformer design and determine if the target L_m matches with a core gapping and operating frequency choice that will meet the design efficiency goals based on calculated losses. Comparing how this specific solution looks in comparison to nearby design points is a useful way to evaluate for insight.

Table 3 Estimated $L_{m\ \&\ loss}$ for 16:1 transformer design "spread" using PQ35 core

	Gap	L_m	*fo* target	Calc. PRI/SEC RMS loss *	Calc core loss
Design 1	~0.2 mm	~250 µH	125 kHz	0.5 W/0.3 W	3.0 W
Design 2	~0.3 mm	~200 µH	160 kHz	0.5W/0.3 W	2.2 W
Design 3	~0.4 mm	~130 µH	230 kHz	0.5W/0.3 W	1.8 W

*Assumes primary winding with 90 strands 0.1 mm wire; secondary of 20 mm x 0.4 mm copper tape

Not discussed are skin and proximity effect and fringing losses, which are generally only feasible to estimate with FEM tools. With the proposed winding structure, secondary effects should have a low impact the winding losses; the key factor is choice of gap, primary inductance, and the resulting core losses. With more advanced semiconductors with lower switching loss and lower Q_{oss}, such as GaN, a case could be made for raising the operating frequency for this core and construction to 250 kHz nominal *fo*. Certainly an F_{max} of 250 kHz should be no problem.

3.1.6 3rd goal: evaluate the chosen L_m against the SIMPLIS peak gain curve nomagraph and system gain requirements - select the working L_n value $[(L_r+L_m)/L_r]$ needed for system gain without capacitive mode.

The earlier calculation when system parameters were entered, established the system regulation gain needed to cover the range from low line at 350 V to maximum input at 410 V. Now the input L_r value will be selected to meet the meet both the system regulation requirements and the system gain, while avoiding operating near the capacitive mode region.

Typically the L_n value of the L_r to L_m ratio would be evaluated by estimation using FHA, as described earlier; but the region of preferred operating Q for power supplies is unfortunately the region in which FHA is least accurate, including in the critical boost up mode, where it usually underestimates the gain. Exact calculation is quite difficult to do, so instead an interactive nomagraph of sorts can be prepared with pre-calculated peak gain curves plotted as a function of L_n and full load Q_{max}. SIMPLIS is used to simulate the LLC converter transfer function open loop, using the Periodic Operating Point mode and variable stepping to relatively quickly simulate and measure the range of conditions (Figure 17). The wide range of measurement functions in SIMPLIS facilitates quick acquisition of a variety of design verification data for the LLC converter, including power dissipated, AC coupled RMS voltage, gain and phase, etc.

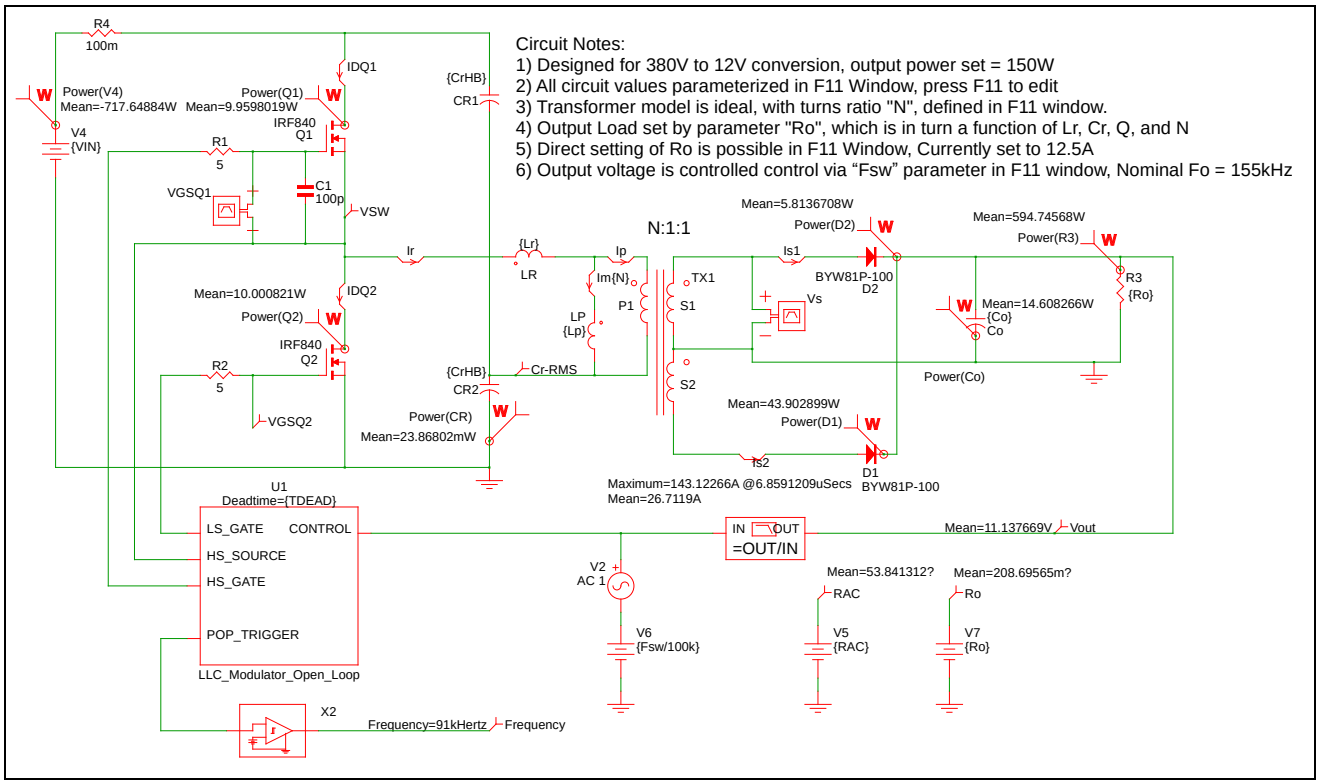

Figure 17 LLC open loop simulation circuit using SIMPLIS

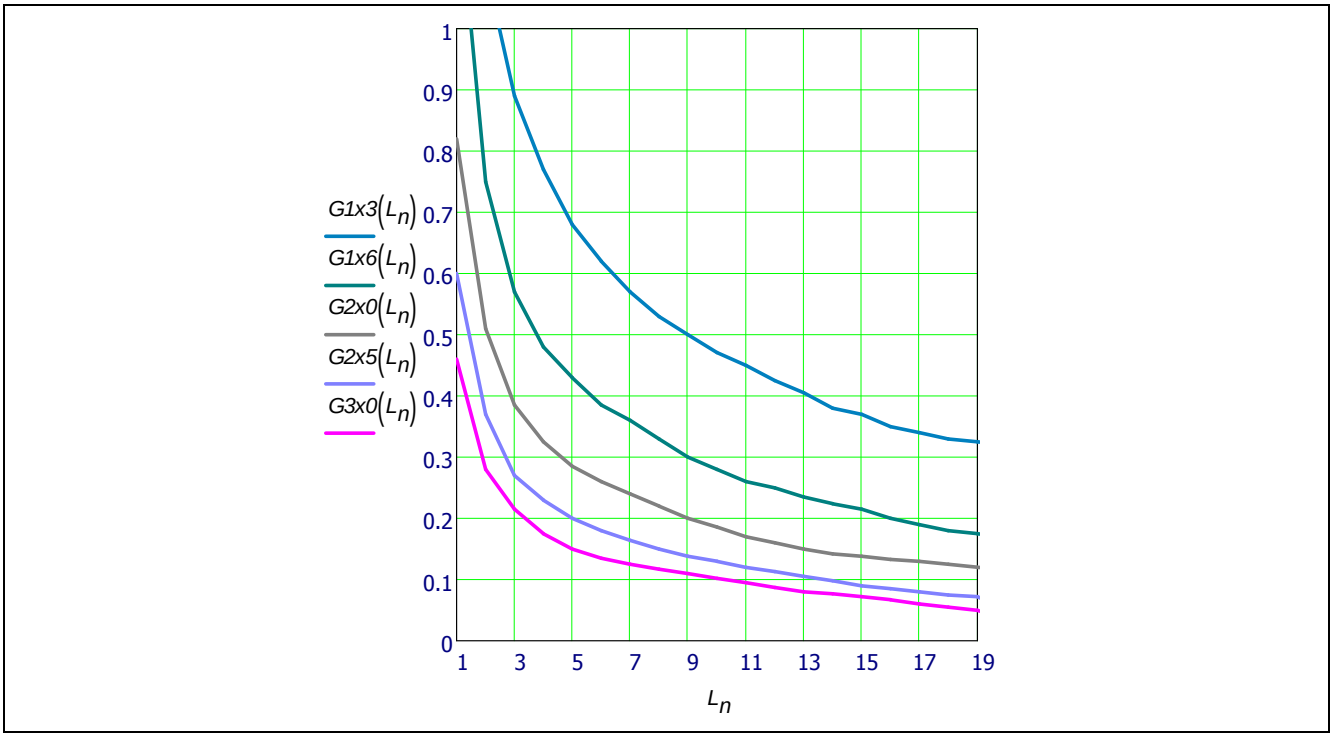

Figure 18 Peak gain curves Q vs L_n from SIMPLIS, showing constant gain gain curves as a function of L_n and Q at 1.3x, 1.6x, 2.0x, 2.5x, and 3.0x

The peak gain nomagraph (Figure 18) illustrates the requirements for L_n ratio and Q to achieve peak system gains. Note how for lower gain curves high Q is possible for the tank loading conditions (better efficiency), and as expected, achieving high tank gains with high L_n ratios requires very low tank Q, and high circulating current and the attendent losses.

To get some truly useful information from this nomagraph, it is necessary to plot the L_m curve for the application with the Q calculated as a function of L_m and the L_n ratio. In this case, the necessary application data for the Lm curve calculation is now available:

$$Q_{TARGET} = 0.25 \rightarrow 0.3$$

$$Lm = 195 \times 10^{-6}$$

$$fo = 155 \times 10^{3}$$

$$R_L = 0.24$$

$$n = 16$$

Where R_l is the effective output load resistance for 12 V at 50 A; and Q_{TARGET} is the preferred initial target range for full load tank Q, based on efficiency goals and a typical desired L_n range between 9 and 14.

The L_m curve as a function of L_n and Q can be calculated from

$$Q\left(L_n, Lm, f_O, R_L, n\right) = \frac{2p' \; Lm' \; f_O}{L_n' \; R_L' \; n^2} \qquad (16)$$

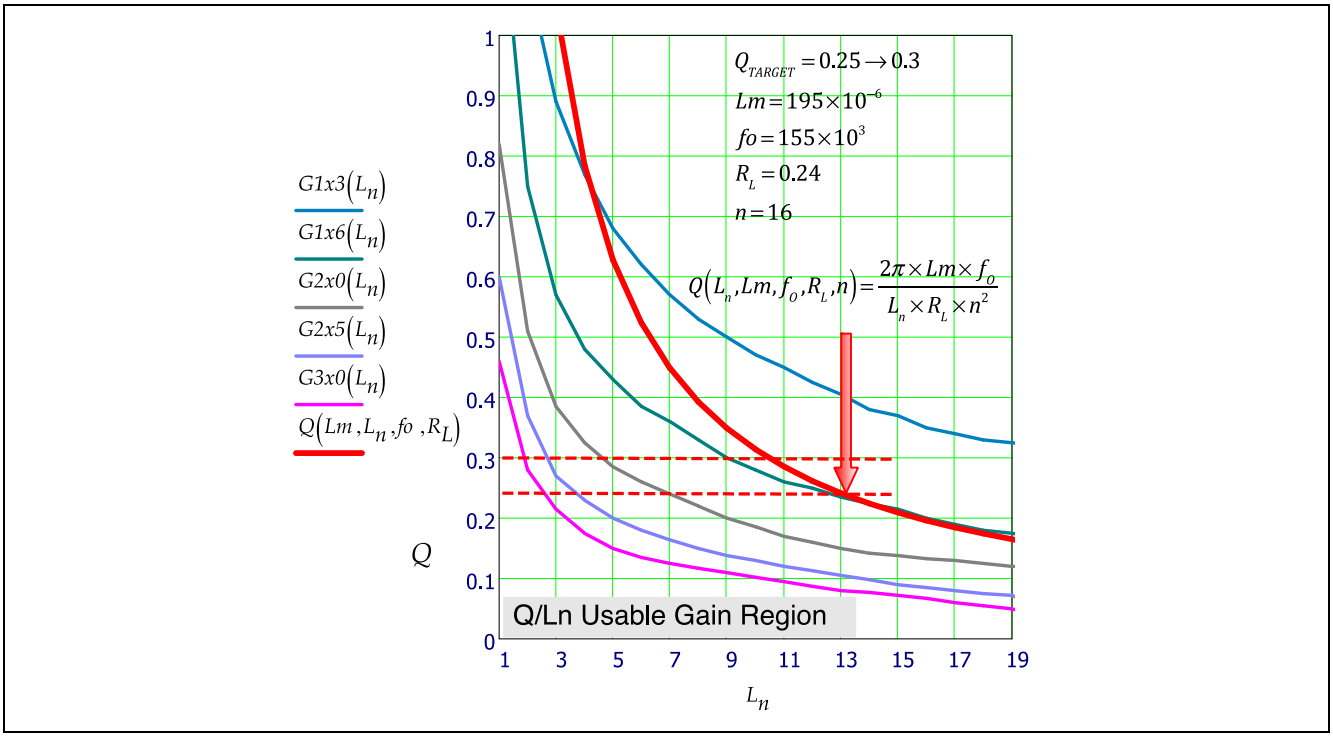

Figure 19 Peak gain curves Q vs L_n from SIMPLIS, with calculated curve vs L_n for L_m being evaluated, and desired FL Q_{max} range (2.5 to 3.0)

How should this plot be used?

Some key points to keep in mind are:

- Lower L_n gives a smaller frequency range for span of regulation, but accompanied with higher tank current and conduction losses
- A higher L_n gives a smaller series inductor, but this in turn requires a larger C_r for the same fo; this can be a problem for capacitor technology and RMS voltage withstanding at high frequencies for $L_n > 14$. Also, a larger C_r value contributes to the likelihood of capacitive mode operation at start up and during burst mode and increases the duration in capacitive mode.
- The optimal trade-off of efficiency and control span is typically with L_n in the range of 9-14
- While operating with Q_{max} just reaching the required peak gain at $fmin$ gives the best efficiency in theory, in practice this makes it quite difficult to consistently avoid capacitive mode operation under dynamic regulation events. Component tolerances also stack up, and mandate having design margin to achieve the required gain and avoid capacitive mode at the same time. This leads to another rule-of-thumb, that is is usually effective to buffer system gain at Q_{max}/FL by at least 20%.
- In summary, target higher peak gain, as a rule-of-thumb use 35-45% higher f_{min} set point for minimum frequency operation compared with f_{min} at nominal FL Q_{max}, and completely avoid capacitive mode operation.
- In this nomagraph calculation, we can see that L_m = 195 µH is on the peak gain for 1.6x, which gives a reasonable buffer margin for the system gain requirement of approx. 1.1. If overload margin was not a concern, L_n could be reduced to a lower value, with a higher value of L_r and smaller C_r, but this could lead to margin issues for operation up to the overload OCP protection point. Additionally, a larger L_r has a significant cost and density impact.

3.1.7 4th goal: resonant tank design & verification: calculate L_r based on L_n ratio and L_m; calculate total C_r value, and verify boost up gain target and F_{min} set values, C_r AC RMS stress

Using L_n = 13, we can use FHA to plot and visualize the actual f_{min} at several load points (Q plotted at 25% load steps) and determine a usable f_{min} set point for the minimum frequency operation for the LLC controller (Figure 20). Q curves are plotted beyond full load, to 115% (suggested OCP) and 150%.

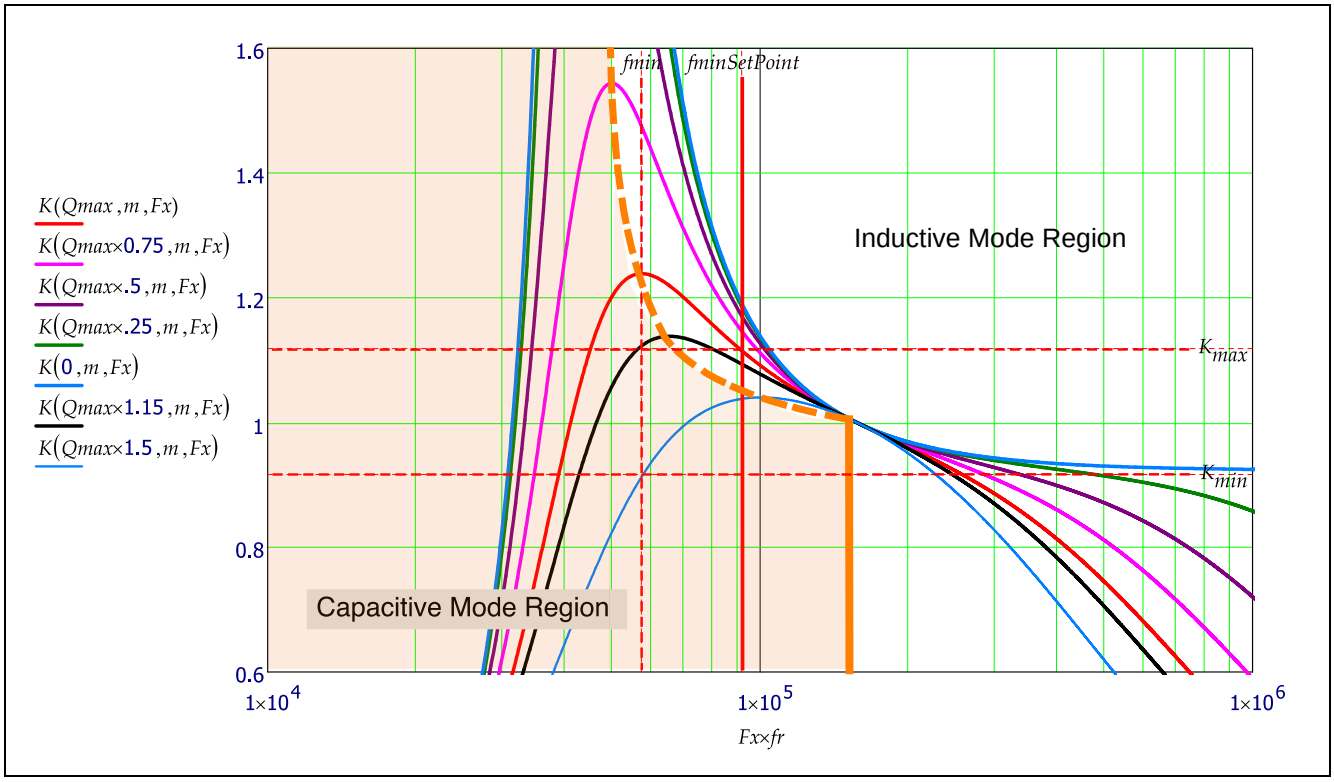

Figure 20 System gain visualisation using K_{max} and K_{min} gain values, and determining functional f_{min} set point versus calculated f_{min} at each load condition

The FHA plot makes the f_{min} set point strategy much clearer; in this case, a 90 kHz limit will be used for the lowest operating frequency programmed for the controller. Ideally, we would like to see the gain curves all intersect the K_{max} boundary before hitting the $f_{minSetPoint}$. In actuality, using SIMPLIS to spot check gains, they do; the FHA gain calculation underestimates the actual value.

Using L_n = 13, then $Lr = \frac{Lm}{Ln} = \frac{195mH}{13} = 15uH$ (18)

In the case of the C7 based LLC converter, the chosen value is 15.5 µH, but as part of this is realized by the leakage inductance of the power transformer, the working design value for the resonant inductor is 14 µH.

The resonant choke design

In LLC designs with stringent power density requirements, the resonant choke is often embedded in the transformer, in the sense that the leakage inductance is created and utilized for this purpose. This technique has the advantage of saving space and the cost of an additional magnetic component, but also some

drwabacks, such as difficult controllability of the L_r value in mass production, and negative impacts on the power transfer.

In this case, an external L_r is used. As the evaluation board was developed for test / benchmarking and high power density is not in the main focus, having the resonant inductance available externally allows experimentation with the resonant tank.

The external resonant choke of 14 µH is realized using a RM-12 core and a winding construction as illustrated in Figure 21 below and implemented by the partner company ICE Transformer s.r.l., Loreto Aprutino (PE) - Italy.

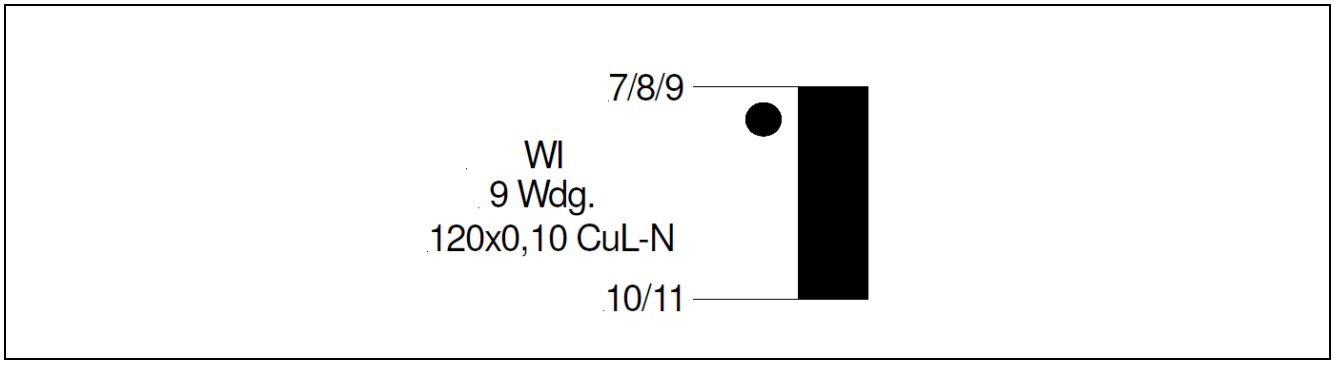

Figure 21 Winding structure of the RM 12 resonant choke (ICE Transformer s.r.l.)

Final component of the resonant tank: resonant capacitor C_r

Now that we have the working value for L_r, calculation of the nominal value for C_r is straight forward.

$$Cr = \frac{1}{4 \cdot p^2 \cdot Lr \cdot f_0^2} = 66.7nF \qquad (19)$$

For the LLC converter, the value of 66 nF will be used, but for two reasons it will be split in to a pair of 33 nF capacitors, using the half bridge configuration shown in Figure 22. This configuration, rather than the single capacitor (the usual way the LLC converter is drawn), has some practical advantages as regards the dynamic properties at start up and in burst mode. The connection point for the transformer will initially start out in a more balanced ‘between the rails’ position, which minimizes the chance and duration of operation in capacitive mode at start up and when exiting the pause in burst mode.

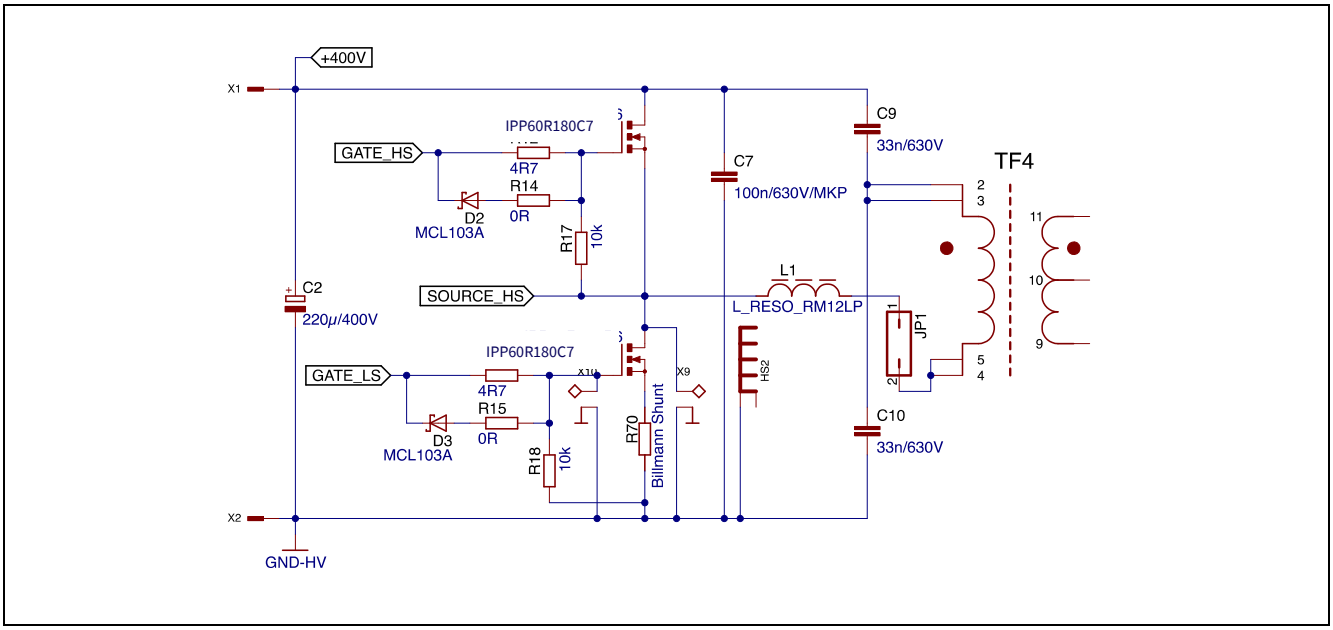

Figure 22 HB C_r capacitor configuration to reduce capactive mode operation and distribute AC voltage stress between two capacitors

Note the configuration for the LLC half bridge should be based on a low inductance working loop for the primary side power transistors and the connection for the local bypass capacitor C7. C7 also assures a low impedance connection at high frequencies for both Cr capacitors C9 and C10 with reference to the primary side ground and the positive bulk voltage.

Another reason for using the split capacitor arrangement is the limited frequency and RMS voltage handling capability for film capacitors. The larger the value of the capacitor for a given technology, the lower the frequency cut off point. Higher voltage capacitors extend the AC frequency capability, but with much larger physical packaging.

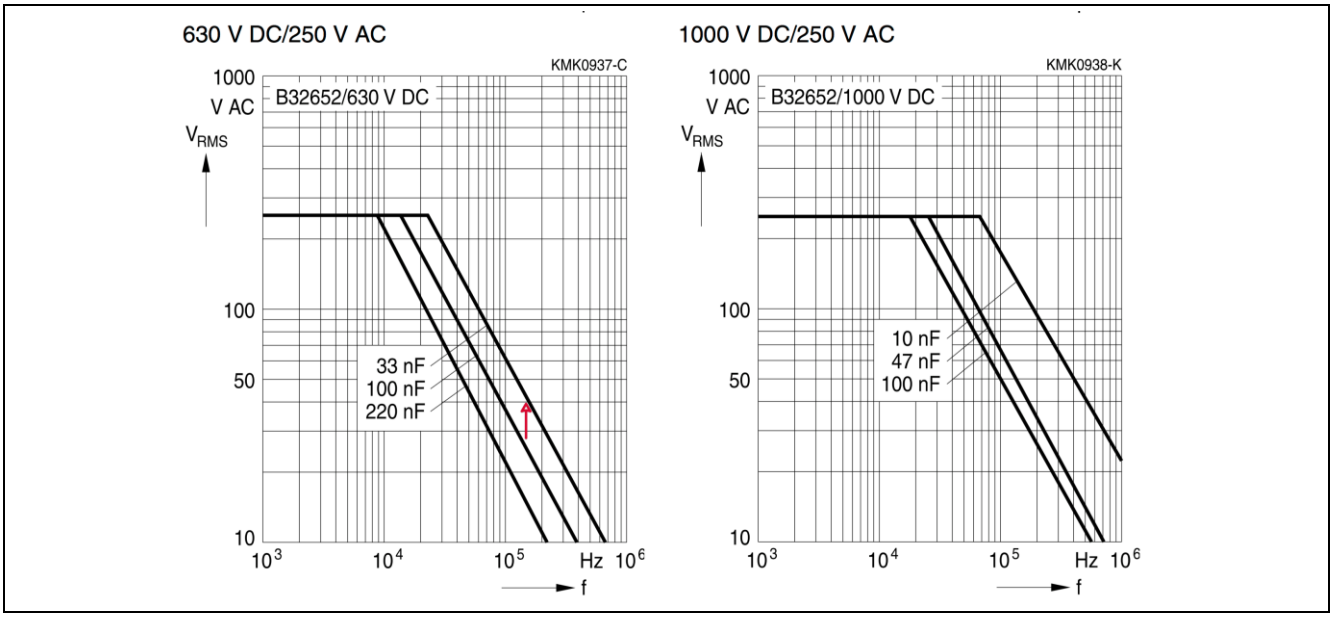

Figure 23 B32652 film capacitor recommended AC operating voltage and frequency limits

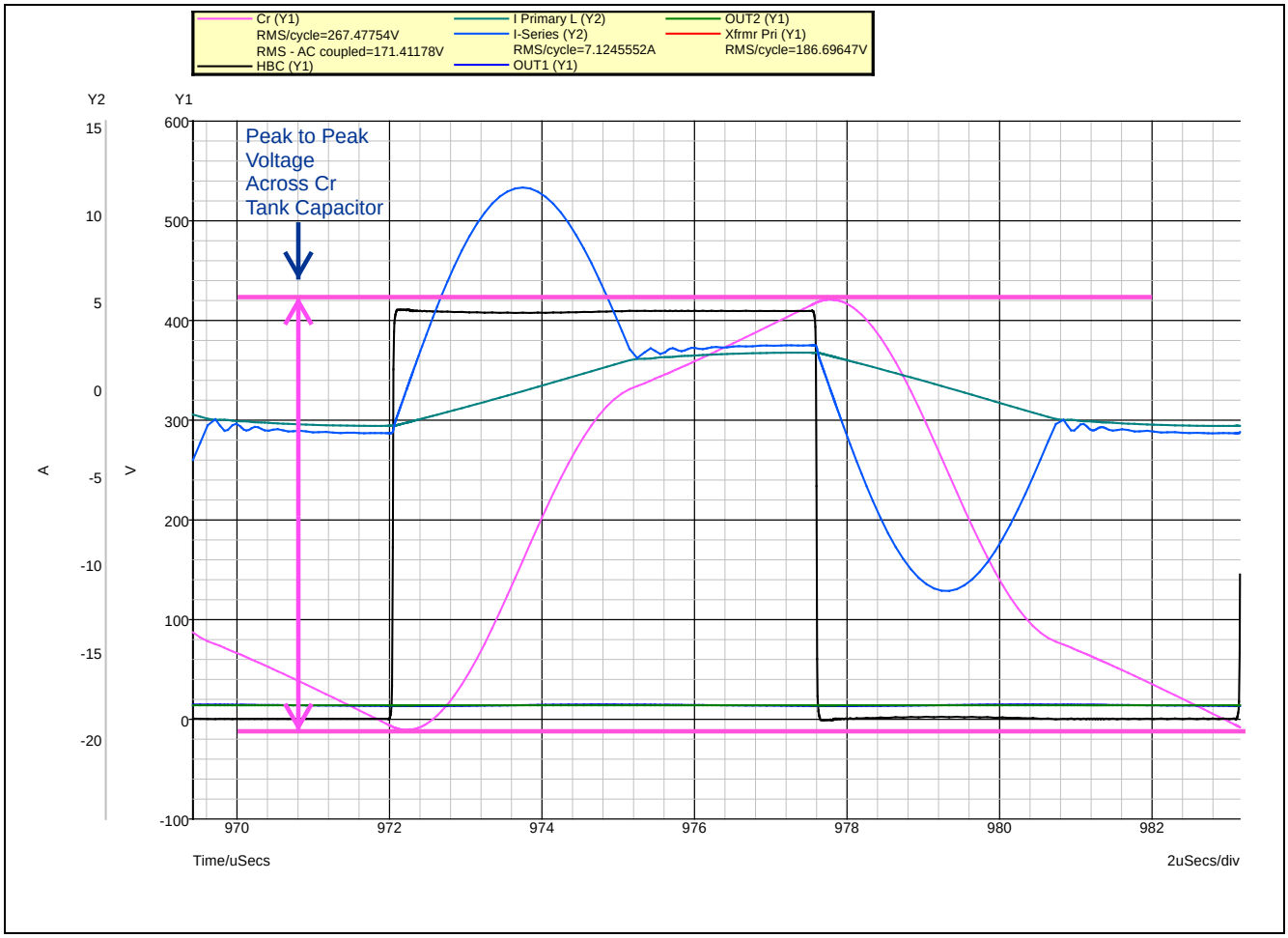

Figure 24 Peak boost up gain at 90 kHz and 171 VRMS AC voltage stress on C_r

Worst case RMS voltage on C_r occurs under conditions that are normally only transitory; this includes overload and boost up operation for low Vin during hold up. SIMPLIS can be easily used to investigate these conditions In Figure 24, we can see that at the OCP threshold range of load at minimum operating frequency with maximum boost up, the simulation predicts a worst case AC coupled RMS voltage of ~170 V RMS across C_r. Under normal full load conditions at 155 kHz, the “measured” AC coupled RMS voltage is ~48 V RMS, which is closely in line with the capabilities of the B32652 630 V_{DC}/250 V_{AC} film capacitor (Figure 22). A slightly more robust solution for higher frequencies would be the 1 kV_{DC}/250 V_{AC} version of this series.

3.2 Synchronous rectification stage design considerations

For server PSUs targeting 80 PLUS Titanium, the hardest efficiency target to achieve is usually the one at half load (efficiency at 50% P_{max}), which is often close to peak efficiency. In the case of this reference board, the power consumption of the bias circuitry was not considered, since we intentionally restrict this document to the LLC design, independent from the design of the auxiliary bias. Consequently, the losses generated by the synchronous rectification driving stage are also not critical in our concept. The main design goal is to keep the conduction losses low in order to fulfil the efficiency target at 50% P_{max}. We selected the BSC010N04LS, which is the best-in-class SuperSO8 MOSFET from Infineon's latest OptiMOS™ 40 V family. A quick evaluation showed that the best option consisted in paralleling three such MOSFETs per synchronous rectification branch, allowing the required efficiency target to be exceeded with some margin.

If the power consumption of the bias stage is included. an optimization of the sync rec losses results in a good balancing of the two dominant loss mechanisms - the conduction and gate driving losses.

Under these conditions, reaching the efficiency target at 50% P_{max} is made even more difficult, due to the requirement to achieve simultaneously a high efficiency at 10% $P_{max,}$ while also making sure that the MOSFETs don't overheat at P_{max} because of excessive losses. Indeed, if dealt with individually, these 3 efficiency targets would require opposing implementations:

- The efficiency at 10% P_{max} requires a MOSFET with relatively small chip size to keep the dominating driving losses low;
- On the contrary, the efficiency targets at 50% P_{max} and P_{max} are better tackled by selecting a MOSFET with a large chip size, so that the conduction losses can be significantly reduced.

To allow these two approaches to work together, we can keep the BSC010N04LS FET as its low $R_{DS(on)}$ does not significantly increase gate charges.

We must now consider how many BSC010N04LS we should parallel per SR branch?

We shall use the following formulae to compute the total conduction and gate driving losses –P_{cond} and P_{gate} respectively as generated by the sync rec MOSFETs:

- $P_{cond} = 2 \times I_{RMS}^2 \times \frac{R_{DS(on)}}{N}$, where $I_{RMS} = I_{OUT} \times \frac{\pi}{4}$ for a resonant topology, N = number of paralleled FETs per SR branch, and the factor 2 highlights that we have 2 SR branches in our center-tap configuration;
- $P_{gate} = 2 \times N \times Q_{g(sync)} \times U_g \times f_{sw}$, with P_{gate} being logically dependent from the gate charge $Q_{g(sync)}$, the gate driving voltage U_g and the switching frequency f_{sw}. The factors 2 and N were already defined for P_{cond}.

In Synchronous Rectification(SR), since no plateau exists on the gate waveform, using $Q_{g(sync)}$ instead of the more familiar total gate charge Q_g provides a more accurate representation of the gate driving losses.

For this demo board, U_g = 12 V, whereas f_{sw} = 150 kHz if the input voltage is 380 V. Moreover, with a driving voltage of 12 V, $Q_{g(sync)}$ = 102 nC for BSC010N04LS. In addition to that, as a first approximation, we have neglected the variation of f_{sw} and $R_{DS(on)}$ with the load.

Since P_{cond} and P_{gate} constitute by far the dominant loss mechanisms for this demo board, as a first approximation, we can consider their sum as roughly equal to the total SR losses. For that matter, the following 3 tables summarize these total SR losses at 10% P_{max}, 50% P_{max} and P_{max}, when using 1 to 3 x BSC010N04LS in parallel.

[1] @ 10% P_{max}	[2] Conduction losses P_{cond}	[3] Gate driving losses P_{gate}	[4] Total SR losses (P_{cond} + P_{gate})
[5] 1 x BSC010N04LS per SR branch	[6] 31 mW	[7] 367 mW	[8] 398 mW
[9] 2 x BSC010N04LS per SR branch	[10] 15 mW	[11] 734 mW	[12] 749 mW
[13] 3 x BSC010N04LS per SR branch	[14] 10 mW	[15] 1102 mW	[16] 1112 mW

[17] @ 50% P_{max}	[18] Conduction losses P_{cond}	[19] Gate driving losses P_{gate}	[20] P_{cond} + P_{gate}
[21] 1 x BSC010N04LS per SR branch	[22] 771 mW	[23] 367 mW	[24] 1138 mW
[25] 2 x BSC010N04LS per SR branch	[26] 386 mW	[27] 734 mW	[28] 1120 mW
[29] 3 x BSC010N04LS per SR branch	[30] 257 mW	[31] 1102 mW	[32] 1359 mW

[33] @ P_{max}	[34] Conduction losses P_{cond}	[35] Gate driving losses P_{gate}	[36] P_{cond} + P_{gate}
[37] 1 x BSC010N04LS per SR branch	[38] 3084 mW	[39] 367 mW	[40] 3451 mW
[41] 2 x BSC010N04LS per SR branch	[42] 1542 mW	[43] 734 mW	[44] 2276 mW
[45] 3 x BSC010N04LS per SR branch	[46] 1028 mW	[47] 1102 mW	[48] 2130 mW

On one hand, at 10% P_{max} and still partly at 50% P_{max}, using 3 x BSC010N04LS per SR branch can penalize the efficiency due to excessive gate driving losses. On the other hand, at P_{max}, the design suffers from very high SR conduction losses if using a single BSC010N04LS per SR branch, with as well the risk of making the MOSFET overheat.

Consequently, if considering the bias losses, using 2 x BSC010N04LS per SR branch would provide the best balancing of the efficiency at low, mid and full load.

4 Board description

4.1 General overview

The overall converter electrical configuration is shown in Figure 24. The main control for the LLC converter is located on the primary side, using either the analog ICE2HS01G or digital XMC4200 control board. The LLC controller board generates both the primary side LLC control signals for the IPP60R180C7 primary side switches, and the secondary side synchronous rectifier control signals for the OptiMOS™ BSC010N04LS synchronous rectifiers, using a high-speed coupler with safety isolation to transmit the SR control. A PID controller for voltage regulation and a fault controller monitoring current through a low ohmic shunt are also located on the secondary side, and communicate to the primary side LLC controller board through conventional opto-couplers. Control circuitry on both sides of the isolation barrier is powered by a bias module using a CoolSET™ ICE2QR2280Z, which integrates a quasi-resonant flyback controller with a flyback power transistor and depletion mode startup cell.

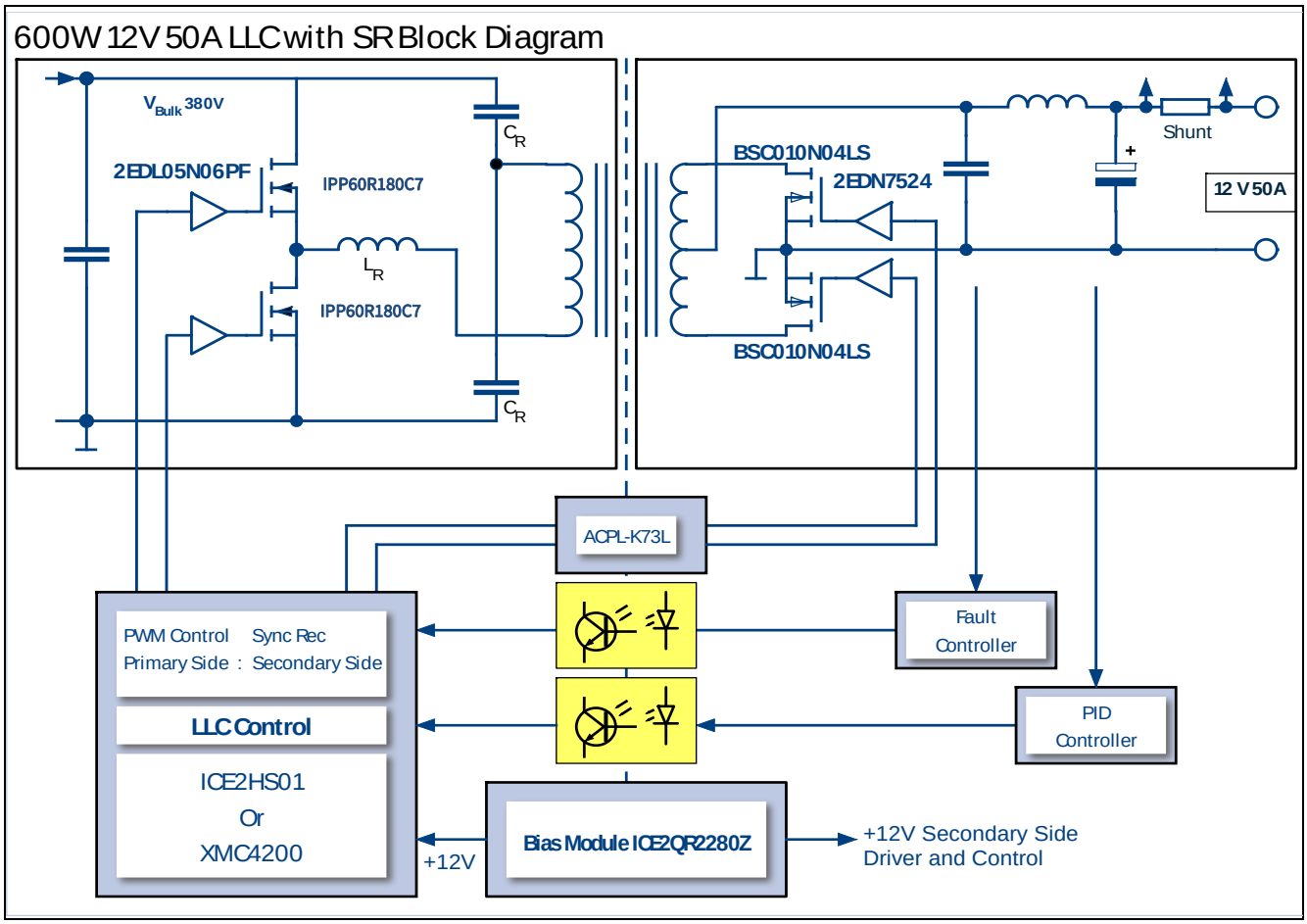

Figure 25 600 W 12 V output LLC converter detail block digram

Figure 3 is the top view, bottom view and the assembly of 600 W HB LLC evaluation board. Key components are: **(1)** heatsink assembly of primary side switches IPP60R190P6 **(2)** Resonant capacitor **(3)** LLC analog controller ICE2HS01G **(4)** Resonant inductor **(5)** Main DC-DC transformer **(6)** PCB assembly of the auxiliary circuit with bias QR Flyback controller ICE2QR2280Z **(7)** Heatsink assembly for cooling the synchronous rectifier **(8)** Output capacitor **(9)** Output inductor **(10)** Half-Bridge MOSFET gate driver 2EDL05N06PFG, **(11)** Synchronous Rectifier OptiMOS™ BSC010N04LS and **(12)** Dual Channel Gate Drive 2EDN7524F used for Synchronous Rectifier MOSFETs.

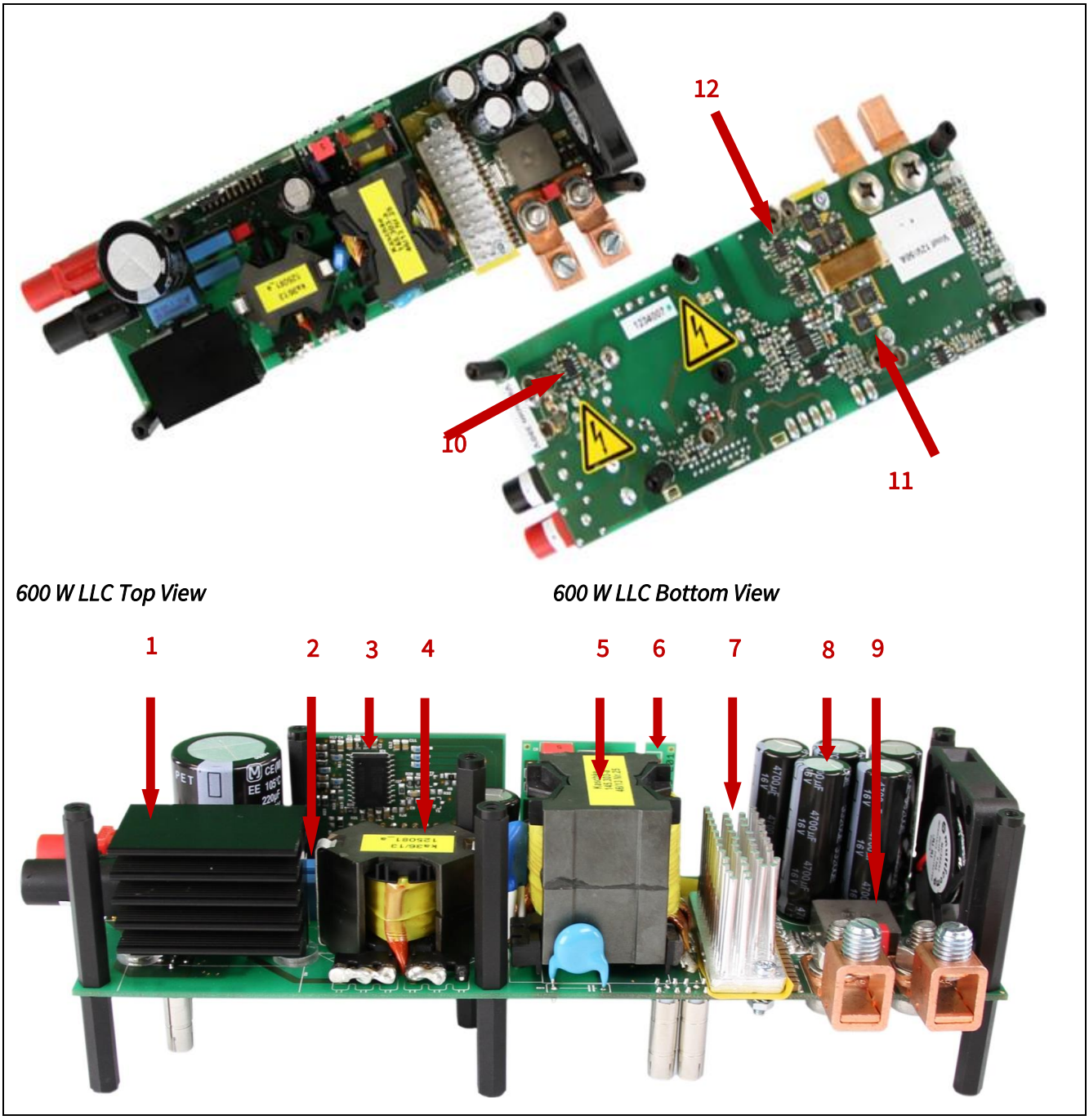

Figure 26 IFX 600 W LLC evaluation board

4.2 Infineon BOM

This HB LLC 600 W evaluation board is a full Infineon solution meeting the highest efficiency standard 80 PLUS® Titanium using the following parts:

4.2.1 Primary HV MOSFETs CoolMOS™ IPP60R180C7

The 600 V CoolMOS™ C7 is the next step of silicon improvement based on the 650 V CoolMOS™ C7. It stays with the strategy to increase switching performance in order to enable the highest efficiency in any kind of target applications, such as for boost topologies including PFC's (power factor correction) and high voltage DC-DC stages such as LLC's (DC-DC stage with resonant tank in order to maintain zero voltage switching). Although the 600 V CoolMOS™ offers very fast switching it also retains the ease of use (ease of controlling the switch) of the 650 V C7 "mothertechnology". Therefore the 600 V CoolMOS™ C7 is an optimized device for highest efficiency SMPS.

The 600 V C7 represents the new standard of SJ MOSFET.

In an LLC application, the converter is in resonant operation with guaranteed ZVS even in a very light load condition. Switching loss caused by E_{oss} during turn-on can be considered negligible in this topology. With this consideration, the CoolMOS™ C7 family of parts offers a superior price/performance ratio with a low FoM (R_{on}*Q_g and R_{on}*Q_{OSS}), which means that MOSFET switching transitions can switch during a shorter deadtime period. This will result in lower turn-off losses further improving the efficiency.The following are additional features and benefits of the CoolMOS™ C7 which make it suitable for resonant switching topologies such as LLC:

- Suitable for hard and soft switching (PFC and high performance LLC)
- Increased MOSFET dv/dt ruggedness to 120 V/ns
- Increased efficiency due to best in class FoM $_{RDS(on)}$*E_{oss} and $_{RDS(on)}$ *Q_g
- Best in class $R_{DS(on)}$/package
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

4.2.2 XMC4200 microcontroller

The XMC4200 combines Infineon's leading-edge peripheral set with an industry-standard ARM® Cortex®-M4F Core.

The control of SMPS is a strong focus for XMC™ microcontrollers where users can benefit from features such as smart analog comparators, high-resolution PWM timers and the ARM® Cortex®–M4F DSP instruction set including floating point or high precision analog to digital converters.

As a key feature it offers a high-resolution PWM unit with a resolution of 150 pS. This unique peripheral makes it especially suitable for digital power conversion in applications such as solar inverters as well as SMPS and uninterruptible power supplies (UPS). The XMC4200 is supported by Infineon's integrated development platform DAVE™, which includes an IDE, debugger and other tools to enable a fast, free of charge and application-orientated software development.

Summary of XMC4200 Features:

- ARM® Cortex®-M4F, 80 MHz, incl. single cycle DSP MAC and floating point unit (FPU)
- 8-channel DMA + dedicated DMA for USB
- CPU frequency: 80 MHz
- High ambient temperature range: -40°C to 125°C

- Wide memory size options: up to 256 kB of Flash and 40 kB of RAM
- HRPWM (High Resolution PWM) allowing PWM adjustment in steps of 150 ps
- 12 bits ADC, 2 MSample/sec. Flexible sequencing of conversions including synchronous conversion of different channels
- Fast and smart analog comparators offer protections such as overcurrent protection, including filtering, blanking and clamping of the comparator output. A 10bit DAC with a conversion rate of 30 MSamples/sec provides an internal reference for the comparators that can be configured to be a negative ramp for slope compensation purposes
- A flexible timing scheme due to CCU timers and HRPWM (High Resolution PWM). These timers allow the creation of almost any PWM pattern and synchronize PWM signals with ADC measurements accurately.
- Interconnection matrix to route different internal signals from one peripheral to another. For example, the comparator output can connect to a PWM timer to indicate an overcurrent protection event and immediately switch off the PWM output
- Communication protocols supported including USB, UART, I^2C, SPI.
- USB 2.0 full-speed device
- Package: PG-LQFP-64

Target applications:

- SMPS
- UPS
- Motor control
- Solar inverters
- Position detection
- IO devices
- HMI
- Sense & control systems
- PLC
- Light networks

4.2.3 Half bridge gate drive 2EDL05N06PF

The 2EDL05N06PF is one of the drivers from Infineon's 2EDL EiceDRIVER™ compact 600 V half bridge gate driver IC family with a monolithic integrated low-ohmic / ultrafast bootstrap diode. Its level-shift SOI technology enables higher efficiency and smaller form factors within applications. Based on the use of SOI-technology there is an excellent immunity to the influence of fast transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch up can occur at any rated temperature or voltage conditions. The two independent driver outputs are controlled on the low-side using two different CMOS input, LSTTL compatible, signals compatible with 3.3 V logic. The device includes an under-voltage detection unit with a hysteresis characteristic that is optimised for either IGBT or MOSFET. The 2EDL05N06PF (DSO-8) and 2EDL05N06PJ (DSO-14) are driver ICs with undervoltage-lockout for MOSFETs. These two parts are recommended for server/telecom, low-voltage drives, e-bike, battery charger and half bridge based switch mode power supply topologies.

- Individual control circuits for both outputs
- Filtered detection of supply under-voltage conditions
- All inputs are diode clamped

- Off line gate clamping function for safety when not powered
- Asymmetric undervoltage lockout thresholds for high side and low side
- Insensitivity of the bridge output to negative transient voltages up to -50 V, given by SOI-technology
- Ultra fast low capacitance bootstrap diode

4.2.4 Advanced dual channel gate drive 2EDN7524F

The fast dual channel 5 A non-isolated gate driver is an advanced dual-channel driver optimized for driving both standard and superjunction MOSFETs, as well as GaN power devices, in all applications in which they are commonly used. The input signals are TTL compatible with a high-voltage capability up to 20 V and down to -5 V. The unique ability to handle -5 V_{DC} at the input pins protects the IC inputs against ground bounce transients.

Each of the two outputs is able to sink and source current up to 5 A utilizing a true rail-to-rail stage, that ensures very low impedances of 0.7 Ω up to the positive and 0.55 Ω down to the negative rail. Very low channel-to-channel delay matching (typically 1 nS) is implemented which enables the double source and sink capability of 10 A by paralleling both channels.

Different logic input/output configurations guarantee high flexibility for all applications; e.g. with two paralleled switches in a boost configuration. The gate driver is available in 3 package options: PG-DSO-8, PG-VDSON-8 and PG-TSDSO-8-X (size minimized DSO-8).

Main features

- Industry-standard pinout
- Two independent low-side gate drivers
- 5 A peak sink/source output driver at V_{DD} = 12 V
- True low-impedance rail-to-rail output (0.7 Ω and 0.5 Ω)
- Enhanced operating robustness due to high reverse current capability
- -10 V_{DC} negative input capability against GND-Bouncing
- Very low propagation delay (19 nS)
- Typ. 1 ns channel to channel delay matching
- Wide input and output voltage range up to 20 V
- Active low output driver even on low power or disabled driver
- High flexibility through different logic input configurations
- PG-DSO-8, PG-VDSON-8 and TSSOP-8 package
- Extended operation from -40°C to 150°C (junction temperature)
- Particularly well suited for driving standard MOSFETs, superjunction MOSFETs, IGBTs or GaN power transistors

4.2.5 Bias QR flyback controller ICE2QR2280Z

ICE2QRxxxx is a second generation quasi-resonant PWM CoolSET™ with power MOSFET and startup cell included in a single package optimized for off-line power supply applications such as LCD TV, notebook adapter and auxiliary/housekeeping converter in SMPS. The digital frequency reduction with decreasing load enables a quasi-resonant operation down to a very low load. As a result, the average system efficiency is significantly improved compared to conventional solutions. The active burst mode operation enables

ultra-low power consumption during standby mode operation and low output voltage ripple. The numerous protection functions give full protection of the power supply system in potential failure situations.

The key features of the ICE2QR2280Z for use as an auxiliary converter of this LLC evaluation board are:

- High voltage (650 V/800 V) avalanche rugged CoolMOS™ with startup cell
- Quasi-resonant operation
- Load dependent digital frequency reduction
- Active burst mode for light load operation
- Built-in high voltage startup cell
- Built-in digital soft-start
- Cycle-by-cycle peak current limitation with built-in leading edge blanking time
- Foldback point correction with digital sensing and control circuits
- V_{CC} undervoltage and overvoltage protection with autorestart mode
- Over load /open loop protection with autorestart mode
- Built-in over temperature protection with autorestart mode
- Adjustable output overvoltage protection with latch mode
- Short-winding protection with latch mode
- Maximum on time limitation
- Maximum switching period limitation

4.2.6 SR MOSFETs OptiMOS™ BSC010N04LS

For the synchronous rectification stage the selected device is BSC010N04LS, from the latest OptiMOS™ 40 V family. SR is naturally the best choice in high efficency LLC designs with low output voltage and high output current, as described in this application note. In applications that target high efficiency at both light and heavy loads – such as 80 PLUS® Titanium - while requiring high power densities, it is critical to select SR MOSFETs that combine following key characteristics:

- Very low $R_{DS(on)}$: BSC010N04LS provides the industry's first 1 mΩ 40 V product in SuperSO8 package.
- Low gate charge Q_g, which is important in order to minimize driving losses, with benefits on light load efficiency
- Very tight $V_{GS(th)}$ range: in parallel usage this allows the MOSFETs to turn-on almost simultaneously. Selected OptiMOS™ offer very close min and max of $V_{GS(th)}$, respectively 1.2 and 2 V.
- Monolithically integrated Schottky type diode, in order to minize the conduction losses and reduce Q_{rr}.
- Package; The BSC010N04LS in SuperSO8 with source fused leads is able to address all of the typical requirements for a SR MOSFET package:
    - Minimized parasitic inductances
    - Combined compact footprint and good power dissipation
    - Enlarged source connection in order to minimize electromigration occurrence and improve solder joint stability with thermal cycles.

4.3 Board schematics

For clarity and legibility, the main board schematic is presented in several logical functional blocks.

4.3.1 LLC switching power stage and output synchronous rectification

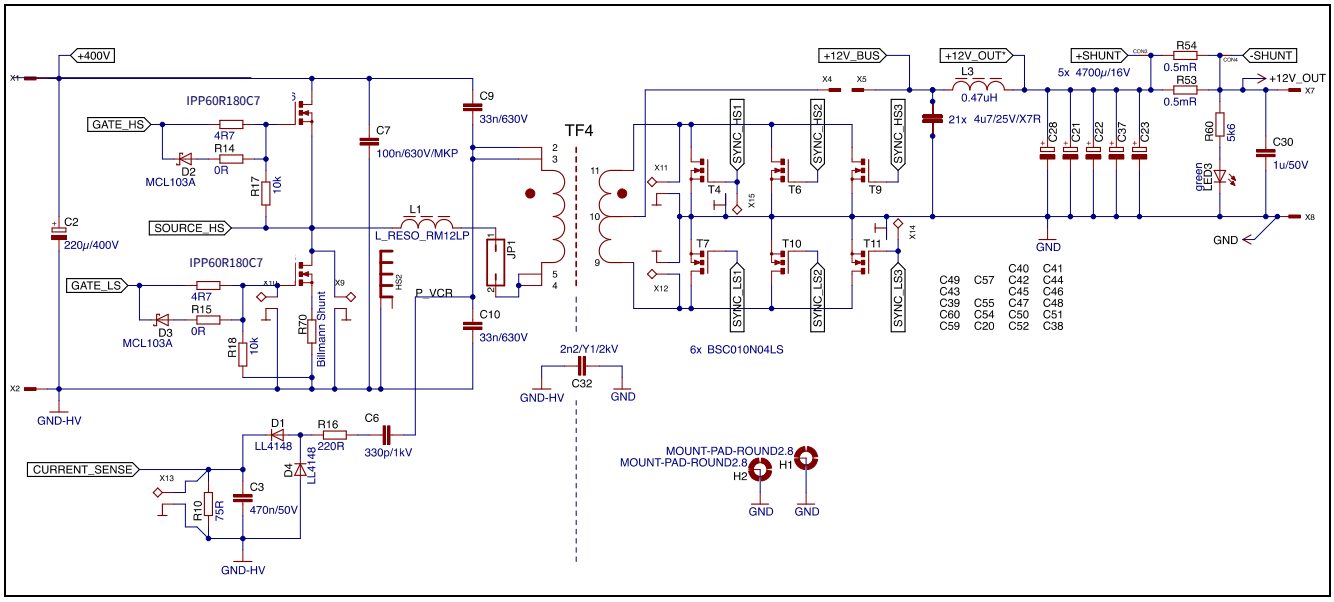

Figure 27 Primary and secondary power stages

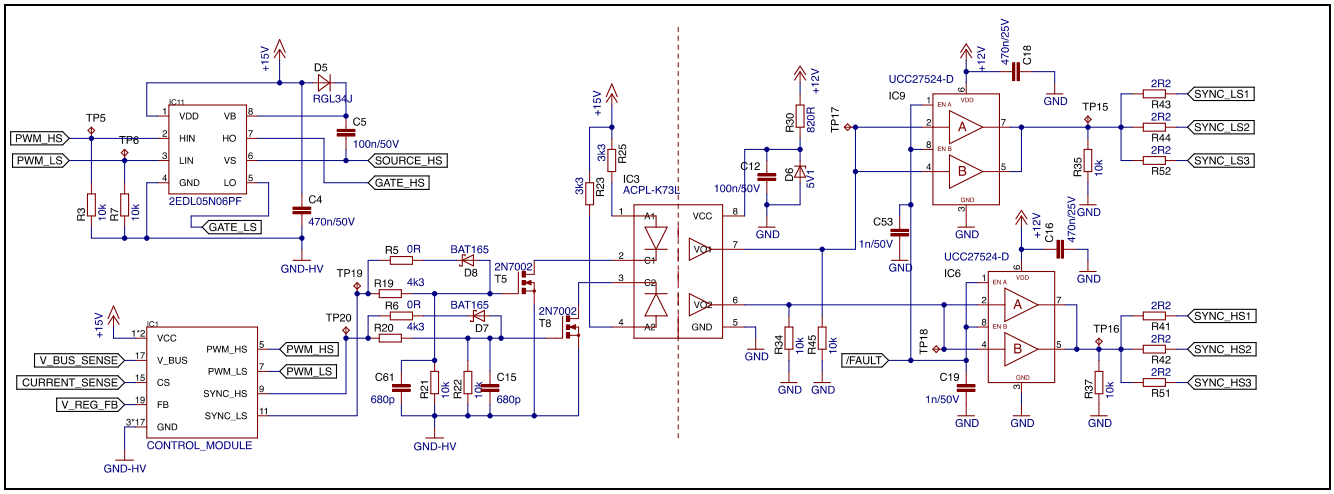

Figure 28 Primary and secondary side driver circuitry

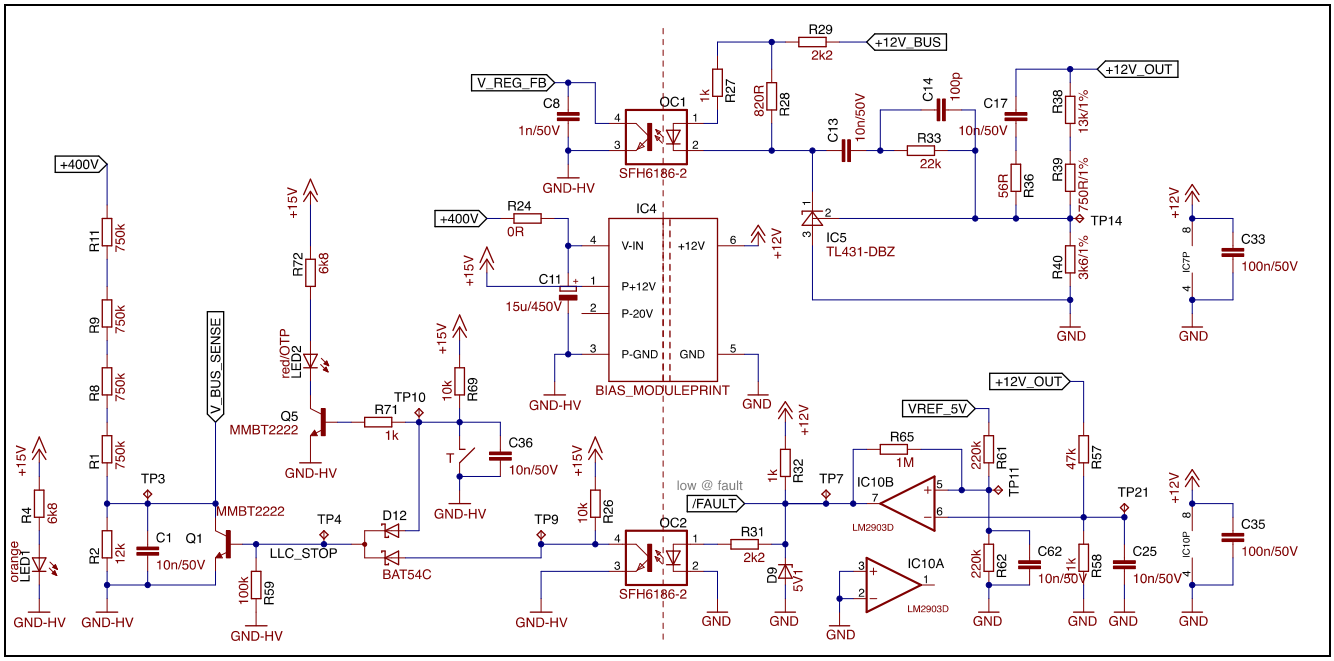

Figure 29 Bias supply and feedback control and fault control

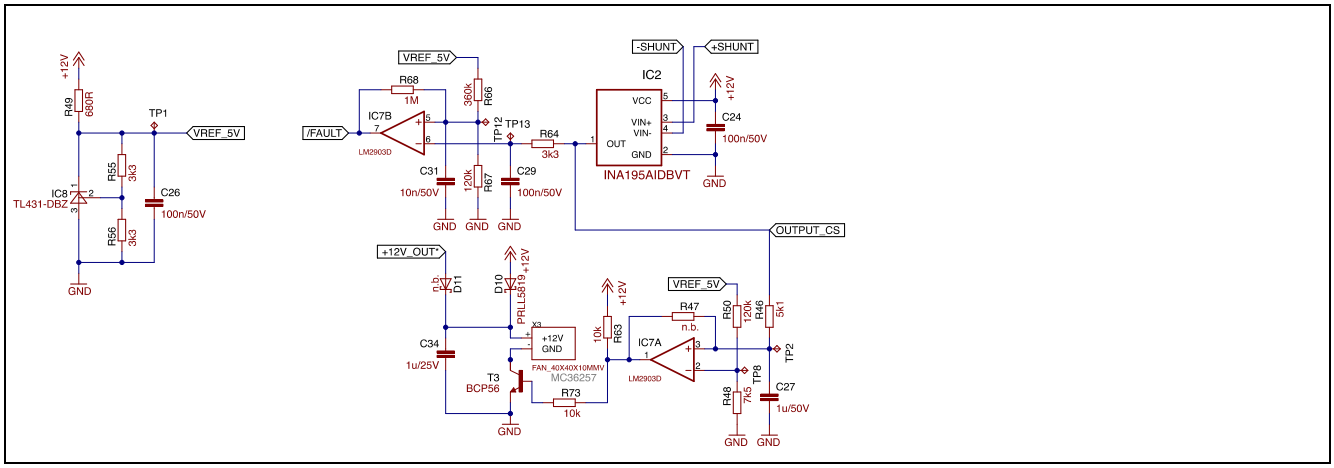

Figure 30 Voltage reference and current shunt

4.3.2 Primary side controller board schematics

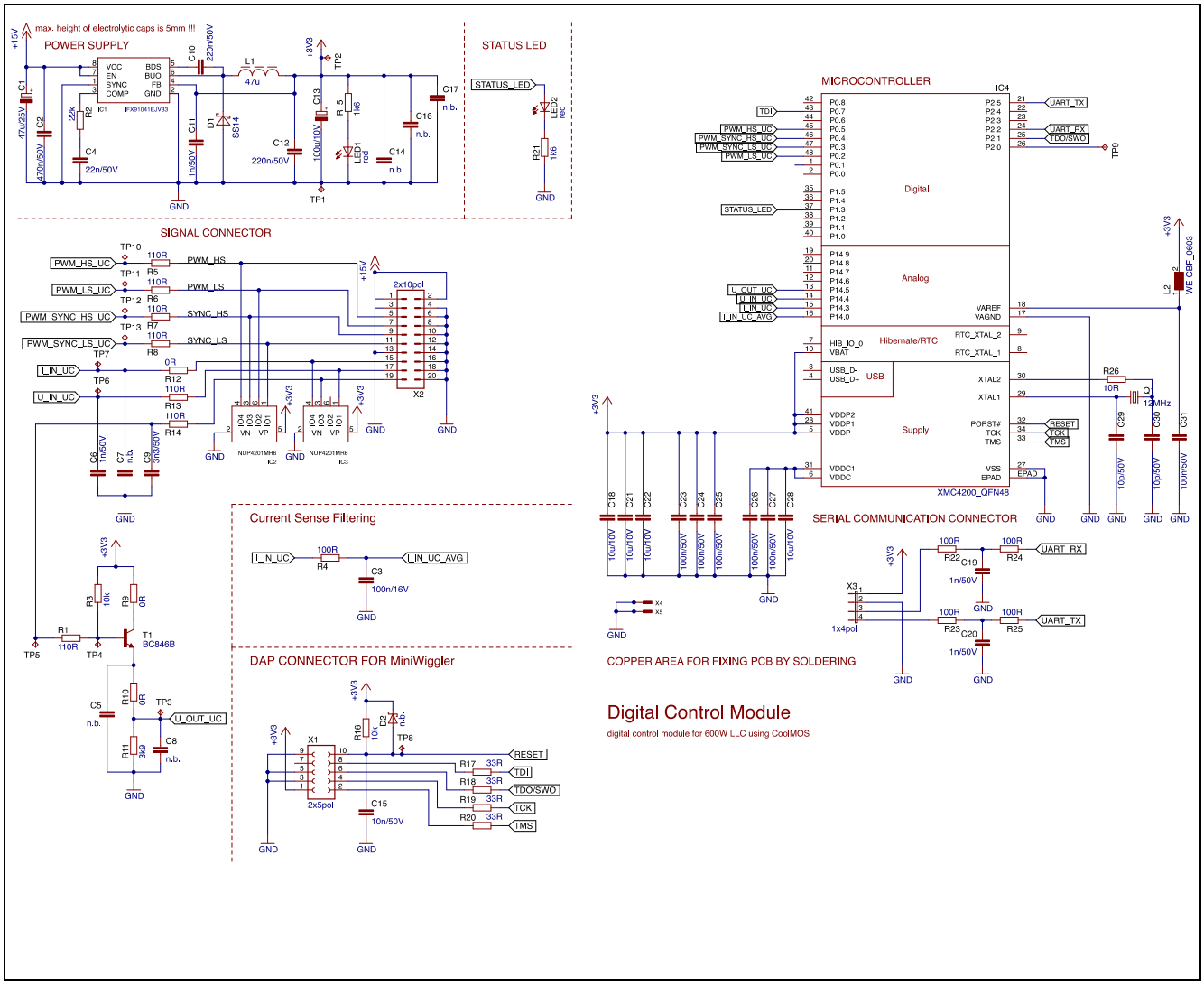

Figure 31 XMC4200 digital controller board schematic

4.3.3 Biasboard schematic

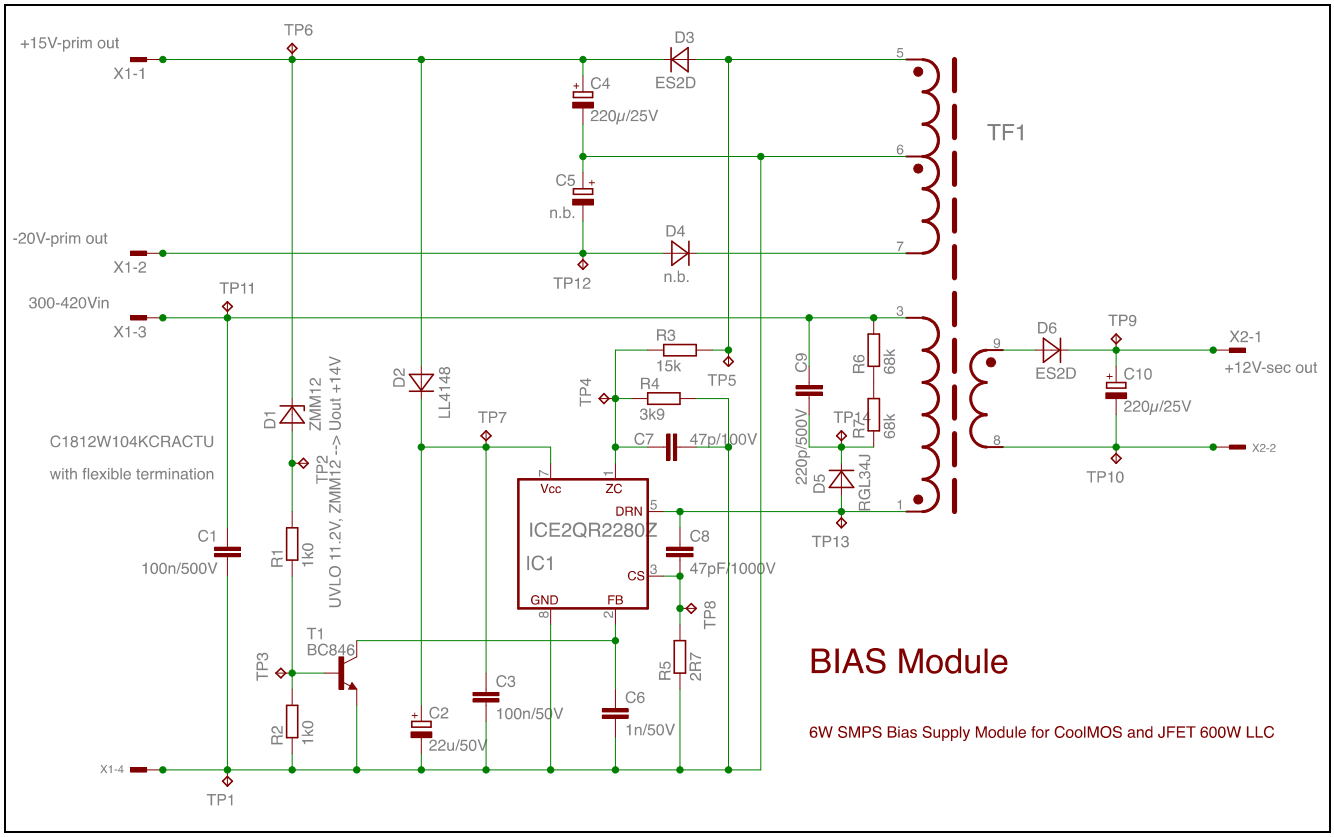

Figure 32 Biasboard schematic

4.3.4 PCB configuration

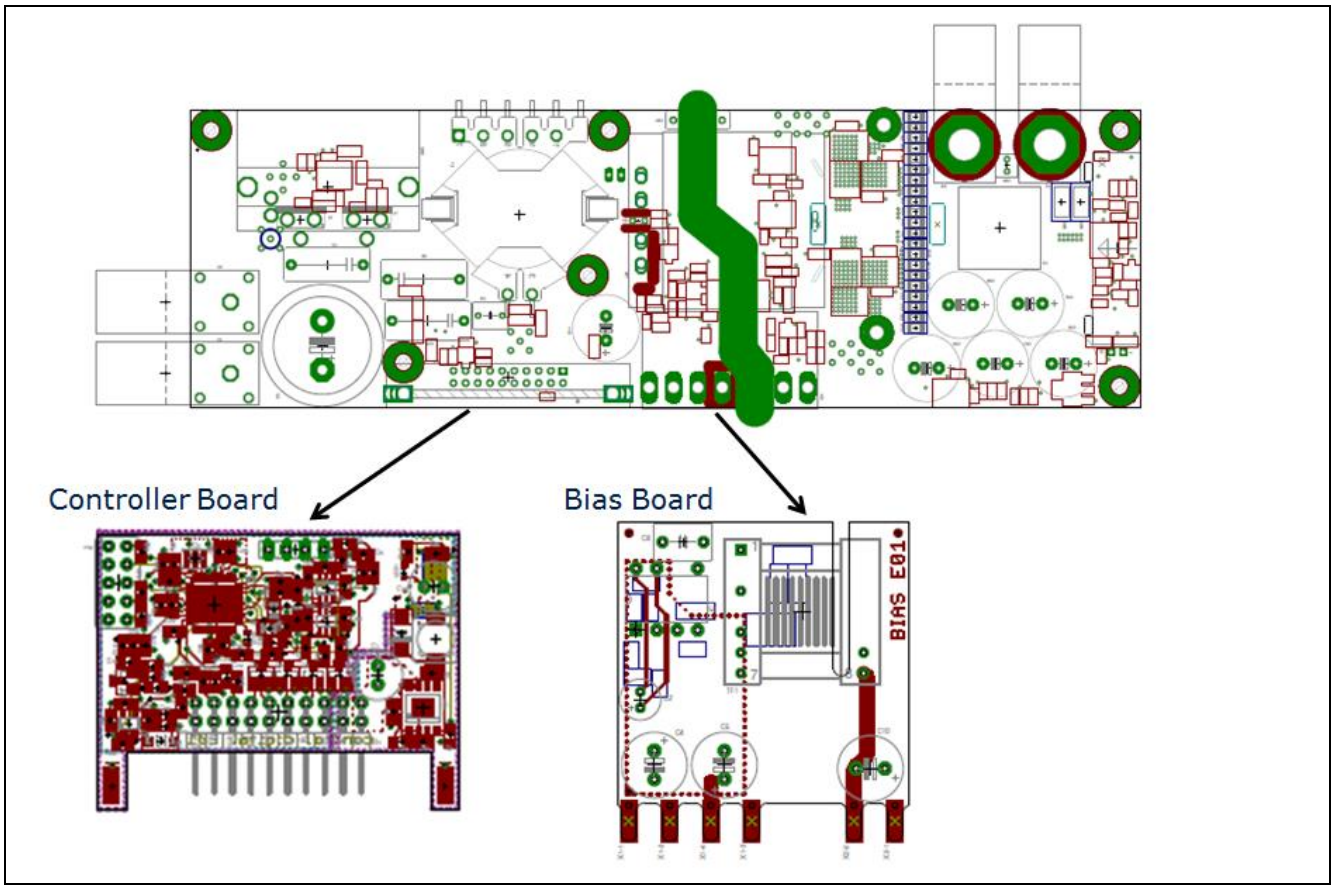

Figure 33 Mainboard PCB with controller – and biasboard

5 Operation of 600 V CoolMOS™ C7 technology in the 600 W LLC evaluation board with digital control by XMC™

5.1 Introduction

The operation of CoolMOS™ C7 in the 600 W LLC evaluation board controlled by the Infineon ICE2HS01G analog controller is already described in [8]; moreover, [7] and [8] give an overview about the design and performance of the converter featured with the above-mentioned analog controller.

This document is focused on the operation of the same 600 W LLC converter, but featuring a digital control by the Infineon XMC4200 microcontroller located on the converter's primary side on a dedicated daughter board pin-to-pin compatible with the analog one.

Because it uses a VCO input pin for regulation (as does the ICE2HS01G), full digital control loop can not be implemented within the XMC4200; the system design used relies upon a loop control built around the industry standard TL431.

The organization and functionality of the XMC4200 for LLC is easily understood for those familiar with the ICE2HS01G. Furthermore, the header block settings for key variables facilitate adjusting the nominal minimum bridge frequency, the maximum bridge frequency, and the dead time (in multiples of 12.5ns), replicating the resistor programming functionality of the ICE2HS01G.

In the following paragraphs, some fundamental operating modes of the LLC converter are analysed and the benefits of the digital control are highlighted with regard to some specific conditions.

5.2 The voltage controlled oscillator

All HB resonant controllers contain a Voltage Controlled Oscillator (VCO). Typically, this oscillator's frequency is designed to be proportional to a control voltage or control current on a control pin, and the signal at the control pin is usually derived from the output error signal by linear amplification and filtering. This means that frequency is proportional to the error signal.

As a base for the following dissertation, it is useful to show the VCO characteristic curve implemented in our digital control loop. This is shown in Figure 34 and simply represents the relationship between the feedback voltage (error amplifier output) and the converter switching frequency.

Moreover, Fig.35 shows the state machine implementation inside the LLC controlled by the XMC4200. This is a fast and intuitive way to show the operation of our digital control through finite state transitions.

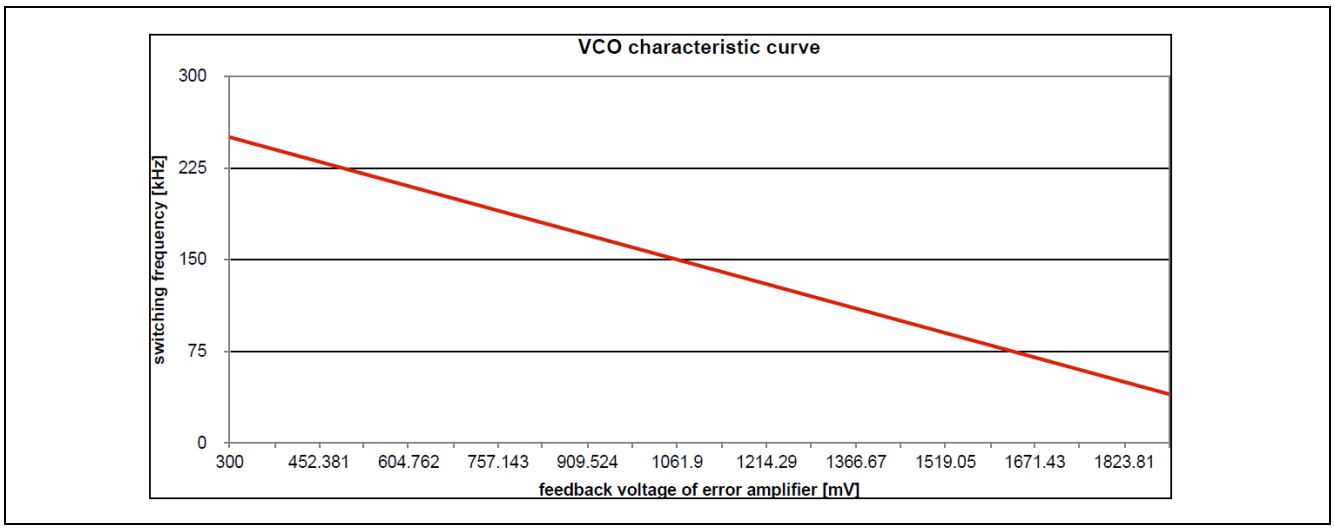

Figure 34 VCO characteristic curve: f_{SW} vs. V_{FREQ}

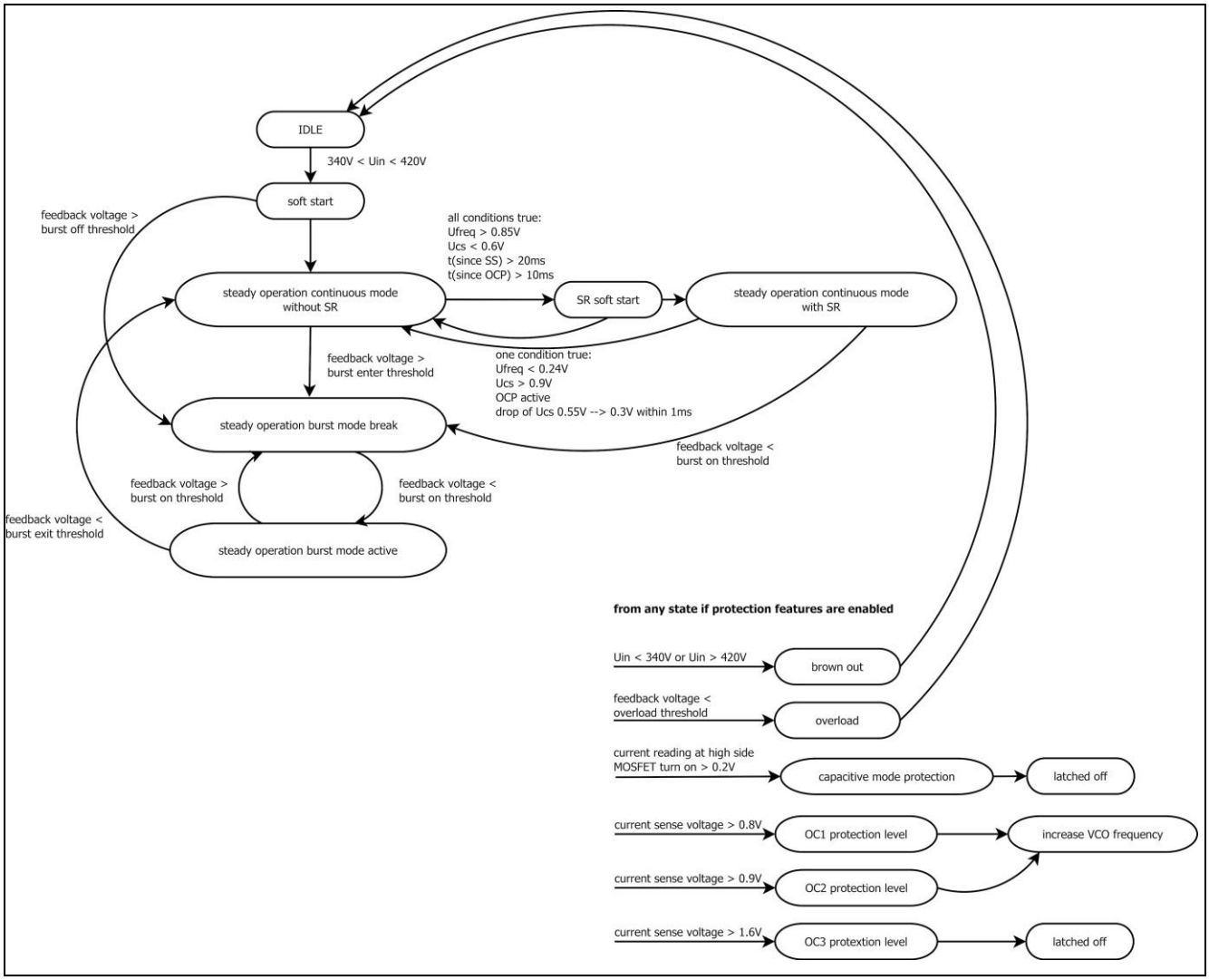

Figure 35 LLC operational state machine implementation using XMC4200

5.3 Full ZVS area

Similar to what has already been described in [7] and [8], almost full ZVS is achieved on the entire output load range as shown in Figure 36. This has significant benefits on the converter's efficiency down to a very light load.

This achievement is only possible through to a combination of a proper resonant tank design and dead time setting: only in this case, the MOSFET output capacitance will be completely discharged before turning the switch ON. You can easily recognize it from the absence of a Miller plateau in the V_{GS} waveform (Ch2).

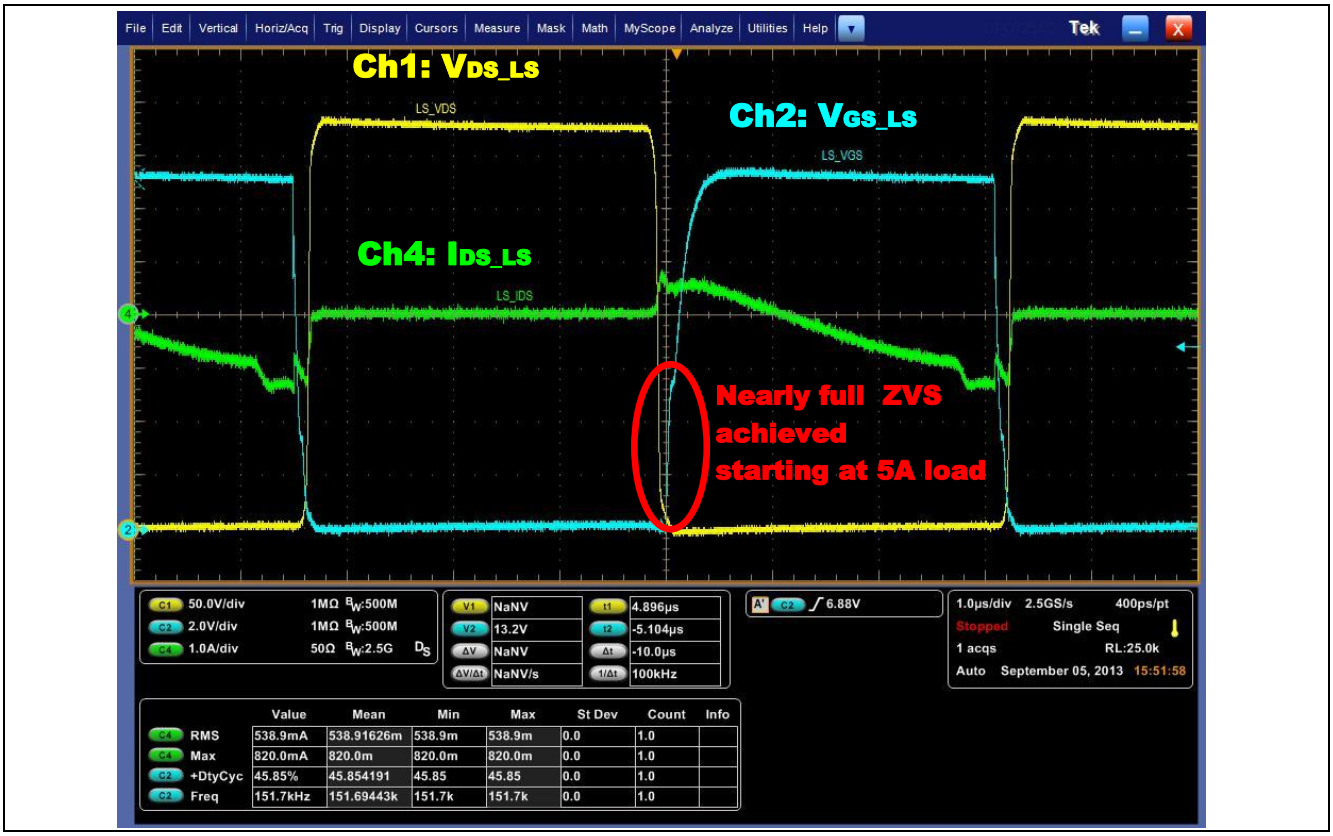

Figure 36 Nearly full Zero Voltage Switching (ZVS) starting at 5 A load

5.4 Burstmode operation

At no load or a very light load condition, the LLC controller provides a frequency approaching the maximum setting. In this condition, in order to achieve full ZVS, the magnetizing current should be high enough to discharge the output capacitors. Due to magnetizing current limitation, switching losses (especially turn-off loss) are relatively high if the devices will continue to switch at the highest frequency. In order to overcome this phenomenon, burst mode function is enabled and implemented. This leads to lower switching losses and driving losses because of the low burst frequency. Additionally, this helps to achieve regulation even at no load condition.

Figure 37 shows the burst mode implementation in the analog controller ICE2HS01G, as already described in [7] and [8] and with even more details in [12].

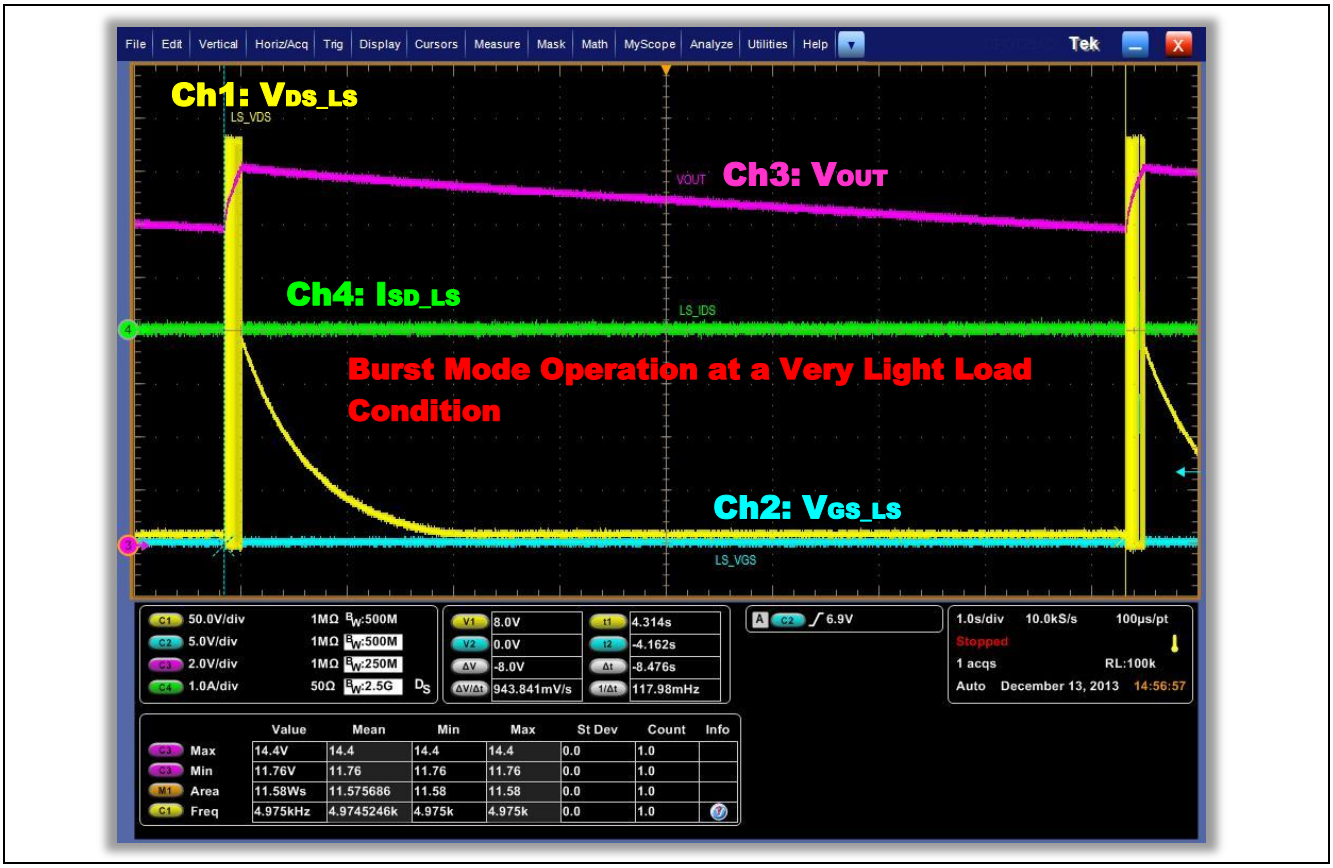

Figure 37 Burst mode opeartion at no-load and very light load condition with ICE2HSO1G

Figures 38 and 39 show the implementation of the burst mode in the version with digital control by the XMC4200.

From the comparison between Figures 37 and 38 one can appreciate – due to the same time division (1S/div) - that the burst frequency is significantly higher in the digitally controlled version. This allows the V_{out} regulation and ripple requirements to be fulfilled in the digital version even in burst mode operation, as shown by the purple waveform in both Figure 36 and 37 (V_{OUT}). This appears to be flat without the variation of 2.62 V that can be seen in Figure 35.

In the digital control, the burst mode is entered or exited according to the monitored value of the feedback voltage of the error amplifier. The goal is to achieve a limitation of power transfer in order to keep V_{out} in regulation and remove possible regulation problems due to the natural flattening of the gain curves at high switching frequencies.

According to this strategy, the burst mode is entered when V_{FREQ} < 0.38 V (f_{sw} = 245 kHz), which and exited when V_{FREQ}> 0.45 V (f_{sw} = 230 kHz).

The SR function is disabled during burst mode.

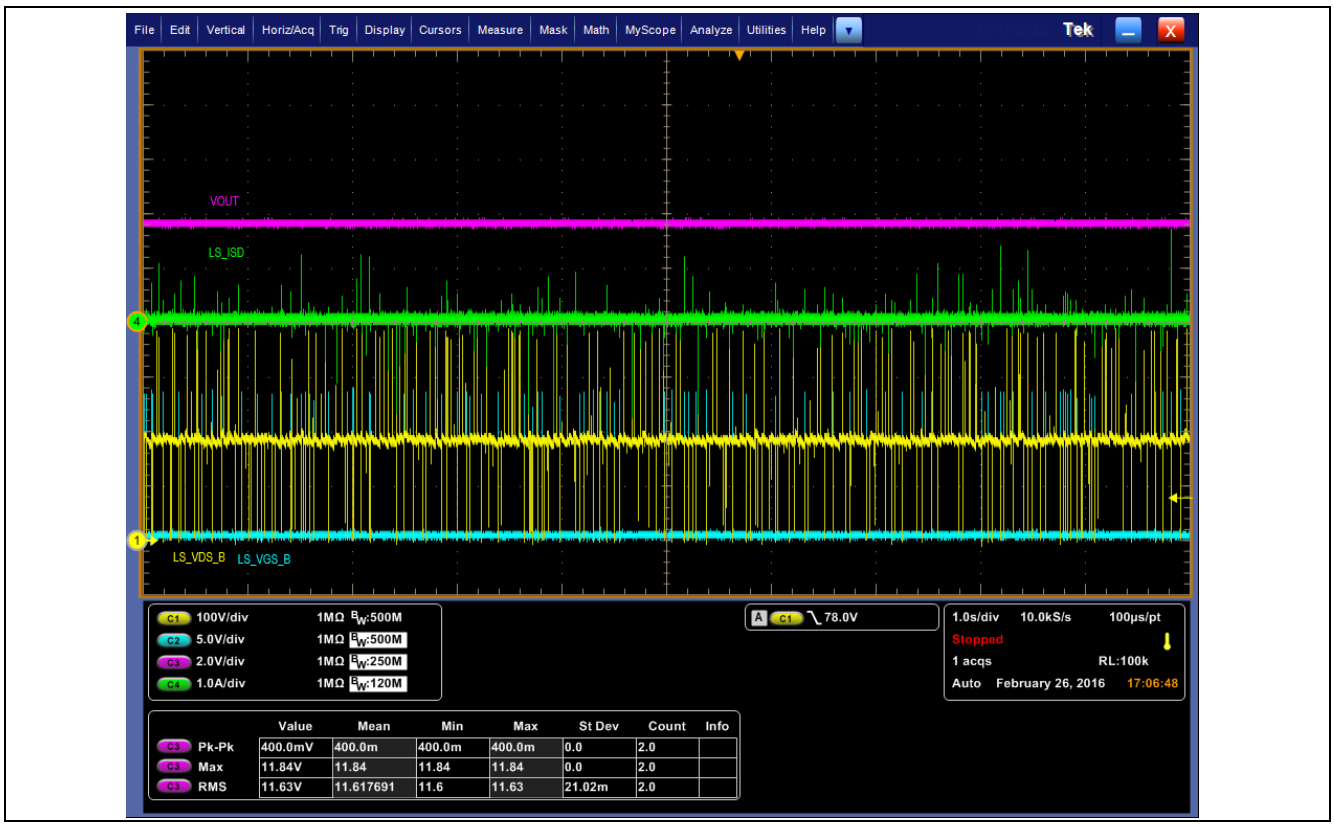

Figure 38 Burst mode operation at no-load and very light load condition with XMC4200

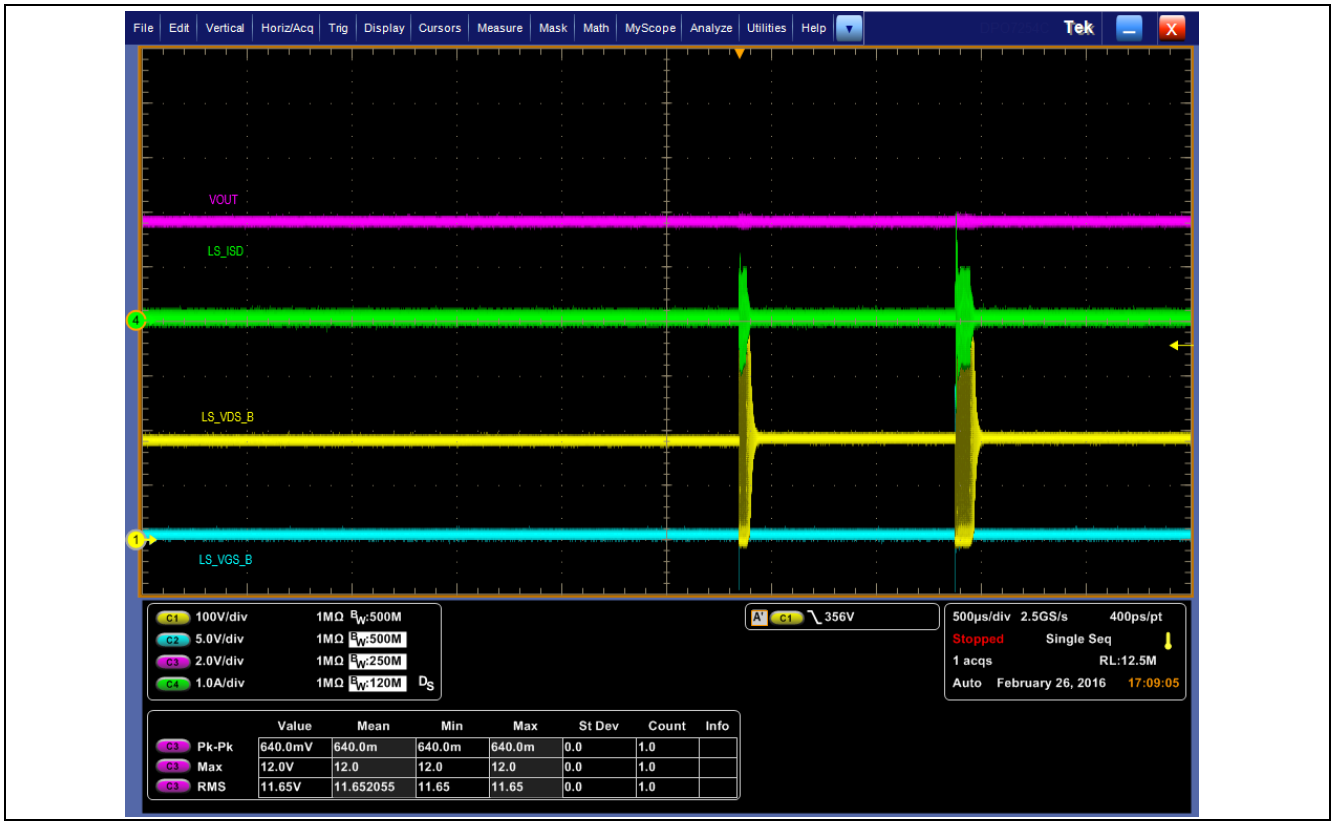

Figure 39 Burst mode operation at no-load and very light load condition with XMC4200

5.5 Adaptive dead time

As already explained in section 3.1.3, the time between the turn-off of one of the two HB switches and the turn-on of the other switch is called “dead time”. Properly setting this time in the control is needed in order to optimize the ZVS behavior, as illustrated in Figure 40.

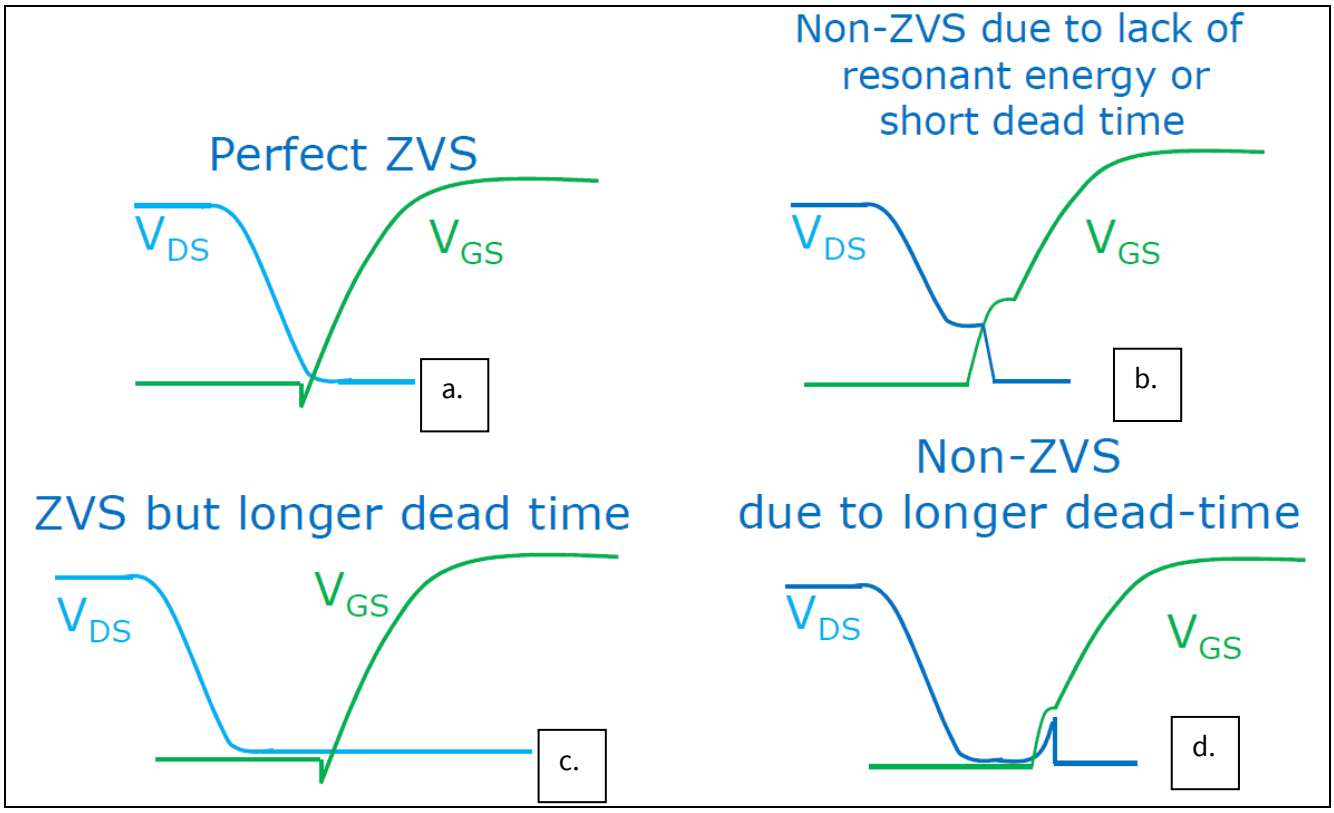

Figure 40 Proper and wrong dead time setting.

Four typical / possible settings are illustrated: the condition (a) represents the correct setting, where the MOSFET is switched on exactly after its output capacitance has been completely discharged. In (b) the ZVS is not achieved for lack of either resonant energy or not enough dead time. In (c) the ZVS is achieved, but the dead time is too long. (d) is the worst case scenario, where the dead time is so long that the device is switched on after the current has changed polarity, when the output capacitance has started to be charged again, resulting in a non-ZVS turn-on.

In our LLC design, the magnetizing current slightly changes as a function of the load. One can expect a certain increase of magnetizing current when the load increases and/or the input voltage decreases. If a fixed dead time is used, it must be set according to the lowest value of the magnetizing current, which happens at very light load, with the goal to achieve a ZVS similar to that shown in Figure 40(a). Since the magnetizing current is expected to increase with the load, thus reducing the time needed to discharge the MOSFET output capacitance, setting a constant dead time might lead to the situation shown in Figure 40(c).

The best way to prevent it is to set an adaptive dead time as a function of the load and input voltage.

Figure 41 shows the adaptation implemented in the digital control of our 600 W LLC.

Figure 42 illustrates the practical implementation, showing a difference of 30 nS in the dead time set respectively at I_{out}=35 A and I_{out}=50 A (being V_{in}=V_{in_nom}=380 V_{DC}): this will allow an optimal setting, through minimizing the MOSFET body diode conduction.

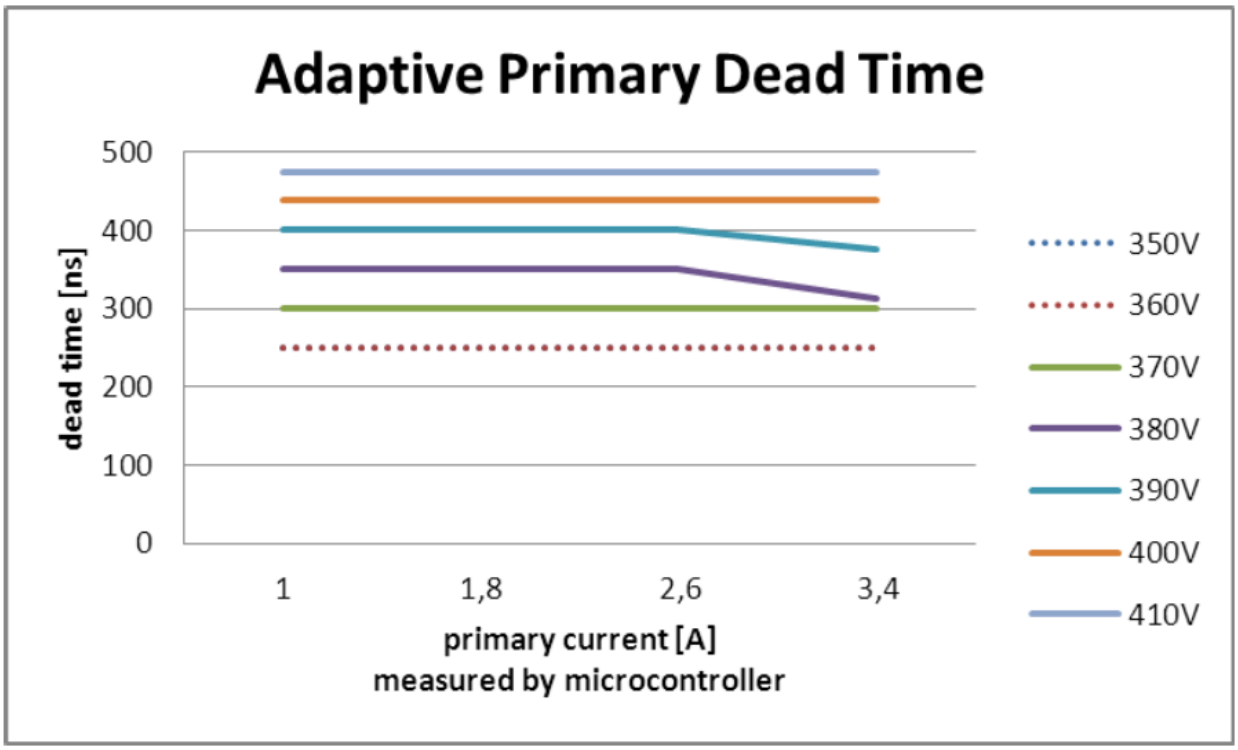

Figure 41 Adaptive dead time setting in 600 W LLC eval. board

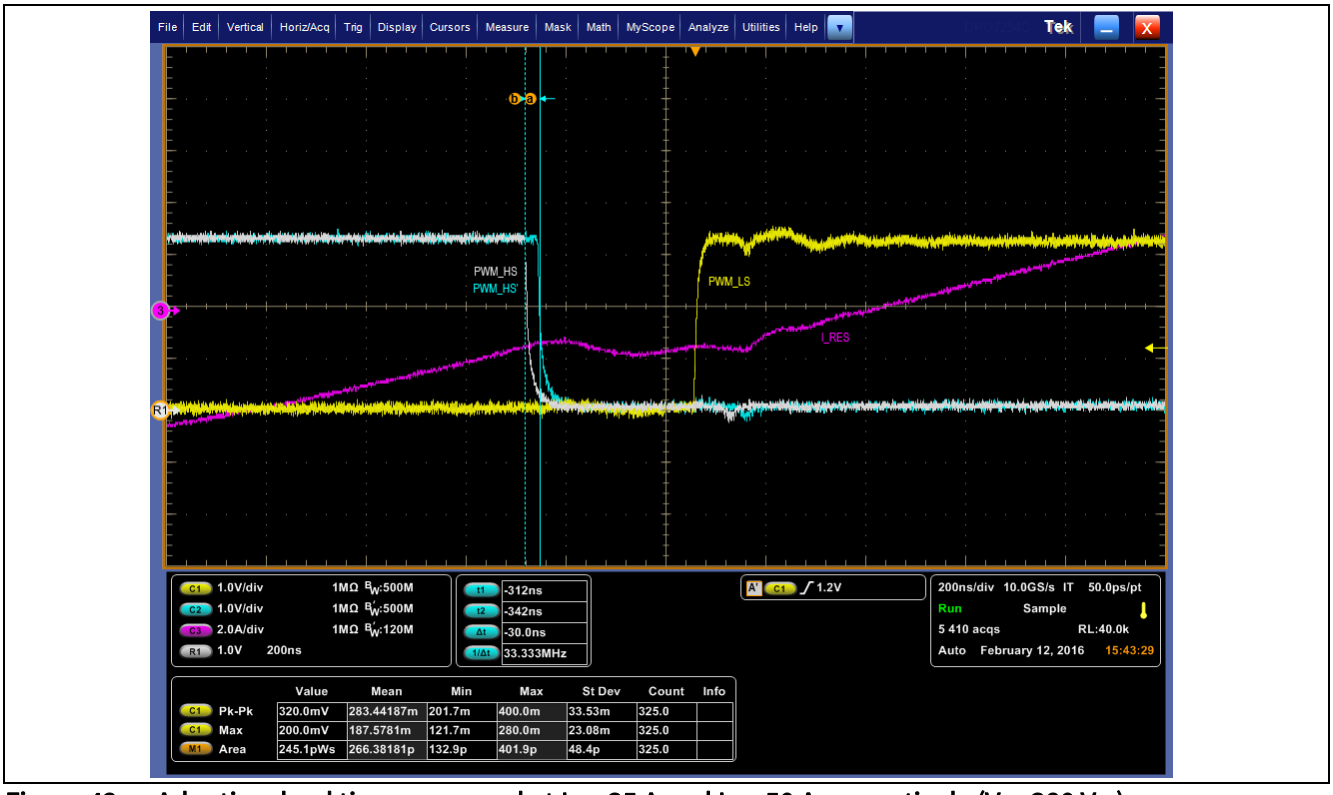

Figure 42 Adaptive dead time measured at I_{out}=35 A and I_{out}=50 A respectively (V_{IN}=380 V_{DC})

5.6 Synchronous rectification operation

Likewise, synchronous rectification follows the functionality hardwired into the ICE2HS01G, while it's programmability allows future adjustment and tuning, dependent on specific power system implementations.

The SR function is disabled during the start-up sequence and burst mode operation.

It is activated through a soft start procedure with an initial 0% duty cycle, and then the pulse width is gradually stepped to reach full duty cycle.

The SR is turned on if all the following conditions are true:

- V_{FREQ} > 1.138 V @V_{IN}=380 V (threshold depending on input voltage)⟶I_{OUT}>3 A
- V_{CS} (current sense) < 0.54 V (no over current protection active)
- Elapsed time since soft-start finished > 20 mS
- Elapsed time since over current protection > 10 mS

SR is turned off is one of the following conditions is true:

- V_{FREQ} < 0.24 V @V_{IN}=380 V (threshold depending on input voltage))⟶I_{OUT}<2 A
- V_{CS} > 0.6 V (over current protection active)
- Soft-start active

The ON time control is set according to the input voltage and switching frequency: the optimized values are stored in a look up table.

The turn-on delay is realized through a phase shift between the primary and secondary PWM signals. If V_{IN} is lower than the resonant voltage, the converter is operating below resonance and there is no phase shift.

If V_{IN} is higher than the resonant voltage, the converter is operating above resonance, a fixed turn-on delay of 240 nS is added, in the sense that each SR MOSFET gate is turned on 240 nS after the corresponding priomary gate. In our design there is no need of any turn-off delay because of the use of a fast optocoupler for SR gate signals.

Figures 43 and 44 illustrate this explanation..

The control includes a special algorithm, which disables the SR during a load jump from 100% to no load, this prevents possible hard commutation occurring in the primary MOSFETs due to feedback of energy from the secondary to primary side.

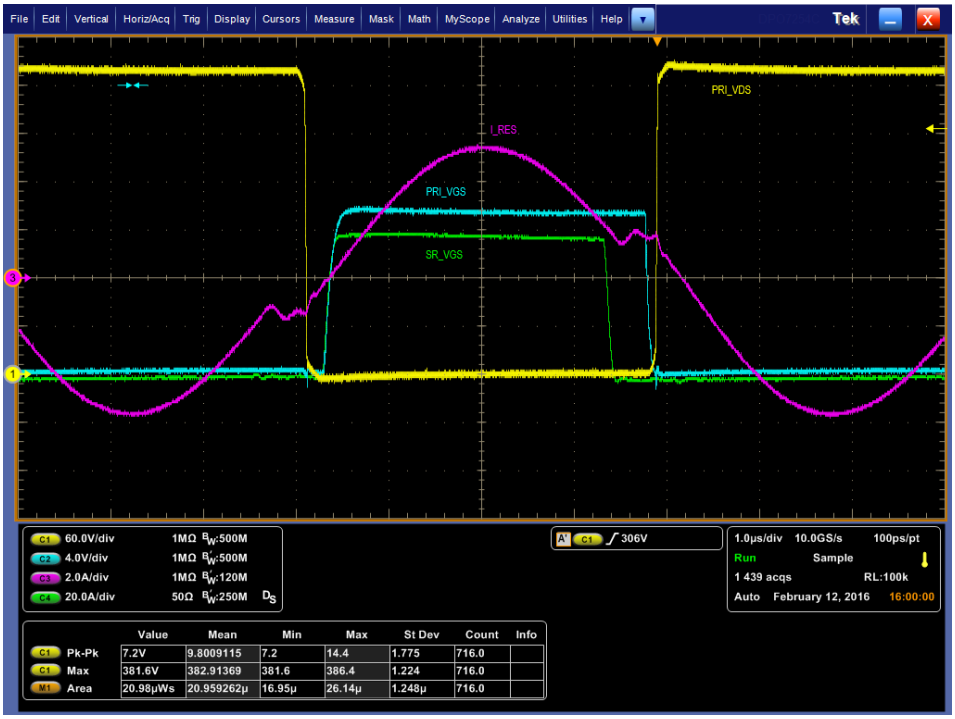

Figure 43 SR turn-on and turn-off delays below resonance

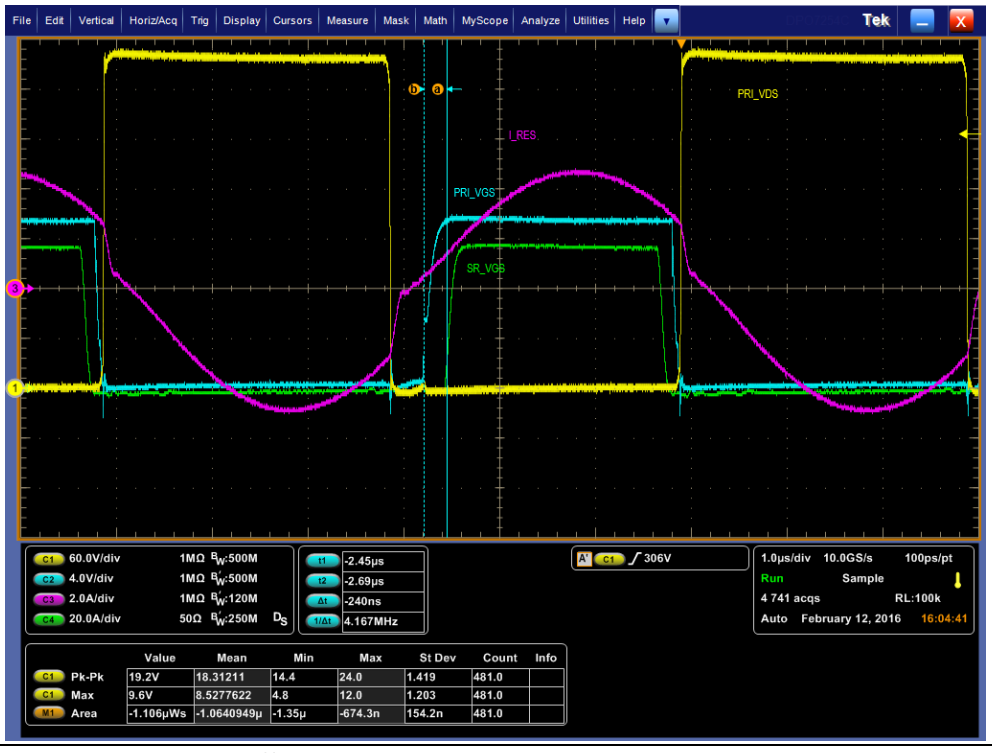

Figure 44 SR turn-on and turn-off delays above resonance

5.7 Critical LLC operations - hard commutation and capacitive load mode

In an LLC converter, hard commutation of the body diode may occur during the start-up, burst mode, overload and short circuit conditions. See also [7], [10] and [11]. Hard commutation happens in an LLC during the commutation period of the body diode. During this time, the resonant current is flowing through the body diode of the MOSFET creating a ZVS condition until this MOSFET turns on. When the current is not able to change direction prior to the turn-on of the other MOSFET, more charge will be stored in the P-N junction of that MOSFET. When the other MOSFET turns on, a large shoot-through current will flow due to the reverse-recovery current of the body diode. This results into a high reverese recovery peak current I_{RRM} and high reverse recovery dV/dT that could sometimes result in a MOSFET breakdown.

Another critical LLC operation is the capacitive load mode, which the converter enters when resonant current “leads” the voltage in the HB midpoint. In that condition, each of the two HB MOSFETs is turned on while the current is still forward circulating in the body diode of the opposite MOSFET. This turns into a stress on both MOSFETs similar to what seen during hard commutation. This condition can be minimized in the design by the proper selection of resonant components and properly setting the minimum and maximum operating frequencies.

The digital control offers the possibility to prevent or, at least, minimize the occurrence of these two critical operations through dedicated algorithms in combination with some additional sensing information from the HW.

A typical condition that could possibly trigger hard commutation is the start-up: an effective way to prevent this is to guarantee that the first “complete” switching sequence starts only when the resonant capacitance is charged at $V_{in}/2$, preventing any initial transformer flux imbalance. This can be achieved by not using 50% duty cycle at start-up, but actually conditioning the MOSFET turn-on time to the zero crossing of the resonant current (see also [10]).

In the 600 W LLC evaluation board HW, originally designed for primary side analog control by the ICE2HS01G2, the primary current zero crossing detection information is not available. Therefore, the hard commutation prevention algorithm at start-up (including the burst mode) consists of stepping the pulse width on HS and LS devices gradually to reach 50%: 0%, 16% , 33%, 50%.

The Figure 45 below shows the 600 W start-up condition with the analog control (a) and digital control by XMC (b). A reduction in the drain current peak from 13 A to 3 A is achieved by moving from analog to digital control, with a consequent reduction of the stress on the MOSFET.

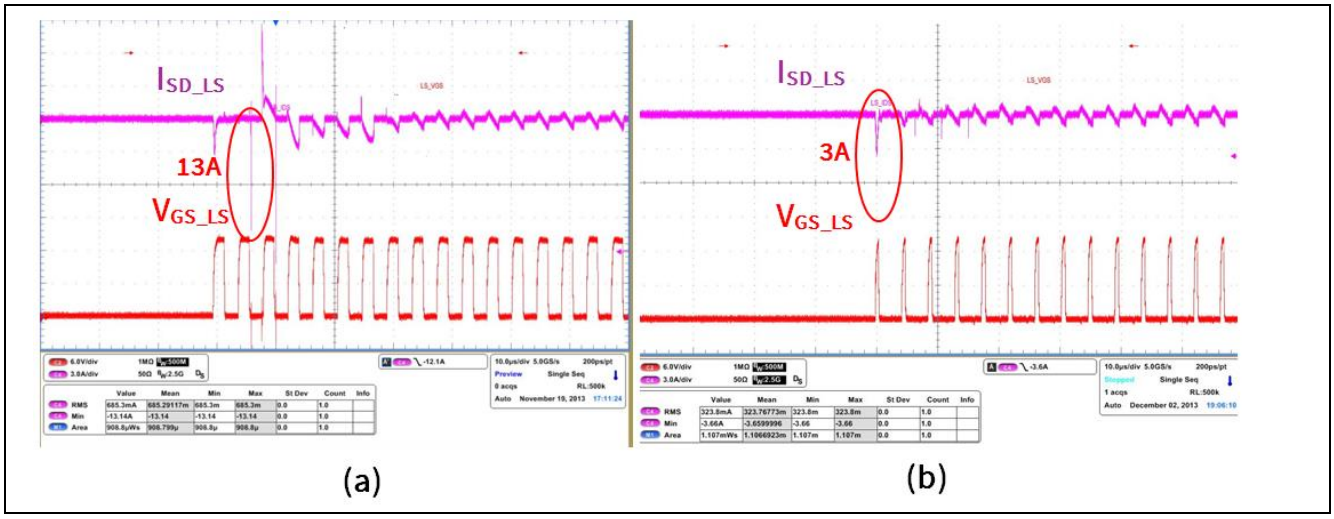

Figure 45 Hard Commutation During Start-up

In the 600 W LLC evaluation board the capacitive load mode is prevented by design, as explained in detail in chapter 3 of this document. However an algorithm to prevent it is also implemented in the source code.

For the prevention of capacitive load mode, resonant current zero crossing detection would be needed in order to measure the phase difference with the voltage in the HB midpoint.

A valuable alternative solution used in our design consists of the measurement of the instantaneous value of the resonant current, which is available in the circuit implemented in Figure 46.

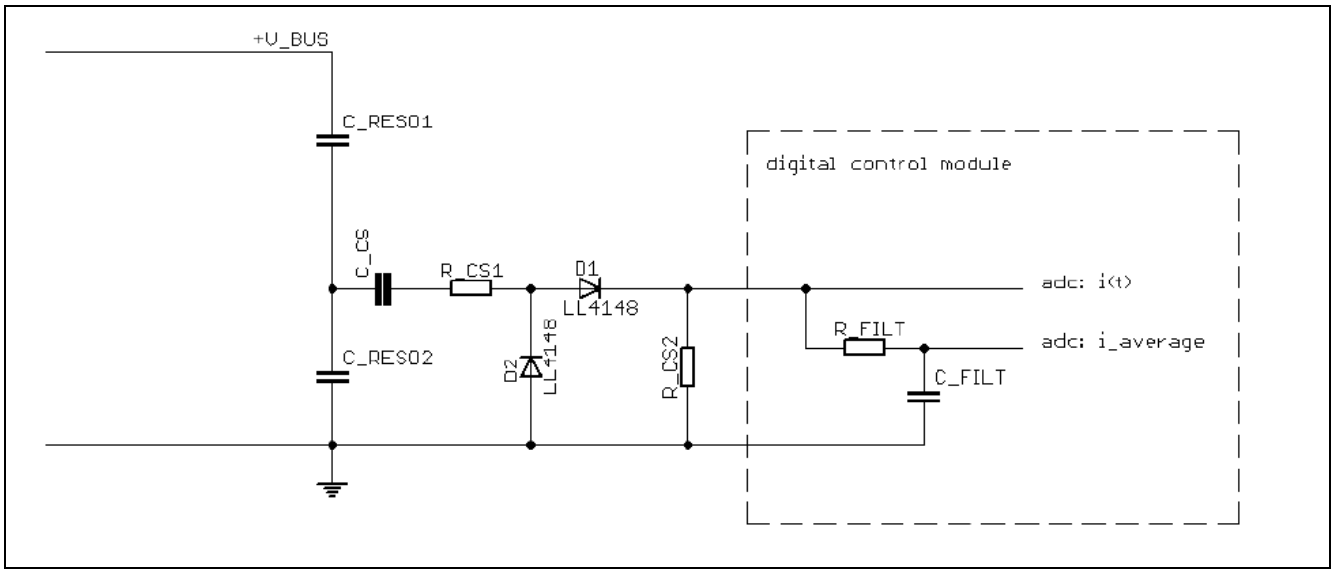

Figure 46 Anti-capacitive load mode: instantaneous primary current measurement

The conversion of the ADC is synchronized with the rising edge of the high side MOSFET PWM signal: a voltage higher than 0.2 V measured on ADC input during that rising edge is a clear indicator of capacitive load mode. If this happens, the SW will immediately shut down the converter and resume operation with a soft start procedure.

5.8 Efficiency plot

Figure 47 shows the efficiency comparison of this 600 W LLC eval board with reference to the 80+ Titanium Standard efficiency.

The efficiency plot has been measured without the bias and the fan absorption.

In fact, in typical single-output power supply (often used in rack mount servers and blade server applications) the fans are sized not only to remove heat from the power supply but also the heat from the system. For this reason, also in order to facilitate the system designer's use of different cooling strategies for the system, the power consumed by the fan is not included for efficiency calculations. If the power supply has an internal fan, then the manufacturer gives provision to supply external power to the fan during the power supply efficiency testing (see also [14] for further details)

In our concept, we intentionally focus the application noteon the LLC design independent from the design of the auxiliary bias, which can be more or less efficient according to the the topology choosen for the auxiliary converter and the target of light load efficiency.

Our 600 W LLC is able to fulfill the 80+ Titanium Standard requirements for the HV DC-DC stage.

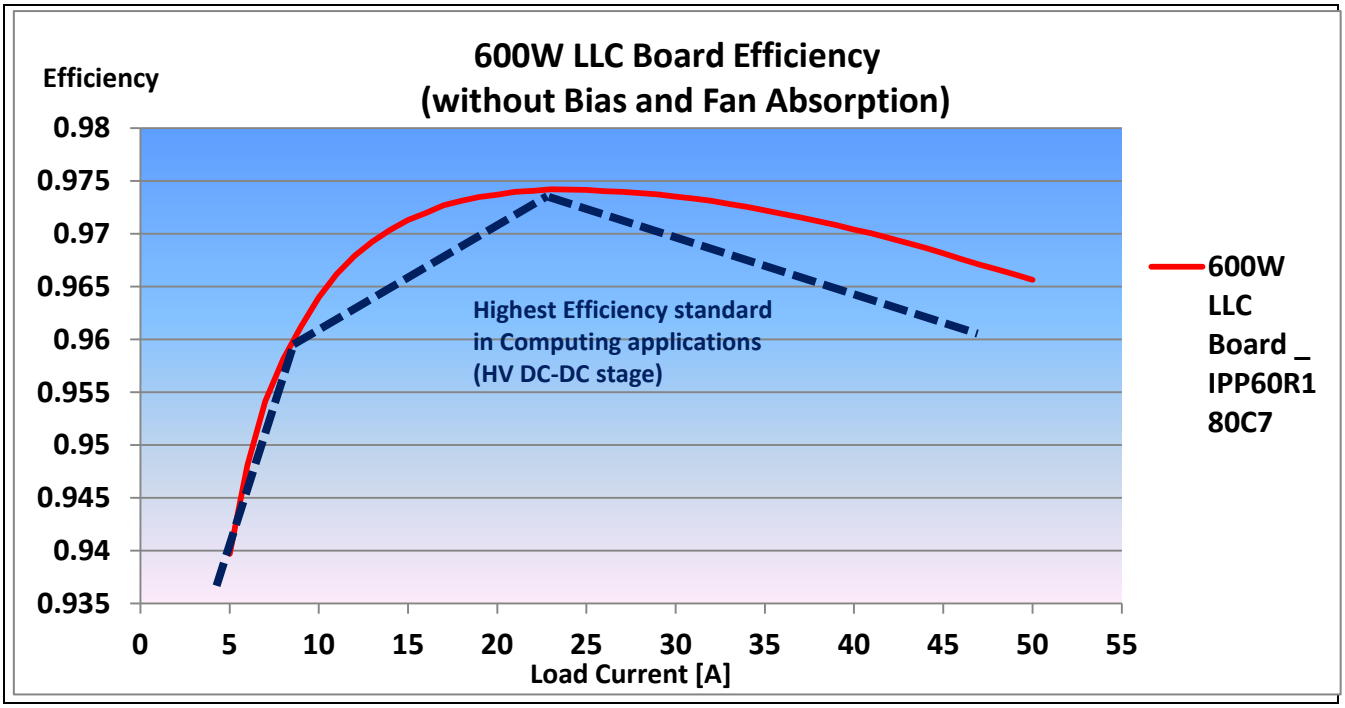

Figure 47 IFX 600 W LLC evaluation board effciency vs Titanium STD efficiency

5.9 Summary

In the version of the 600 W LLC design with digital control, all of the features of the analog design using the ICE2HS01G have been implemented.

The final efficiency result is very similar for both versions.

However, additional features have been introduced in order to make the design more flexible and reliable: these are typical expectations for a digitally controlled SMPS application and they have been completely fulfilled in our design.

In order to make our evaluation board user friendly, a Graphical User Interface (GUI) would be a natural evolution of our digital controll. This is planned as next step, by using serial communication between the MCU and the board via an RS232/TTL or USB/TTL interface.

The GUI will allow the user/designer to quickly set some design parameters and to check in real time some typical indicators (e.g. input/output current/voltage) and the status of the converter, including possible fault conditions.

6 Test/power-up procedure

Test	Test procedure	Condition
1. Auxiliary circuit turn-on	Apply 30 V_{DC} on the input.	V_{in}: ~30 V_{DC}
		Orange LED will light up
2. LLC converter turn-on	Apply 350 V_{DC}. Converter will give V_{out} =12 V_{DC}.	V_{in}: 350 V_{DC}
		V_{out}:12 V
3. Operational switching frequency	Using voltage probe, monitor switching frequency at following test conditions:	V_{in}:380 V_{dc}
		V_{out}:12 V
	@5 A Output load 10% load - ~ 155 kHz*	**I_{out}: 5 A**
	@25 A Output load 50% load - ~ 142 kHz*	**I_{out}: 25 A**
	@50 A Output load 100% load - ~ 132 kHz*	**I_{out}: 50 A**
	*(*measure freq. at "Pri_LS_VGS"-connector)*	
	[* +-10 kHz]	
4. Fan enable	Switch the load from 50 A to 5 A. Increase the output load current from 11-14 A, fan should turn on.	V_{in} =380 V_{dc}
		I_{out}= 5 A
		ÞFan is off
		V_{in} =380 V_{dc}
		I_{out}= 11-14 A
		ÞFan is on
5. Switch off input start-up at no load	Switch off the input	V_{in}= 0 V_{dc}
		I_{out}= 0 A
	Switch at 380 V_{dc} on **no load output**. Operation should be in burst mode.	V_{in} =380 V_{dc}
		I_{out} = 0 A
		V_{out} = 11,5 – 12,5
6. Switch off input; Start-up at full load	Switch off the input	**V_{in}= 0 V_{dc}**
		I_{out}= 0 A
	Apply 380 V_{dc} with full load @50 A output. V_{out} is in between 11.8 – 12.2 V_{dc}* *(*measure on the board-*	V_{in} =380 V_{dc}
		V_{out}: 11,8 – 12,3 V_{dc}
		I_{out} = 50 A

	connector)	
7. Running no load -> output short circuit	Switch off load from 380 V_{dc} **50 A** to 380 V_{dc} **0 A.**	V_{in} =380 V_{dc}
	Short circuit the load using the short circuit function of the e-load. **Converter should latch.**	*(after short circuit)* **V_{out} = 0 V_{dc}**
		I_{out} = 0 A
8. Switch off input & remove short circuit	Switch off the input.	**V_{in}= 0 V_{dc}**
9. Running full load -> over current protection	Remove short circuit function on the load.	I_{out}= 0 A
	Apply 380 V_{dc} 50 A with full load output. Increase the current on the output 1 A each step until the converter goes into protection starting from 50 A. OCP occurs between 55 A and 62 A.	V_{in} =380 V_{dc}
		I_{out} = 50 A
		OCP = between 55 A – 62 A
10. Running full load -> output short circuit	Apply 380 V_{dc} 50 A with full load output. Short circuit the load using the short circuit functions of the load. Converter should latch.	I_{out}= 0 A
		V_{in} =380 V_{dc}
		I_{out} = 50 A
		(after short circuit) **V_{out}=0 Vdc**
11. Switch off input; start-up -> output short circuit	Switch off the input.	V_{in}= 0 V_{dc}
		I_{out}= 0 A
	Apply 380 V_{dc} with output load short circuit. *Converter should be in hiccup/latch mode.*	V_{in} =380 V_{dc}
		I_{out} = short circuit
		V_{out} = 0 V short circuit (hiccup/latch)
12. Switch off input & remove short circuit	Switch off the Input.	V_{in}= 0 V_{dc}
	Remove short circuit function on the load.	I_{out}= 0 A
13. Dynamic loading	Apply 380V_{dc}. Set the electronic load to dynamic loading mode with the following settings:	V_{in} =380 V_{dc}
	CCDH1: I_{out} 5 A	**I_{out} = 5 A…50 A**
	CCDH2: I_{out} 50 A	**V_{out} = 11,5 – 12,5 V_{dc}**
	Dwell time: 10 mS	
	Load slew rate: 1 A/µS	

7 Useful material and links

In the following links, you can find more detailed information about the devices used from Infineon and the magnetic components.

- **Primary HV MOSFETs CoolMOS™ IPP60R180C7:**

http://www.infineon.com/dgdl/Infineon-IPP60R180C7-DS-v02_00-EN.pdf?fileId=5546d4624cb7f111014d483fe4ba707b

- **Microcontroller XMC4200**

http://www.infineon.com/dgdl/Infineon-XMC4100_XMC4200-DS-v01_02-en.pdf?fileId=db3a30433afc7e3e013b3cf9b2816573

- **Advanced dual channel gate drive 2EDN7524F**

http://www.infineon.com/dgdl/Infineon-2EDN752x_2EDN852x-DS-v01_00-EN.pdf?fileId=5546d4624cb7f111014d672f9fbb5142

- **Half bridge gate drive 2EDL05N06PF**

http://www.infineon.com/cms/en/product/power/motor-control-and-gate-driver-ics/isolated-gate-driver-ics/2EDL05N06PF/productType.html?productType=db3a30443e36c802013e3c260fb915fd

- **Bias QR flyback controller ICE2QR2280Z**

http://www.infineon.com/dgdl/Datasheet_ICE2QR2280Z_v21_20110830.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=db3a30432a7fedfc012a8d8038e00473

- **SR MOSFETs OptiMOS™ BSC010N04LS**

http://www.infineon.com/cms/en/product/power/power-mosfet/20v-300v-n-channel-power-mosfet/40v-75v-n-channel-power-mosfet/BSC010N04LS/productType.html?productType=db3a3044353fd87f013551a8816e094a

- **Main transformer and resonant choke ferrite cores**

http://en.tdk.eu/blob/519704/download/2/ferrites-and-accessories-data-book-130501.pdf

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[10] Lawrence Lin, Gary Chang: “Consideration of Primary side MOSFET Selection for LLC topology”, Infineon Technologies AN, 2014

[11] F. Stückler, S. Abdel-Rahman, K. Siu: “ 600V CoolMOS™ C7 Design Guide”, Infineon Technologies AN May 2015

[12] Anders Lind: “LLC Converter Design Note”, Infineon Technologies AN 2013-03

[13] Liu Jianwei, Li Dong: “Design Guide for LLC Converter with ICE2HS01G”, Infineon Technologies AN V1.0, July 2011

[14] Dr. Arshad Mansoor, Brian Fortenbery, Peter May-Ostendop and others: “Generalized Test Protocol for Calculating the Energy Efficiency of Internal Ac-Dc and Dc-Dc Power Supplies”, Revision 6.7, March 2014

9 List of abbreviations

BOM……..Bill Of Materials
BM……Burst Mode
C_{GD} .....internal gate drain capacitance CGD=Crss
C_{iss}.....input capacitance $C_{iss}=C_{GS}+C_{GD}$
$C_{o(er)}$ .....effective output capacitance, energy related
$C_{o(tr)}$ .....effective output capacitance, time related
C_r .....resonant capacitance
di/dt .....steepness of current slope at turn off / turn on
DUT .....device under test
dv/dt .....steepness of voltage slope at turn off / turn on
E_{off}.....energy losses at switch off
E_{on}.....energy losses loss at switch on
E_{oss}.....stored energy in output capacitance (Coss) at typ. V_{DS}=400V
FHA.....First Harmonic Approximation Method
FOM.....Figures of Merit
f_r .....resonant frequency
GUI……Graphic User Interface
I_D..... drain current
I_{RMS}.....effective root mean square current
I_{mag} .....magnatizing current
$I_{m,pk}$.....peak magnetizing current
K..... gain factor
L_r ..... resonant inductance
L_m..... magnetizing inductance
m ..... inductance factor
N_p ..... primary winding
N_S.....secondary winding
n ..... transformer turn ratio
MOSFET.....metal oxide semiconductor field effect transistor
P_{cond_SR} .....synchronous rectification conduction losses
PFC.....power factor correction
PNP..... bipolar transistor type (pnp vs. npn)
Q_{OSS} .....Charge stored in the C_{OSS}
Q .....quality factor
R_{ac}.....total equivalent resistor
$R_{DS(on)}$..... ……drain-source on-state resistance
$R_{g,tot}$ .....total gate resistor
R_o .....output resistor
R_{th} .....thermal resistance
SMPS……Switch Mode Power Supply
t_{dead} .....dead time

t_{ecs} .....early channel shut down time
V_{DS} .....drain to source voltage, drain to source voltage
$V_{gs,th}$.....drain to source threshold voltage
V_{O_AC} .....output voltage; alternating current
V_{In_AC} .....input voltage, alternating current
V_{In_nom} .....nominal input voltage
V_{out_nom}.....nominal output voltage
ZCS.....zero current switching
ZVS.....zero voltage switching

Revision history

Major changes since the last revision

Page or Reference	Description of change
--	First Release

www.infineon.com

Edition 2015-05-01

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

AN_201411_PL52_005

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