# BLP05H6700XR; BLP05H6700XRG

**Power LDMOS transistor**

**Rev. 2 — 13 September 2018**

AMPLEON

**Product data sheet**

## 1. Product profile

### 1.1 General description

A 700 W extra rugged LDMOS power transistor optimized for broadcast, industrial, aerospace and defense applications in the HF to 600 MHz band.

**Table 1. Application information**

| Test signal | f | $V_{DS}$ | $P_L$ | $G_p$ | $\eta_D$ |
|---|---|---|---|---|---|
| | (MHz) | (V) | (W) | (dB) | (%) |
| pulsed RF | 108 | 50 | 700 | 26 | 75 |

### 1.2 Features and benefits

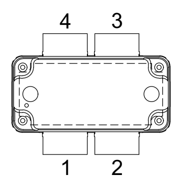
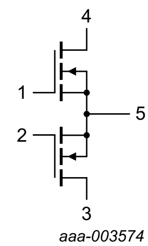
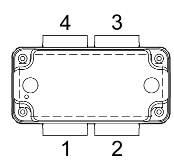
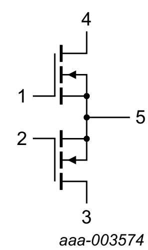
- Easy power control
- Integrated dual sided ESD protection enables class C operation and complete switch off of the transistor
- Excellent ruggedness VSWR 65 : 1
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 600 MHz)
- 50 V operation for easy broadband matching
- Package available in both straight leads and gull wing form
- For RoHS compliance see the product details on the Ampleon website

### 1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications
- Aerospace and defense applications

## 2. Pinning information

**Table 2. Pinning**

| Pin | Description | Simplified outline | Graphic symbol |
|---|---|---|---|
| **BLP05H6700XR (SOT1138-3)** | | | |
| 1 | gate 2 |   |   |
| 2 | gate 1 | | |
| 3 | drain 1 | | |
| 4 | drain 2 | | |
| 5 | source [1] | | |
| **BLP05H6700XRG (SOT1204-3)** | | | |
| 1 | gate 2 |   |   |
| 2 | gate 1 | | |
| 3 | drain 1 | | |
| 4 | drain 2 | | |
| 5 | source [1] | | |

[1] Connected to flange.

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BLP05H6700XR | - | plastic, heatsink small outline package; 4 leads (flat) | SOT1138-3 |
| BLP05H6700XRG | - | plastic, heatsink small outline package; 4 leads | SOT1204-3 |

## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | | - | 135 | V |
| $V_{GS}$ | gate-source voltage | | –6 | +11 | V |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $T_{case}$ | case temperature | | - | 150 | °C |
| $T_j$ | junction temperature | [1] | - | 225 | °C |

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

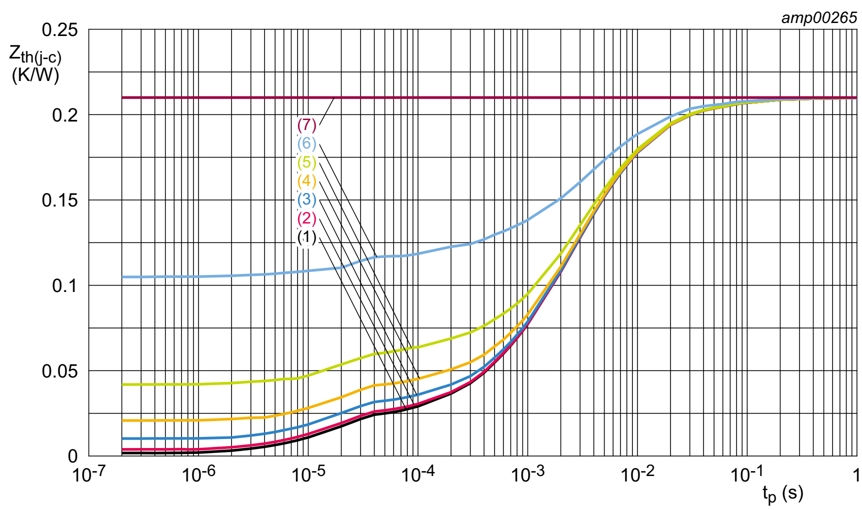
**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $R_{th(j\text{-}case)}$ | thermal resistance from junction to case | $T_j$ = 150 °C | [1][2] | 0.21 | K/W |
| $Z_{th(j\text{-}case)}$ | transient thermal impedance from junction to case | $T_j$ = 150 °C; $t_p$ = 100 μs; δ = 20 % | [3] | 0.064 | K/W |

[1] $T_j$ is the junction temperature.

[2] $R_{th(j\text{-}c)}$ is measured under RF conditions.

[3] See Figure 1.




(1) δ = 1 %
(2) δ = 2 %
(3) δ = 5 %
(4) δ = 10 %
(5) δ = 20 %
(6) δ = 50 %
(7) δ = 100 % (DC)

**Fig 1. Transient thermal impedance from junction to case as a function of pulse duration**

# 6. Characteristics

**Table 6. DC characteristics**

*$T_j$ = 25 °C per section; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{GS}$ = 0 V; $I_D$ = 2.75 mA | 135 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $V_{DS}$ = 10 V; $I_D$ = 275 mA | 1.33 | 1.9 | 2.33 | V |
| $V_{GSq}$ | gate-source quiescent voltage | $V_{DS}$ = 50 V; $I_D$ = 50 mA | - | 2.1 | - | V |
| $I_{DSS}$ | drain leakage current | $V_{GS}$ = 0 V; $V_{DS}$ = 50 V | - | - | 1.4 | μA |
| $I_{DSX}$ | drain cut-off current | $V_{GS}$ = $V_{GS(th)}$ + 3.75 V; $V_{DS}$ = 10 V | - | 36 | - | A |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 11 V; $V_{DS}$ = 0 V | - | - | 140 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS}$ = $V_{GS(th)}$ + 3.75 V; $I_D$ = 9.625 A | - | 0.16 | - | Ω |

**Table 7. AC characteristics**

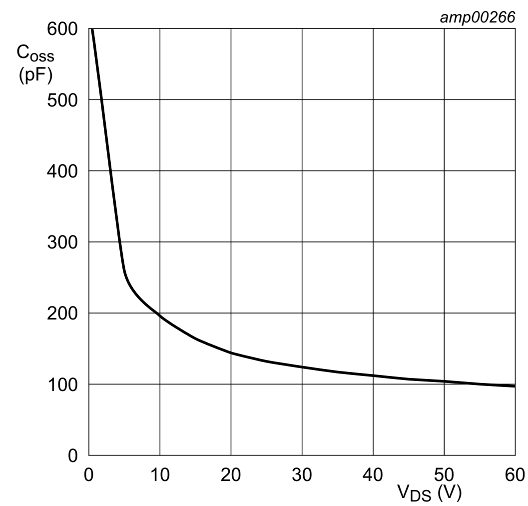
*$T_j$ = 25 °C per section; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_{rs}$ | feedback capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 50 V; f = 1 MHz | - | 2.75 | - | pF |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 50 V; f = 1 MHz | - | 297 | - | pF |
| $C_{oss}$ | output capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 50 V; f = 1 MHz | - | 104 | - | pF |

**Table 8. RF characteristics**

*Test signal: pulsed RF; $t_p$ = 100 μs; δ = 20 %; f = 108 MHz; RF performance at $V_{DS}$ = 50 ; $I_{Dq}$ = 100 mA; $T_{case}$ = 25 °C; unless otherwise specified; in a class-AB production test circuit.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $G_p$ | power gain | $P_L$ = 700 W | 25 | 26 | - | dB |
| $RL_{in}$ | input return loss | $P_L$ = 700 W | - | −13 | - | dB |
| $\eta_D$ | drain efficiency | $P_L$ = 700 W | 72 | 75 | - | % |




$V_{GS}$ = 0 V; f = 1 MHz.

**Fig 2. Output capacitance as a function of drain-source voltage; typical values per section**

# 7. Test information

## 7.1 Ruggedness in class-AB operation

The BLP05H6700XR and the BLP05H6700XRG are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions: $V_{DS}$ = 50 V; $I_{Dq}$ = 100 mA; $P_L$ = 700 W pulsed; f = 108 MHz.

## 7.2 Impedance information

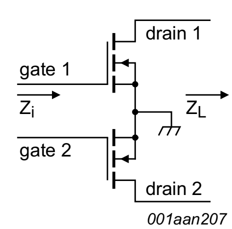


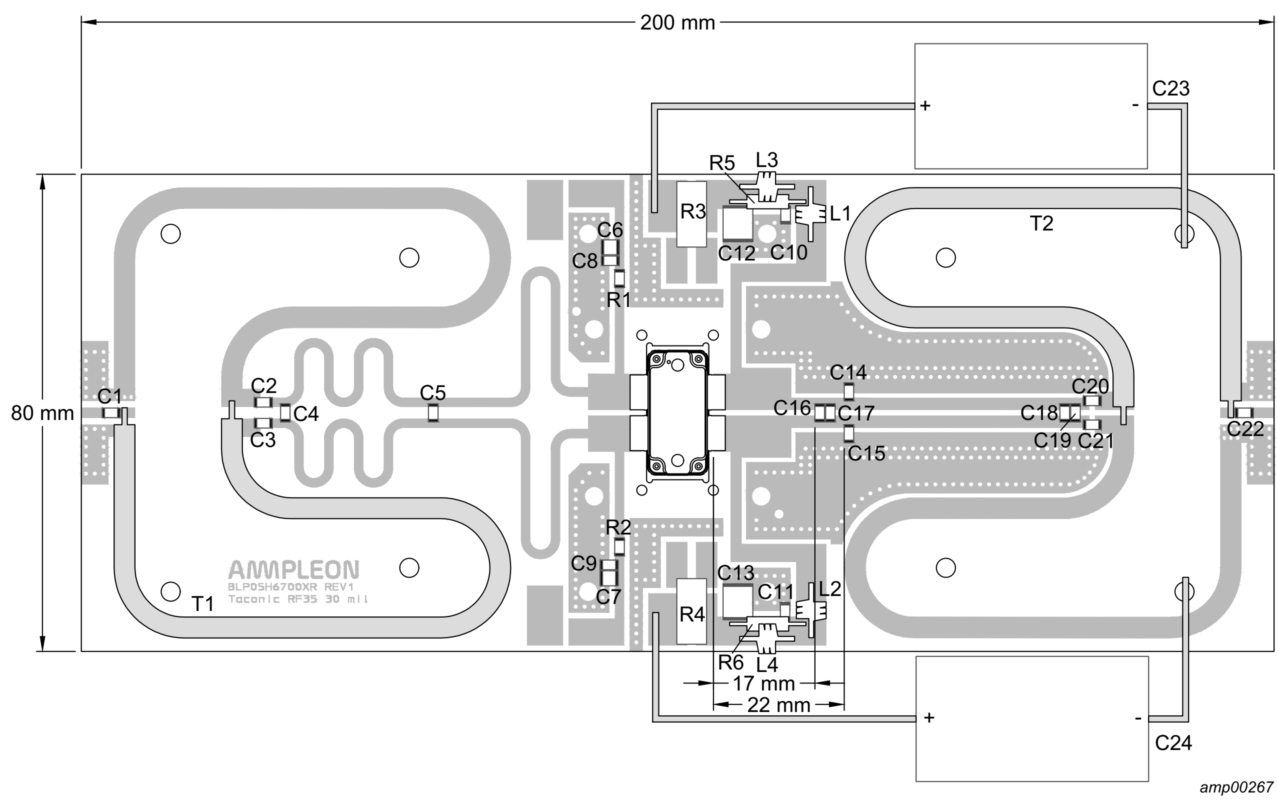

**Fig 3. Definition of transistor impedance**

**Table 9. Typical push-pull impedance**

*Simulated $Z_i$ and $Z_L$ device impedance; impedance info at $V_{DS}$ = 50 V and $P_L$ = 700 W.*

| f | $Z_i$ | $Z_L$ |
|---|---|---|
| (MHz) | (Ω) | (Ω) |
| 108 | 5.9 – j19.1 | 5.5 + j1.1 |

## 7.3 Test circuit




Printed-Circuit Board (PCB): Taconic RF-35; $\varepsilon_r$ = 3.5 F/m; thickness = 0.765 mm; thickness copper plating = 35 μm.

See Table 10 for a list of components.

**Fig 4. Component layout for class-AB production test circuit**

**Table 10. List of components**

*For test circuit see Figure 4.*

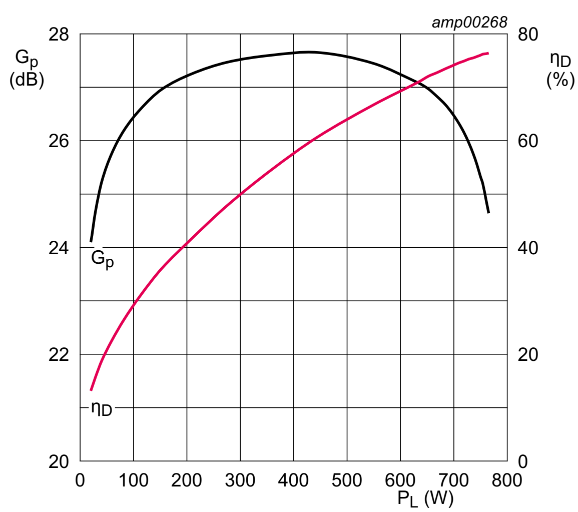
| Component | Description | Value | | Remarks |
|---|---|---|---|---|
| C1 | multilayer ceramic chip capacitor | 510 pF | [1] | ATC 100B |
| C2, C3 | multilayer ceramic chip capacitor | 62 pF | [1] | ATC 100B |
| C4 | multilayer ceramic chip capacitor | 20 pF | [1] | ATC 100B |
| C5 | multilayer ceramic chip capacitor | 160 pF | [1] | ATC 100B |
| C6, C7 | multilayer ceramic chip capacitor | 4.7 μF, 100 V | | |
| C8, C9 | multilayer ceramic chip capacitor | 820 pF | [1] | ATC 100B |
| C10, C11 | multilayer ceramic chip capacitor | 820pF | [1] | ATC 100B |
| C12, C13 | multilayer ceramic chip capacitor | 4.7 μF, 100 V | | |
| C14, C15 | multilayer ceramic chip capacitor | 91 pF | [1] | ATC 100B |
| C16 | multilayer ceramic chip capacitor | 36 pF | [1] | ATC 100B |
| C17 | multilayer ceramic chip capacitor | 22 pF | [1] | ATC 100B |
| C18, C19 | multilayer ceramic chip capacitor | 47 pF | [1] | ATC 100B |
| C20, C21 | multilayer ceramic chip capacitor | 120 pF | [1] | ATC 100B |

**Table 10. List of components** *...continued*
*For test circuit see Figure 4.*

| Component | Description | Value | Remarks |
|---|---|---|---|
| C22 | multilayer ceramic chip capacitor | 220 pF [1] | ATC 100B |
| C23, C24 | electrolytic capacitor | 2200 μF, 64 V | |
| L1, L2 | air inductor | 10 turns, d = 2 mm | 0.5 mm copper wire |
| L3, L4 | air inductor | 6 turns, d = 2 mm | 0.5 mm copper wire |
| R1, R2 | resistor | 4.7 kΩ | SMD 1206 |
| R3, R4 | shunt resistor | 0.01 Ω | FC4L110R010FER |
| R5, R6 | metal film resistor | 10 Ω, 0.6 W | |
| T1, T2 | semi rigid coax | 50 Ω, 160 mm | EZ 86-TP/M17 |

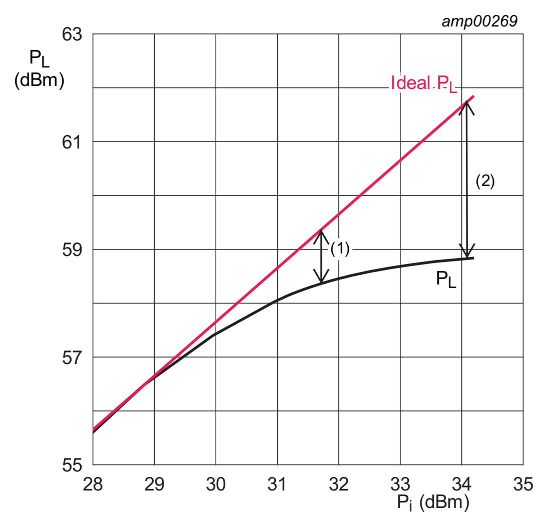
[1] American Technical Ceramics type 100B or capacitor of same quality.

## 7.4 Graphical data




$V_{DS}$ = 50 V; $I_{Dq}$ = 100 mA; f = 108 MHz; $t_p$ = 100 μs; δ = 20 %.

**Fig 5. Power gain and drain efficiency as function of output power; typical values**

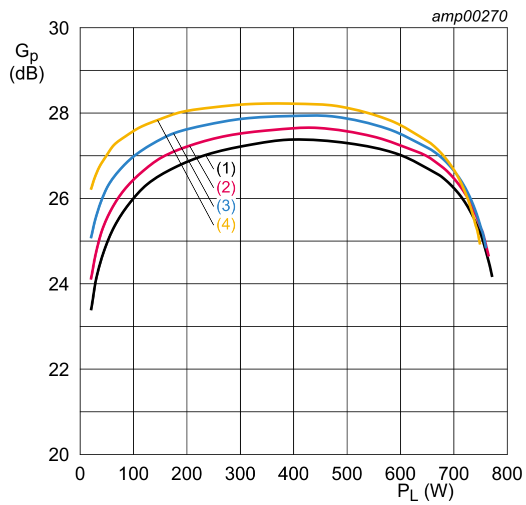



$V_{DS}$ = 50 V; $I_{Dq}$ = 100 mA; f = 108 MHz; $t_p$ = 100 μs; δ = 20 %.

(1) $P_{L(1dB)}$ = 58.4 dBm (692 W)

(2) $P_{L(3dB)}$ = 58.8 dBm (765 W)

**Fig 6. Output power as a function of input power; typical values**




$V_{DS}$ = 50 V; f = 108 MHz; $t_p$ = 100 μs; δ = 20 %.

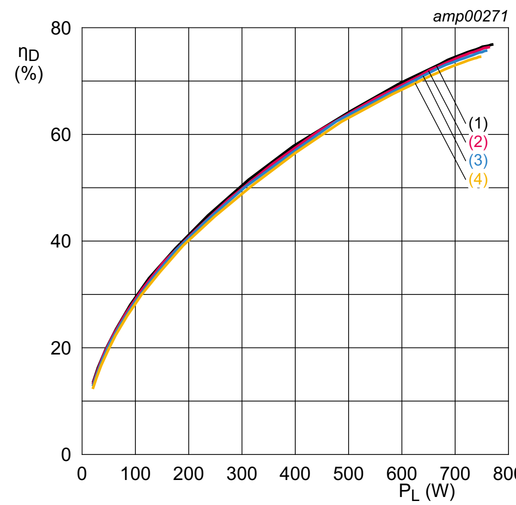
(1) $I_{Dq}$ = 50 mA

(2) $I_{Dq}$ = 100 mA

(3) $I_{Dq}$ = 200 mA

(4) $I_{Dq}$ = 400 mA

**Fig 7. Power gain as a function of output power; typical values**




$V_{DS}$ = 50 V; f = 108MHz; $t_p$ = 100 μs; δ = 20 %.

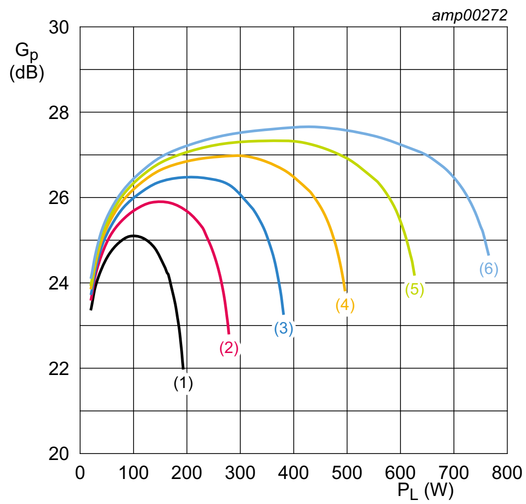
(1) $I_{Dq}$ = 50 mA

(2) $I_{Dq}$ = 100 mA

(3) $I_{Dq}$ = 200 mA

(4) $I_{Dq}$ = 400 mA

**Fig 8. Drain efficiency as a function of output power; typical values**




$I_{Dq}$ = 100 mA; f = 108 MHz; $t_p$ = 100 μs; δ = 20 %.

(1) $V_{DS}$ = 25 V

(2) $V_{DS}$ = 30 V

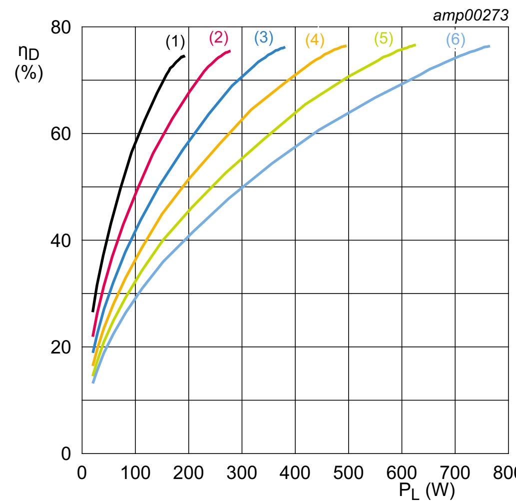
(3) $V_{DS}$ = 35 V

(4) $V_{DS}$ = 40 V

(5) $V_{DS}$ = 45 V

(6) $V_{DS}$ = 50 V

**Fig 9. Power gain as a function of output power; typical values**




$I_{Dq}$ = 100 mA; f = 108 MHz; $t_p$ = 100 μs; δ = 20 %.

(1) $V_{DS}$ = 25 V

(2) $V_{DS}$ = 30 V

(3) $V_{DS}$ = 35 V

(4) $V_{DS}$ = 40 V

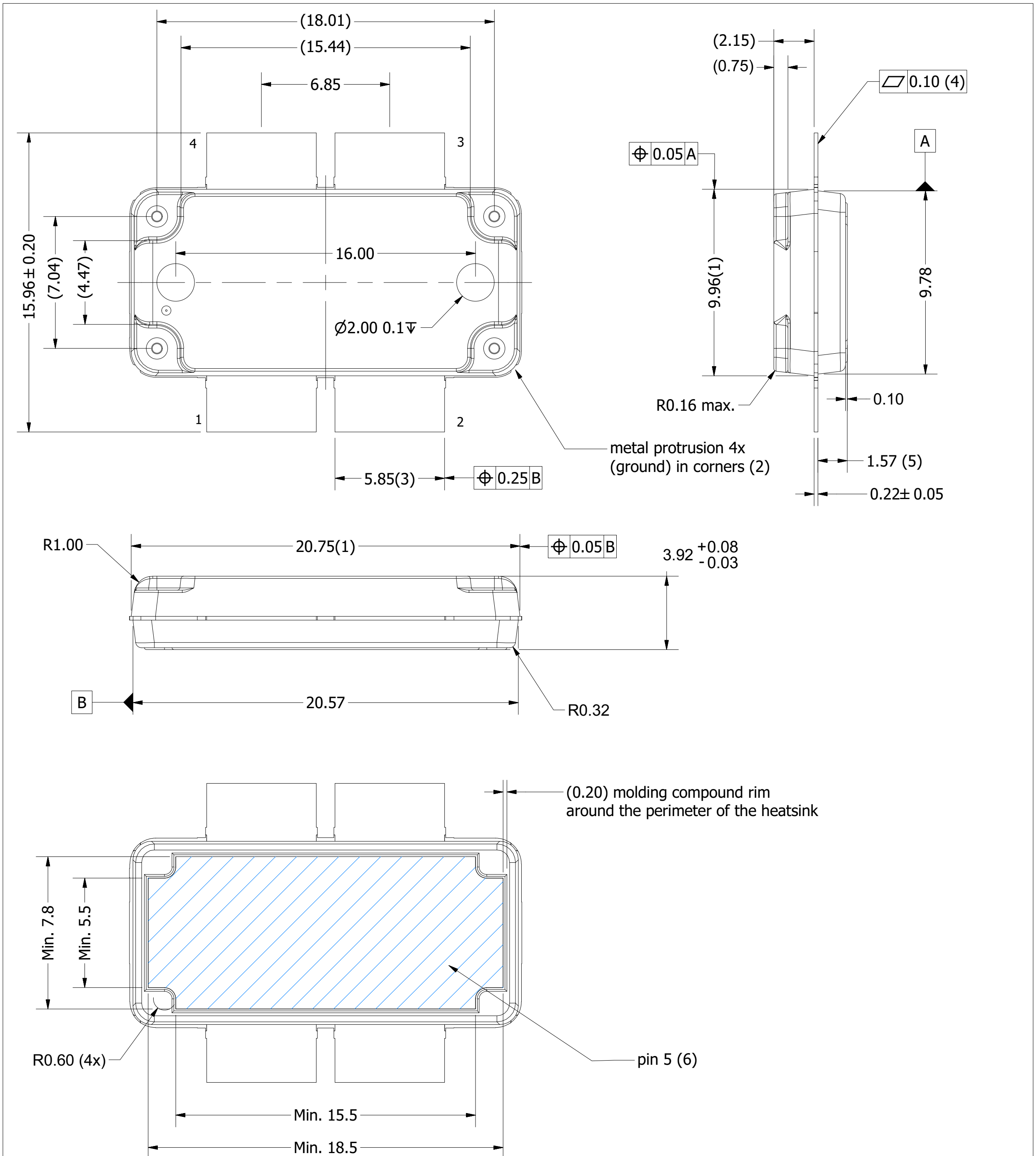
(5) $V_{DS}$ = 45 V

(6) $V_{DS}$ = 50 V

**Fig 10. Drain efficiency as a function of output power; typical values**

# 8. Package outline

SOT1138-3

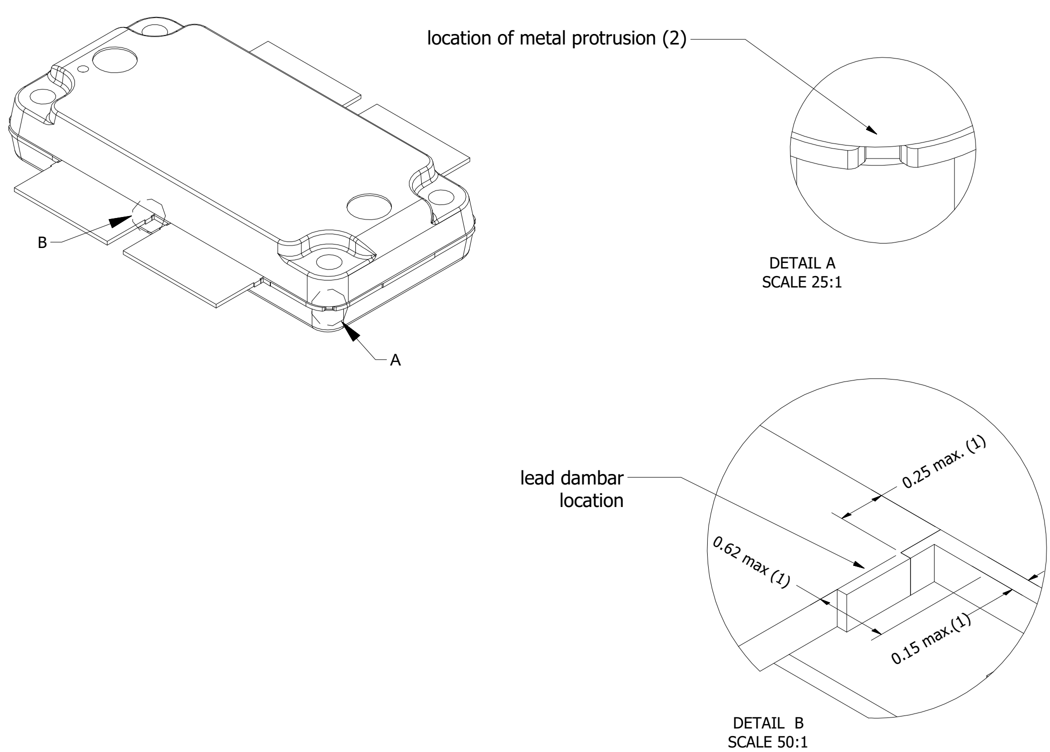



| | | | |
|---|---|---|---|
| Package outline drawing:<br><br>SOT1138-3 | units in mm. | Tolerances unless otherwise stated:<br>Dimension: ± 0.05 Angle: ± 1° | Revision: 1<br>Revision date: 7/26/2018 |
| | | Third angle projection | Sheet 1 of 2 |

**Fig 11. Package outline SOT1138-3 (sheet 1 of 2)**

SOT1138-3

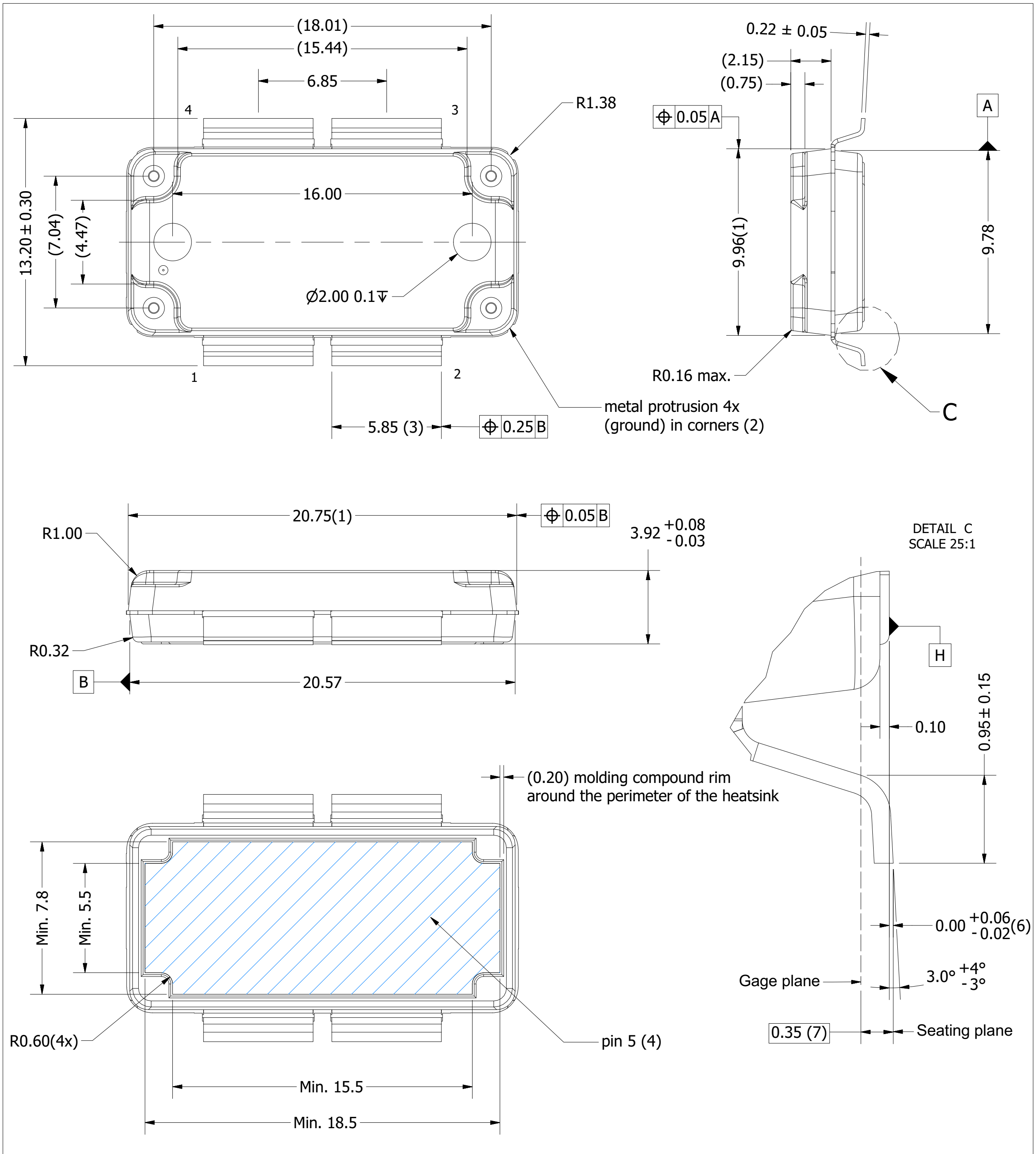
| Drawing Notes | |
|---|---|
| Items | Description |
| (1) | Dimensions are excluding mold protrusion. All areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and max. 0.62 mm in length.<br>At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B. |
| (2) | The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A). |
| (3) | The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location. |
| (4) | The lead coplanarity over all leads is 0.1 mm maximum. |
| (5) | Dimension is measured 0.5 mm from the edge of the top package body. |
| (6) | The hatched area indicates the exposed metal heatsink. |
| (7) | The leads and exposed heatsink are plated with matte Tin (Sn). |




| | | | |
|---|---|---|---|
| Package outline drawing:<br><br>SOT1138-3 | units in mm. | Tolerances unless otherwise stated:<br>Dimension: ± 0.05 Angle: ± 1° | Revision: 1<br>Revision date: 7/26/2018 |
| | | Third angle projection | Sheet 2 of 2 |

**Fig 12. Package outline SOT1138-3 (sheet 2 of 2)**

SOT1204-3

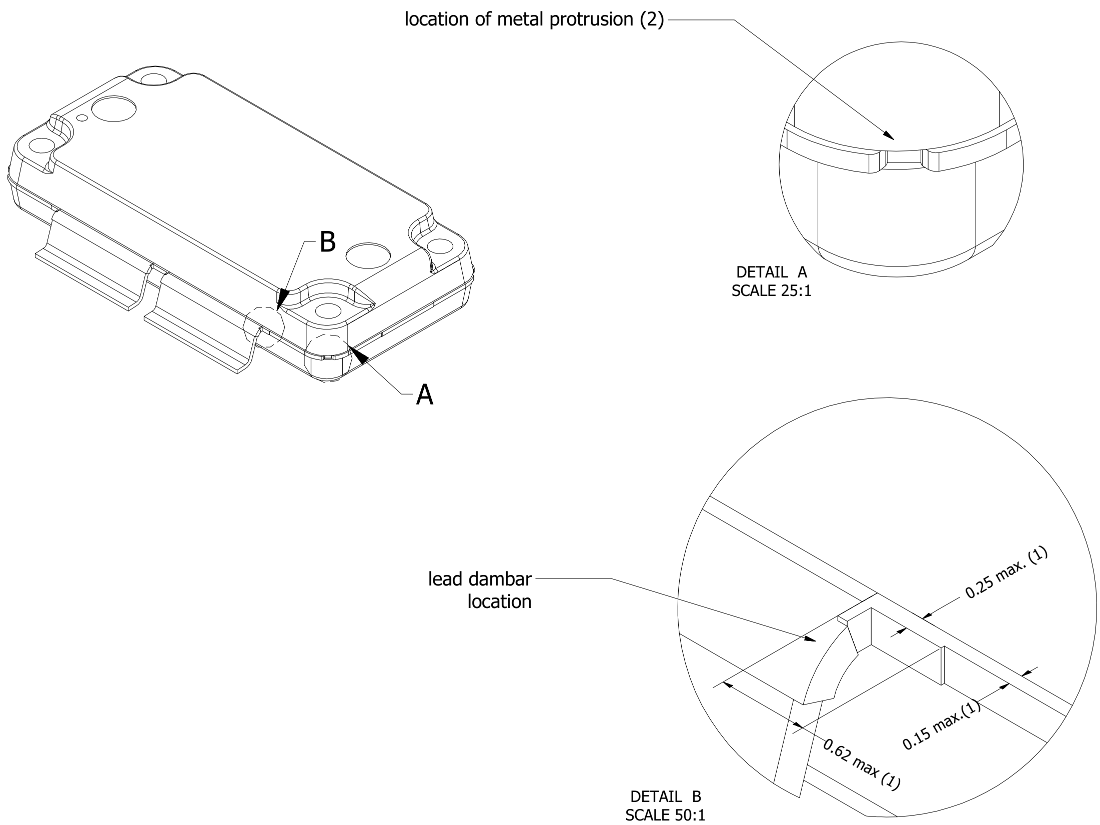



| | | | |
|---|---|---|---|
| Package outline drawing:<br>SOT1204-3 | units in mm. | Tolerances unless otherwise stated:<br>Dimension: ± 0.05 Angle: ± 1° | Revision: 1<br>Revision date: 7/26/2018 |
| | | Third angle projection | Sheet 1 of 2 |

**Fig 13. Package outline SOT1204-3 (sheet 1 of 2)**

SOT1204-3

| Drawing Notes | |
|---|---|
| Items | Description |
| (1) | Dimensions are excluding mold protrusion. All areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and 0.62 mm max. in length.<br>At other areas the mold protrusion is maximum 0.15 mm per side. See also detail B. |
| (2) | The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A). |
| (3) | The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location. |
| (4) | The hatched area indicated the exposed heatsink. |
| (5) | The leads and exposed heatsink are plated with matte Tin (Sn). |
| (6) | Dimension is measured with respect to the bottom of the heatsink Datum H. Positive value means that the bottom of the heatsink is higher than the bottom of the lead. |
| (7) | Gage plane (foot length) to be measured from the seating plane. |




| Package outline drawing: SOT1204-3 | units in mm. | Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1° | Revision: 1<br>Revision date: 7/26/2018 |
|---|---|---|---|
| | | Third angle projection | Sheet 2 of 2 |

**Fig 14. Package outline SOT1204-3 (sheet 2 of 2)**

## 9. Handling information

**CAUTION**

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 11. ESD sensitivity**

| ESD model | Class |
|---|---|
| Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002 | C2A [1] |
| Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001 | 2 [2] |

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

## 10. Abbreviations

**Table 12. Abbreviations**

| Acronym | Description |
|---|---|
| ESD | ElectroStatic Discharge |
| HF | High Frequency |
| LDMOS | Laterally Diffused Metal-Oxide Semiconductor |
| MTF | Median Time to Failure |
| SMD | Surface Mounted Device |
| RoHS | Restriction of Hazardous Substances |
| VSWR | Voltage Standing Wave Ratio |

## 11. Revision history

**Table 13. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BLP05H6700XR_H6700XRG v.2 | 20180913 | Product data sheet | - | BLP05H6700XR_H6700XRG v.1 |
| Modifications | • Table 2 on page 2: package outline versions changed to SOT1138-3 and SOT1204-3<br>• Table 3 on page 2: package outline versions changed to SOT1138-3 and SOT1204-3<br>• Figure 4 on page 6: figure updated<br>• Section 8 on page 9: package outline versions changed from SOT1138-2 and SOT1204-2 to SOT1138-3 and SOT1204-3 | | | |
| BLP05H6700XR_H6700XRG v.1 | 20170217 | Product data sheet | - | - |

# 12. Legal information

## 12.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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