PCN Number:	20220208002.0**A**	PCN Date:	**June 29, 2022**
Title:	TPS6594-Q1 Firmware and Datasheet change		
Customer Contact:	PCN Manager	**Dept:**	Quality Services

Change Type:					
☐	Assembly Site	☐	Assembly Process	☐	Assembly Materials
☒	Design	☒	Electrical Specification	☐	Mechanical Specification
☐	Test Site	☐	Packing/Shipping/Labeling	☐	Test Process
☐	Wafer Bump Site	☐	Wafer Bump Material	☐	Wafer Bump Process
☐	Wafer Fab Site	☐	Wafer Fab Materials	☐	Wafer Fab Process
		☐	Part number change		

PCN Details

Description of Change:

This purpose of this Revision A is to communicate that there is a firmware change for the TPS65941213RWERQ1 (in addition to previously communicated datasheet change). Changes associated with this PCN addendum are bolded and in yellow highlight.

This notification is to communicate and update to the NVM configuration for the TPS6594-Q1 family of devices. Affected devices are listed in the Product Affected section of this document.

The change is to extend voltage monitoring (VMON) masking time after Analog Built-In Self-Test (ABIST). The Register value in the datasheet, NVM_CODE_2, is changing from 10b to 11b.

In addition to the above changes, the TPS65941213RWERQ1 also includes updates to the static NVM settings to allow to the device to be fully compliant with the setting states in User's Guides SLVUC99A Optimized TPS65941213-Q1 and TPS65941111-Q1 PMIC User Guide for J721E, PDN-0C (Rev. A) and SLVUCF3, TPS65941213-Q1 and LP876411B4-Q1 PMIC User Guide for J721E, PDN-1A. The settings updated to be compliant to the User's Guides are:

- ***BUCK3 VMON threshold setting update from +-5% to +-10% limit***
- ***BUCK3 VMON activation time adjustment from slightly after release of nRSTOUT to SoC to before release of NRSTOUT to SOC***
- ***LPM_EN-bit default value change from 1 to 0***
- ***LBIST execution as part of BOOT BIST***

The product datasheet(s) is being updated as summarized below.

Changes from Revision A (April 2021) to Revision B (February 2022) **Page**

- Section 8.8 Specifications - BUCK1, BUCK2, BUCK3, BUCK4 and BUCK5 Regulators: Change typical value for parameter 4.112 (from 300-mA to 420-mA), parameter 4.113 (from 200-mA to 100-mA), parameter 4.122 (from 250-mA to 370-mA), parameter 4.123 (from 150-mA to 30-mA), parameter 4.131 (from 400-mA to 310-mA), parameter 4.132 (from 170-mA to 290-mA), parameter 4.133 (from 230-mA to 20-mA), parameter 4.151 (from 335-mA to 290-mA), parameter 4.152 (from 150-mA to 230-mA), parameter 4.153 (from 185-mA to 50-mA) 18
- Added description about OVGDRV - VSYSSENSE relation 47
- BUCK Regulator Overview: added Current Limit and Short-to-Ground Detection on SW_Bx pins 49
- Added section: BUCK Regulator Current Limit 58
- Added section: SW_Bx Short-to-Ground Detection 58

- Added LDO1, LDO2, LDO3 Current Limit description 61
- Added LDO4 Current Limit description 62
- Added note about unmasking the UV/OV right before the release of the nRSTOUT resp. nRSTOUT_SoC pins. 65
- Added note which explains the required voltage accuracy for external supply rails (including VCCA input supply) that are monitored by the TPS6594-Q1 in order to pass the ABIST 65
- Added explanation on how to use Voltage Monitors of unused BUCK and LDO regulators 65
- Corrected Watchdog Reference Answer Calculation figure 94
- Added note which explains necessary system-software steps for using RUNTIME_BIST 121
- Added BOOT_BIST and RUNTIME_BIST 121
- Changed all instances of legacy terminology into "controller" and "target", also in all sub-sections 146
- For I2C, changed all instances of legacy terminology into "controller" and "target". For SPI, changed all instances of legacy terminology into "controller" and "peripheral". For the CRC, changed all instances of legacy terminology into "CRC on received data (R_CRC)", and "CRC on transmitted data" (T_CRC). These changes also applies to all sub-sections. 154
- Corrected figure on Calculation of 8-Bit Controller CRC (R_CRC) Output, corrected figure on Calculation of 8-Bit Target CRC (T_CRC) Input 154
- Added note about missing R_CRC after am I2C write 157
- Added note which describes a device erratum related to COMM_FRM_ERR_INT bit 159
- Added note which explains the I^2C addresses for each register map page on the I^2C bus. Added note which explains how each register map page is addressed when using SPI. 161
- Added note about writing to RESERVED bits causing a Register Map CRC error 162
- Corrected description of register DEV_REV 163
- Updated PDN example figure, and updated the table with the Local and POL Capacitors used for Buck Use Case Validation 368
- Updated the recommendations for the Digital Signal Connections 371
- Updated Layout Guidelines with respect to output capacitor on VOUT_LDOVINT pin 383
- Updated Layout Example figure 385

The datasheet number will be changing.

	Current	New
Product Family	**Datasheet Number**	**Datasheet Number**
TPS6594-Q1	SLVSEA7A	SLVSEA7B

These changes may be reviewed at the datasheet links provided:
http://www.ti.com/product/TPS6594-Q1

Reason for Change:

Improved device functionality

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

None.

Product Affected:

Group 1 - Firmware and Datasheet updates:

TPS65941111RWERQ1	TPS65941212RWERQ1	**TPS65941213RWERQ1**

~~**Group 2 - Datasheet update only:**~~

~~TPS65941213RWERQ1~~

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
WW PCN Team	PCN_ww_admin_team@list.ti.com

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.