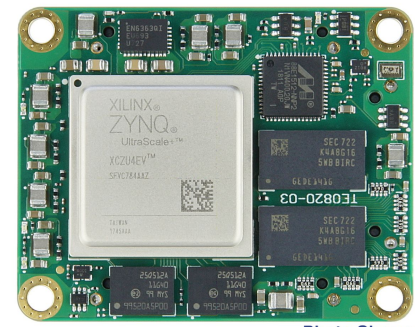
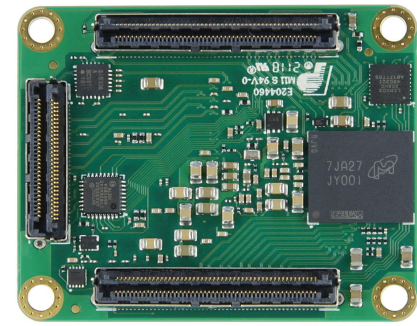


**Photo Shows Similar Product**



**Photo Shows Similar Product**



**Photo Shows Similar Product**

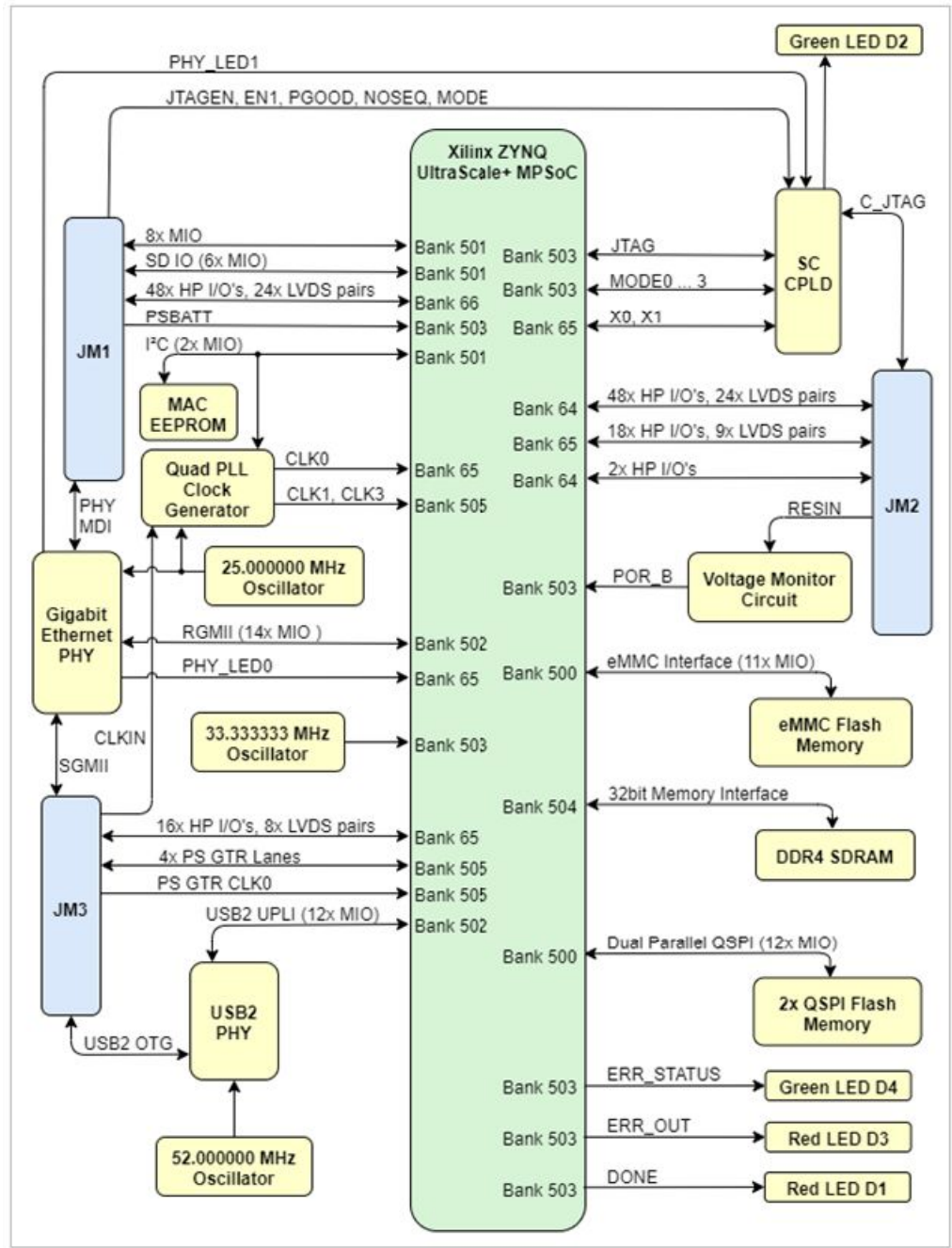
Regarding the usage of our schematics and alike documentation for Trenz module TE0820.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0820 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!



Title: <b>TE0820 - Legal Notices</b>		
A4	Number: <b>TE0820 2BI21FA</b>	Rev. <b>04</b>
Date: <b>2020-07-16</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>1</b> of <b>23</b>
Filename: <b>Legal Notices Modules.SchDoc</b>		



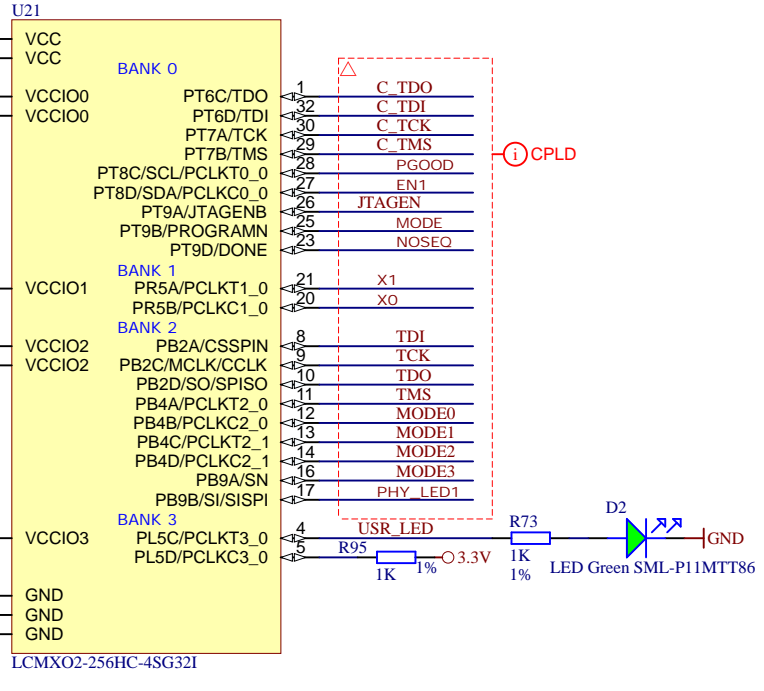
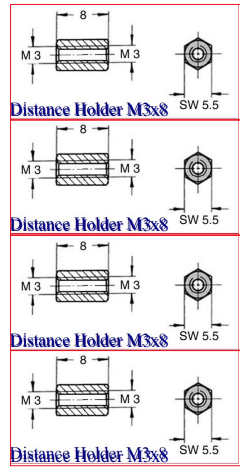
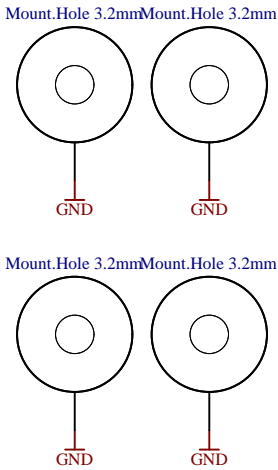
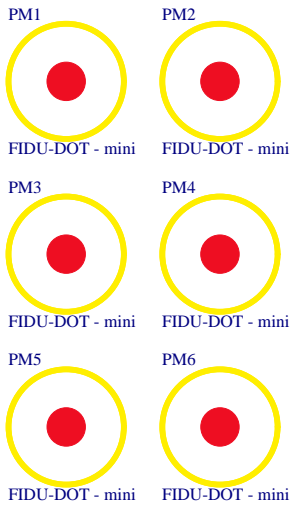
Title: TE0820 - System Overview		
A4	Number: TE0820 2BI21FA	Rev. 04
Date: 2020-10-20	Copyright: Trenz Electronic GmbH	Page 2 of 23
Filename: Overview.SchDoc		

U_USB-PHY USB-PHY.SchDoc
U_ETH-PHY ETH-PHY.SchDoc
U_B_HD B_HD.SchDoc
U_B64 B64.SchDoc
U_B65 B65.SchDoc
U_B66 B66.SchDoc
U_CONFIG CONFIG.SchDoc
U_B_MIO B_MIO.SchDoc
U_B_PS_GT B_PS_GT.SchDoc
U_CLK CLK.SchDoc
U_BD Overview.SchDoc

U_B2B-Connectors B2B-Connectors.SchDoc
U_eMMC eMMC.SchDoc
U_PS_DDR PS_DDR.SchDoc
U_ZU_POWER ZU_POWER.SchDoc
U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_DDR4-RAM_2 DDR4-RAM_2.SchDoc
U_DDR4-RAM DDR4-RAM.SchDoc
U_POWER POWER.SchDoc
U_POWER_1 POWER_1.SchDoc
U_REV_CH Revision Changes.SchDoc
U_LN Legal Notices Modules.SchDoc

Special notes:

Serial  
Serialnumber 6,3 x 6,3mm



Assembly variant	2BI21FA
Created by	VY
Modified by	VY
Modified at	2020-05-04
SVN Revision	12571



Title: TE0820		
A4	Number: TE0820 2BI21FA	Rev. 04
Date: 2020-07-16	Copyright: 2015 Trenz Electronic GmbH	Page 3 of 23
Filename: TE0820.SchDoc		

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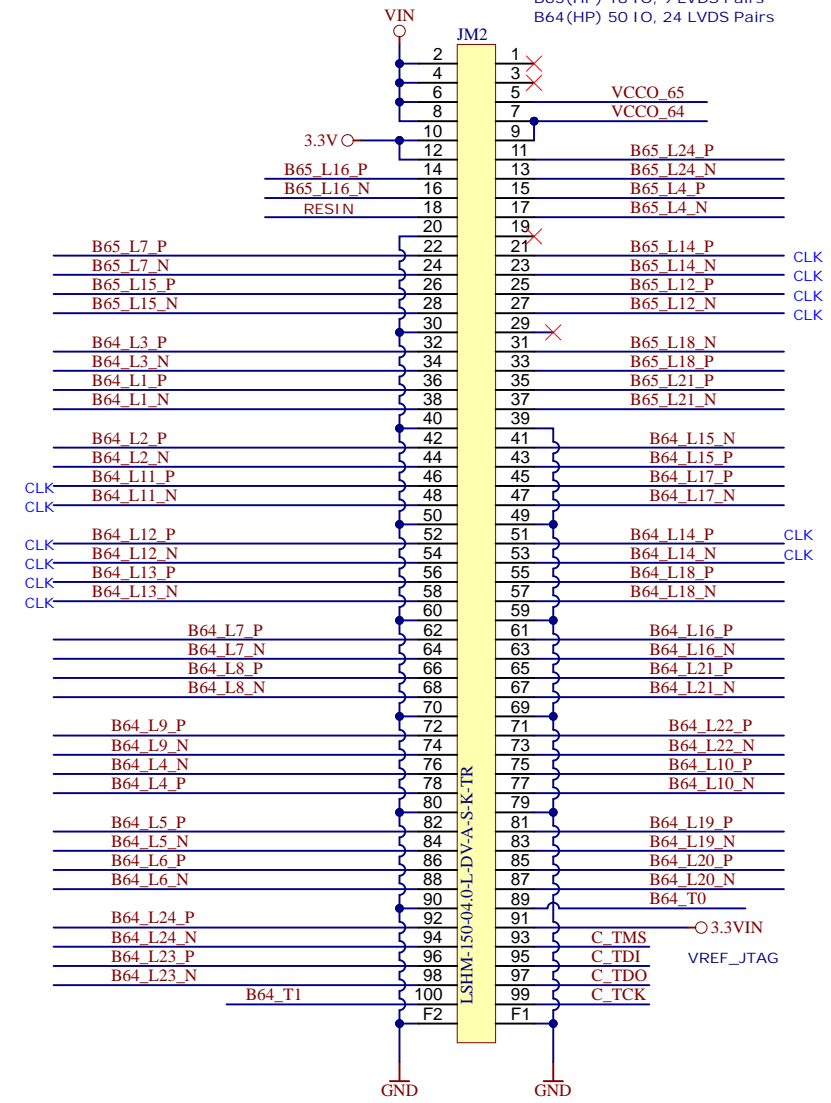
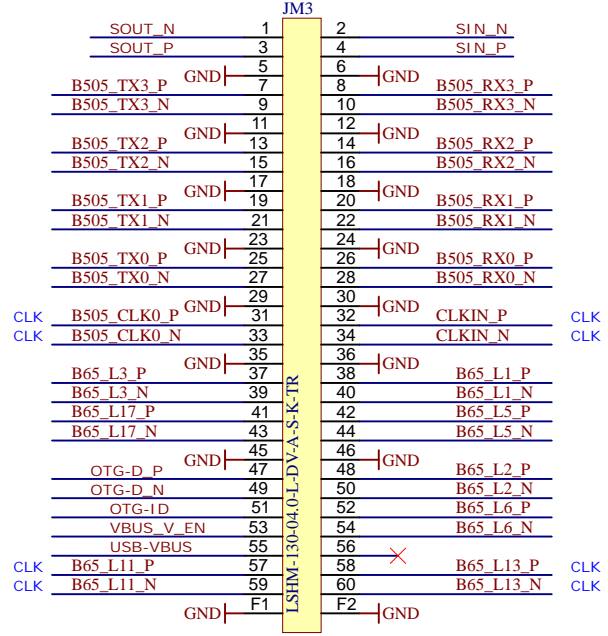
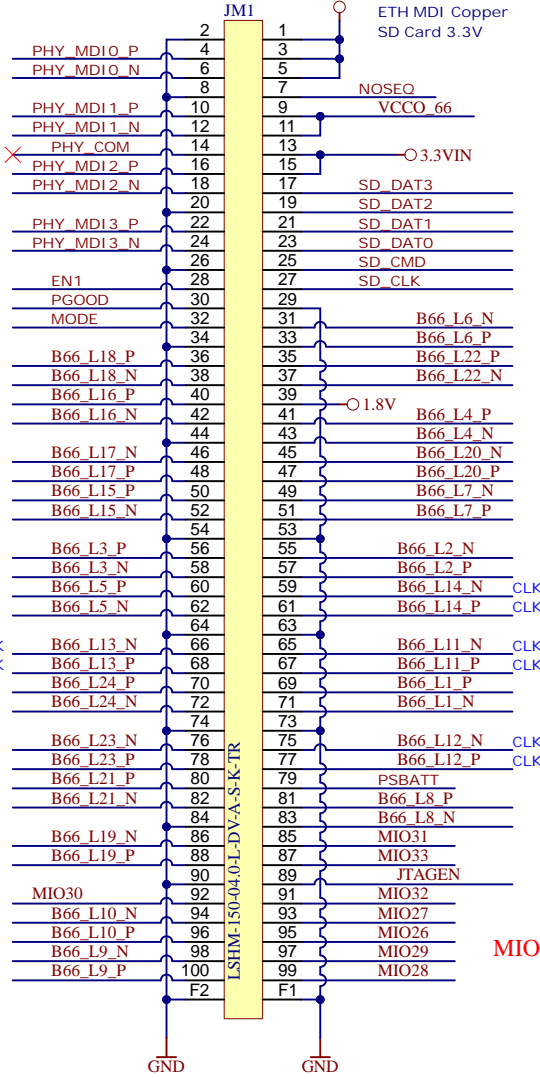
D

D

B66(HP) 48 IO, 24 LVDS Pairs  
 MIO501 8 IO, 3.3V  
 ETH MDI Copper  
 SD Card 3.3V

B65(HP) 16 IO, 8 LVDS Pairs  
 USB OTG  
 ETH SGMII  
 PS\_GTR 4 Lanes  
 PS\_GTR CLK IN  
 PLL CLK IN

B65(HP) 18 IO, 9 LVDS Pairs  
 B64(HP) 50 IO, 24 LVDS Pairs



VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1



Title: TE0820 - B2B Connectors		
A4	Number: TE0820 2BI21FA	Rev. 04
Date: 2020-07-16	Copyright: 2015 Trenz Electronic GmbH	Page4 of 23
Filename: B2B-Connectors.SchDoc		



UIC

<del>F14</del>	VCCO_26	BANK 26 HD (ZU4/5 BANK 46 HD)	
<del>C15</del>	VCCO_26		
<del>B15</del>	IO_L1P_AD11P_26	IO_L7P_HDGC_AD5P_26	<del>G13</del>
<del>A15</del>	IO_L1N_AD11N_26	IO_L7N_HDGC_AD5N_26	<del>F13</del>
<del>B14</del>	IO_L2P_AD10P_26	IO_L8P_HDGC_AD4P_26	<del>F15</del>
<del>A14</del>	IO_L2N_AD10N_26	IO_L8N_HDGC_AD4N_26	<del>E15</del>
<del>B13</del>	IO_L3P_AD9P_26	IO_L9P_AD3P_26	<del>G15</del>
<del>A13</del>	IO_L3N_AD9N_26	IO_L9N_AD3N_26	<del>G14</del>
<del>C14</del>	IO_L4P_AD8P_26	IO_L10P_AD2P_26	<del>H14</del>
<del>C13</del>	IO_L4N_AD8N_26	IO_L10N_AD2N_26	<del>H13</del>
<del>D15</del>	IO_L5P_HDGC_AD7P_26	IO_L11P_AD1P_26	<del>K14</del>
<del>D14</del>	IO_L5N_HDGC_AD7N_26	IO_L11N_AD1N_26	<del>J14</del>
<del>E14</del>	IO_L6P_HDGC_AD6P_26	IO_L12P_AD0P_26	<del>L14</del>
<del>E13</del>	IO_L6N_HDGC_AD6N_26	IO_L12N_AD0N_26	<del>L13</del>

BANK 44 HD (ZU4/5 BANK 43 HD)

<del>AC10</del>	VCCO_44		
<del>AG12</del>	VCCO_44		
<del>AG10</del>	IO_L1P_AD11P_44	IO_L7P_HDGC_AD5P_44	<del>AD11</del>
<del>AH10</del>	IO_L1N_AD11N_44	IO_L7N_HDGC_AD5N_44	<del>AD10</del>
<del>AF11</del>	IO_L2P_AD10P_44	IO_L8P_HDGC_AD4P_44	<del>AB11</del>
<del>AG11</del>	IO_L2N_AD10N_44	IO_L8N_HDGC_AD4N_44	<del>AC11</del>
<del>AH12</del>	IO_L3P_AD9P_44	IO_L9P_AD3P_44	<del>AA11</del>
<del>AH11</del>	IO_L3N_AD9N_44	IO_L9N_AD3N_44	<del>AA10</del>
<del>AE10</del>	IO_L4P_AD8P_44	IO_L10P_AD2P_44	<del>W10</del>
<del>AF10</del>	IO_L4N_AD8N_44	IO_L10N_AD2N_44	<del>Y10</del>
<del>AE12</del>	IO_L5P_HDGC_AD7P_44	IO_L11P_AD1P_44	<del>Y9</del>
<del>AF12</del>	IO_L5N_HDGC_AD7N_44	IO_L11N_AD1N_44	<del>AA8</del>
<del>AC13</del>	IO_L6P_HDGC_AD6P_44	IO_L12P_AD0P_44	<del>AB10</del>
<del>AD12</del>	IO_L6N_HDGC_AD6N_44	IO_L12N_AD0N_44	<del>AB9</del>

UIB


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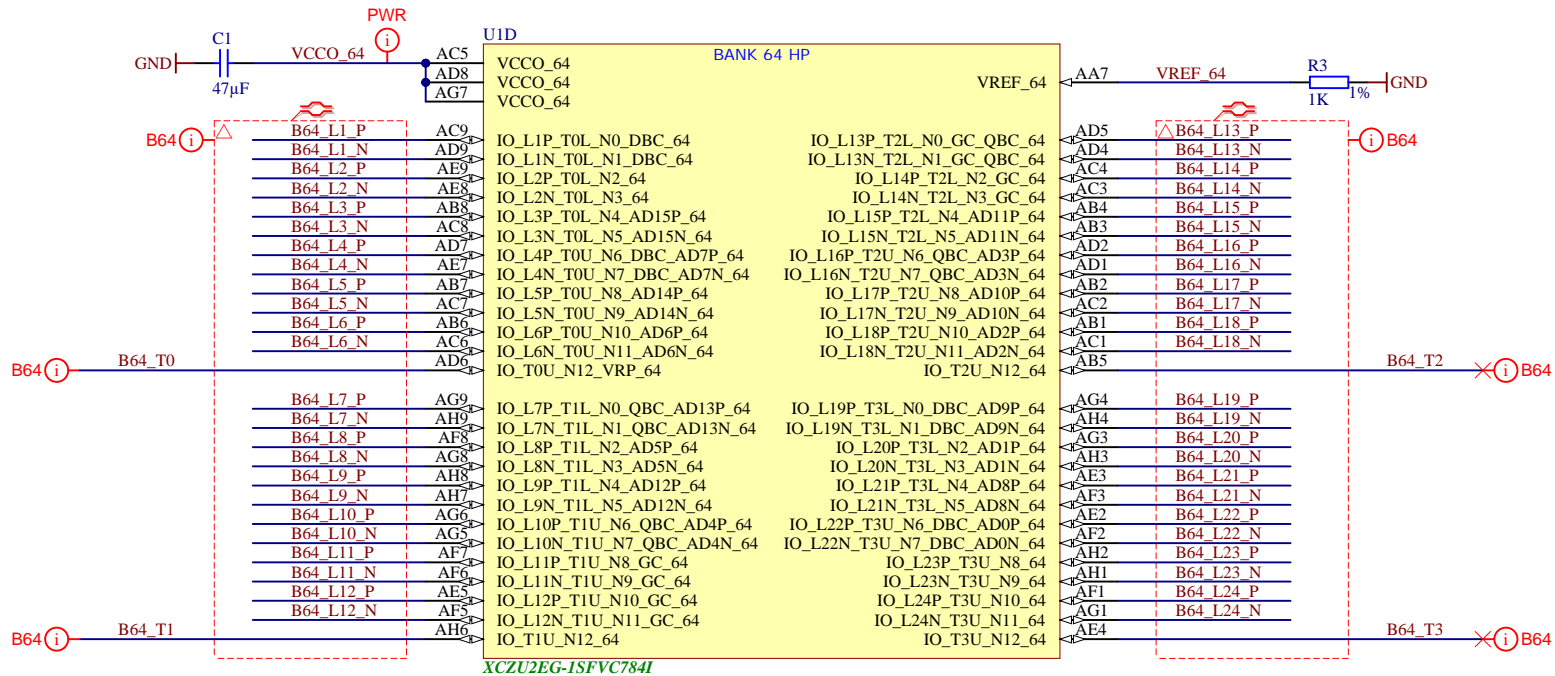
<del>AA14</del>	VCCO_24	BANK 24 HD (ZU4/5 BANK 44 HD)	
<del>AD13</del>	VCCO_24		
<del>AE15</del>	IO_L1P_AD15P_24	IO_L7P_HDGC_24	<del>AA13</del>
<del>AE14</del>	IO_L1N_AD15N_24	IO_L7N_HDGC_24	<del>AB13</del>
<del>AG14</del>	IO_L2P_AD14P_24	IO_L8P_HDGC_24	<del>AB15</del>
<del>AH14</del>	IO_L2N_AD14N_24	IO_L8N_HDGC_24	<del>AB14</del>
<del>AG13</del>	IO_L3P_AD13P_24	IO_L9P_AD11P_24	<del>W14</del>
<del>AH13</del>	IO_L3N_AD13N_24	IO_L9N_AD11N_24	<del>W13</del>
<del>AE13</del>	IO_L4P_AD12P_24	IO_L10P_AD10P_24	<del>Y14</del>
<del>AF13</del>	IO_L4N_AD12N_24	IO_L10N_AD10N_24	<del>Y13</del>
<del>AD13</del>	IO_L5P_HDGC_24	IO_L11P_AD9P_24	<del>W12</del>
<del>AD14</del>	IO_L5N_HDGC_24	IO_L11N_AD9N_24	<del>W11</del>
<del>AC14</del>	IO_L6P_HDGC_24	IO_L12P_AD8P_24	<del>Y12</del>
<del>AC13</del>	IO_L6N_HDGC_24	IO_L12N_AD8N_24	<del>AA12</del>

BANK 25 HD (ZU4/5 BANK 45 HD)

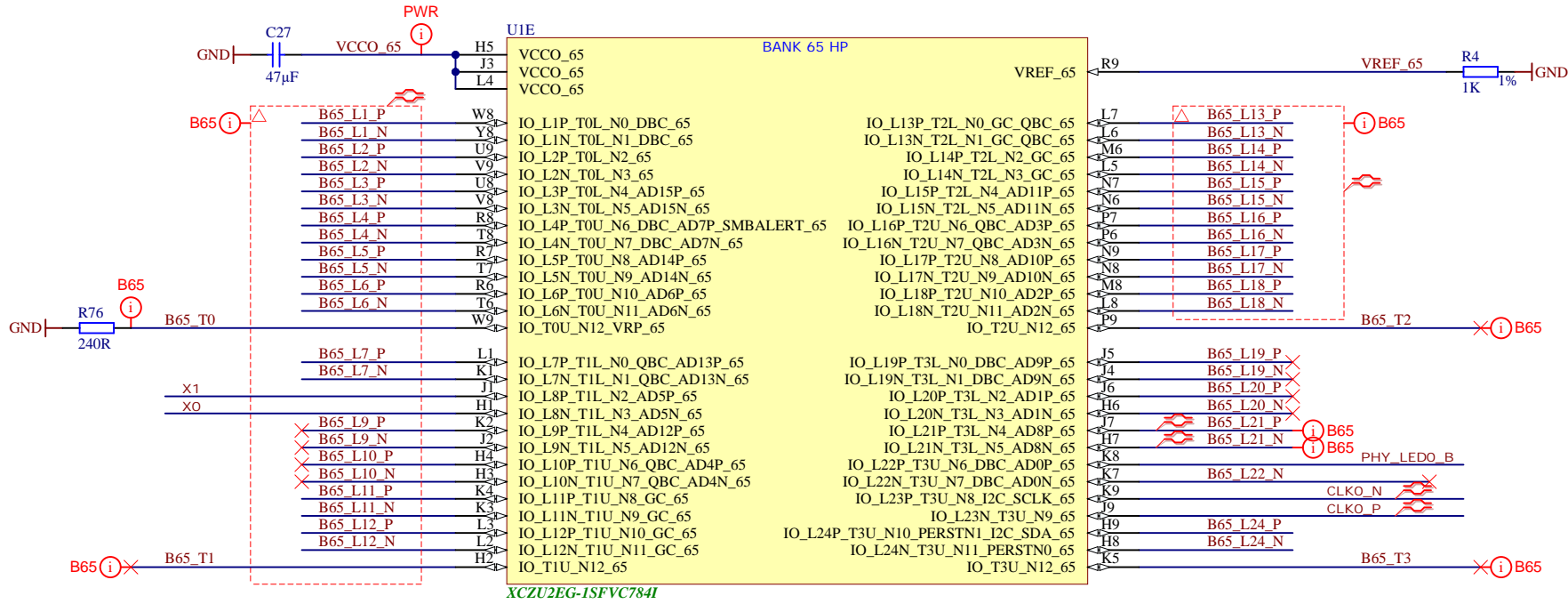
<del>B12</del>	VCCO_25		
<del>E11</del>	VCCO_25		
<del>J11</del>	IO_L1P_AD15P_25	IO_L7P_HDGC_25	<del>E10</del>
<del>J10</del>	IO_L1N_AD15N_25	IO_L7N_HDGC_25	<del>D10</del>
<del>K13</del>	IO_L2P_AD14P_25	IO_L8P_HDGC_25	<del>E12</del>
<del>K12</del>	IO_L2N_AD14N_25	IO_L8N_HDGC_25	<del>D11</del>
<del>H11</del>	IO_L3P_AD13P_25	IO_L9P_AD11P_25	<del>C11</del>
<del>G10</del>	IO_L3N_AD13N_25	IO_L9N_AD11N_25	<del>B10</del>
<del>J12</del>	IO_L4P_AD12P_25	IO_L10P_AD10P_25	<del>B11</del>
<del>H12</del>	IO_L4N_AD12N_25	IO_L10N_AD10N_25	<del>A10</del>
<del>G11</del>	IO_L5P_HDGC_25	IO_L11P_AD9P_25	<del>A12</del>
<del>F13</del>	IO_L5N_HDGC_25	IO_L11N_AD9N_25	<del>A11</del>
<del>F12</del>	IO_L6P_HDGC_25	IO_L12P_AD8P_25	<del>D12</del>
<del>F11</del>	IO_L6N_HDGC_25	IO_L12N_AD8N_25	<del>C12</del>

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	Title: TE0820 - HD Banks		
	A4	Number: TE0820 2BI21FA	Rev. 04
	Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page6 of 23
	Filename: B_HD.SchDoc		

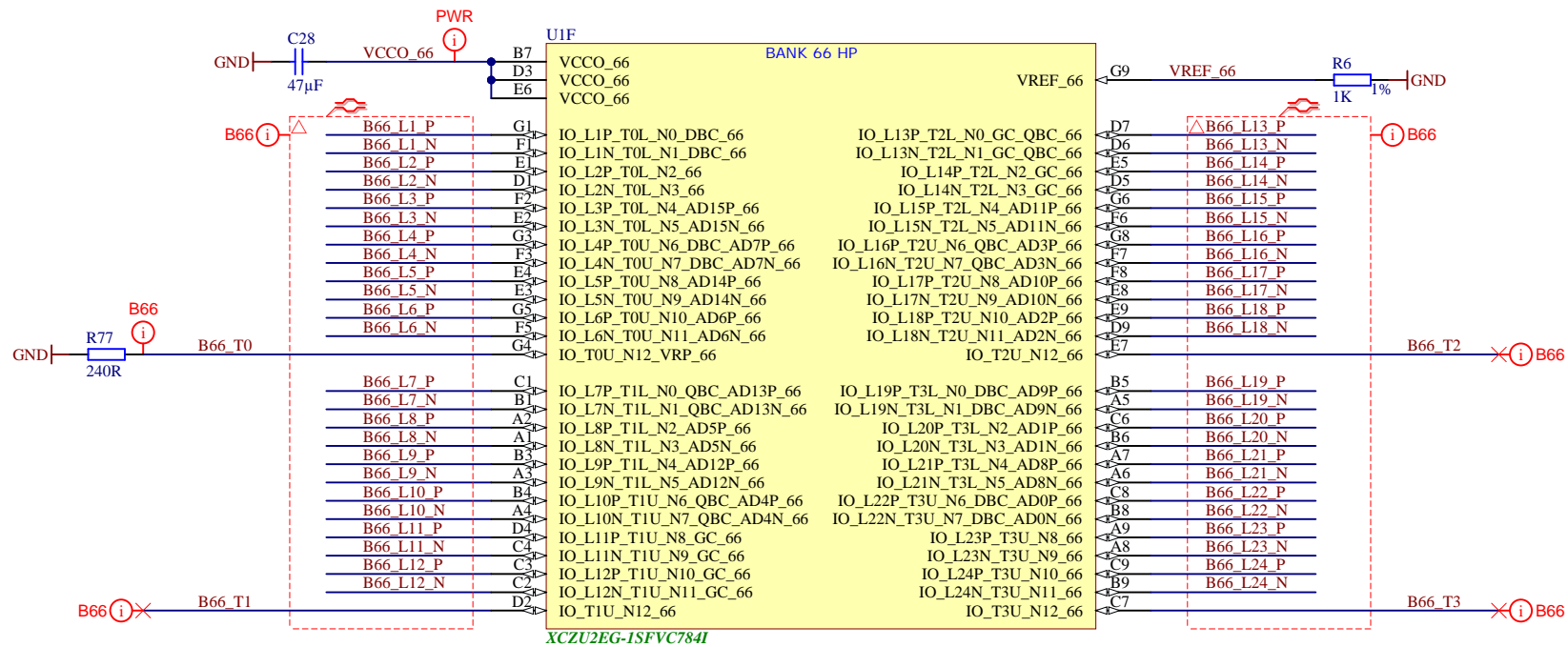


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Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 7 of 23
Filename: B64.SchDoc		

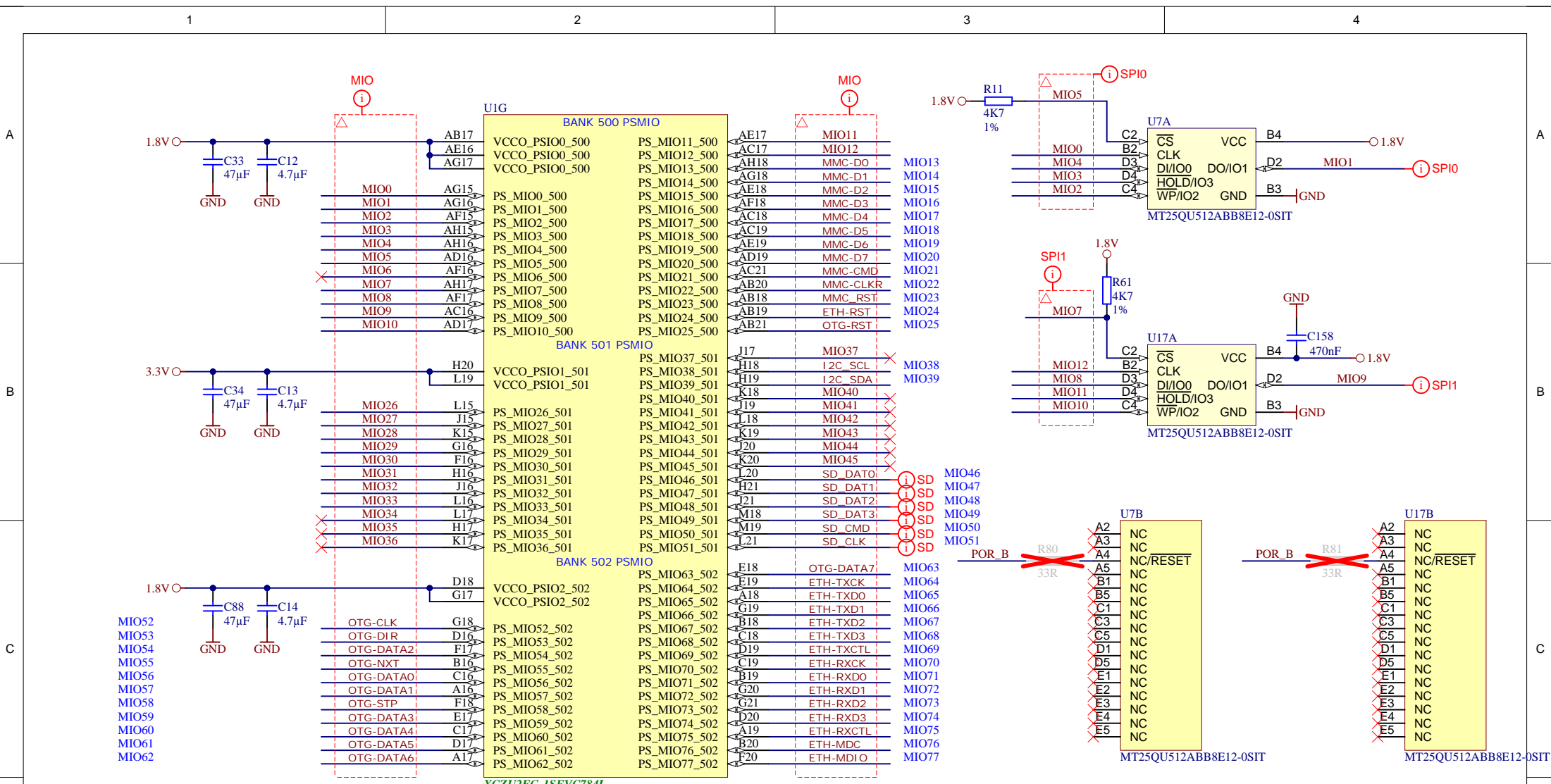


Title: TE0820 - B65		
A4	Number: TE0820 2BI21FA	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 8 of 23
Filename: B65.SchDoc		





Title: TE0820 - B66		
A4	Number: TE0820 2BI21FA	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page9 of 23
Filename: B66.SchDoc		



			Title: <b>TE0820 - MIO Banks</b>	
			A4	Number: <b>TE0820 2BI21FA</b>
Date: 2020-07-16		Copyright: Trenz Electronic GmbH / TT		Page 10 of 23
Filename: <b>B_MIO.SchDoc</b>				

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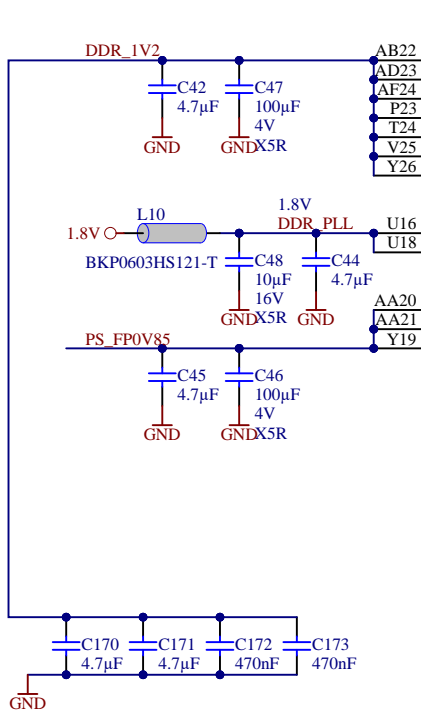
D

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U1I		BANK 504 PSDDR	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0 P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0 N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AA22	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AB23	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AA25	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AA26	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AB25	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AB26	DDR4-A13
VCC_PSDDR_PLL	PS_DDR_A14_504	AB24	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A15_504	AC24	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A16_504	AC23	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A17_504	AC22	DDR4-A17
VCC_PSINTFP_DDR	PS_DDR_CS_N0_504	W27	DDR4-CS
VCC_PSINTFP_DDR	PS_DDR_CS_N1_504	V26	
VCC_PSINTFP_DDR	PS_DDR_BA0_504	V23	DDR4-BA0
VCC_PSINTFP_DDR	PS_DDR_BA1_504	W22	DDR4-BA1
VCC_PSINTFP_DDR	PS_DDR_BG0_504	W24	DDR4-BG0
VCC_PSINTFP_DDR	PS_DDR_BG1_504	V22	DDR4-BG1
VCC_PSINTFP_DDR	PS_DDR_PARITY_504	V24	DDR4-PAR
VCC_PSINTFP_DDR	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET
VCC_PSINTFP_DDR	PS_DDR_ACT_N_504	Y23	DDR4-ACT
VCC_PSINTFP_DDR	PS_DDR_ALERT_N_504	U25	DDR4-ALERT
VCC_PSINTFP_DDR	PS_DDR_ZQ_504	U24	
VCC_PSINTFP_DDR	PS_DDR_ODT0_504	U28	DDR4-ODT0
VCC_PSINTFP_DDR	PS_DDR_ODT1_504	U26	

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U1J		BANK 504 PSDDR	
DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504
DDR4-DQS0 P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504
DDR4-DQS0 N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504
DDR4-DQS1 P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504
DDR4-DQS1 N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504
DDR4-DQS2 P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504
DDR4-DQS2 N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504
DDR4-DQS3 P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504
DDR4-DQS3 N	AE27	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504
	N23	PS_DDR_DQS_P4_504	PS_DDR_DM0_504
	M23	PS_DDR_DQS_N4_504	PS_DDR_DM1_504
	L23	PS_DDR_DQS_P5_504	PS_DDR_DM2_504
	K23	PS_DDR_DQS_N5_504	PS_DDR_DM3_504
	N26	PS_DDR_DQS_P6_504	PS_DDR_DM4_504
	N27	PS_DDR_DQS_N6_504	PS_DDR_DM5_504
	J26	PS_DDR_DQS_P7_504	PS_DDR_DM6_504
	J27	PS_DDR_DQS_N7_504	PS_DDR_DM7_504
	R27	PS_DDR_DQS_P8_504	PS_DDR_DM8_504
	T27	PS_DDR_DQS_N8_504	

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Title: TE0820 - PS_DDR		
A4	Number: TE0820 2BI21FA	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 11 of 23
Filename: PS_DDR.SchDoc		

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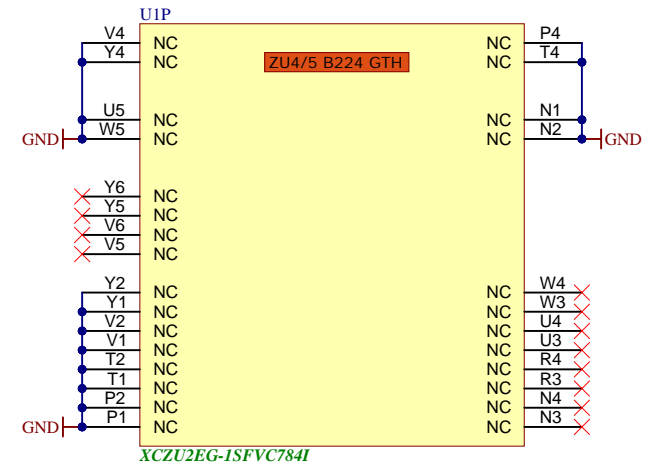
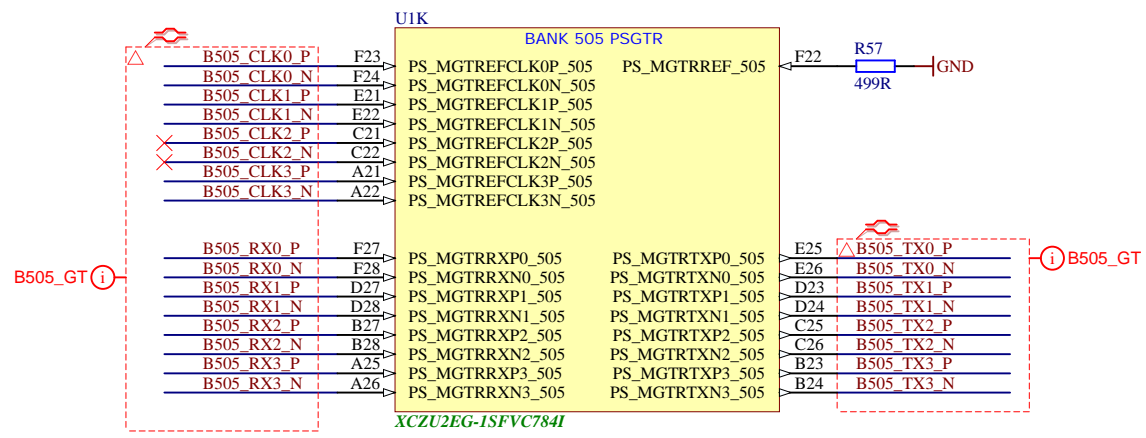

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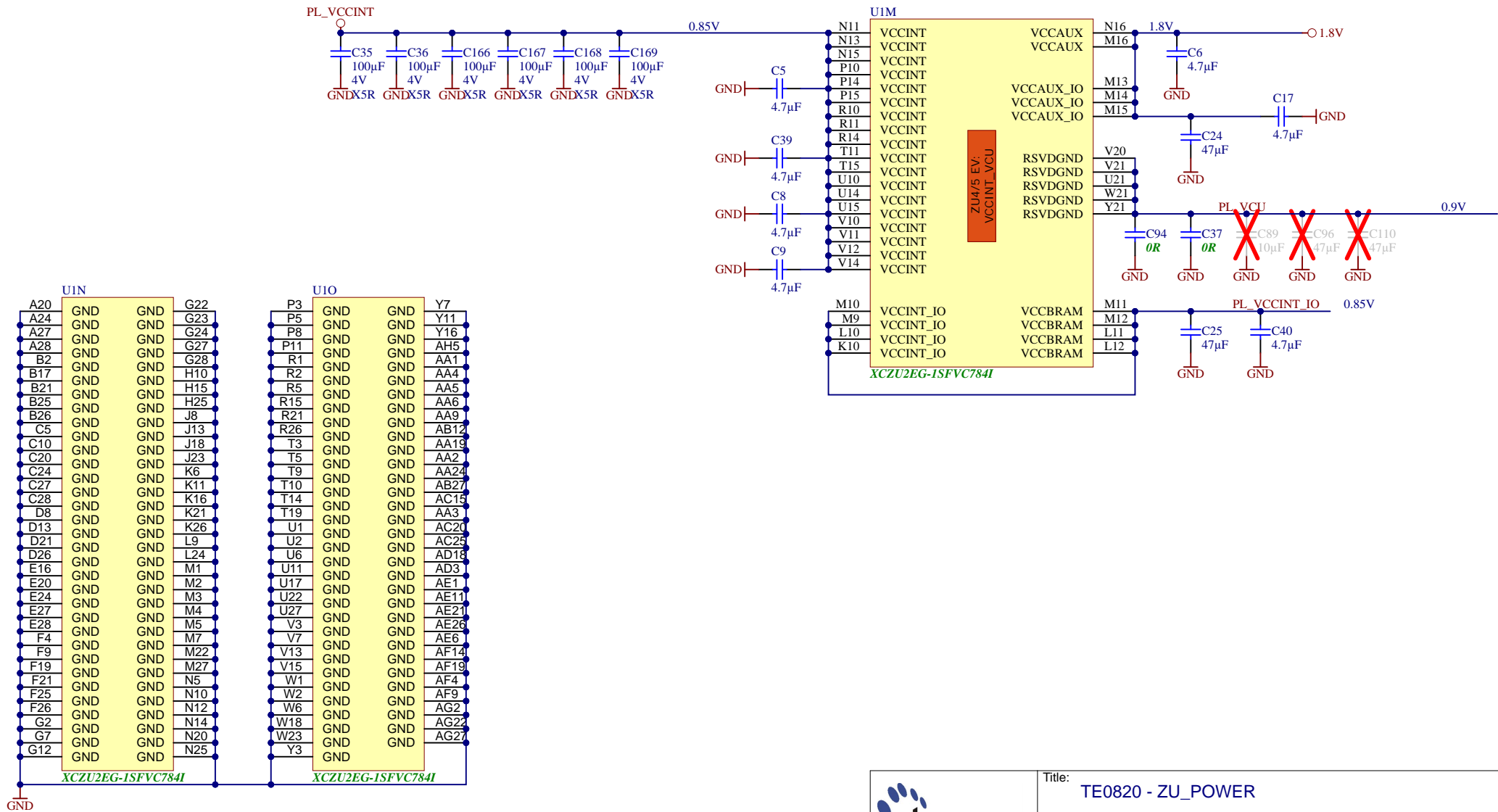
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A4	Number: TE0820 2BI21FA	Rev. 04
Date: 2020-07-16	Copyright: Trenz Electronic GmbH / TT	Page 12 of 23
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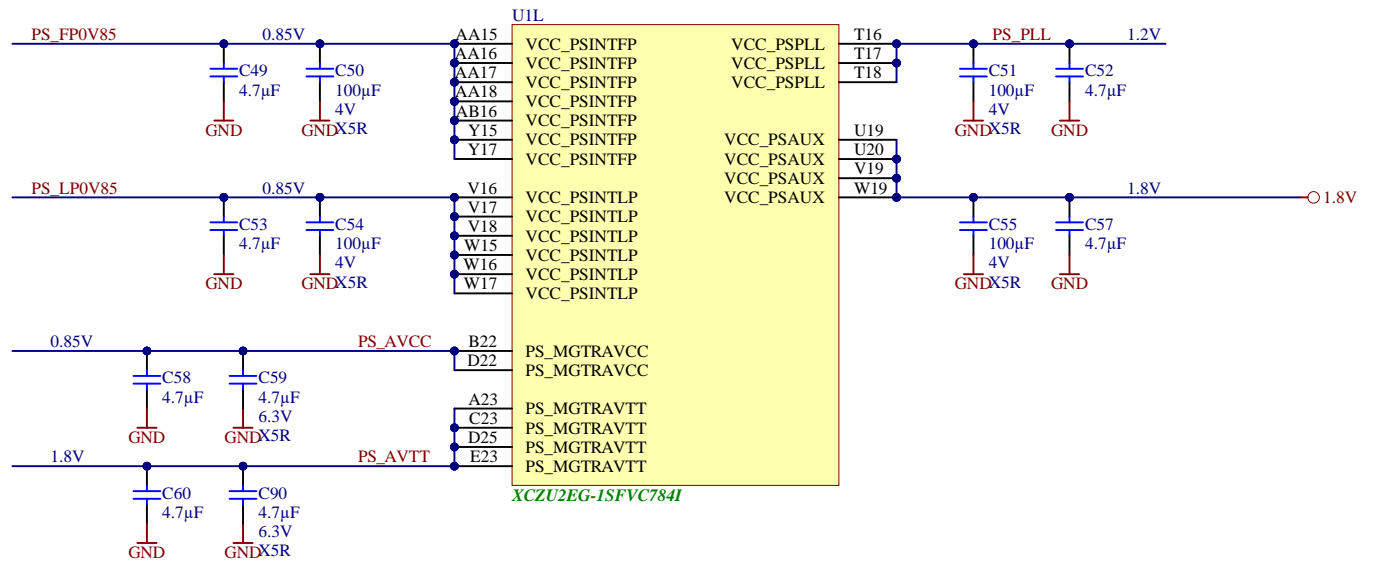
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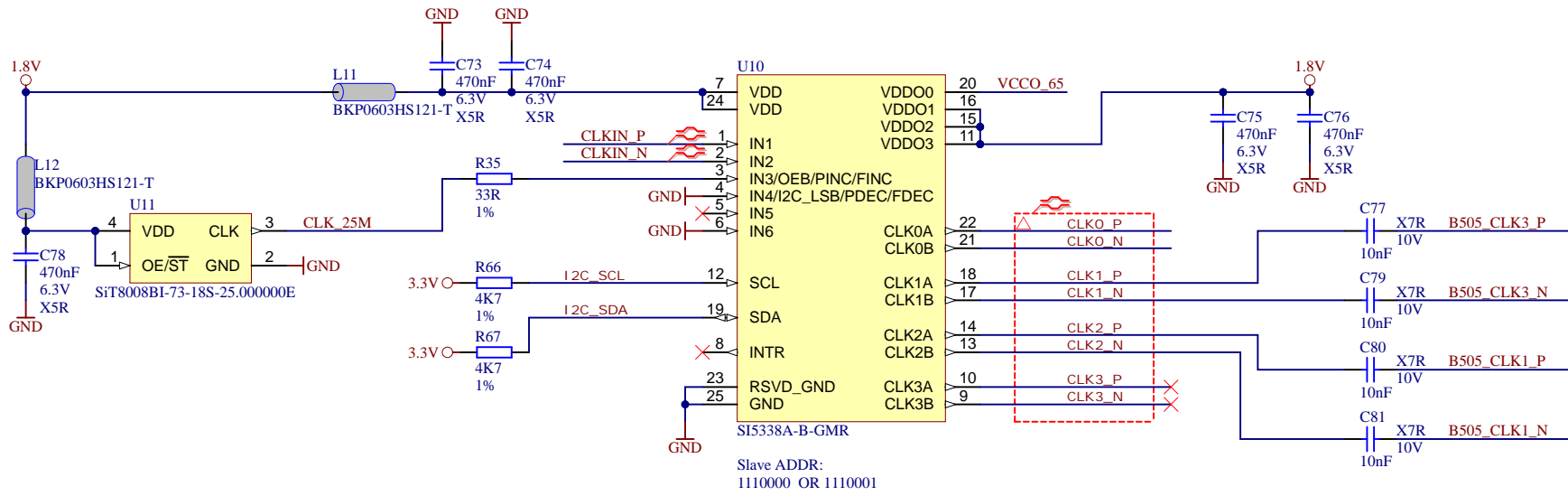
U1N				U1O				Y7			
A20	GND	GND	G22	P3	GND	GND	Y11				
A24	GND	GND	G23	P5	GND	GND	Y16				
A27	GND	GND	G24	P8	GND	GND					
A28	GND	GND	G27	P11	GND	GND	AH5				
B2	GND	GND	G28	R1	GND	GND	AA1				
B17	GND	GND	H10	R2	GND	GND	AA4				
B21	GND	GND	H15	R5	GND	GND	AA5				
B25	GND	GND	H25	R15	GND	GND	AA6				
B26	GND	GND	J8	R21	GND	GND	AA9				
C5	GND	GND	J13	R26	GND	GND	AB12				
C10	GND	GND	J18	T3	GND	GND	AA19				
C20	GND	GND	J23	T5	GND	GND	AA2				
C24	GND	GND	K6	T9	GND	GND	AA24				
C27	GND	GND	K11	T10	GND	GND	AB27				
C28	GND	GND	K16	T14	GND	GND	AC15				
D8	GND	GND	K21	T19	GND	GND	AA3				
D13	GND	GND	K26	U1	GND	GND	AC20				
D21	GND	GND	L9	U2	GND	GND	AC25				
D26	GND	GND	L24	U6	GND	GND	AD18				
E16	GND	GND	M1	U11	GND	GND	AD3				
E20	GND	GND	M2	U17	GND	GND	AE1				
E24	GND	GND	M3	U22	GND	GND	AE11				
E27	GND	GND	M4	U27	GND	GND	AE21				
E28	GND	GND	M5	V3	GND	GND	AE26				
F4	GND	GND	M7	V7	GND	GND	AE6				
F9	GND	GND	M22	V13	GND	GND	AF14				
F19	GND	GND	M27	V15	GND	GND	AF19				
F21	GND	GND	N5	W1	GND	GND	AF4				
F25	GND	GND	N10	W2	GND	GND	AF9				
F26	GND	GND	N12	W6	GND	GND	AG2				
G2	GND	GND	N14	W18	GND	GND	AG22				
G7	GND	GND	N20	W23	GND	GND	AG27				
G12	GND	GND	N25	Y3	GND	GND					




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A

B

C

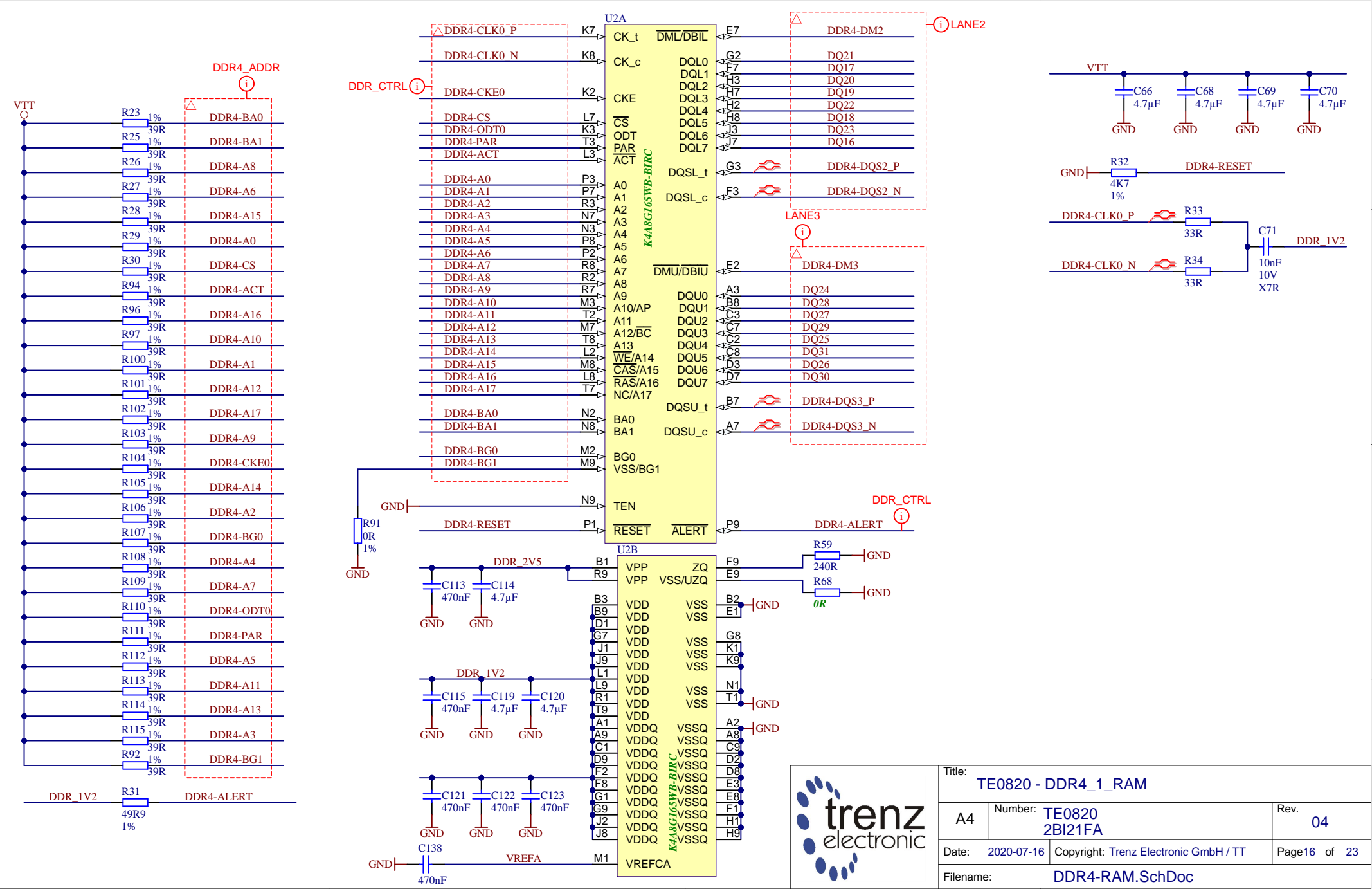
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A

B

C

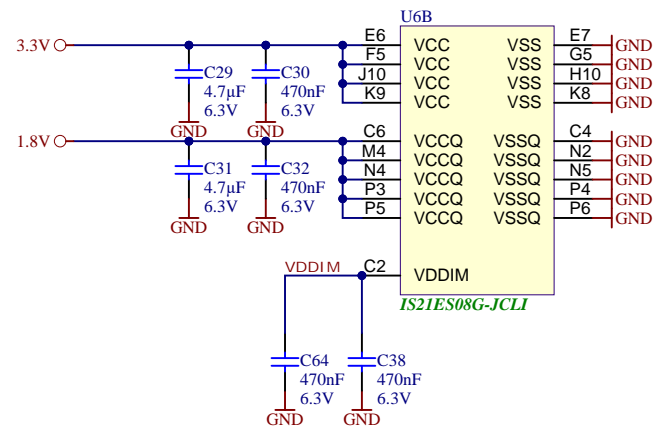
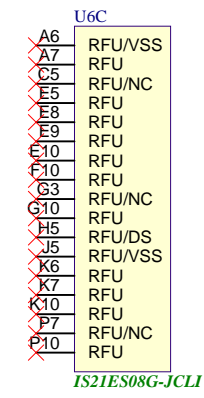
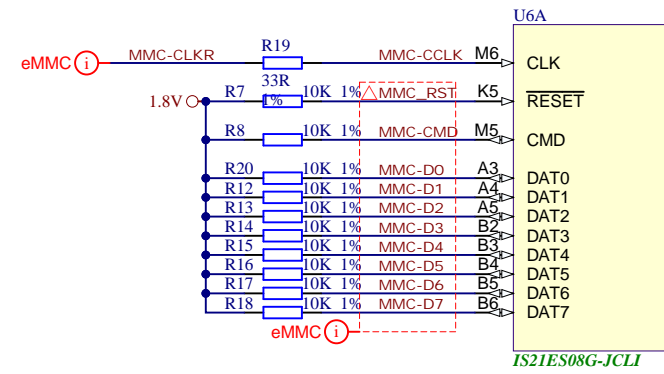
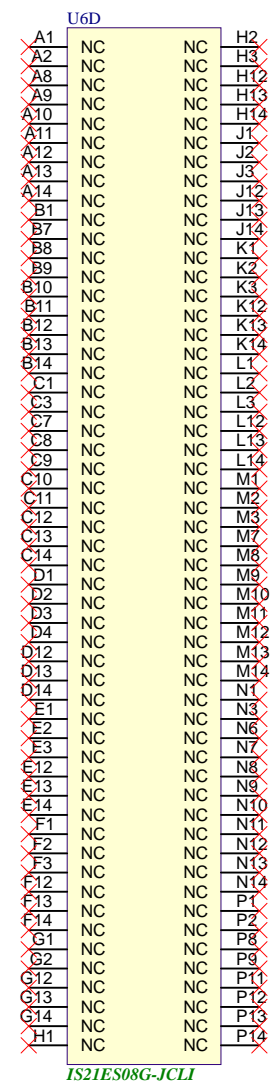
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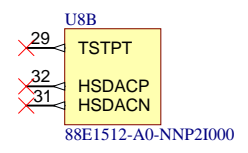
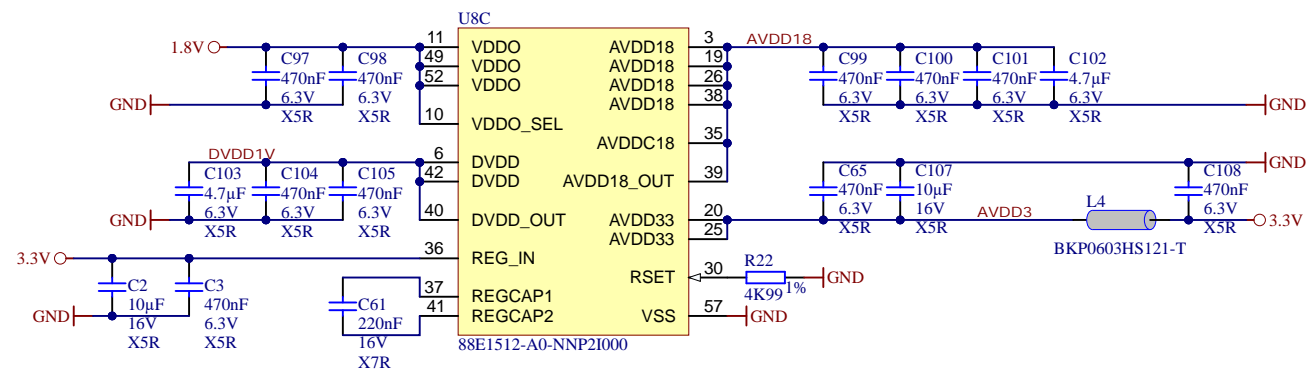
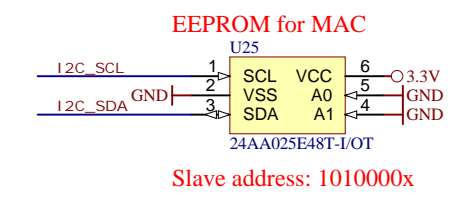
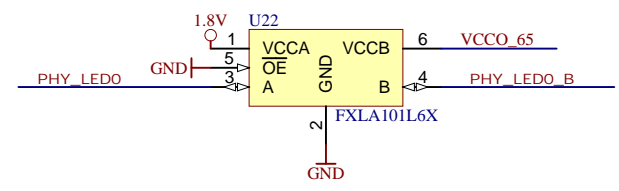
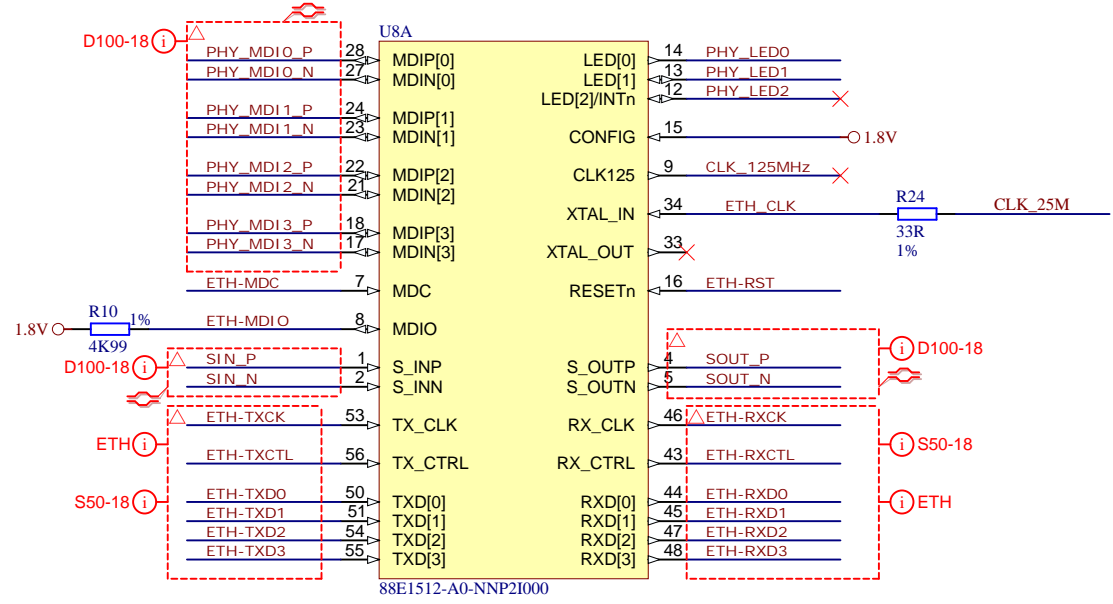
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A4	Number: TE0820 2BI21FA	Rev. 04
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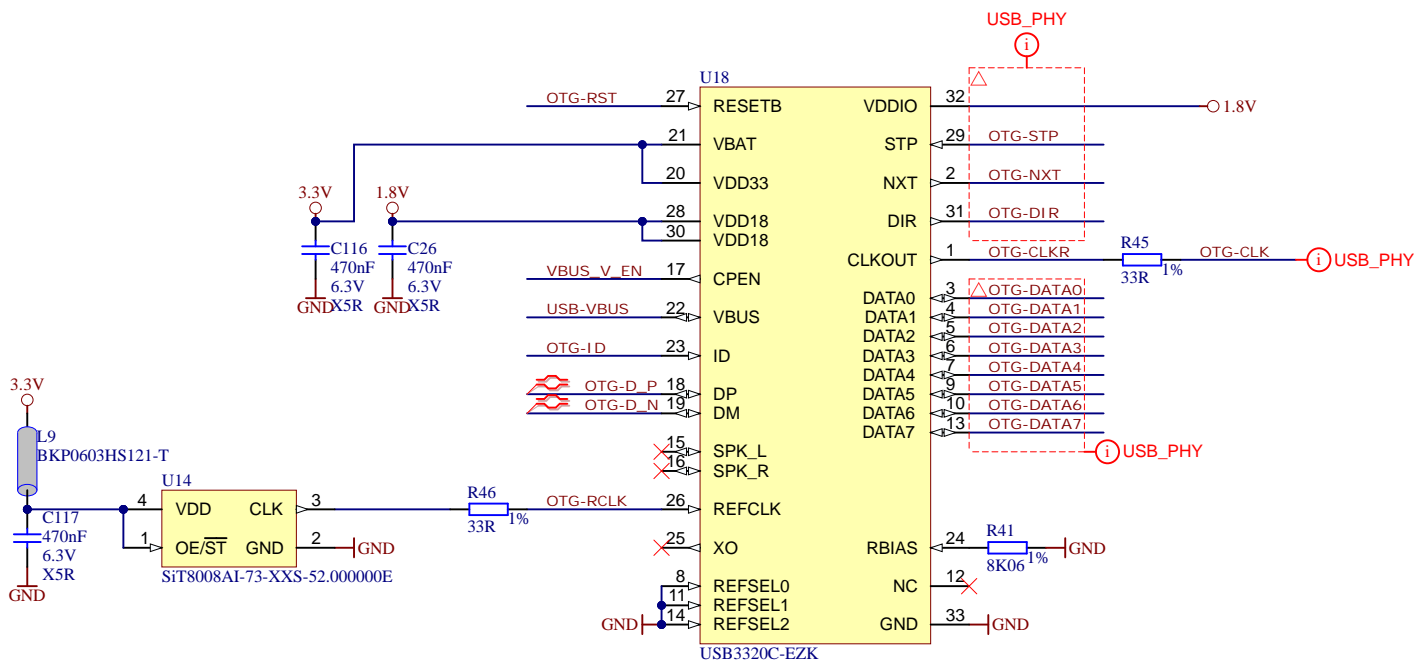




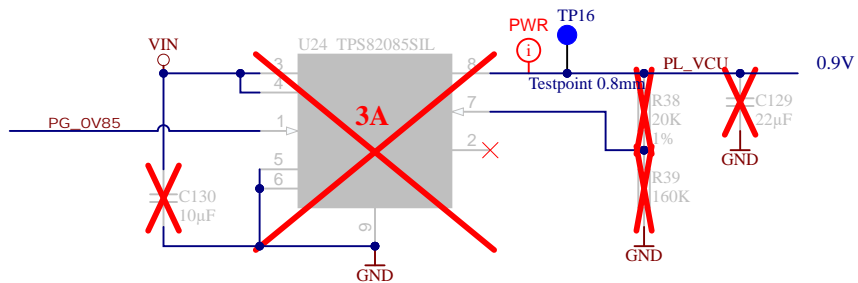
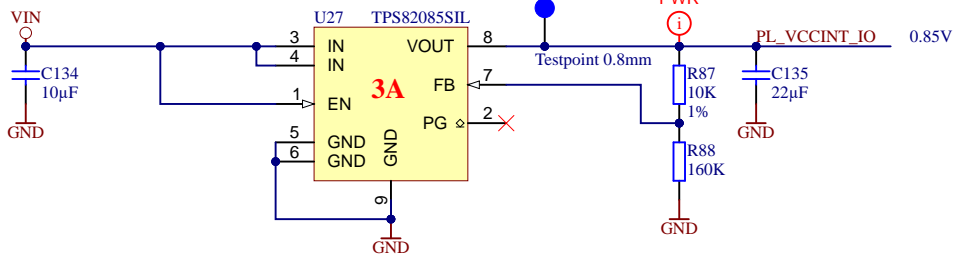
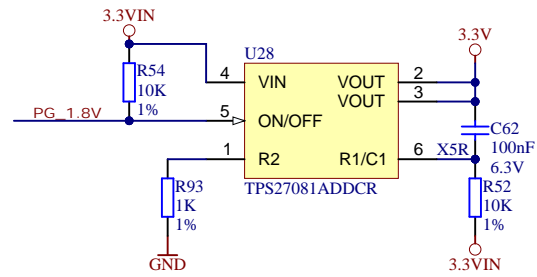
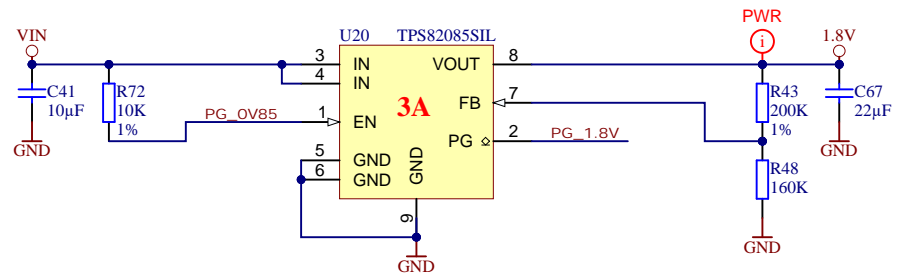
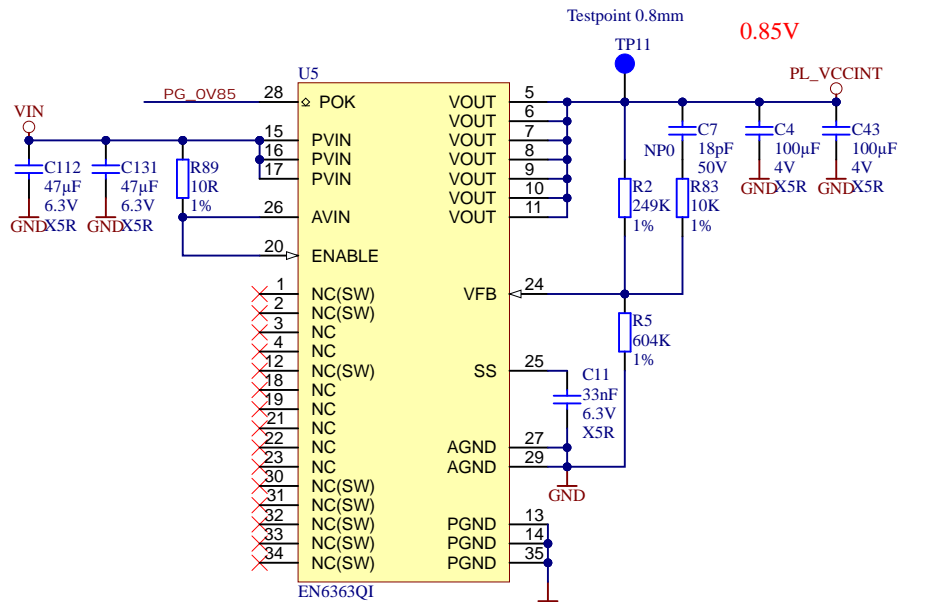
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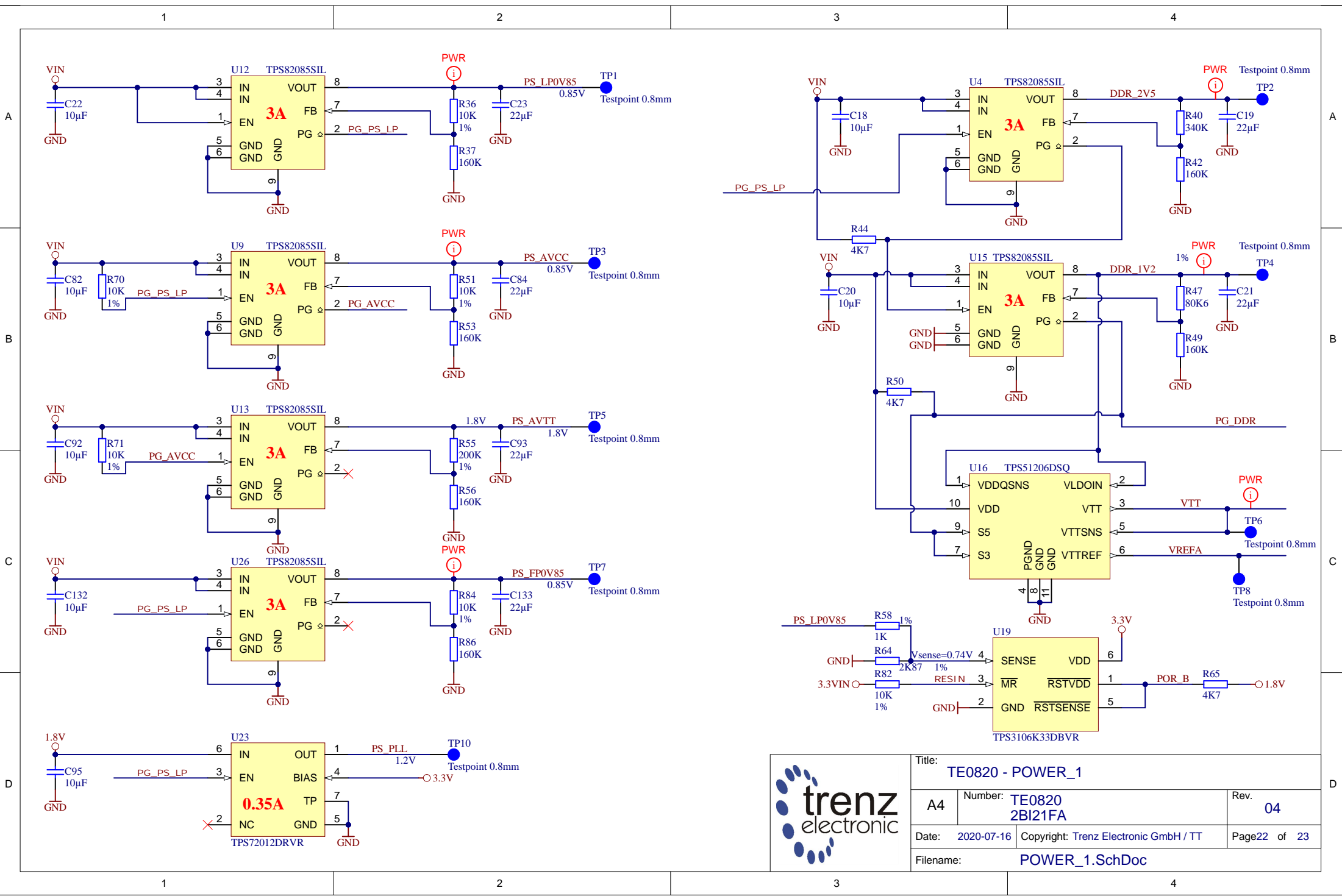
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CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

CHANGES REV02 to REV03


- 1) Fixed VCU connection: add additional DCDC (0.9V)
- 2) LIB components update
- 3) Change package 1K resistors (0402 -> 0201)
- 4) Added LEDs (1x user LED, 1x LED for ERR\_STATUS, 1xLED for ERR\_OUT)
- 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
- 6) Added additional DCDCs (PL\_VCCINT\_IO, PS\_FP0V85)
- 7) Changed DCDC (U5) 6A (optional 4A)

CHANGES REV03 to REV04

- VT: 1) Fixed DDR4 connection (BG1), support B-die DDR4 Industrial grade chips
- VT: 2) Added R93, changed value C62, change obsolete U28
- VT: 3) Added R89 (10R)
- VT: 4) Added additional caps 4.7uF to PS\_AVTT/PS\_AVCC (Xilinx doc UG583)
- VT: 5) Changed R51 20k ->10K (PS\_AVCC = 0.85V, Xilinx doc DS925 v1.17)
- VT: 6) Fixed DDR4 connection (Alert)
- VT: 7) Added 3.3V signal to CPLD
- VT: 8) Added testpoints
- VT: 9) LIB components update

Revision 04a (29.10.2020):

- 1. VY: added block diagram, updated module pictures

		Title: <b>TE0820 - Revision Changes</b>		
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