EVBUM2274/D

KAI-2001/KAI-2020 Image Sensors Evaluation Timing Specification

12-bit 20 MHz AFE

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EVAL BOARD USER'S MANUAL

Altera Code Version Description

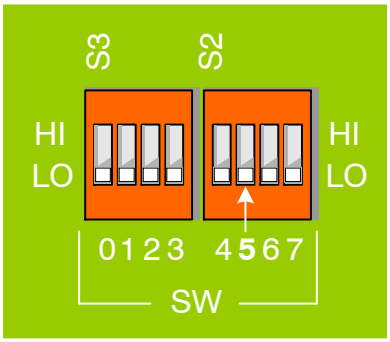
The Altera code described in this document is intended for use in the KSC−1000 Timing Board. The code is developed specifically for use with the following system configuration:

Table 1. SYSTEM CONFIGURATION

Evaluation Board Kit	PN 4H0705
Timing Generator Board	PN 3F5051 (AD9845A 20 MHz)
KAI−2001/KAI−2020 CCD Imager Board	PN 3F5121
Framegrabber Board	National Instruments Model PCI−1424

Special User Note: SW5 Device Select

This Evaluation Board Kit and Altera code support both the KAI−2001 and KAI−2020 Image Sensors. Since the two devices are virtually identical, they use identical timing. For this Evaluation Board Kit, the only relevant difference between the two devices is the Saturation Output Voltage, which requires adjusting the AFE gain settings in the AD9845A. The default AFE gain settings are selected by setting Timing Board dipswitch SW5 appropriately, to the HIGH position for the KAI−2001 device, and to the LOW position for the KAI−2020 device. The user is responsible for selecting the correct position for the device being used. See Figure 1, Table 9, and References.



SW5 HI = KAI−2001
SW5 LO = KAI−2020

Figure 1. Timing Board Configuration Switches

ALTERA CODE FEATURES/FUNCTIONS

The Altera Programmable Logic Device (PLD) serves as a state machine, which performs a variety of functions. Three basic functions are required, common to all CCD image sensor configurations: serial input steering, AFE default programming, and KSC−1000 default programming. In addition, certain other functions specific to the KAI−2001/KAI−2020 Image Sensors are implemented.

Serial Input Steering

The 3-wire serial interface enters the Timing Board through the DIO Interface connector, and is routed to the PLD. The Altera PLD decodes the addressing of the serial input, and steers the datastream to the correct device. The serial input must be formatted so that the Altera PLD can correctly decode and steer the data to the correct device.

The serial interface can be used to dynamically change the operating conditions of the AFE or KSC−1000 chips by reprogramming the appropriate registers. Reprogramming these registers through the serial interface will have no effect on the default settings that are automatically programmed into these devices on power-up or board reset.

Table 2. SERIAL INPUT DEVICE SELECT

Device Select DS[2..0]	Serial Device
000	PLD
001	AFE1
010	AFE2
011	KSC−1000
100	(Not Used)
101	(Not Used)
110	(Not Used)
111	(Not Used)

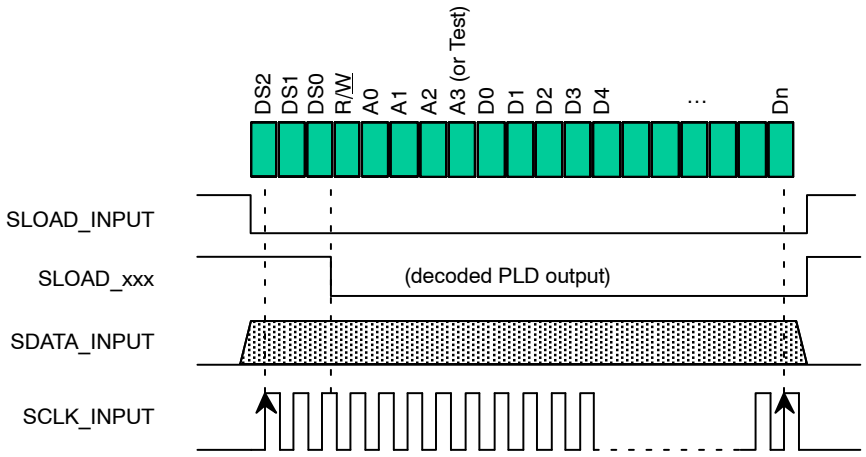


Figure 2. Serial Input Timing

The first 3 bits in the datastream are the Device Select bits DS[2..0], sent MSB first, as shown in Figure 2. The Device Select bits are decoded as shown in Table 2.

The next bit in the datastream is the Read/Write bit (R/W). Only writing is supported; therefore this bit is always LOW.

The definition of next four bits in the datastream depends on the device being addressed with the Device Select bits. For the KSC−1000 device, they are Register address bits A[0..3], LSB first. For the AD9845A AFE, they are Register Address bits A[0..2], LSB first, followed by a Test bit which is always set LOW.

The remaining bits in the bitstream are Data bits, LSB first, with as many bits as are required to fill the appropriate register.

AFE Default Initialization

Upon power up, or when the BOARD_RESET button is pressed, the PLD programs the registers of the two AFE chips on the Timing Generator Board to their default settings via the 3-wire serial interface. See Table 9 for details. The AD9845A AFE must be reprogrammed on power-up, as it does not retain register settings when power is removed.

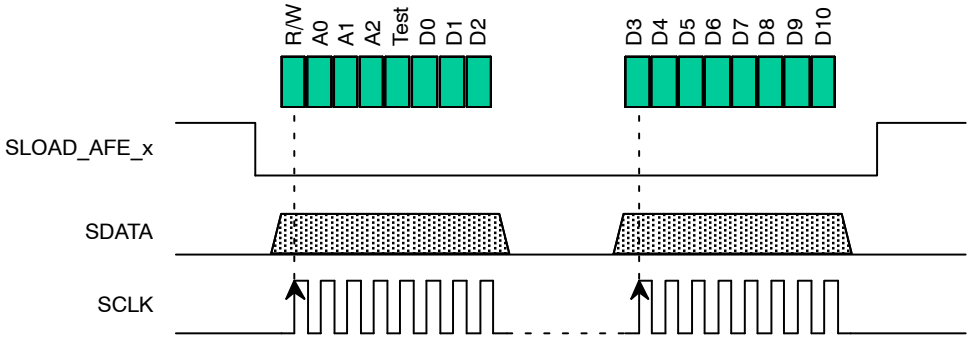


Figure 3. AFE Initialization Timing

The data for each AFE register is formatted into two bytes of data, as shown in Figure 3. The Read/Write bit is always low, and the Address bits specify the register being programmed, as shown in Table 9. Each byte is read into an 8-bit shift register, and is shifted out as a serial stream of eight bits. Each register in the AFE is programmed in this fashion until the entire AFE is programmed.

KSC−1000 Default Initialization

Upon power-up, or when the BOARD_RESET button is pressed, the Altera PLD programs the registers of the KSC−1000 chip on the AFE Timing Generator Board to their default settings via the 3-wire serial interface. The default settings are selected by the user through the PLD inputs SW[7..0] and DIO[15..0] (See Table 10 through Table 29 for details). The KSC−1000 must be reprogrammed on power-up, as it does not retain register settings when power is removed.

The KSC−1000 default settings automatically programmed by the PLD allow the Evaluation Board Kit user to operate the CCD image sensor with minimal intervention and no programming. The default settings are chosen to comply with the appropriate CCD device specifications (See References). The registers, line tables and frame tables described in this document also serve as examples for those who wish to create their own KSC−1000 timing.

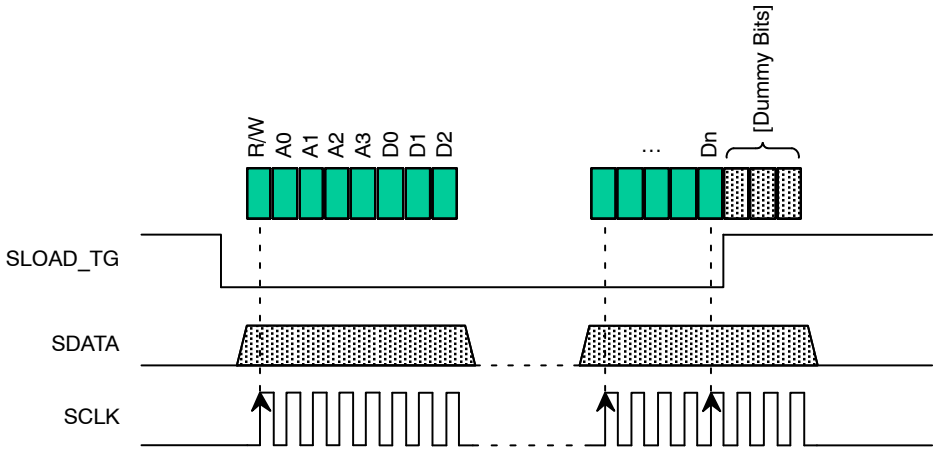


Figure 4. KSC−1000 Initialization Timing

The data for each KSC−1000 register is formatted into bytes of data, as shown in Figure 4. The Read/Write bit is always low, and the Address bits specify the register being programmed, as shown in Table 3. Each byte is read into an 8-bit shift register, and is shifted out of the PLD as a serial stream of eight bits. The last byte of data sent to a particular register may need to be padded with extra “dummy” bits; the SLOAD_TG signal is brought HIGH at the appropriate time so that the correct number of bits are streamed into each register, and the extra bits are ignored. Each register in the KSC−1000 is programmed in this fashion until the entire device is programmed.

Table 3. KSC−1000 REGISTERS

Register Address	Register Description	Data Bits
0	Frame Table Pointer	3
1	General Setup	202
2	General Control	2
3	INTG_STRT Setup	30
4	INTG_STRT Line	13
5	Signal Polarity	25
6	Offset	78
7	Width	65
8	Frame Table Access	(Variable)
9	Line Table Access	(Variable)

PLD State Machine

The Altera PLD contains a State Machine that parallels the operation of the KSC−1000. The PLD controls the KSC−1000 through the VD_TG output, and monitors several of the KSC−1000 outputs, enabling it to track and control the operation of the Timing Generator.

Still Capture Remote Triggering

When the Timing Board is configured to operate in Still Capture mode, the DIO12 input is used as a remote trigger input. The Altera PLD monitors this input, and in turn controls and monitors the KSC−1000 Still Capture timing.

Remote Board Reset

The DIO14 input is used as a remote Board Reset control line. The Altera PLD monitors this input, and when DIO14 goes HIGH, the ARSTZ (active low) output to the KSC−1000 is asserted, disabling and clearing the timing generator. When DIO14 goes LOW, the ARSTZ output is de-asserted, and the Power-up/Board Reset initialization sequence is executed. This allows programmable control of the timing sequences to change the Electronic Shutter position, for example.

Integration Clock

The Altera PLD uses the System Clock and an internal counter to generate a 1.0 ms-period clock. This clock is used to generate an internal delay after power-up or Board Reset. It may also be used to control precise integration times for the image sensor.

Output Channel Control

PLD input SW0 is used to select one of the supported operation modes: Full Field Single Output, and Full Field Dual Output. When making a change to the switch settings, the user must initiate a Board Reset for the change to take effect, either by pressing the BOARD_RESET button (S1) on the Timing Board, or by setting and resetting the Remote Reset (DIO14) input.

Integration & Electronic Shutter Control

In the Full Field Timing Modes, PLD inputs DIO[11..7] may be used to select the integration time. See Table 30 for timing details. In general, when making a change to the DIO[11..7] settings, the user must initiate a Board Reset for the change to take effect, either by pressing the BOARD_RESET button (S1) on the Timing Board, or by setting and resetting the Remote Reset (DIO14) input.

Binning Control

PLD input SW2 is used to select between 2×2 Binning Single Output, and normal operation (no binning). When making a change to the switch settings, the user must initiate a Board Reset for the change to take effect, either by pressing the BOARD_RESET button (S1) on the Timing Board, or by setting and resetting the Remote Reset (DIO14) input.

Video Mux Switch

The PLD input SW6 controls the Video Mux Switch, which steers either CCD output V_{outL} or V_{outR} to the auxiliary video output connector J1.

ALTERA CODE I/O

Inputs

The Altera PLD has multiple inputs that may be used to control certain functions. The inputs include: user selectable switches SW[7..0] on the Timing Board; remote digital inputs DIO[15..0] and a 3-wire serial interface through Timing Board connector J7; Timing Board signals; and various outputs from the KSC−1000 Timing Generator. The KSC−1000 outputs are monitored by the PLD to control auxiliary timing functions, and keep the KSC−1000 and Altera PLD synchronized. The remote digital inputs DIO[15..0] are optional, and are not required for KAI−2001/KAI−2020 operation, but may be used to control integration time and remote triggering.

Table 4. ALTERA INPUTS

Symbol	Description
POWER_ON_DELAY	The Rising Edge of this Signal Clears and Re-initializes the PLD
SYSTEM_CLK	40 MHz Clock, 2X the Desired Pixel Clock Rate
PIXCLK	NI1424 20 MHz Pixel Rate Clock from the KSC1000TG (Not Used)
SW0	HIGH = Dual Output, Full Image, LOW = Single Output, Full Image
SW1	(Not Used, Must be LOW)
SW2	Binning Mode: HIGH = 2×2 Binning, Single Output, LOW = No Binning
SW3	HIGH = Still Capture Mode, LOW = Free-Running Mode
SW4	(Not Used, Must be LOW)
SW5	HIGH = KAI−2001, LOW = KAI−2020
SW6	Video Mux Switch Control: HIGH = VoutR, LOW = VoutL
SW7	(Not Used, Must be LOW)

Table 4. ALTERA INPUTS (continued)

Symbol	Description
DIO[6..0]	(Not Used)
DIO[11..7]	Integration Control (See Table 30)
DIO12	Remote Capture Control Line, Falling Edge Triggered (Still Capture Mode)
DIO13	(Not Used)
DIO14	Remote Board Reset (HIGH Activates ARSTZ, Falling Edge Activates BOARD_RESET)
SLOAD_INPUT	3-wire Serial Interface LOAD Signal Input
SDATA_INPUT	3-wire Serial Interface DATA Signal Input
SCLOCK_INPUT	3-wire Serial Interface CLOCK Signal Input
LINE_VALID	Used to Monitor KSC−1000
FRAME_VALID	Used to Monitor KSC−1000
AUX_SHUT	(Not Used for KAI−2001/KAI−2020 Operation)
INTG_START	Used to Monitor KSC−1000

Outputs

The Altera PLD outputs include: the 3-wire serial interface; control signals to the KSC−1000; the INTEGRATE signal used for external monitoring and synchronization; the PLD[2..0] signals which are auxiliary Imager Board control bits; and the GIO[2..0] bits which are used for PLD monitoring and testing.

Table 5. ALTERA OUTPUTS

Symbol	Description
PLD_OUT0	KAI−2001/KAI−2020 Video MUX Control
PLD_OUT1	(Not Used for KAI−2001/KAI−2020 Operation)
PLD_OUT2	(Not Used for KAI−2001/KAI−2020 Operation)
GIO[2..0]	(Not Used for KAI−2001/KAI−2020 Operation)
SLOAD_AFE_1	Serial Load Enable, Ch1 AD9845A AFE
SLOAD_AFE_2	Serial Load Enable, Ch2 AD9845A AFE
SLOAD_TG	Serial Load Enable, KSC−1000
SDATA	3-wire Serial Interface DATA Signal Output
SCLOCK	3-wire Serial Interface CLOCK Signal Output
INTEGRATE	High During CCD Integration Time
HD_TG	(Not used for KAI−2001/KAI−2020 Operation)
VD_TG	Control Signal to KSC−1000
ARSTZ	Asynchronous Reset to KSC−1000 (from DIO14)

KAI−2001/KAI−2020 TIMING CONDITIONS

System Timing Conditions

Table 6. SYSTEM TIMING

Description	Symbol	Time	Notes
System Clock Period	T_{sys}	25.0 ns	40 MHz System Clock
Unit Integration Time	U_{int}	1.0 ms	Generated by PLD
Power Stable Delay	T_{pwr}	100 ms	Typical
Default Serial Load Time	T_{sload}	2.06 ms	Typical
Integration Time	T_{int}		Operating Mode Dependent

CCD Timing Conditions

Table 7. CCD TIMING

Description	Symbol	Time	Pixel Counts	Notes
H1, H2, RESET Period	T_{pix}	50.0 ns	1	20 MHz Clocking of H1, H1L, H2, RESET
VCCD Delay	T_{VD}	50.0 ns	1	Delay after Hclks Stop
VCCD Transfer Time	T_{VCCD}	1.6 μs	32	V2 Rising Edge to V2 Falling Edge
HCCD Delay	T_{HD}	1.55 μs	31	Delay before Hclks Resume
Vertical Transfer Period	V_{period}	3.2 μs	64	$V_{period} = T_{VD} + T_{VCCD} + T_{HD}$
Horizontal Pixels	H_{PIX}	83.2 μs	1664	1648 CCD Pixels + 16 Overclock Pixels
Vertical Pixels	V_{PIX}		1220	1214 CCD Lines + 6 Overclock Lines
Line Transfer Time	T_L	86.4 μs	1728	$T_L = V_{period} + H_{PIX}$
VCCD Pedestal Time	T_{3P}	25.1 μs	502	
Photodiode Transfer Time	T_{V3rd}	12.1 μs	242	V2 3rd level
Photodiode Delay	T_{3D}	20.0 μs	400	
Photodiode Frame Delay	T_{3FD}	85.5 μs	1710	Delay before 1st Line Transfer
Photodiode Transfer Period	T_{3PT}	142.7 μs	2854	$T_{3PT} = T_{3P} + T_{V3rd} + T_{3D} + T_{3FD}$
Shutter Pulse Setup	T_{EL}	1.5 μs	30	
Shutter Pulse Time	T_S	5.0 μs	100	
Shutter Pulse Delay	T_{SD}	1.5 μs	30	

PCI−1424 Timing Conditions

Table 8. PCI−1424 TIMING

Description	Symbol	Time	Pixel Counts	Notes
PIX Period	T_{PIX}	50.0 ns	1	20 MHz Clocking of DATACLK Sync Signal
FRAME Time	T_{FRAME}	105.5 ms	2,110,604	$T_{FRAME} = T_{PIX} * ((V_{period} + H_{PIX}) * V_{PIX} + T_{3PT})$

MODES OF OPERATION

The following modes of operation are available to the user:

Electronic Shutter Modes

The Evaluation Board electronic shutter circuitry provides a method of precisely controlling the image exposure time without any mechanical components. Charge may be cleared from the CCD photodiodes at some time during the readout of the previous frame. This allows integration times of less than one frame time, to compensate for high light exposures that would otherwise saturate the CCD.

In Free-Running Mode, the default integration time can be set from 1× to 1/8× frame time via the digital inputs DIO[11..7] (See Table 14 and Table 30). In Still Capture Mode, the default integration time can be set the same way, although the resulting integration times are different from those in Free-Running Mode. When changing the integration time, the user must initiate a Board Reset for the change to take effect, either by pressing the BOARD_RESET button (S1) on the Timing Board, or by setting and resetting the Remote Reset (DIO14) input.

Black Clamp Mode

One of the features of the AD9845A AFE chip is an optical black clamp. The black clamp (CLPOB) is asserted during the CCD's dark pixels and is used to remove residual offsets in the signal chain, and to track low frequency variations in the CCD's black level. The location of these pulses is fixed in the default KSC−1000 settings, but can be adjusted dynamically through the 3-wire serial interface. The default settings are shown in Table 11.

POWER-ON/BOARD RESET INITIALIZATION

When the board is powered up, the Board Reset button is pressed, or the Remote Rest (DIO14) is toggled, the Altera PLD is internally reset. When this occurs, state machines in the PLD will first serially load the initial default values into the AFE registers, then will load the KSC−1000 frame tables, line tables, and registers.

Upon completion, the KSC−1000 will be ready to proceed according to its programmed configuration. In the background, the Altera PLD monitors the activity of the KSC−1000, and the 3-wire Serial Interface.

AFE Register Default Settings

On power-up or board reset, the AFE registers are programmed to the default levels shown in Table 9. The VGA Gain settings vary depending on the position SW5 (See Table 4), which selects between the KAI−2001 (HIGH) and KAI−2020 (LOW) devices. See the AD9845A specifications (References) for details of the AFE registers.

Table 9. DEFAULT AD9845A AFE REGISTER PROGRAMMING

Register Address	Description	Value (decimal)	Notes
0	Operation	128	
1	VGA Gain (KAI−2020)	350	Corresponds to a VGA Stage Gain of 9.9 dB
1	VGA Gain (KAI−2001)	260	Corresponds to a VGA Stage Gain of 6.9 dB
2	Clamp	96	The Output of the AD9845A will be Clamped to Code 96 During the CLPOB Period
3	Control	8	CDS Gain Enabled
4, 5, 6, 7	PXGA Gain	43	Corresponds to a PXGA Stage Gain of 0.0 dB

KSC−1000 Timing Generator Default Settings

On power-up or board reset, The KSC−1000 is programmed to the default settings as detailed in Table 10 through Table 29. See the KSC−1000 Device Specification (References) for details of the KSC−1000 registers.

Register 0: Frame Table Pointer

Register 0 contains the Frame Table Pointer, which instructs the KSC−1000 to perform the timing sequence defined in that table. Frame Table 0 is used for Free-Running Single Channel and Dual Channel modes, Frame Table 1 is used for Still Capture Single-Channel Mode, and Frame Table 2 is used for Single Channel 2×2 Binning mode. The default setting depends on the position of SW2 and SW3.

Table 10. REGISTER 0 DEFAULT SETTING

Register Entry	Data (Normal Mode)	Data (Still Mode)	Data (2×2 Binning)
Frame Table Address	0	1	2

Register 1: General Setup

The default settings written to Register 1 depend on the position of SW0 on the Timing Board, used to select between 1-channel and 2-channel operation.

Table 11. REGISTER 1 DEFAULT SETTING

Register Entry	Data (1-channel)	Data (2-channel)
Pixels Per Line[0..12]	1664	832
Line Valid Pixel Start[0..12]	9	9
Line Valid Pixel Quadrature Start[0..1]	0	0
Line Valid Pixel End[0..12]	1652	826
CLPOB1_Pix_Start[0..12]	1630	828
CLPOB1_Pix_End[0..12]	1640	829
CLPOB2_Pix_Start[0..12]	0	0
CLPOB2_Pix_End[0..12]	0	0
CLPDM1_Pix_Start[0..12]	6	3
CLPDM1_Pix_End[0..12]	16	8
CLPDM2_Pix_Start[0..12]	0	0
CLPDM2_Pix_End[0..12]	0	0
PBLK_Pix_Start[0..12]	1650	832
PBLK_Pix_End[0..12]	1	1
RG_Enable	1	1
H6_Enable	0	0
H4_Enable	1	1
H5_Enable	0	0
SH2_Enable	1	1
SH4_Enable	1	1
DATACLK1_Enable	1	1
DATACLK2_Enable	1	1
PIXCLK_Enable	1	1
H3_Enable	1	1
H1_Enable	1	1
H2_Enable	1	1
SH1_Enable	1	1
SH3_Enable	1	1
H6 24 mA Output Enable	0	0
H4 24 mA Output Enable	0	0
H5 24 mA Output Enable	0	0
RG 24 mA Output Enable	0	0
SH2 24 mA Output Enable	0	0
SH4 24 mA Output Enable	0	0

Table 11. REGISTER 1 DEFAULT SETTING (continued)

Register Entry	Data (1-channel)	Data (2-channel)
DATACLK1 24 mA Output Enable	0	0
DATACLK2 24 mA Output Enable	0	0
H3 24 mA Output Enable	0	0
H1 24 mA Output Enable	0	0
H2 24 mA Output Enable	0	0
SH1 24 mA Output Enable	0	0
SH3 24 mA Output Enable	0	0
DLL Frequency Range Select	8	8

Register 2: General Control

Register 2 controls the Power Management and Operation state of the KSC−1000. The Low Power Mode is not used on the KAI−2001/KAI−2020, so this bit is always LOW. The Memory Table Mode bit is used to halt execution of the KSC−1000 timing sequences and to enable programming of the registers. The KSC−1000 Initialization sequence begins with setting the Memory Table Mode bit in Register 2 to Program Mode, and ends by setting the bit to Execution Mode. See the KSC−1000 Device Specification (References) for more details.

Table 12. REGISTER 2 SETTINGS

Register Entry	Program Mode	Execution Mode
Low Power Enable	0	0
Memory Table Mode	0	1

Register 3: INTG_START Setup

The default settings written to Register 3 establish the setup, pulse width, and hold timing of the Electronic Shutter pulse. The Shutter Pulse may occur on a particular line, as controlled by Register 4, or may be asserted by setting the “Force INTG_STRT” bit in the Frame Table (Register 8). In either case, the Electronic Shutter Pulse occurs before the vertical clocking interval of the Frame Table entry.

Table 13. REGISTER 3 DEFAULT SETTING

Register Entry	Data
Electronic Shutter Setup Clocks[0..9]	30
Electronic Shutter Pulse Width[0..9]	100
Electronic Shutter Hold Clocks[0..9]	30

Register 4: INTG_START Line

Short integration times may be controlled through use of the Electronic Shutter. The default setting written to Register 4 controls the line number on which the Electronic Shutter will occur. The DIO[11..7] inputs are used to control the Integration time, by selecting pre-programmed line numbers, as shown in Table 14.

In Free-Running Mode, the Electronic Shutter pulse occurs during the previous frame readout. In Still Mode, the Electronic Shutter pulse occurs during the VCCD Flush sequence; since the Flush sequence contains more lines than one frame, the pre-programmed line numbers are different from those in Free-Running Mode (See Table 14). In either case, the values are chosen to allow integration times adjustable in increments of one-eighth the Frame or Flush time.

If the line number is greater than the number of lines specified in a Frame Table (Register 8), the Electronic Shutter will not occur. This is the method used to turn the Shutter off; in this case, the integration time is controlled by a counter in the Altera PLD (See Table 30).

Table 14. REGISTER 4 DEFAULT SETTING

DIO[11..7]	Frame/Flush Integration	Free-Running Mode Integrate Start Pulse Line Number[0..12]	Still Mode Integrate Start Pulse Line Number[0..12]
0	1	4088 (Default – No Pulse)	4088 (Default – No Pulse)
1	1/8	1064	3192
2	1/4	912	2736
3	3/8	760	2280
4	1/2	608	1824
5	5/8	456	1368
6	3/4	304	912
7	7/8	152	456

Register 5: Signal Polarity

The default settings written to Register 5 depend on the position of SW0 on the Timing Board, used to select between 1-channel and 2-channel operation.

Table 15. REGISTER 5 DEFAULT SETTING

Register Entry	1-channel	2-channel	Evaluation Board Signal Name
H6_IDLE_VAL	0	0	(Not Used)
H3_IDLE_VAL	1	1	H1A
H4_IDLE_VAL	0	0	H2A
H1_IDLE_VAL	1	0	H2B
H5_IDLE_VAL	0	0	(Not Used)
H2_IDLE_VAL	0	1	H1B
RG_IDLE_VAL	1	1	RESET
SH2_IDLE_VAL	1	1	SHP1
SH1_IDLE_VAL	1	1	SHP2
SH4_IDLE_VAL	1	1	SHD1
SH3_IDLE_VAL	1	1	SHD2
DATACLK1_IDLE_VAL	1	1	ADCLK (to AFEs)
DATACLK2_IDLE_VAL	0	0	DATACLK (to Framegrabber)
CLPOB_IDLE_VAL	1	1	CLPOB
CLPDM_IDLE_VAL	1	1	CLPDM
AMP_ENABLE_IDLE_VAL	0	0	AMP_ENABLE
FRAME_VALID_IDLE_VAL	0	0	FRAME_VALID
LINE_VALID_IDLE_VAL	0	0	LINE_VALID
INTEGRATE_START_IDLE_VAL	0	0	INTG_START/VES
V1_IDLE_VAL	0	0	V3RD
V2_IDLE_VAL	0	0	(Not Used)
V3_IDLE_VAL	0	0	V2
V4_IDLE_VAL	1	1	V1
V5_IDLE_VAL	0	0	(Not Used)
V6_IDLE_VAL	0	0	FDG

Register 6: Pixel-Rate Signal Offset

The default settings written to Register 6 depend on the position of SW0 on the Timing Board, used to select between 1-channel and 2-channel operation.

Table 16. REGISTER 6 DEFAULT SETTING

Register Entry	Data (1-channel)	Data (2-channel)	CCD Signal Name
H6_OFFSET[0..5]	0	0	(Not Used)
H3_OFFSET[0..5]	32	32	H1A
H4_OFFSET[0..5]	29	29	H2A
H1_OFFSET[0..5]	33	31	H2B
H5_OFFSET[0..5]	0	0	(Not Used)
H2_OFFSET[0..5]	31	33	H1B
RG_OFFSET[0..5]	0	0	RESET
SH2_OFFSET[0..5]	31	31	SHP1
SH1_OFFSET[0..5]	31	31	SHP2
SH4_OFFSET[0..5]	63	63	SHD1
SH3_OFFSET[0..5]	63	63	SHD2
DATACLK1_OFFSET[0..5]	42	42	ADCLK (to AFEs)
DATACLK2_OFFSET[0..5]	0	0	DATACLK (to Framegrabber)

Register 7: Pixel-Rate Signal Width

The default settings written to Register 7 depend on the position of SW0 on the Timing Board, used to select between 1-channel and 2-channel operation.

Table 17. REGISTER 7 DEFAULT SETTING

Register Entry	Data (1-channel)	Data (2-channel)	CCD Signal Name
H6_WIDTH[0..4]	16	16	(Not Used)
H3_WIDTH[0..4]	13	13	H1A
H4_WIDTH[0..4]	18	18	H2A
H1_WIDTH[0..4]	13	18	H2B
H5_WIDTH[0..4]	16	16	(Not Used)
H2_WIDTH[0..4]	18	14	H1B
RG_WIDTH[0..4]	8	8	RESET
SH2_WIDTH[0..4]	14	14	SHP1
SH1_WIDTH[0..4]	14	14	SHP2
SH4_WIDTH[0..4]	14	14	SHD1
SH3_WIDTH[0..4]	14	14	SHD2
DATACLK1_WIDTH[0..4]	31	31	ADCLK (to AFEs)
DATACLK2_WIDTH[0..4]	16	16	DATACLK (to Framegrabber)

Register 8: Frame Tables

Several Frame Tables are written by default to the KSC−1000 Frame Table registers, but only one Frame Table is active at one time, as determined by the Frame Table Pointer (Register 0). Frame Table 0 is used for Free-Running Single Channel and Dual Channel modes, Frame Table 1 is used for Still Capture Mode, and Frame Table 2 is used for Single Channel 2×2 Binning mode. Note that the last row in Table 18 through Table 20 are the mnemonics associated with the Flag, Count, and Address bits. See the KSC−1000 Device Specification (References) for more details.

Table 18. FRAME TABLE 0 DEFAULT SETTING

Bit Location	Frame Table Data	FT0 Entry			
		0	1	2	3
0	Check and Increment Line Counter	1	0	0	0
1	Clear Line Counter	0	1	1	1
2	Force INTG_STRT	0	0	0	0
3:4	Horizontal Binning Factor	0	0	0	0
5	HCLK_V Enable	0	0	0	0
6	LINE_VALID Enable	1	0	0	0
7	FRAME_VALID Enable	1	0	0	0
8	Video Amplifier Enable	0	0	0	0
9	AFE Clock Enable	1	1	1	1
10	CLPDM2 Enable	0	0	0	0
11	CLPDM1 Enable	0	0	0	0
12	CLPOB2 Enable	0	0	0	0
13	CLPOB1 Enable	1	0	0	0
14	PBLK Enable	1	0	0	0
15	Pblk_Idle_Val	1	1	1	1
16	Flag	0	1	0	0
17:29	Count	1220	0	1	0
30:32	Address 2:0	0	5	1	0
33	Address 3	0	0	0	0
–	Mnemonic	ELT0	ExLTNVD 5	ELT 1	JMPFT 0

Table 19. FRAME TABLE 1 DEFAULT SETTING

Bit Location	Frame Table Data	FT1 Entry										
		0	1	2	3	4	5	6	7	8	9	10
0	Check and Increment Line Counter	0	0	0	0	0	0	1	0	0	0	0
1	Clear Line Counter	1	1	1	1	1	1	0	1	1	1	1
2	Force INTG_STRT	0	0	1	0	1	0	0	0	0	0	0
3:4	Horizontal Binning Factor	0	0	0	0	0	0	0	0	0	0	0
5	HCLK_V Enable	1	0	0	0	0	0	1	0	0	0	0
6	LINE_VALID Enable	0	0	0	0	0	0	0	1	0	1	0
7	FRAME_VALID Enable	0	0	0	0	0	0	0	0	0	1	0
8	Video Amplifier Enable	0	0	0	0	0	0	0	0	0	0	0
9	AFE Clock Enable	1	1	1	1	1	1	1	1	1	1	1
10	CLPDM2 Enable	0	0	0	0	0	0	0	0	0	0	0
11	CLPDM1 Enable	0	0	0	0	0	0	0	0	0	1	0
12	CLPOB2 Enable	0	0	0	0	0	0	0	0	0	0	0
13	CLPOB1 Enable	0	0	0	0	0	0	0	0	0	1	0
14	PBLK Enable	0	0	0	0	0	0	0	0	0	1	0
15	Pblk_Idle_Val	1	1	1	1	1	1	1	1	1	1	1
16	Flag	1	0	0	0	0	1	0	0	0	0	0
17:29	Count	0	1	30	1	1	0	3660	1	1	1220	0
30:32	Address 2:0	2	6	8	7	2	2	4	2	1	0	1
33	Address 3	0	0	0	0	0	0	0	0	0	0	0
–	Mnemonic	ExLTN VD 2	ELT6	ELT8	ELT7	ELT2	ExLTN VD 2	ELT4	ELT2	ELT1	ELT0	JMPFT1

Table 20. FRAME TABLE 2 DEFAULT SETTING

Bit Location	Frame Table Data	FT2 Entry			
		0	1	2	3
0	Check and Increment Line Counter	1	0	0	0
1	Clear Line Counter	0	1	1	1
2	Force INTG_STRT	0	0	0	0
3:4	Horizontal Binning Factor	1	0	0	0
5	HCLK_V Enable	0	1	0	0
6	LINE_VALID Enable	1	0	0	0
7	FRAME_VALID Enable	1	0	0	0
8	Video Amplifier Enable	0	0	0	0
9	AFE Clock Enable	1	1	1	1
10	CLPDM2 Enable	0	0	0	0
11	CLPDM1 Enable	0	0	0	0
12	CLPOB2 Enable	0	0	0	0
13	CLPOB1 Enable	1	0	0	0
14	PBLK Enable	1	0	0	0
15	Pblk_Idle_Val	1	1	1	1
16	Flag	0	1	0	0
17:29	Count	610	0	1	0
30:32	Address 2:0	3	2	1	2
33	Address 3	0	0	0	0
–	Mnemonic	ELT0	ExLTNVD 5	ELT 1	JMPFT 2

Register 9: Line Tables

There are eight Line Tables written by default to the KSC−1000 Line Table registers.

Line Table 0 is the normal Line Transfer sequence. See Figure 5.

Table 21. LINE TABLE 0 DEFAULT SETTING

CCD Signal	Line Table Data Name	LT0 Entry						
		0	1	2	3	4	5	6
	Count[0..12]	1	1	30	1	30	1	0
	HCLK_H Enable	0	0	0	0	0	1	0
FDG	V6	0	0	0	0	0	0	0
	V5	0	0	0	0	0	0	0
V1	V4	0	0	1	0	0	0	0
V2	V3	0	1	1	1	0	0	0
	V2	0	0	0	0	0	0	0
V3RD	V1	0	0	0	0	0	0	0

Line Table 1 is the normal Photodiode Transfer sequence that transfers charge from all the photodiodes to the vertical registers. See Figure 6.

Table 22. LINE TABLE 1 DEFAULT SETTING

CCD Signal	Line Table Data Name	LT1 Entry							
		0	1	2	3	4	5	6	7
	Count[0..12]	1	500	1	240	1	400	1310	0
	HCLK_H Enable	0	0	0	0	0	0	0	0
FDG	V6	0	0	0	0	0	0	0	0
	V5	0	0	0	0	0	0	0	0
V1	V4	0	0	0	1	0	0	0	0
V2	V3	0	1	1	1	1	1	0	0
VCLK_ENABLE	V2	0	0	0	0	0	0	0	0
V3RD	V1	0	0	1	1	1	0	0	0

Line Table 2 is the Integration sequence. The vertical clocks are not active, and the Horizontal register is continually flushed of charge. See Figure 7.

Table 23. LINE TABLE 2 DEFAULT SETTING

CCD Signal	Line Table Data Name	LT2 Entry	
		0	1
	Count[0..12]	1	0
	HCLK_H Enable	1	0
FDG	V6	0	0
	V5	0	0
V1	V4	0	0
V2	V3	0	0
VCLK_ENABLE	V2	0	0
V3RD	V1	0	0

Line Table 3 is the Binning Mode Line Transfer sequence. Two V1 and V2 pulses occur during each Vertical clocking interval, followed by Horizontal Register readout. See Figure 8.

Table 24. LINE TABLE 3 DEFAULT SETTING

CCD Signal	Line Table Data Name	LT3 Entry									
		0	1	2	3	4	5	6	7	8	9
	Count[0..12]	1	1	30	1	30	1	30	1	30	0
	HCLK_H Enable	0	0	0	0	0	0	0	0	1	0
FDG	V6	0	0	0	0	0	0	0	0	0	0
	V5	0	0	0	0	0	0	0	0	0	0
V1	V4	0	0	1	0	0	0	1	0	0	0
V2	V3	0	1	1	1	0	1	1	1	0	0
	V2	0	0	0	0	0	0	0	0	0	0
V3RD	V1	0	0	0	0	0	0	0	0	0	0

Line Table 4 is the Flush sequence. It is similar to the Line Transfer Sequence (Line Table 0), but the Fast Dump Gate is held high, and the Horizontal clocks are not enabled after the Vertical transfer. See Figure 9.

Table 25. LINE TABLE 4 DEFAULT SETTING

CCD Signal	Line Table Data Name	LT4 Entry					
		0	1	2	3	4	5
	Count[0..12]	1	1	198	1	199	0
	HCLK_H Enable	0	0	0	0	0	0
FDG	V6	1	1	1	1	1	0
	V5	0	0	0	0	0	0
V1	V4	0	0	1	0	0	0
V2	V3	0	1	1	1	0	0
	V2	0	0	0	0	0	0
V3RD	V1	0	0	0	0	0	0

Line Table 5 is an Integration sequence. Neither the Vertical clocks nor the Horizontal clocks are active. See Figure 10.

Table 26. LINE TABLE 5 DEFAULT SETTING

CCD Signal	Line Table Data Name	LT5 Entry	
		0	1
	Count[0..12]	1	0
	HCLK_H Enable	0	0
FDG	V6	0	0
	V5	0	0
V1	V4	0	0
V2	V3	0	0
VCLK_ENABLE	V2	0	0
V3RD	V1	0	0

Line Tables 6, 7, and 8 are used to implement the photodiode flush sequence. See Figure 11, Figure 12, and Figure 13, respectively, as well as Figure 17.

Table 27. LINE TABLE 6 DEFAULT SETTING

CCD Signal	Line Table Data Name	LT6 Entry				
		0	1	2	3	4
	Count[0..12]	1	25	1	25	0
	HCLK_H Enable	0	0	0	0	0
FDG	V6	0	0	0	0	0
	V5	0	0	0	0	0
V1	V4	0	0	0	1	0
V2	V3	0	1	1	1	0
	V2	0	0	0	0	0
V3RD	V1	0	0	1	1	0

Table 28. LINE TABLE 7 DEFAULT SETTING

CCD Signal	Line Table Data Name	LT7 Entry				
		0	1	2	3	4
	Count[0..12]	10	10	25	2	0
	HCLK_H Enable	0	0	0	0	0
FDG	V6	0	0	0	0	0
	V5	0	0	0	0	0
V1	V4	1	0	0	0	0
V2	V3	1	1	1	0	0
	V2	0	0	0	0	0
V3RD	V1	1	1	0	0	0

Table 29. LINE TABLE 8 DEFAULT SETTING

CCD Signal	Line Table Data Name	LT8 Entry					
		0	1	2	3	4	5
	Count[0..12]	20	200	20	10	1	0
	HCLK_H Enable	0	0	0	0	0	0
FDG	V6	0	0	0	0	0	0
	V5	0	0	0	0	0	0
V1	V4	0	0	0	1	1	0
V2	V3	1	0	1	1	1	0
	V2	0	0	0	0	0	0
V3RD	V1	0	0	0	0	1	0

KAI−2001/KAI−2020 TIMING

Line Table 0 (Line Transfer)

Line Table 0 is the Line Transfer timing sequence that transfers one entire row of charge toward the horizontal register. V1 and V2 are asserted, with overlap adjustability to compensate for the clock driver rise and fall times. Charge is moved down the vertical CCD registers, and the last row of charge is dumped into the horizontal register. The VCCD clocking interval is followed by the Horizontal clocks, which shift one line out through the output amplifier(s).

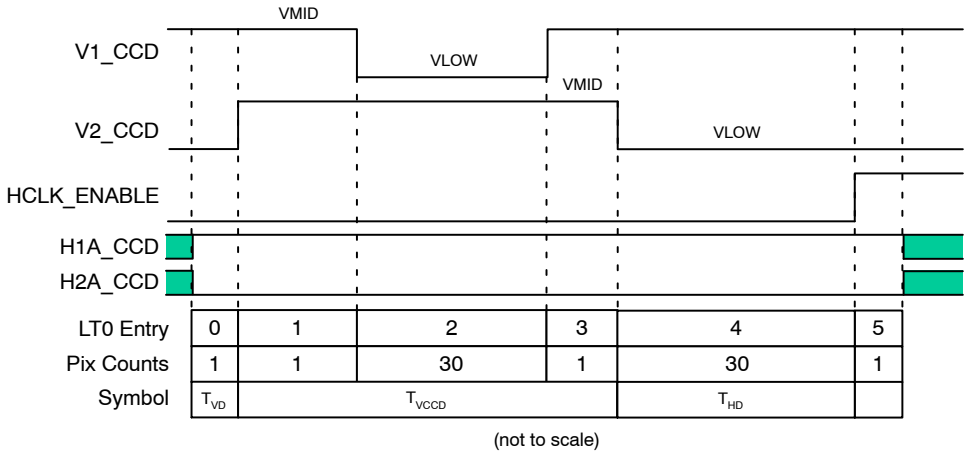


Figure 5. Line Table 0 Default Timing

Line Table 1 (Diode Transfer)

Line Table 1 is the Photodiode Transfer timing, in which the V2 clock 3rd-level shifts charge from all the photodiodes into the vertical CCD registers. The V1 and V2 clocks have overlap adjustability to compensate for the clock driver rise and fall times.

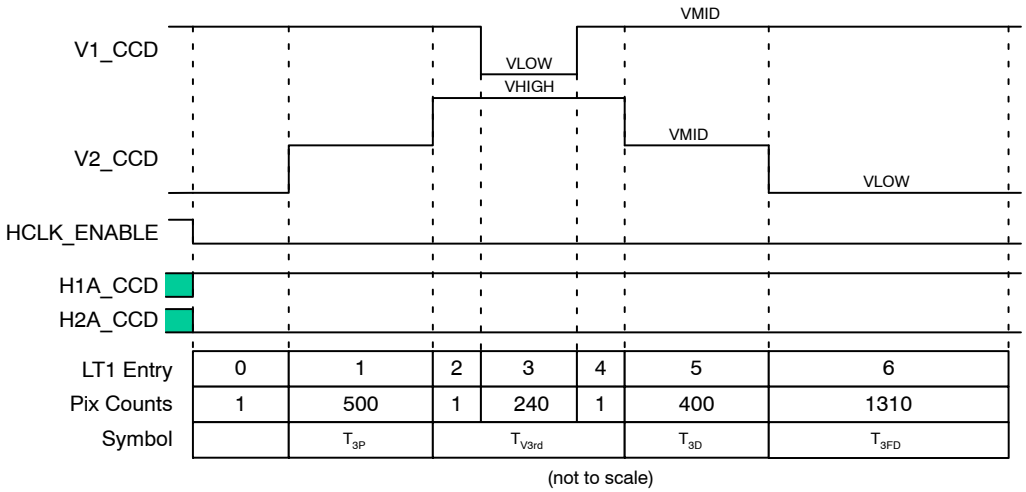


Figure 6. Line Table 1 Default Timing

Line Table 2 (Integration)

Line Table 2 is the Integration timing sequence, during which the Vertical clocks are inactive and the Horizontal clocks are running continuously. This sequence runs until Integration is complete, signaled by the assertion of the VD_TG signal from the Altera PLD.

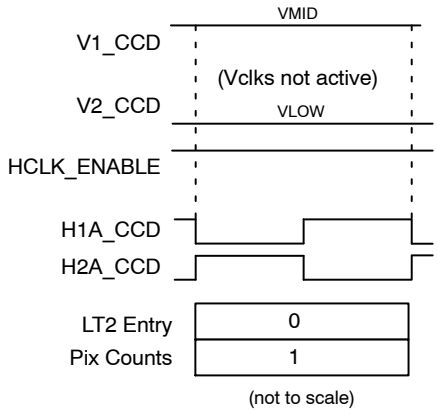


Figure 7. Line Table 2 Default Timing

Line Table 3 (Binning Mode Line Transfer)

Line Table 3 is the Binning Mode Line Transfer sequence, during which the Vertical clocks are asserted twice per line. This effectively sums two pixels' worth of charge into each Horizontal CCD pixel. After the binning line transfer, the Horizontal clocks are run in Binning Mode.

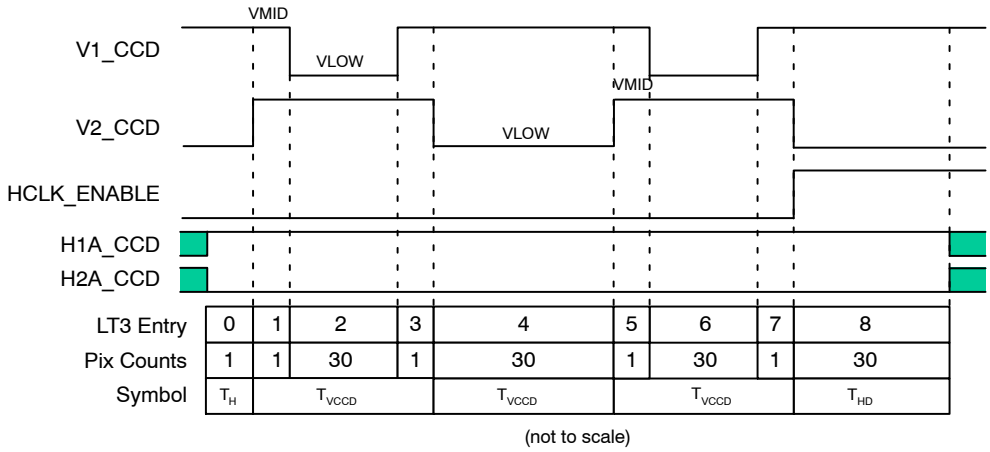


Figure 8. Line Table 3 Default Timing

Line Table 4 (Line Flush)

Line Table 4 is the Line Flush timing sequence that transfers one entire row of charge toward the horizontal register. The sequence is virtually identical to the normal Line Transfer Sequence (Line Table 0), but the Fast Dump Gate is held high, which effectively dumps the charge from the Vertical registers before it reaches the Horizontal CCD registers. See the KAI−2001/KAI−2020 Device Specification for details.

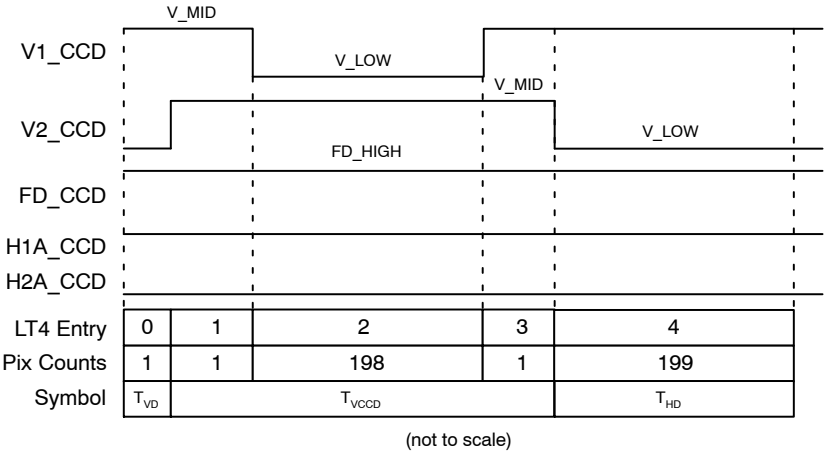


Figure 9. Line Table 4 Default Timing

Line Table 5 (Trigger Hold)

Line Table 5 is a sequence one pixel time in length, used when the KSC−1000 is waiting to be triggered by the Altera PLD. Neither the Vertical clocks nor the Horizontal Clocks are active during this sequence.

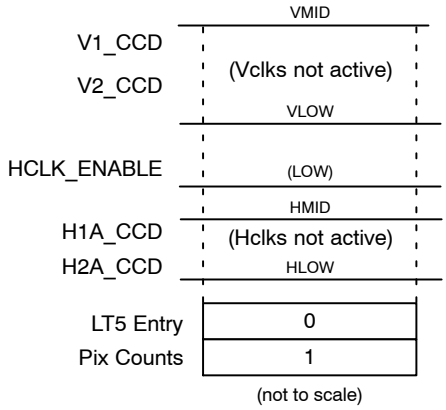


Figure 10. Line Table 5 Default Timing

Line Table 6 (Photodiode Flush Start)

Line Table 6 is used in Still Capture Mode at the beginning of the photodiode flush sequence. The Vertical clocks are left in their active Frame Transfer levels in preparation for the Electronic Shutter pulse.

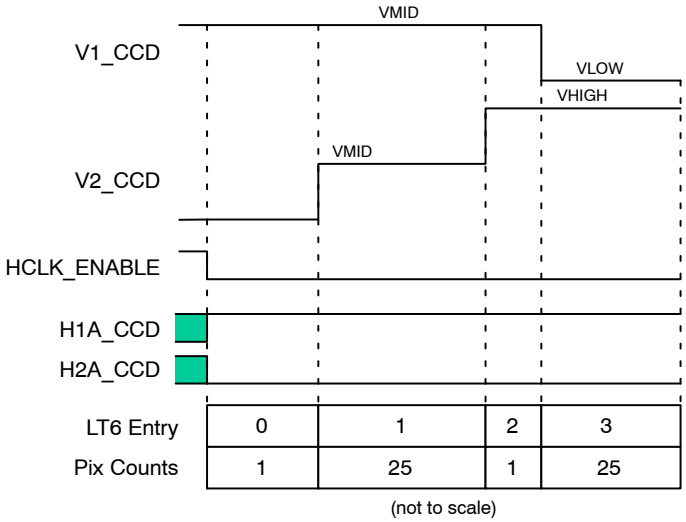


Figure 11. Line Table 6 Default Timing

Line Table 7 (Photodiode Flush End)

Line Table 7 is used in Still Capture Mode at the end of the photodiode flush sequence. The Vertical clocks are deactivated from their Frame Transfer levels, in preparation for the VCCD Flush sequence.

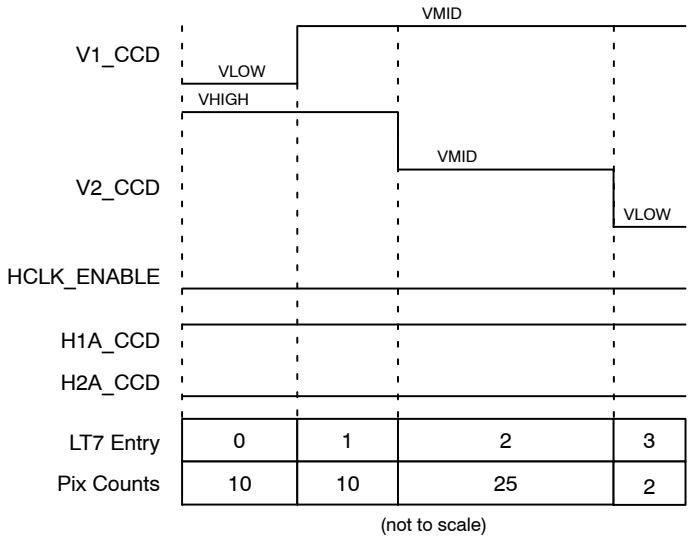


Figure 12. Line Table 7 Default Timing

Line Table 8 (Photodiode Flush)

Line Table 8 is used in Still Capture Mode between Electronic Shutter pulses during the photodiode flush sequence. The Vertical clocks are deactivated from their Frame Transfer levels, to allow the Electronic Shutter circuitry to prepare for the next pulse. See Figure 17.

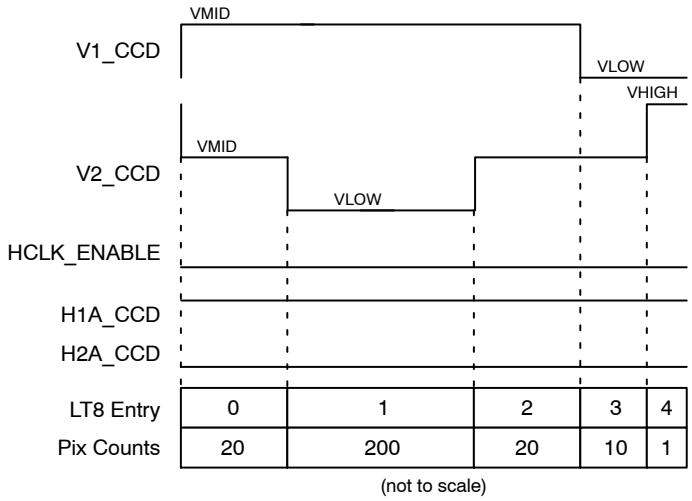


Figure 13. Line Table 8 Default Timing

Frame Table 0 Sequence

Frame Table 0 contains the Free-Running (video mode) timing sequence used to continuously read out all rows of the CCD. The sequence begins with the Line Transfer sequence, followed by the Timed Integration sequence. When integration is complete, the Altera PLD asserts the VD_TG signal to the KSC−1000. This initiates the Photodiode transfer, and the cycle repeats with the next Line Transfer sequence.

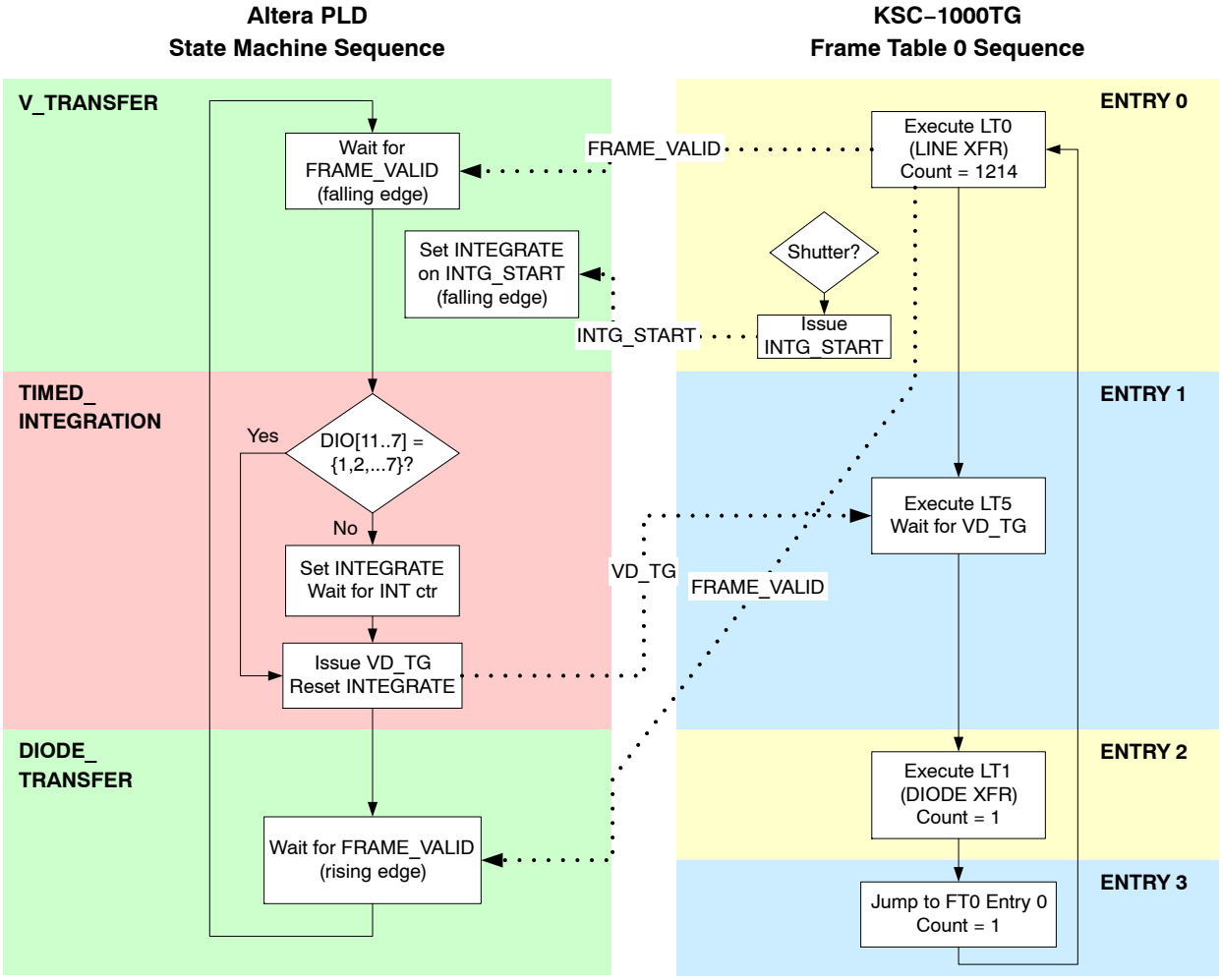
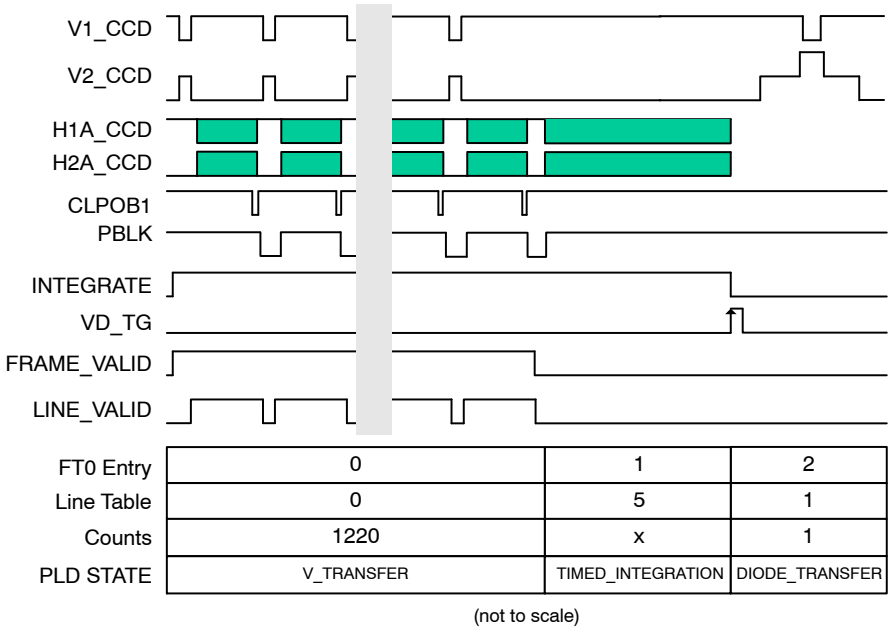


Figure 14. Free-Running Mode Timing Sequence



FT0 Entry	0	1	2
Line Table	0	5	1
Counts	1220	x	1
PLD STATE	V_TRANSFER	TIMED_INTEGRATION	DIODE_TRANSFER

(not to scale)

Figure 15. Frame Table 0 Default Timing

Frame Table 1 Sequence

Frame Table 1 contains the Still Capture mode timing sequence used to read one frame of the CCD. When externally triggered through the DIO interface, a Timed Integration and Flush sequence is begun. The Electronic Shutter is pulsed multiple times to clear the photodiodes of any accumulated charge. The Vertical clocks are positioned to allow excess charge from the Vertical CCDs to flow back to the photosites, where the Electronic Shutter can drain this charge to the substrate. One final pulse while the Vertical clocks are inactive clears the photodiodes in preparation for Integration.

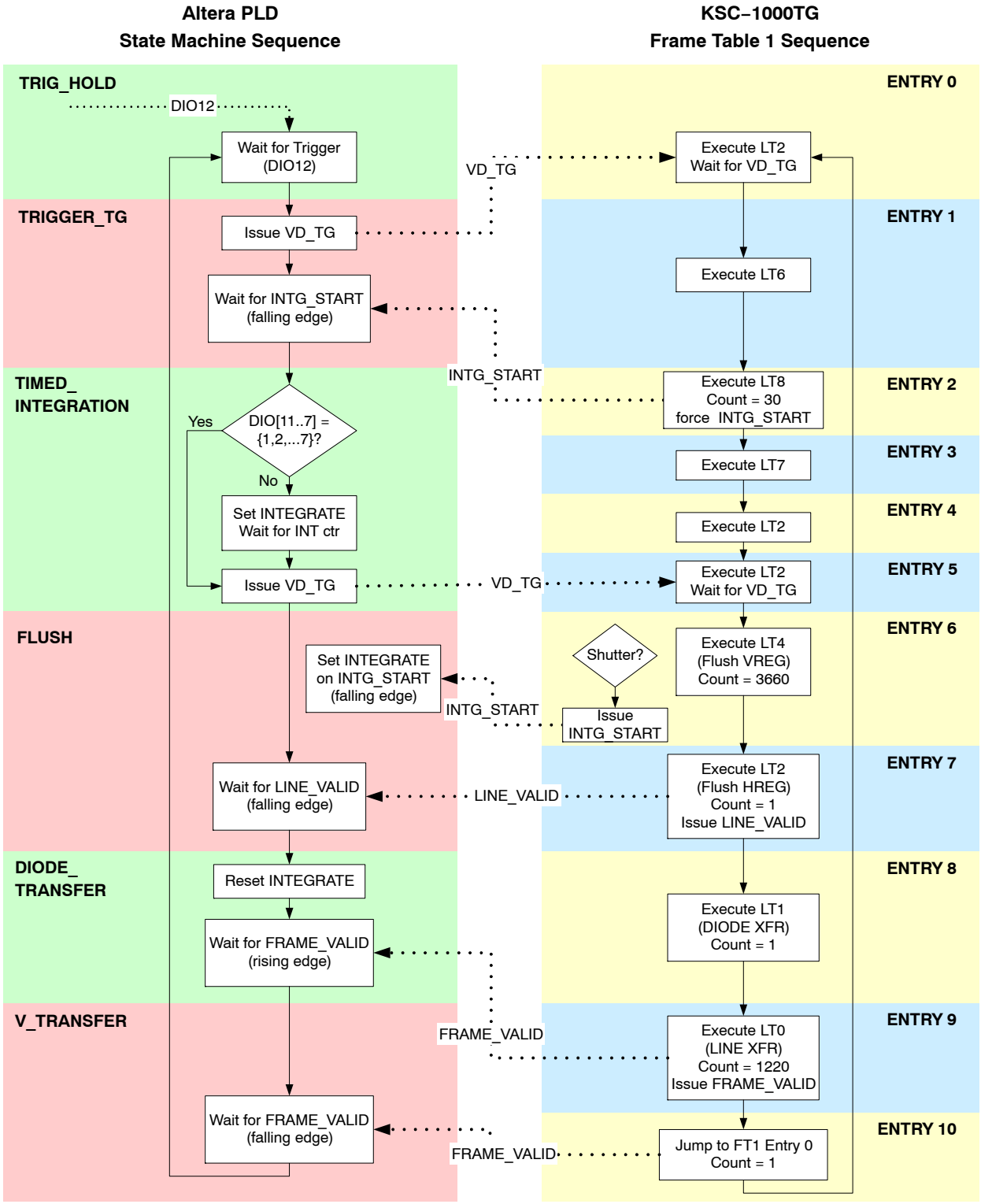


Figure 16. Still Capture Mode Timing Sequence

At this point, the KSC−1000 waits for the PLD to issue a VD_TG pulse when the Integration Counter expires. By default (DIO[11..7] = 0), the counter is set to 0 and the INTEGRATE pulse is set with the next rising edge of the 1 ms clock. For longer integration times, the Integration Counter may be set to a non-zero value, and millisecond increments of time are added to the Integration time (See Figure 28 and Table 30).

Depending on the DIO[11..7] inputs (See Table 30), the Integration period may include some or all of the VCCD Flush period. If the Electronic Shutter is used to achieve shorter integration times, the INTEGRATE pulse is not set until the end of the Shutter pulse. When the integration counter expires, the vertical and horizontal registers are flushed of accumulated charge. When the Timed Integration and Flush sequence is complete, the INTEGRATE pulse is reset, and the Photodiode transfer is followed by repeated Line Transfer sequences, until all the lines are read out.

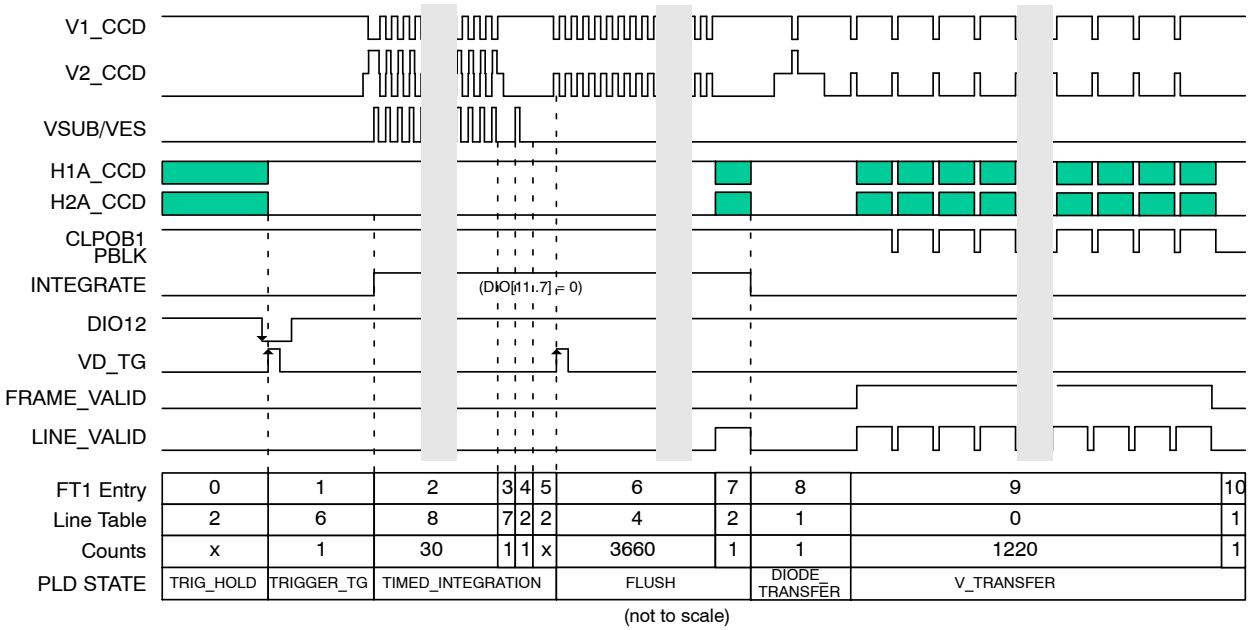


Figure 17. Frame Table 1 Default Timing

Frame Table 2 Sequence

Frame Table 2 contains the 2×2 Binning Mode timing sequence used to sum the charge collected in four photosites into one CCD pixel. The sequence is identical to that of Frame Table 0, except that the Vertical Clocks are asserted twice per line, which dumps charge from two vertical CCD pixels into each Horizontal register CCD pixel.

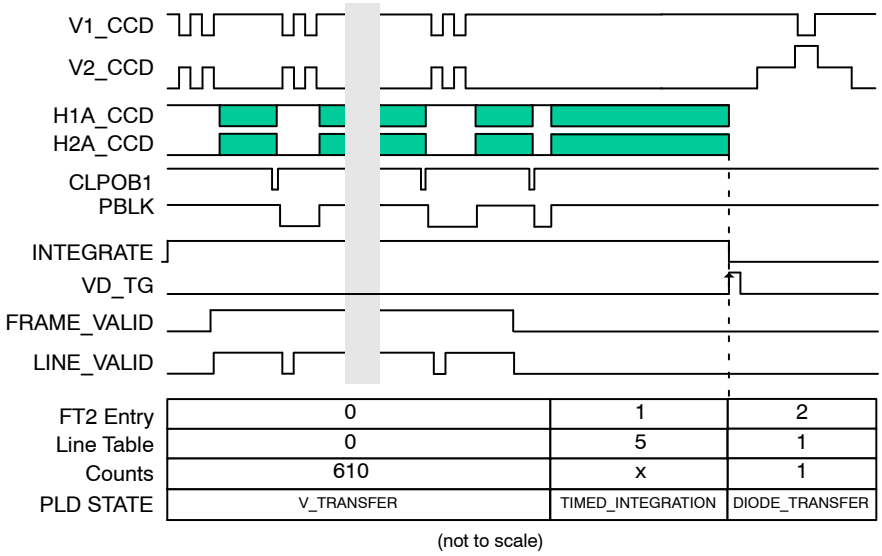


Figure 18. Frame Table 2 Default Timing

Electronic Shutter Timing

The electronic shutter timing is controlled by the values in Register 3 of the KSC−1000. There are two methods of actuating the Electronic Shutter pulse: by setting the *Integrate Start Pulse Line Number* value in Register 4 so that the pulse occurs on a specific line, or by setting the *Force INTG_START* bit in a Frame Table entry. In either case, the Electronic Shutter pulse setup, width, and hold times are determined by the values in Register 3. The shutter sequence is inserted before the specified line, causing that particular line time to be extended accordingly.

If the *Integrate Start Pulse Line Number* value in Register 4 is set to 0, the Electronic Shutter will occur immediately following the Diode Transfer sequence, before the first line is read out. If the *Integrate Start Pulse Line Number* value is greater than the number of vertical lines in the Frame Table, there will be no Electronic Shutter. This is the method used to disable the Electronic Shutter.

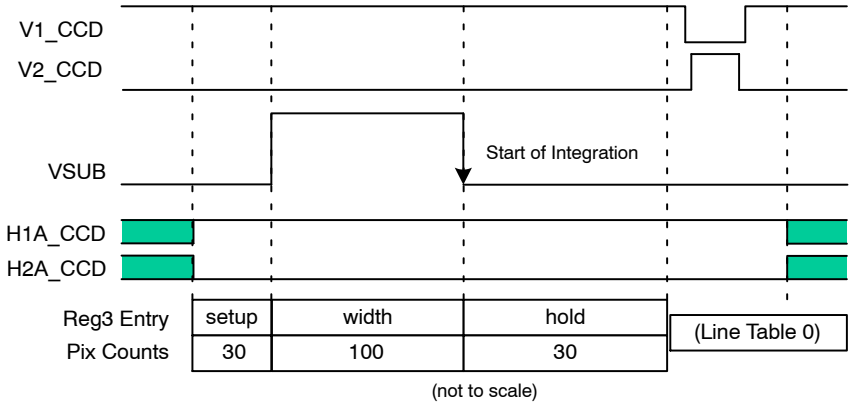


Figure 19. Electronic Shutter Timing

Horizontal Timing

Figure 20 depicts the basic theoretical relationship between the pixel-rate clocks to the CCD, the Video output of the CCD, and the pixel-rate clocks to the AFE.

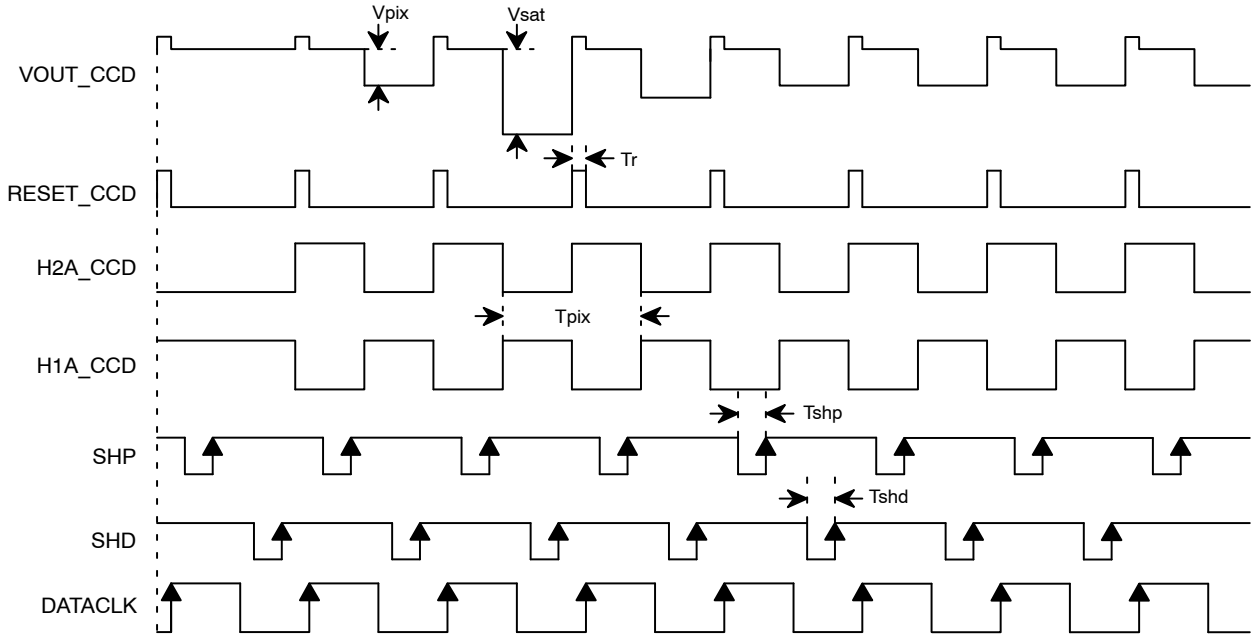


Figure 20. Horizontal Timing

Binning Mode Horizontal Timing

In order to sum the charge from two Horizontal CCD pixels into one, the Reset clock is suspended on alternating Horizontal clock cycles. In this way, two pixels of charge are dumped onto the floating diffusion of the output amplifier before this node is reset to VRD, the Reset Drain voltage. See the KAI−2001 and KAI−2020 Device Specifications (References) for further details.

In order to correctly convert the output amplifier voltage to digital data, the AFE clocks must be adjusted accordingly. The Clamp pulse (SHP) samples the output after the Reset pulse has been issued, but before the Horizontal clocks have moved charge onto the floating diffusion. The Sample pulse (SHD) samples the output after two Horizontal clock cycles have moved two charge packets onto the floating diffusion. The DATACLK then clocks the AFE to perform the conversion.

The KSC−1000 has the capability of implementing the Horizontal Timing necessary to bin up to four pixels. This feature is controlled by setting bits 3:4 of the active Frame Table (Register 8) in the KSC−1000. Figure 21 depicts the basic theoretical relationship between the pixel-rate clocks to the CCD, the Video output of the CCD, and the pixel-rate clocks to the AFE in 2x Horizontal Binning Mode.

The Altera PLD default KSC−1000 settings contain 2×2 Binning Mode timing in Frame Table 2 (See Figure 18). In order to activate the 2×2 Binning Mode, the Frame Table Pointer (Register 0) must be changed to a value of 2. This is done by setting SW2 HIGH and pressing the BOARD_RESET button (S1 on the Timing Board).

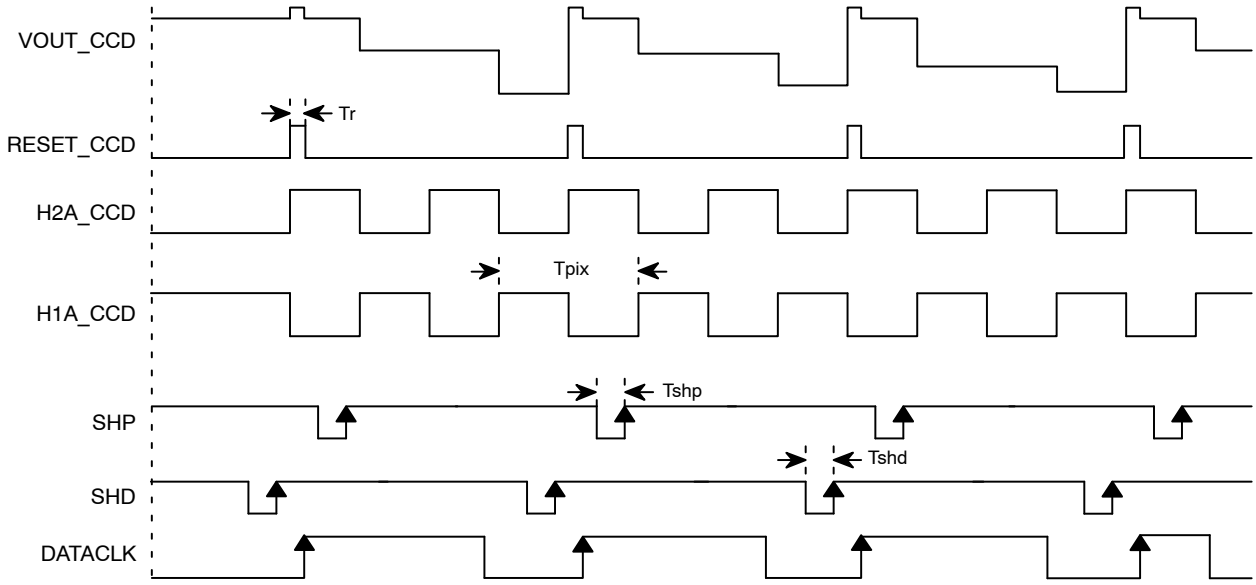


Figure 21. Binning Mode Horizontal Timing

Integration & Shutter Timing

Free-Running Mode

The default Integration Time in Free-Running Mode is approximately one Frame Time, or the time between Frame Transfers, during which the photodiodes are collecting charge. This time may be decreased by use of the Electronic Shutter, and may be increased by lengthening the Frame Time. The user may control the Integration Time through the DIO connector bits DIO[11..7]. This connector is optional, and when disconnected, all bits are pulled LOW. The available pre-programmed Integration Times are detailed in Table 30.

The Electronic Shutter is controlled by changing the Integrate Start Pulse Line Number value of the KSC−1000 Register 4. The Altera PLD has 8 pre-programmed Shutter settings, controlled through the DIO[11..7] bits, as shown in Table 14 and Table 30. These settings result in Integration times of one Frame Time or less, in increments of 1/8 of the Frame Time (See Figure 24). When the Integrate Start Pulse Line Number value is set to 4088, the Shutter is never pulsed, as this value exceeds the number of lines in a frame (Figure 23 and Figure 25). The BOARD_RESET switch must be pressed after changing the DIO[11..7] bits in order for the change to the KSC−1000 to take effect.

The Integration time is controlled by the Altera PLD. In Free-Running mode, the KSC−1000 waits for a trigger signal (VD_TG) before beginning the Diode Transfer sequence (See Figure 23). The Altera PLD issues this trigger pulse when the Integration Counter has reached a pre-programmed value, as shown in Table 30. The Integration counter is clocked by an internally-generated 1 ms clock. The default value of 0 means that the VD_TG trigger is issued on the next rising edge of the 1 ms clock after the frame readout is complete. A value greater than 0 adds that many milliseconds to the Integration Time, allowing Integration times greater than 8 seconds (Figure 25).

Table 30. PROGRAMMED INTEGRATION TIMES

DIO[11..7]	Int Count	Free-Run Mode Reg4 Entry	Free-Run Mode Tint(s)	Still Mode Reg4 Entry	Still Mode Tint(s)
0 (Default)	0	4088 (No Shutter)	0.105	4088 (No Shutter)	0.074
1	0	1064	0.013	3192	0.010
2	0	912	0.027	2736	0.019
3	0	760	0.040	2280	0.028
4	0	608	0.053	1824	0.037
5	0	456	0.066	1368	0.046
6	0	304	0.079	912	0.055
7	0	152	0.092	456	0.065
8	1	4088 (No Shutter)	0.106	4088 (No Shutter)	0.075
9	3	4088 (No Shutter)	0.108	4088 (No Shutter)	0.077
10	5	4088 (No Shutter)	0.110	4088 (No Shutter)	0.079
11	10	4088 (No Shutter)	0.115	4088 (No Shutter)	0.084
12	25	4088 (No Shutter)	0.130	4088 (No Shutter)	0.099
13	50	4088 (No Shutter)	0.155	4088 (No Shutter)	0.124
14	70	4088 (No Shutter)	0.175	4088 (No Shutter)	0.144
15	100	4088 (No Shutter)	0.205	4088 (No Shutter)	0.174
16	200	4088 (No Shutter)	0.305	4088 (No Shutter)	0.274
17	300	4088 (No Shutter)	0.405	4088 (No Shutter)	0.374
18	400	4088 (No Shutter)	0.505	4088 (No Shutter)	0.474
19	500	4088 (No Shutter)	0.605	4088 (No Shutter)	0.574
20	600	4088 (No Shutter)	0.705	4088 (No Shutter)	0.674
21	700	4088 (No Shutter)	0.805	4088 (No Shutter)	0.774
22	800	4088 (No Shutter)	0.905	4088 (No Shutter)	0.874
23	900	4088 (No Shutter)	1.005	4088 (No Shutter)	0.974
24	1000	4088 (No Shutter)	1.105	4088 (No Shutter)	1.074
25	2000	4088 (No Shutter)	2.105	4088 (No Shutter)	2.074
26	3000	4088 (No Shutter)	3.105	4088 (No Shutter)	3.074
27	4000	4088 (No Shutter)	4.105	4088 (No Shutter)	4.074
28	5000	4088 (No Shutter)	5.105	4088 (No Shutter)	5.074
29	6000	4088 (No Shutter)	6.105	4088 (No Shutter)	6.074
30	7000	4088 (No Shutter)	7.105	4088 (No Shutter)	7.074
31	8000	4088 (No Shutter)	8.105	4088 (No Shutter)	8.074

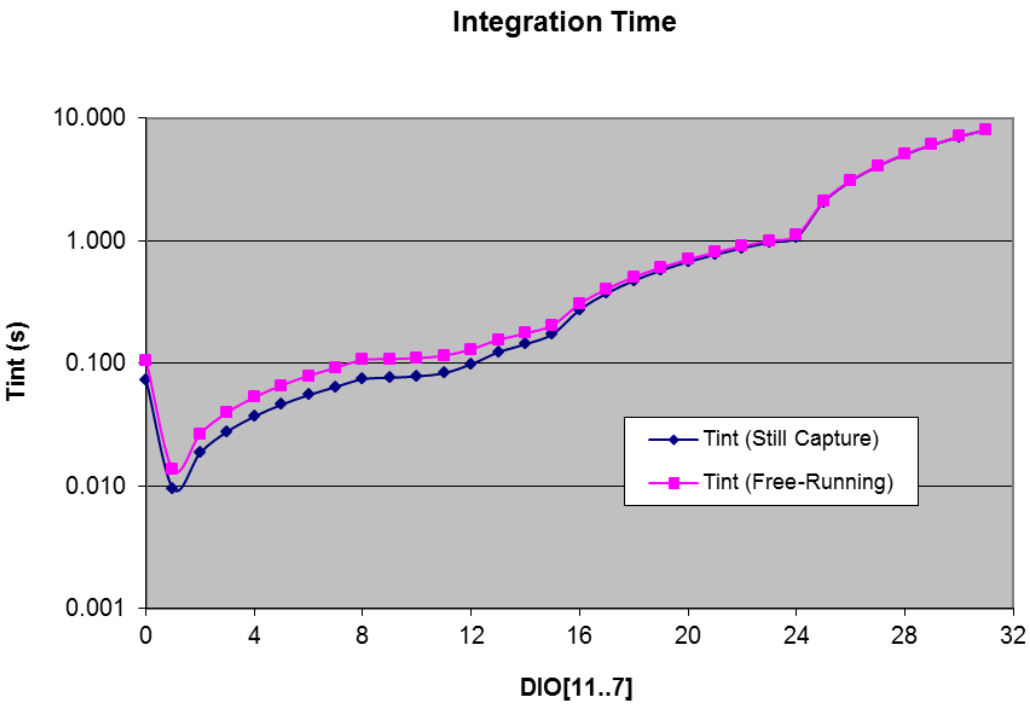


Figure 22. Programmed Integration Times

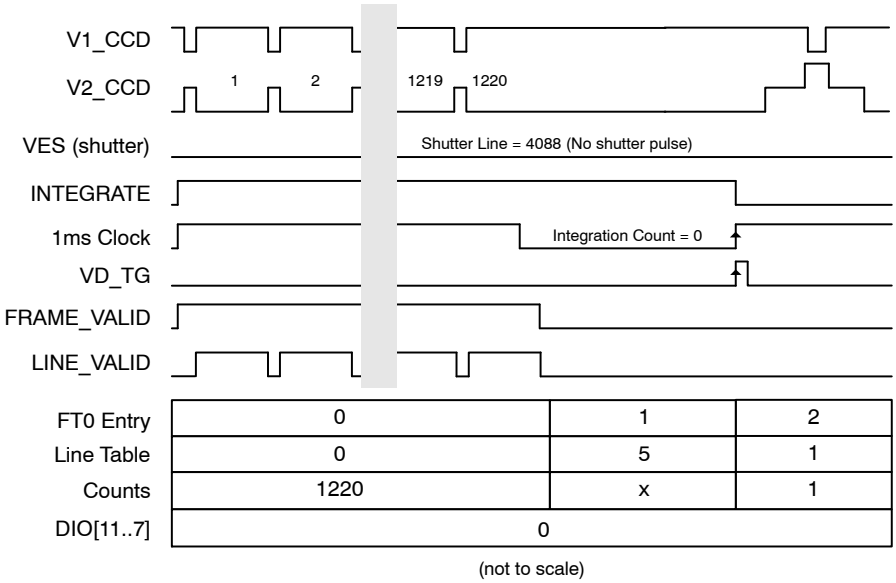


Figure 23. Free-Running Mode Default Integration Timing

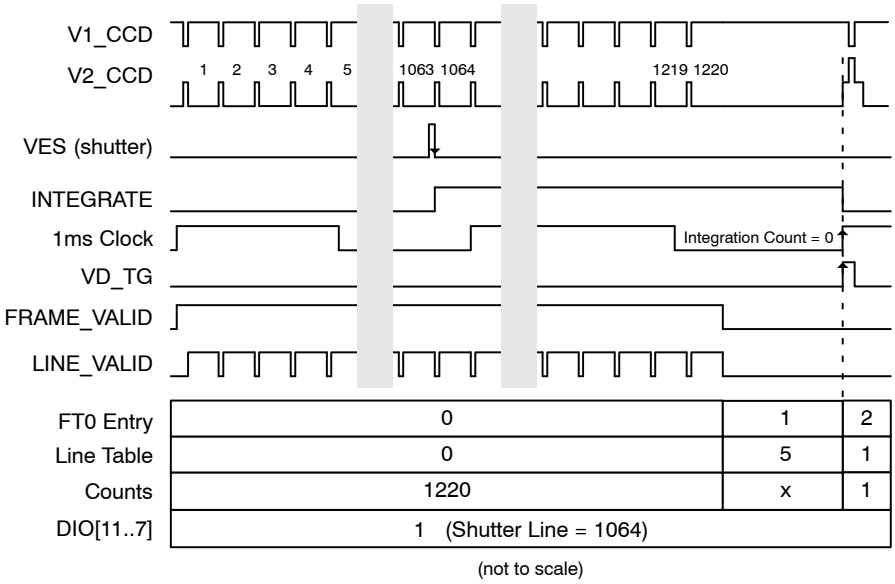


Figure 24. Free-Running Mode Integration Timing with Shutter

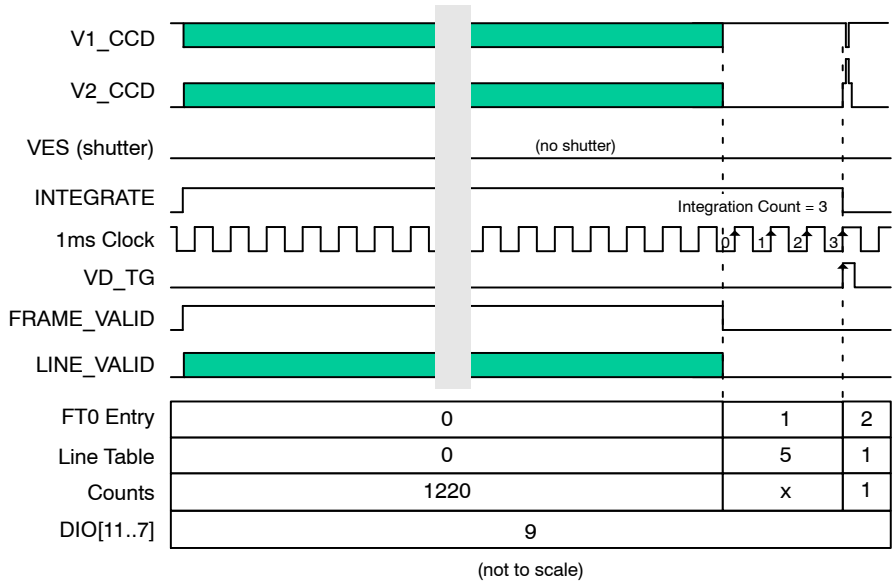


Figure 25. Free-Running Mode Extended Integration Timing

Still Capture Mode

The default Integration Time in Still Capture Mode is approximately equal to the Flush period, or the time required to Flush the Vertical and Horizontal Register of accumulated charge. In this case the Integration period begins at the end of the Electronic Shutter pulses which precede the Flush cycle. The Integration period may be increased by delaying the beginning of the Flush sequence; the user may control the Integration Time through the DIO connector bits DIO[11..7]. This connector is optional, and when disconnected, all bits are pulled LOW. The available pre-programmed Integration Times are detailed in Table 30.

As in Free-Running Mode, the Electronic Shutter is controlled by changing the *Integrate Start Pulse Line Number* value of the KSC−1000 Register 4. In Still Capture Mode, however, the Shutter is pulsed during the VCCD Flush cycle to control the Integration time. The Altera PLD has 8 pre-programmed Shutter settings, controlled through the DIO[11..7] bits, as shown in Table 14 and Table 30. These settings result in Integration times of one Flush Period or less, in increments of 1/8 of the Flush Period (See Figure 27). When the *Integrate Start Pulse Line Number* value is set to 4088, the Shutter is never pulsed during the Vertical Flush sequence, as this value exceeds the number of lines in a the Flush cycle (Figure 26 and Figure 28). The BOARD_RESET switch must be pressed after changing the DIO[11..7] bits in order for the change to the KSC−1000 to take effect.

The Integration time is controlled by the Altera PLD. In Still Capture mode, the KSC−1000 waits for a trigger signal (VD_TG) before beginning the Flush sequence (See Figure 26). The Altera PLD issues this trigger pulse when the Integration Counter has reached a pre-programmed value, as shown in Table 30. The Integration counter is clocked by an internally-generated 1 ms clock. The default value of 0 means that the VD_TG trigger is issued on the next rising edge of the 1 ms clock after the shutter pulse is complete. A value greater than 0 adds that many milliseconds to the Integration Time, allowing Integration times greater than 8 seconds (Figure 28).

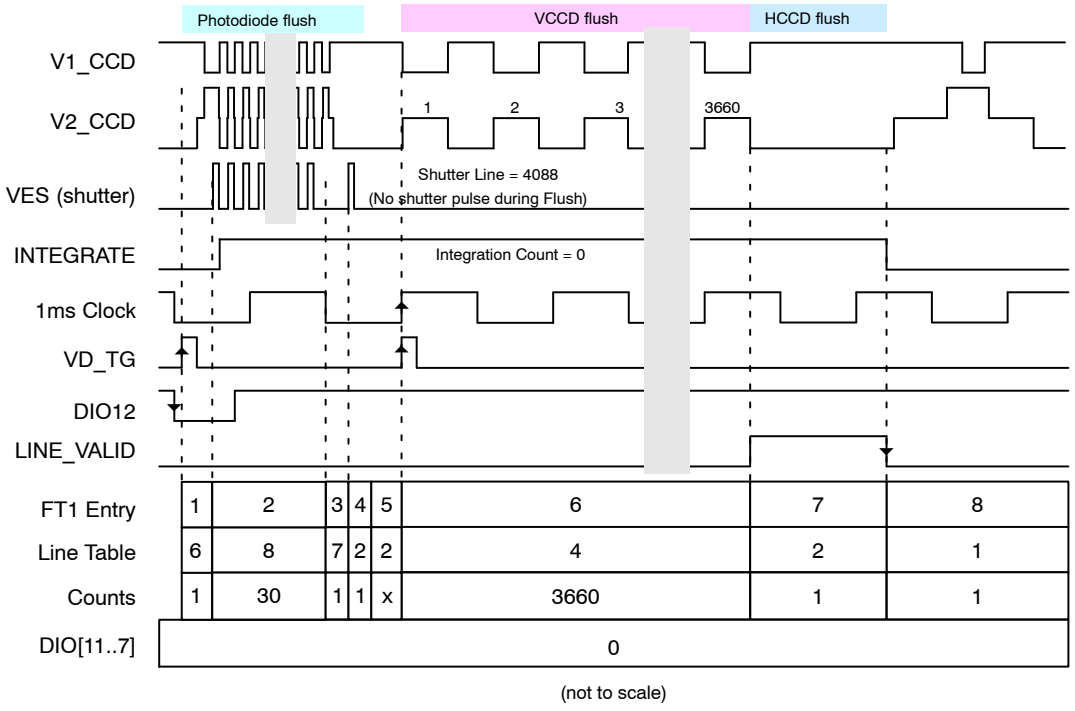


Figure 26. Still Capture Mode Default Integration Timing

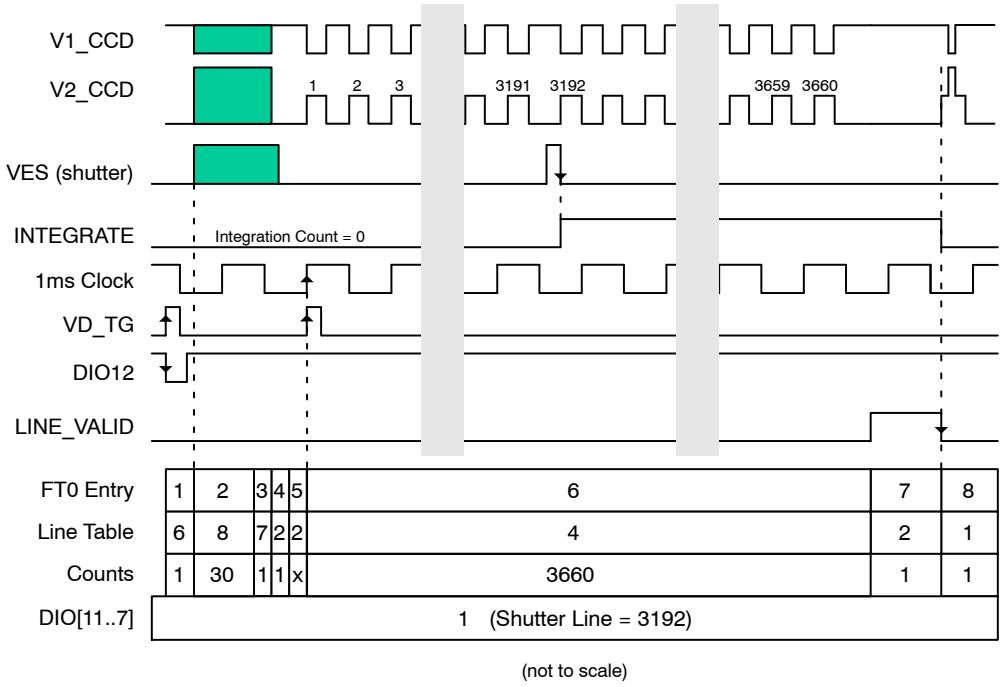


Figure 27. Still Mode Integration Timing with Shutter

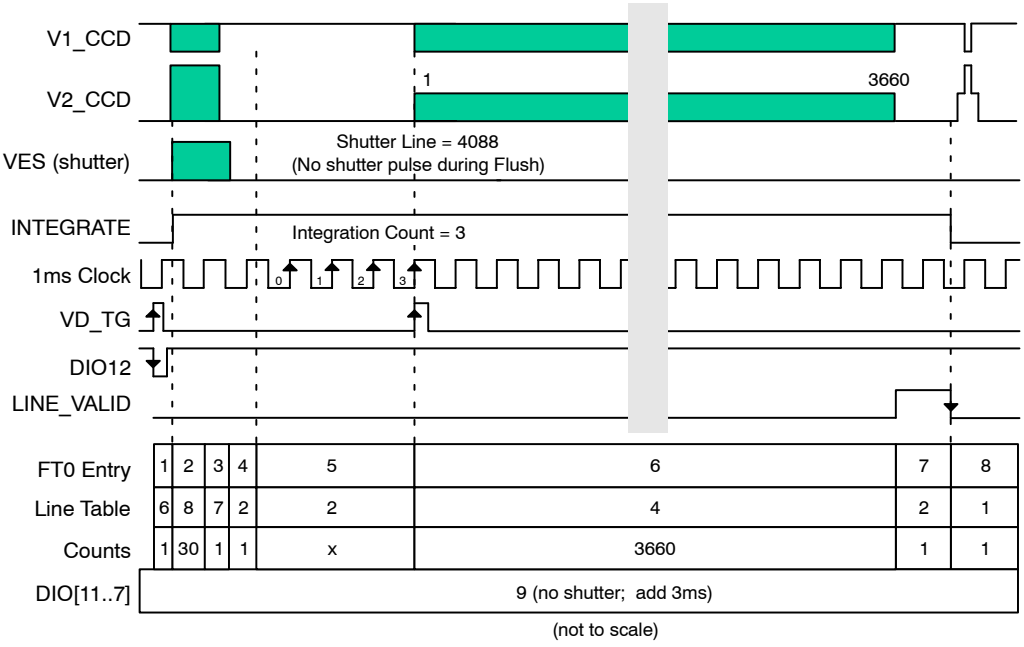


Figure 28. Still Mode Extended Integration Timing

BOARD INTERFACE CONNECTOR SIGNAL MAP

For reference, the board interface timing signals from the 3F5051 Timing Board to the 3F5121 Imager Board are shown in Table 31. Note that the power connections are not shown here.

Table 31. TIMING BOARD/IMAGER BOARD SIGNAL MAP

KSC−1000 Timing Board			KAI−2001/KAI2020 Imager Board		
KSC−1000 Signal Name	**LVDS Interface Signal Name**	**3F5051 J6 Pins**	**3F5121 J1 Pins**	**LVDS Interface Signal Name**	**Imager Board Signal Name**
V5	TIMING_OUT0	1/2	1/2		
INTG_START	TIMING_OUT1	5/6	5/6	IMAGER_IN11	VES
V6	TIMING_OUT2	9/10	9/10	IMAGER_IN10	FDG
V1	TIMING_OUT3	13/14	13/14	IMAGER_IN9	V3RD
V2	TIMING_OUT4	17/18	17/18	IMAGER_IN8	
V3	TIMING_OUT5	21/22	21/22	IMAGER_IN7	V2
V4	TIMING_OUT6	25/26	25/26	IMAGER_IN6	V1
RG	TIMING_OUT7	29/30	29/30	IMAGER_IN5	RESET
H1	TIMING_OUT8	33/34	33/34	IMAGER_IN4	H2B
H4	TIMING_OUT9	37/38	37/38	IMAGER_IN3	H2A
H2	TIMING_OUT10	41/42	41/42	IMAGER_IN2	H1B
H3	TIMING_OUT11	45/46	45/46	IMAGER_IN1	H1A
H6	TIMING_OUT12	51/52	51/52		
H5	TIMING_OUT13	55/56	55/56		
AMP_EN	TIMING_OUT14	59/60	59/60	IMAGER_IN0	AMP_ENABLE
SCLOCK	TIMING_OUT15	63/64	63/64	IMAGER_IN15	
SDATA	TIMING_OUT16	67/68	67/68	IMAGER_IN14	
PLD_OUT2	TIMING_OUT17	71/72	71/72	IMAGER_IN13	
PLD_OUT0	TIMING_OUT18	75/76	75/76	IMAGER_IN12	VIDEO_SWITCH
PLD_OUT1	TIMING_OUT19	79/80	79/80		

VIDEO SIGNAL PATH

The entire video signal path through the Imager Board and Timing Board is represented in Figure 29. The individual blocks are discussed in the Imager Board User Manual and the Timing Board User Manual.

The hardware gain for the entire pre-AFE signal path can be calculated by multiplying the gains of the individual stages:

$$0.96 \times 1.25 \times 0.5 \times 1.25 = 0.75 \qquad \text{(eq. 1)}$$

The gain of the hardware signal path is designed so that the saturation output voltage of the KAI−2001/KAI−2020 CCD will not overload the AFE input. The AFE default PXGA gain is set at 1.0 (0.0 dB), and the default VGA gain is set to maximize the dynamic range of the AFE (See Table 9 and References).

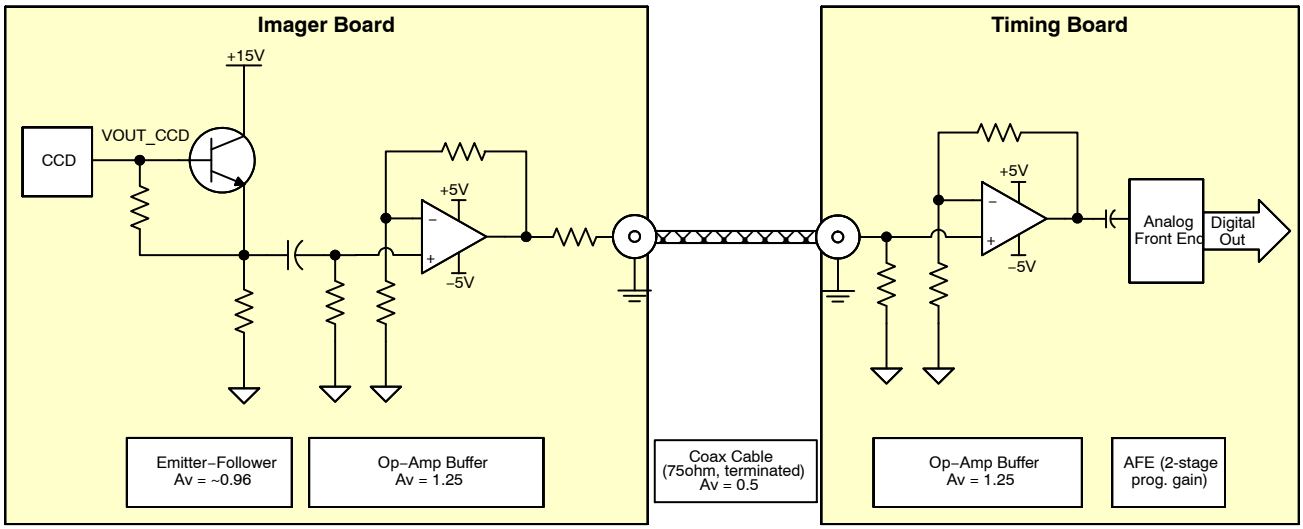


Figure 29. Video Signal Path Block Diagram

WARNINGS AND ADVISORIES

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of a ON Semiconductor Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, Truesense Imaging. Changes to the firmware are at the risk of the customer.

ORDERING INFORMATION

Please address all inquiries and purchase orders to:

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Phone: (585) 784−5500
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ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

REFERENCES

[1] KAI−2020 Device Specification
[2] KAI−2001 Device Specification
[3] KAI−2001/KAI−2020/KAI−2093 Imager Board User Manual
[4] KAI−2001/KAI−2020/KAI−2093 Imager Board Schematic
[5] KSC−1000 Timing Generator Board User Manual
[6] KSC−1000 Timing Generator Board Schematic
[7] Analog Devices AD9845 Product Data Sheet (20, 24, 28, 30 MHz operation)

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