IS32LT3181

RCL DUAL INTENSITY, SIX CHANNEL LED DRIVER WITH FAULT DETECTION

August 2022

GENERAL DESCRIPTION

The IS32LT3181 is a six channels linear current regulator for automotive rear tail light applications such as RCL (Rear Combination Lamps) and CHMSL (Center High Mounted Stop Lamps). It is fully programmable with two LED brightness levels for the different intensity requirements of “stop” bright (DC mode) and “tail” dim (PWM mode).

A logic level at the PWM pin is used to select between the tail and stop output conditions. The stop condition provides the highest intensity output, while the tail condition utilizes an internally generated PWM signal to reduce the intensity of the LEDs’ light output.

An active low fault output signal reports a device error condition. The FAULTB pin of several devices can be tied together to disable all the output stages when a fault is detected by any one of the devices.

The sink current at the OUTx pins is easily set with a single resistor at the STOP pin. The constant-current sink outputs can be combined in parallel to create higher current-driving capability on a single string. A second resistor at the TAIL pin sets the duty cycle of the internal PWM oscillator for dimming the LED output when operating in the tail condition.

An external FET (optional) can be implemented for operation with wide varying supply voltages to minimize device thermal dissipation.

The IS32LT3181 is offered in an eTSSOP-16 package.

FEATURES

- Operating voltage from 6V to 42VDC
  - Withstand 50V load dump
- 6 constant-current channel sinks
  - Adjustable from 10mA to 75mA per channel
  - Channel paralleling for higher current
  - Low dropout voltage of 0.8V@35mA
  - Slew rate control on each output for better EMI performance
- Integrated PWM dimming engine provides two LED brightness levels without external logic
  - Tail duty cycle programmable from 1% to 95%
  - PWM logic level input selects between full brightness and PWM dimming levels
- Support for optional FET to minimize device power consumption
- Open Drain FAULTB reporting pin
  - Programmable FAULTB delay time
  - Programmable UVLO threshold
  - LED open circuit detection
  - STOP pin over current protection
  - Over temperature protection
- Device disable upon fault detection
  - Parallel connection to other devices
- AEC-Q100 qualification
- RoHS & Halogen-Free compliant (Pb-free) package

APPLICATIONS

- Rear Combinational Lamp (RCL)
- Center High Mount Stop Light (CHMSL)
- Daytime running lamp
- Fog lamps
- Turn signal

TYPICAL APPLICATION CIRCUIT

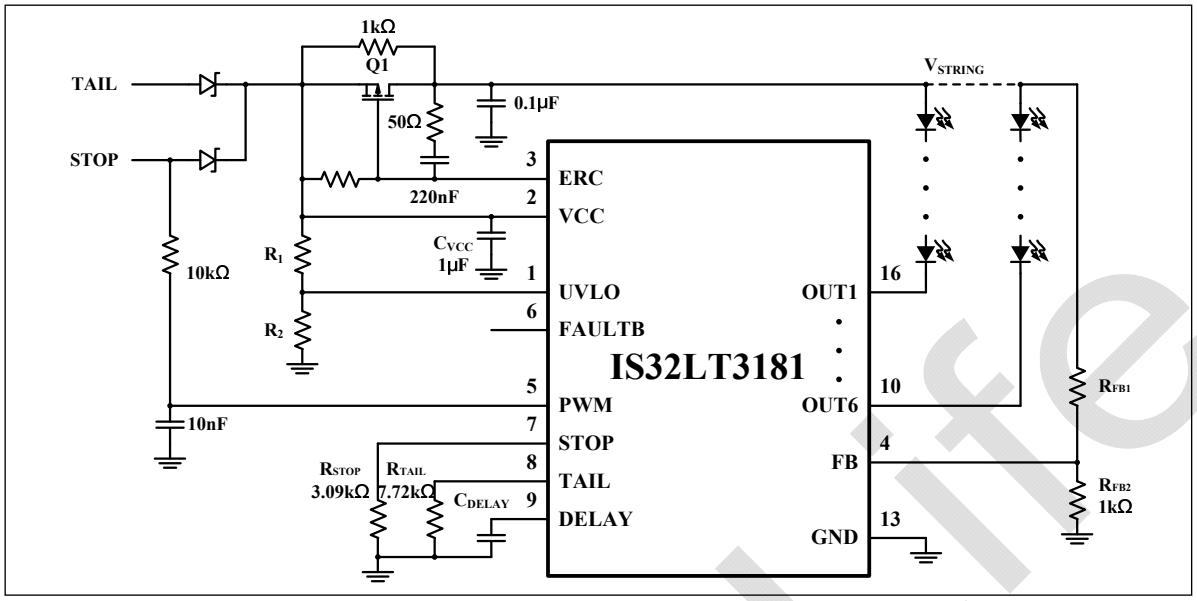


Figure 1 Typical Application Circuit

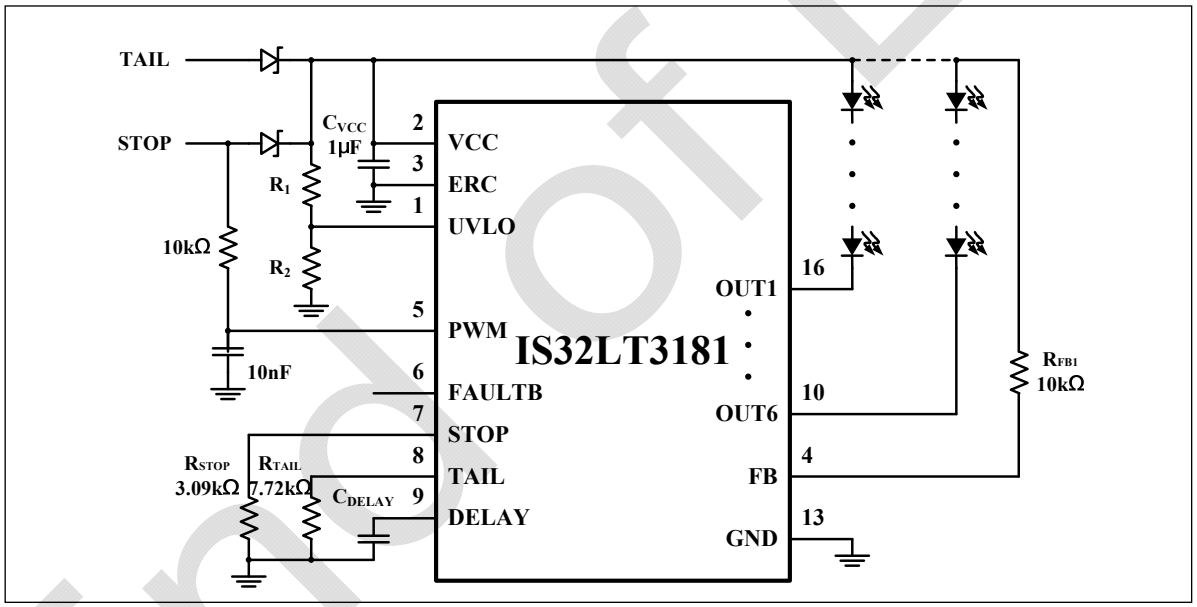


Figure 2 Typical Application Circuit (Without External FET)

TYPICAL APPLICATION CIRCUIT (CONTINUE)

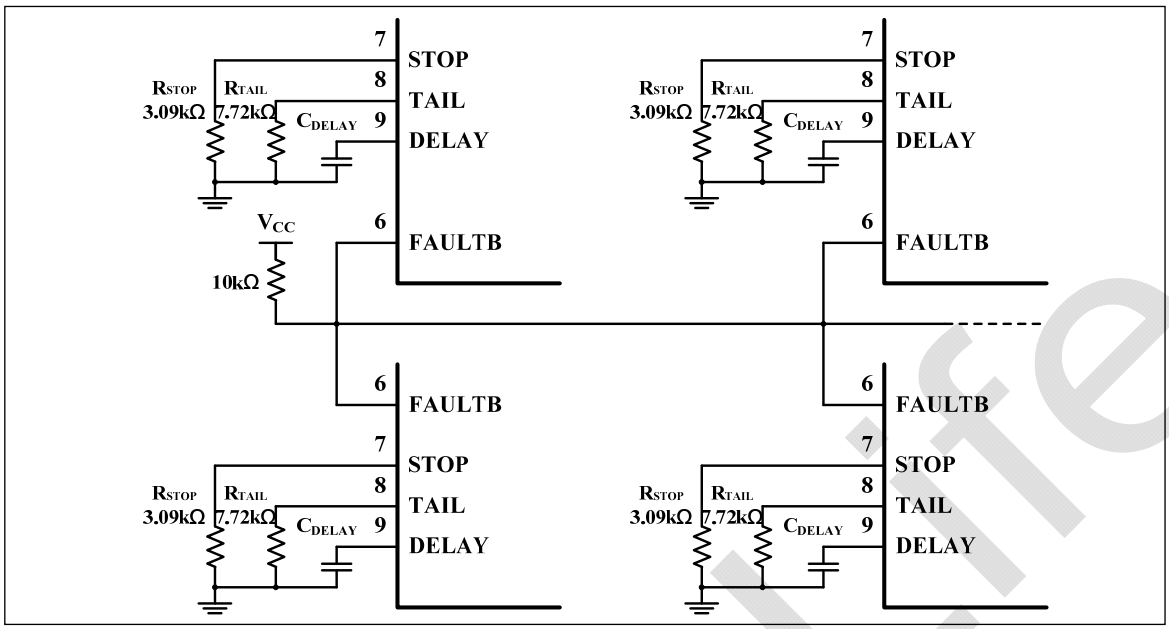
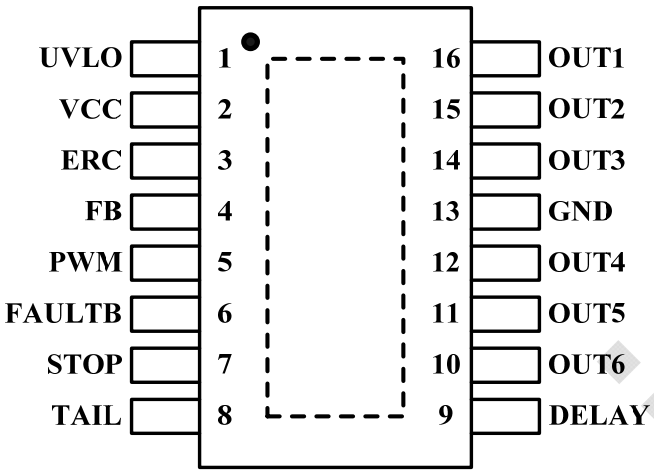


Figure 3 Several Devices Connect FAULTB Pin In Parallel

PIN CONFIGURATION

Package	Pin Configuration (Top view)
eTSSOP-16	

PIN DESCRIPTION

No.	Pin	Description
1	UVLO	A resistive voltage divider from VCC to GND sets the under voltage lockout to prevent false triggering during power up.
2	VCC	Power input for the IC.
3	ERC	External regulator control output. Drive the gate of an external PMOS FET to operate it in linear voltage regulator mode.
4	FB	Reference input voltage for the external resistor divider (1.05V typical) for voltage regulation. If no external PMOS FET is used then connect to VCC with a 10k ohm resistor.
5	PWM	Digital logic input. Logic high to select full intensity (DC output current) and logic low (or floating) to select lower intensity (PWM output current).
6	FAULTB	Active low open drain fault flag to indicate error condition. This pin can be connected to other device FAULTB pins to disable LED array under a fault condition.
7	STOP	Resistor to GND on this pin globally sets the maximum sink current for each LED channel.
8	TAIL	Resistor to GND on this pin sets the duty cycle of the internally generated PWM signal which determines the lower LED intensity TAIL condition.
9	DELAY	Capacitor to GND on this pin sets a delay time before fault reporting. The minimum capacitor value is 10pF. This pin CANNOT be left floating.
10~12	OUT6 ~OUT4	Output current sink channel 6~4.
13	GND	Ground connection for the IC.
14~16	OUT3 ~ OUT1	Output current sink channel 3~1.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Automotive Range: -40°C To +125°C

Order Part No.	Package	QTY
IS32LT3181-ZLA3-TR IS32LT3181-ZLA3	eTSSOP-16, Lead-free	2500/Reel 96/Tube

ABSOLUTE MAXIMUM RATINGS

UVLO, VCC, ERC, PWM, FAULTB, OUTx, FB, DELAY	-0.3 to 50V
TAIL, STOP	-0.3 to 5.5V
OUTx current	100mA
Operating junction temperature, T_J	150°C
Storage temperature range, T_{STG}	-55°C ~ +150°C
Operating ambient temperature range, $T_J = T_A$	-40°C ~ +150°C
Package thermal resistance (Junction to ambient), θ_{JA}	39.9°C/W
Power dissipation, $P_{D(MAX)}$ (Note 2)	3.1W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Refer to Figure 29, package power derating curve on Page 15.

ELECTRICAL CHARACTERISTICS

Valid are at T_J = -40°C ~+150°C, V_{CC} = 6V~16V, R_{STOP} =3.09kΩ, R_{TAIL} =7.72kΩ, unless otherwise noted (Note 3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		6		42	V
I_{CC}	Input current	I_{OUTx} =35mA, V_{CC} =16V, 6 channels T_J = -40°C ~+125°C		6.0	8.0	mA
		T_J = +150°C (Note 5)		6.0		
I_{OUT_MAX}	Maximum sink current	V_{OUTx} =1.2V	75			mA
I_{OUTACC}	Sink current accuracy	I_{OUTx} = 35mA = (I_{OUT_MAX}+I_{OUT_MIN})/2 V_{OUTx} = 0.8V, T_J = -40°C ~+125°C (Note 4)	-10	0	10	%
		T_J = +150°C	-12	0	12	
ΔI_{OUT}	Current matching	1-2×I_{OUT}/(I_{OUT_MAX}+I_{OUT_MIN}) I_{OUTx} =35mA, T_J = -40°C ~+125°C	-5	0	5	%
		T_J = +150°C	-7	0	7	
I_L	Current leakage	V_{OUTx} =42V			1	μA
L_R	Line regulation	6V< V_{CC} <16V, 0.8V<V_{OUTx}<3V I_{OUTx} = 35mA, 6 channels T_J = -40°C ~+125°C		0.6	4	mA
V_{OC}	Open LED detection threshold		0.3	0.45	0.6	V
V_{TH}	Output disable threshold			100	250	mV
R_{CS}	Current slew rate	I_{OUTx} = 35mA, 10%~90% T_J = -40°C ~+125°C		5	20	mA/μs
		T_J = +150°C (Note 5)		5		

ELECTRICAL CHARACTERISTICS (CONTINUE)

Valid are at T_J = -40°C ~+150°C, V_{CC} = 6V~16V, R_{STOP} =3.09kΩ, R_{TAIL} =7.72kΩ, unless otherwise noted (Note 3)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{SD}	Thermal shutdown Threshold	(Note 5)	150	160		°C
T_{SD_HY}	Thermal hysteresis	(Note 5)		15		°C
V_{FAULTB}	FAULTB pin voltage	Sink current = 5mA		0.1	0.2	V
V_{FAULT_H}	FAULTB pin high enable threshold	Voltage rising			2	V
V_{FAULT_L}	FAULTB pin low disable threshold	Voltage falling	0.6			V
V_{UVLO_TH}	FAULTB reporting under voltage locked out threshold	Voltage rising	1.1	1.2	1.35	V
V_{UVLO_HY}	Hysteresis of UVLO			100		mV
V_{DELAY}	DELAY pin voltage threshold		1.1	1.2	1.35	V
I_{DELAY}	DELAY pin source current		1.5	2	2.5	μA
I_{LF}	FAULTB pin input leakage current	V_{FAULTB} = 20V		0.1	1	μA
V_{PWM_H}	PWM high threshold			1.9	2.2	V
V_{PWM_L}	PWM minimum threshold		0.7	1.0		V
V_{FB}	FB regulation voltage		0.95	1.05	1.15	V
I_{ERC}	ERC drive current	V_{ERC} ≥ 3V	5	6		mA
V_{STOP}	STOP pin output voltage	T_J = -40°C ~+125°C (Note 4)	1.05	1.08	1.11	V
	STOP pin current to I_{OUTx}	(Note 4)		100		A/A
I_{TAIL}	TAIL pin output current		90	100	110	μA
	PWM accuracy	Duty cycle set to 5%, V_{TAIL} = 0.6V	2.5	5	7.5	%
		Duty cycle set to 50%, V_{TAIL} = 2.4V	45	50	55	%
		Duty cycle set to 80%, V_{TAIL} = 3.6V	70	80	90	%
t_{ON}	Turn-on delay	V_{CC} =0V step to V_{CC} =12V, the delay between 0.9×V_{CC} with 0.9×I_{OUTx}		1	2	ms
t_{PWM}	PWM on delay	V_{CC} =12V V_{PWM} =12V step to V_{PWM} =0V		50	100	μs
f_{PWM}	PWM frequency	V_{PWM} = 0V		1		kHz

Note 3: All parts are production tested at T_J = -40°C ~ +150°C, unless otherwise noted. Other temperature limits are guaranteed by design.

Note 4: Accuracy of the STOP pin output voltage need not meet the specification so long as the output current accuracy specification over the full programmable current range can be guaranteed.

Note 5: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

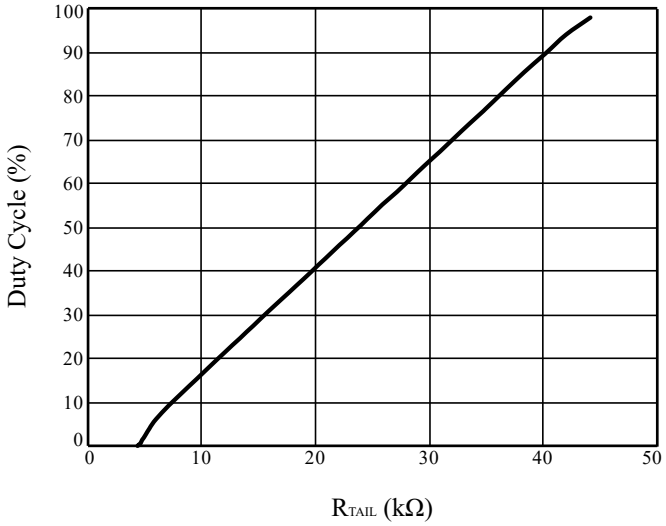


Figure 4 Duty Cycle vs. R_{TAIL}

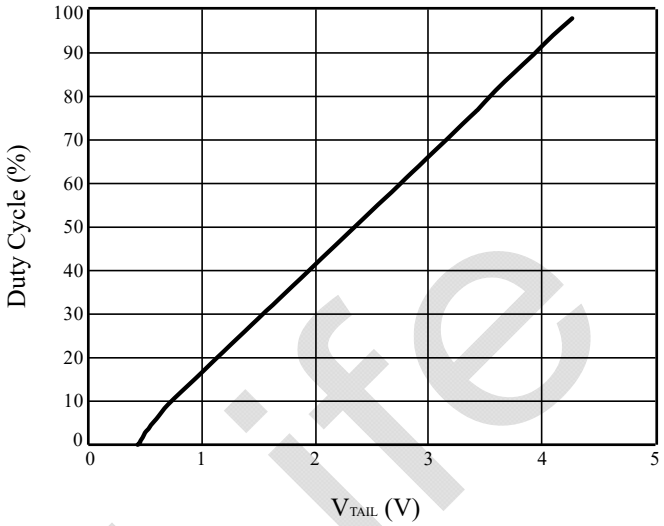


Figure 5 Duty Cycle vs. V_{TAIL}

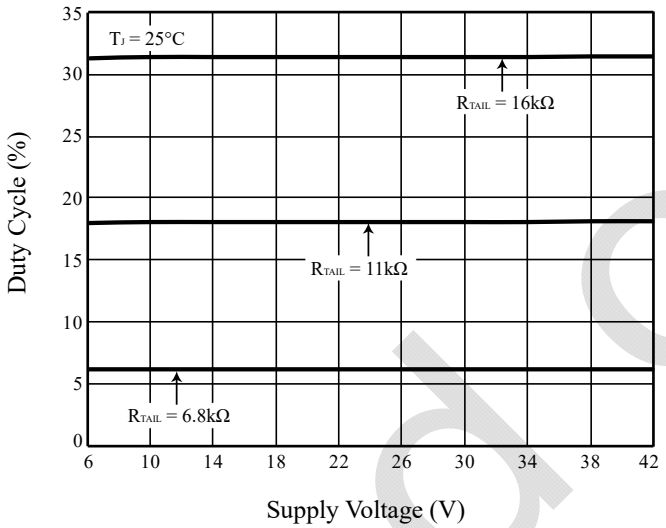


Figure 6 Duty Cycle vs. Supply Voltage

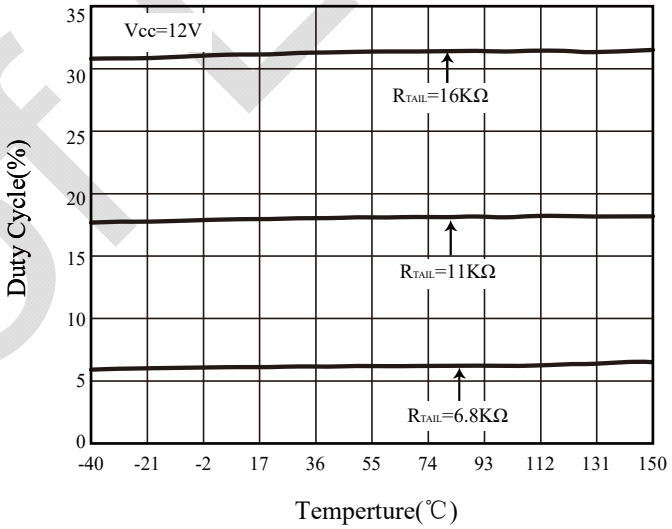


Figure 7 Duty Cycle vs. Temperature

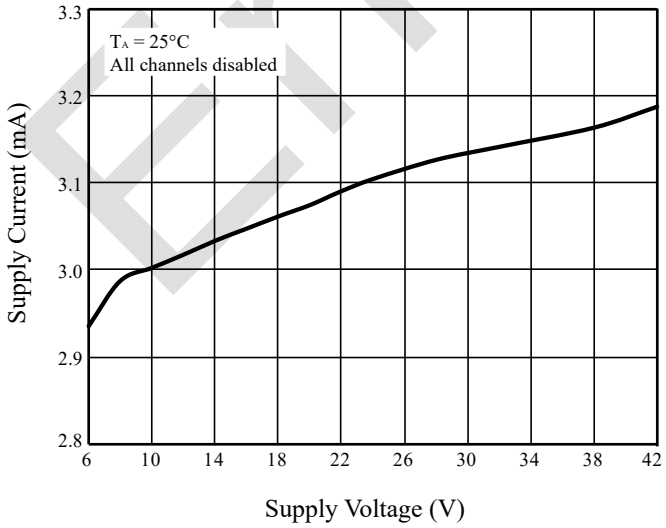


Figure 8 Supply Current vs. Supply Voltage

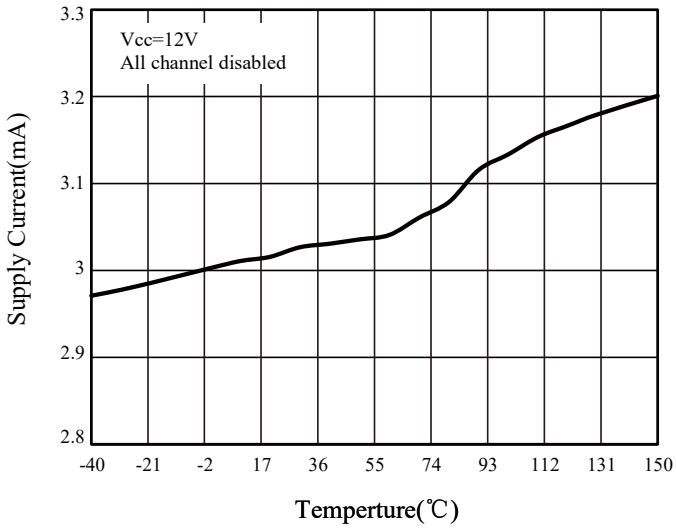


Figure 9 Supply Current vs. Temperature

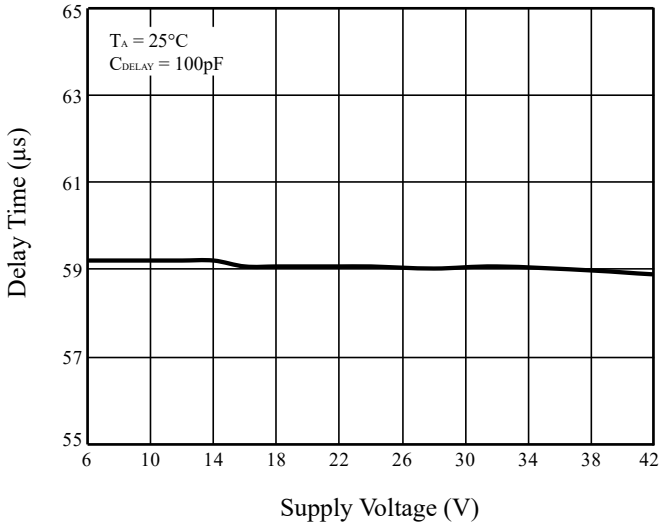


Figure 10 Delay Time vs. Supply Voltage

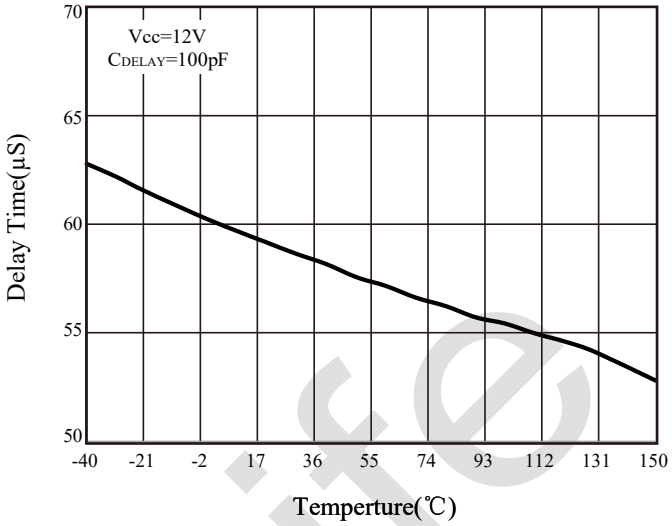


Figure 11 Delay Time vs. Temperature

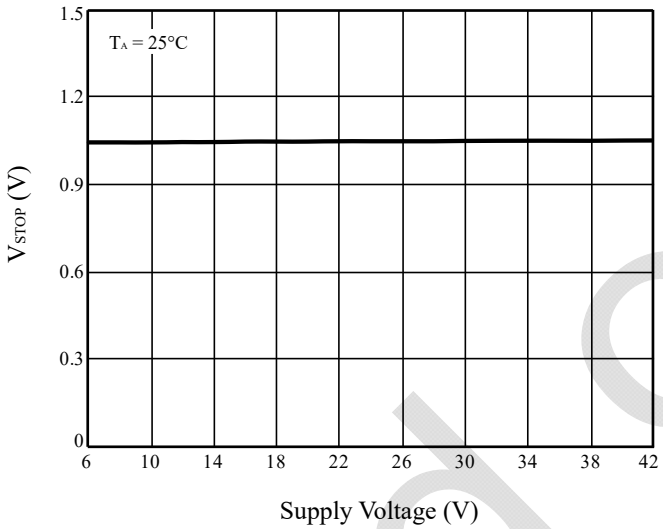


Figure 12 V_{STOP} vs. Supply Voltage

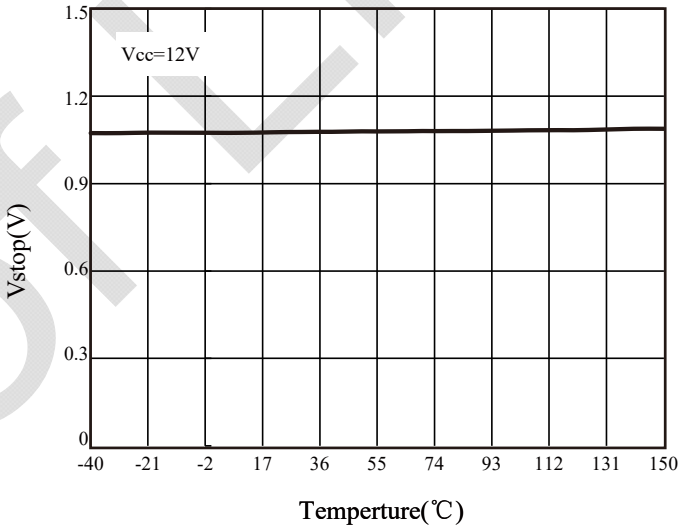


Figure 13 V_{STOP} vs. Temperature

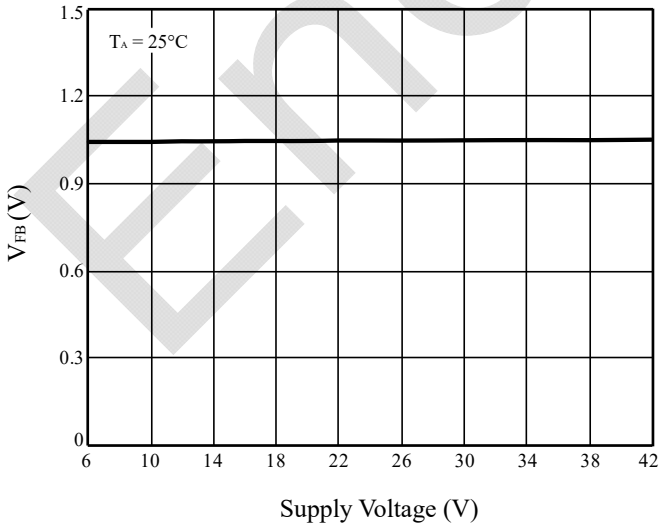


Figure 14 V_{FB} vs. Supply Voltage

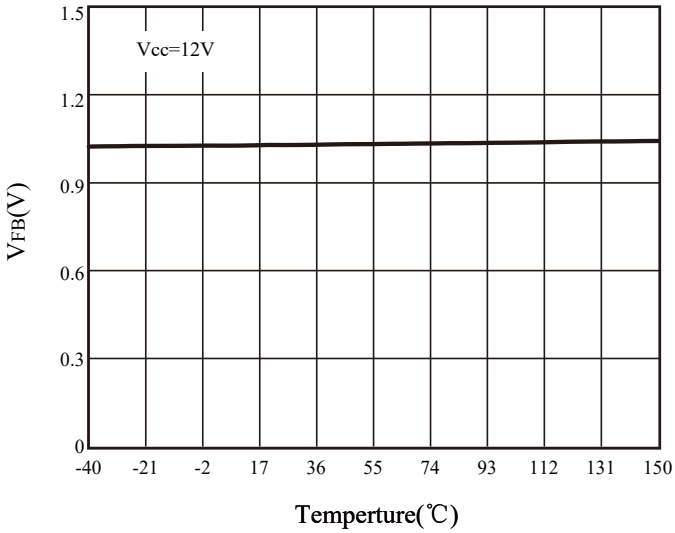


Figure 15 V_{FB} vs. Temperature

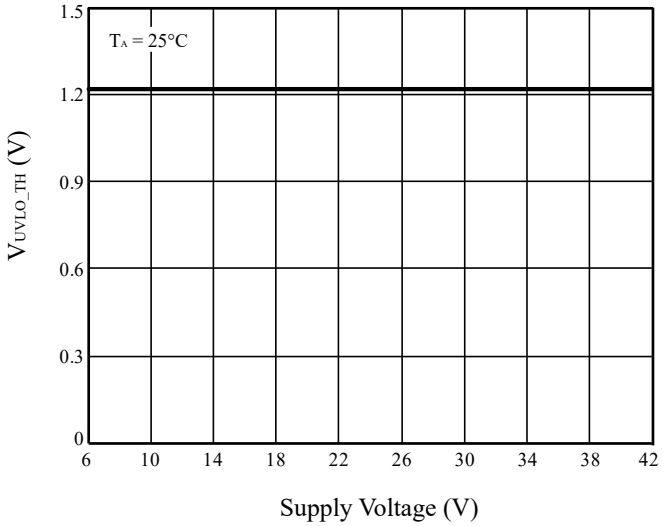


Figure 16 V_{VULO_TH} vs. Supply Voltage

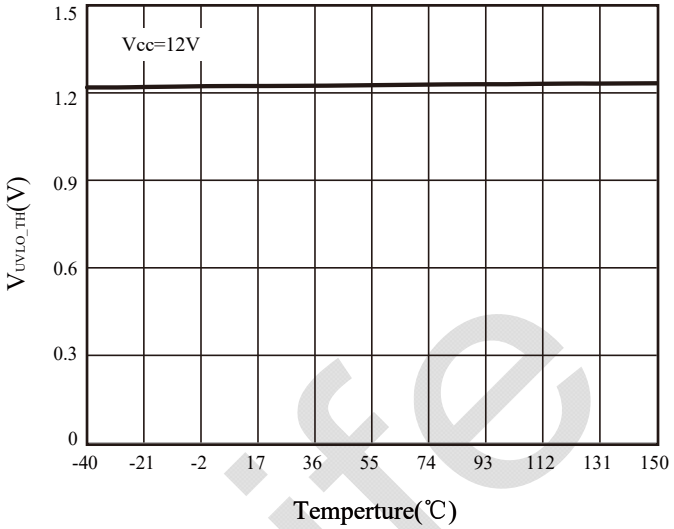


Figure 17 V_{UVLO_TH} vs. Temperature

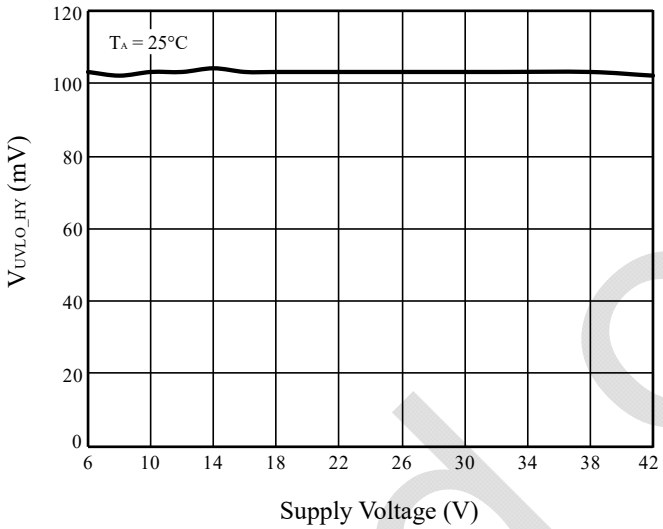


Figure 18 V_{VULO_HY} vs. Supply Voltage

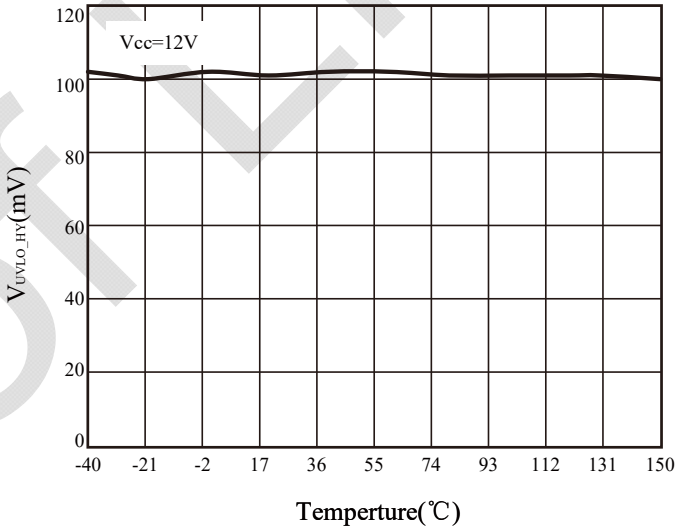


Figure 19 V_{UVLO_HY} vs. Temperature

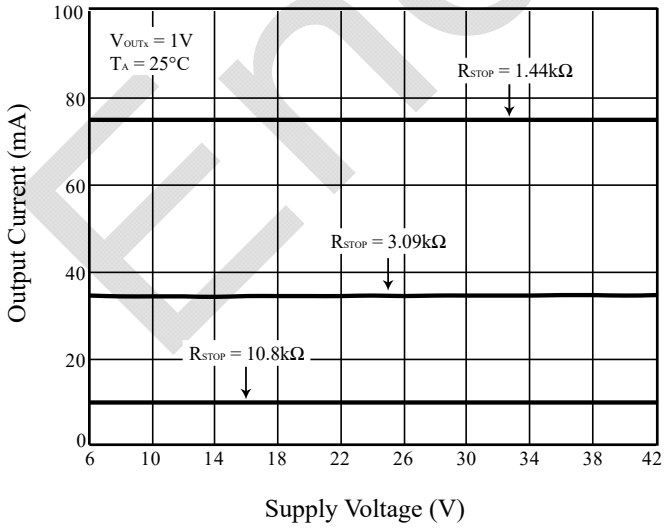


Figure 20 Output Current vs. Supply Voltage

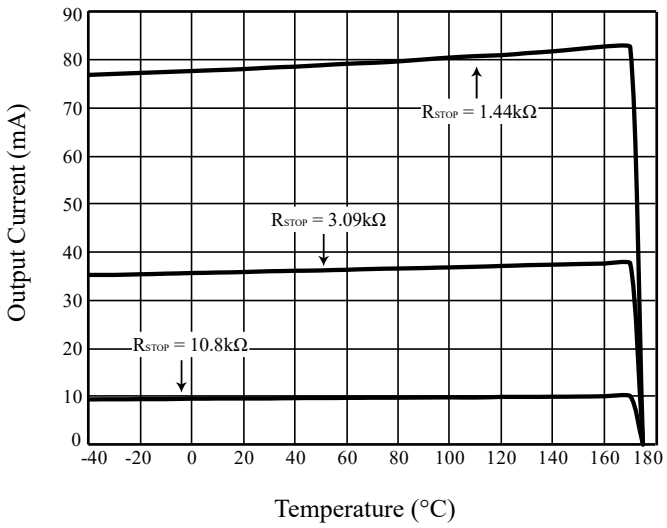


Figure 21 Output Current vs. Temperature

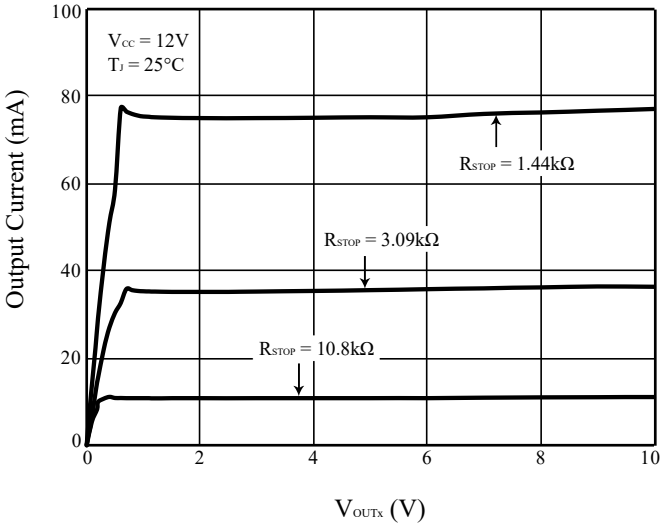


Figure 22 Output Current vs. V_{OUTx}

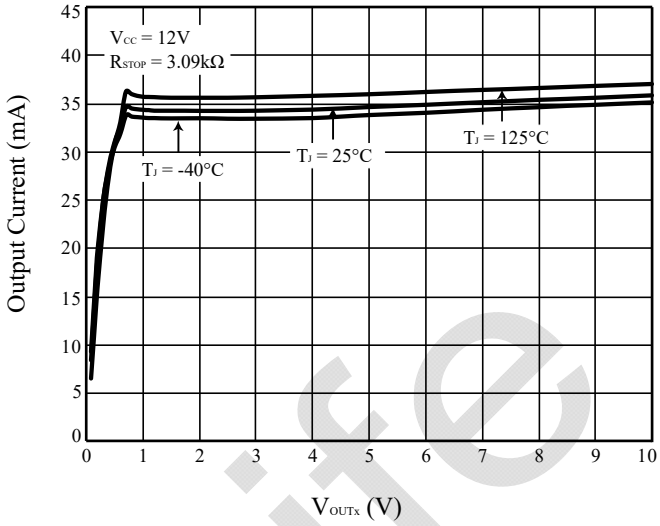


Figure 23 Output Current vs. V_{OUTx} (for Different T_j)

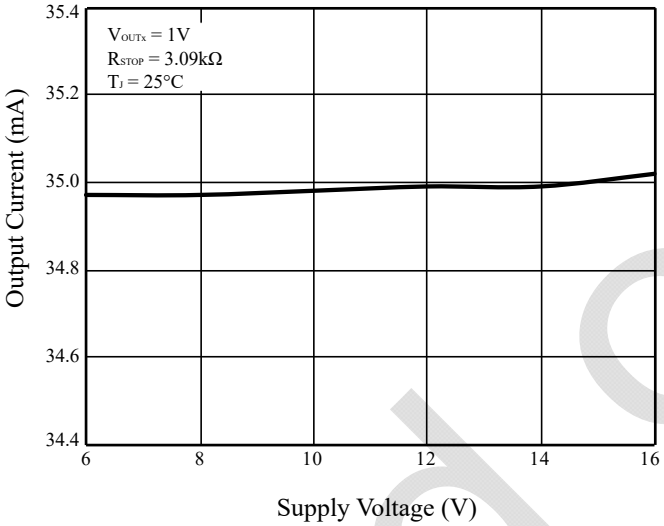


Figure 24 Output Current vs. Supply Voltage (Low Voltage)

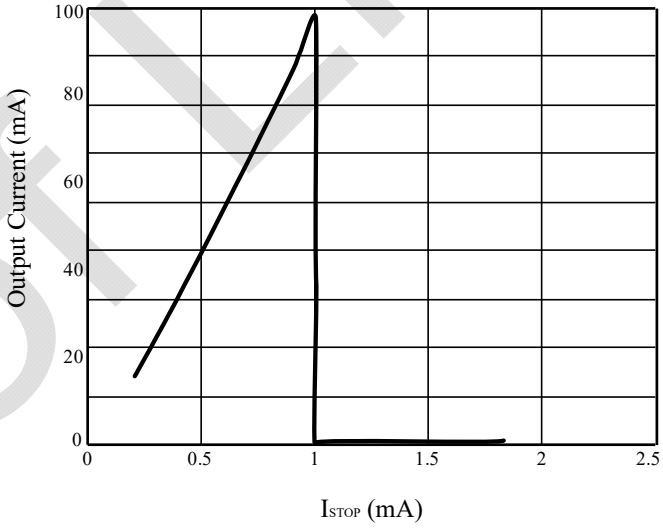


Figure 25 Output Current vs. I_{STOP}

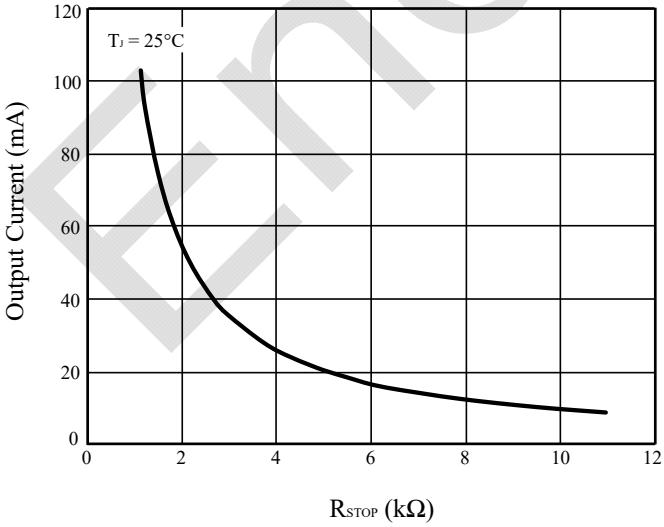


Figure 26 Output Current vs. R_{STOP}

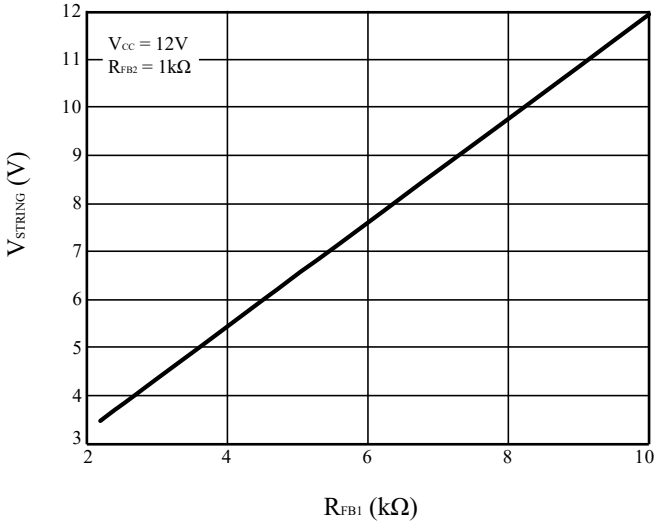
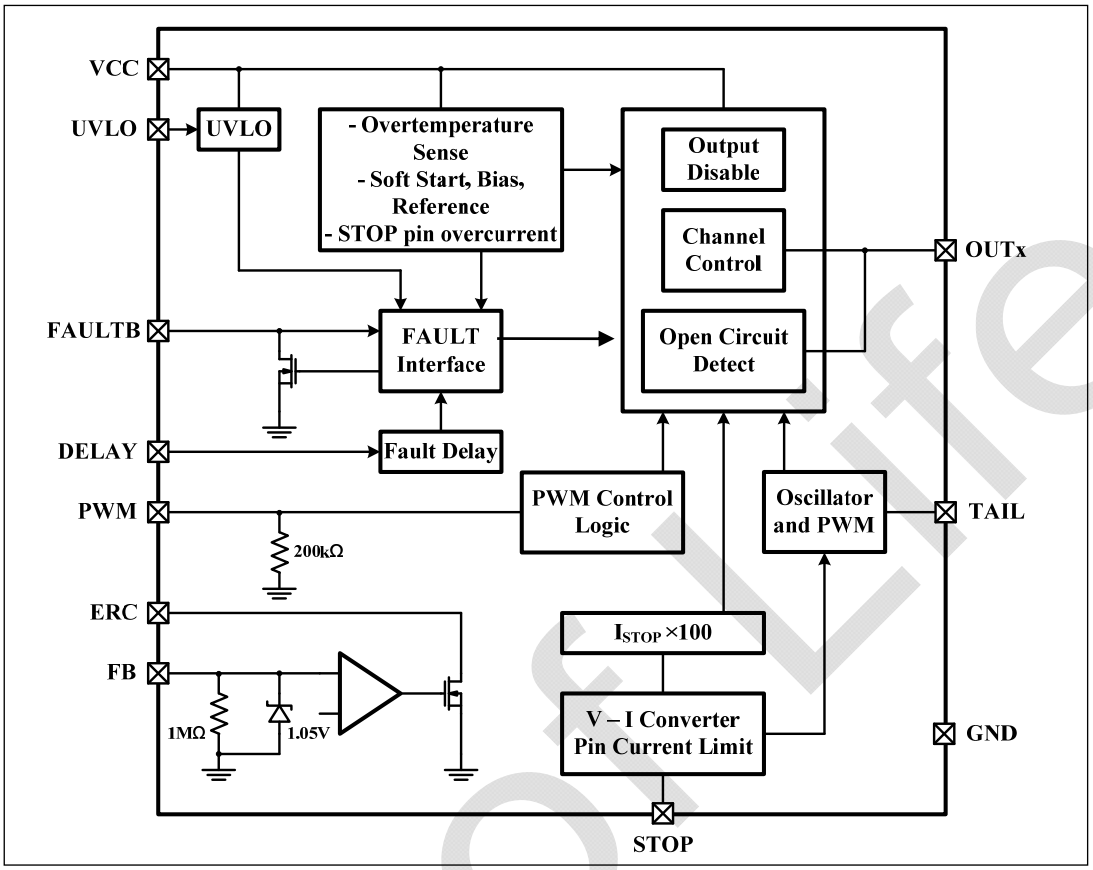


Figure 27 V_{STRING} vs. R_{FB1}

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The IS32LT3181 is a 6-channel linear current driver optimized to drive Rear Combination Lamp for automotive applications. A single input is used to select between two fully programmable intensity levels, one for the 'STOP' condition, and the other for the 'TAIL' condition. The full intensity 'STOP' condition is easily set using an external resistor, R_{STOP}. The lower intensity 'TAIL' condition is realized via an integrated PWM circuit, the duty cycle of which is easily programmed using an external resistor, R_{TAIL}.

IS32LT3181 also includes an integrated drive circuit for an external PMOS FET linear regulator for the case where the voltage across the LED loads must be accurately maintained to control power dissipation.

The ERC pin current (I_{ERC}) flows through 1kΩ resistor (R_{GS}) and generates a voltage across gate and drain of PMOS FET. IS32LT3181 regulates this ERC current by sensing feedback reference voltage (V_{FB}) to control the R_{DS_ON} of PMOS FET and get the expected V_{STRING}, which is set by resistor divider R_{FB1} and R_{FB2}.

The integrated feedback reference is trimmed to be 9% accuracy, while the ERC pin current (I_{ERC}) for the external regulator control can drive up to 6mA.

PROGRAMMING THE OUTPUT CURRENT

A single programming resistor (R_{STOP}) controls the maximum sink current for each LED channel. The STOP pin provides a reference voltage of 1.08V (Typ.). The programming resistor may be computed using the following Equation (1):

$$I_{OUT} = 100 \times \frac{1.08V}{R_{STOP}} \qquad (1)$$

The current which is drawn from the STOP pin is internally mirrored to each of the 6 outputs with a multiplication factor of 100A/A. Thus, an output current of 50mA would require a current to be drawn from STOP of 500μA, corresponding to an external programming resistance of 2.16kΩ.

OVER CURRENT PROTECTION

A 1mA current limiting on STOP pin limits the current which can be referenced from the STOP pin. Exceeding the STOP pin current limit will shut down the output currents to prevent unexpected excessive power dissipation (Figure 10). When the STOP pin current reaches 1mA, the current outputs are shutdown, the fault register is triggered and FAULTB pin will be asserted low after the FAULTB delay time.

PROGRAMMING THE PWM DUTY CYCLE

A single external resistor on the TAIL pin sets the PWM duty cycle which determines the lower intensity TAIL condition. The TAIL pin supplies a constant current of 100μA. The PWM duty cycle (D_{cycle}) is set by the following Equation (2):

$$D_{cycle} = \left(\frac{100\mu A \times R_{TAIL}}{4V} - 0.1 \right) \times 100\% \qquad (2)$$

Internally, a sawtooth waveform with a peak value of 4.4V and a minimum value of 0.4V is compared to the voltage of the TAIL pin (100uA x R_{TAIL}). The fixed frequency of the sawtooth waveform is 1kHz resulting in a PWM signal of 1kHz at the programmed duty cycle. Thus, for example, a 50% duty cycle would require the reference voltage at TAIL to be 2.4V, corresponding to an external resistance value of 24kΩ.

The internal PWM generator can also be driven by an external DC voltage supply. Providing a DC input voltage to the TAIL pin in the range from 0.4V to 4.4V programs the output duty cycle linearly from 0% to 100% duty cycle.

THERMAL SHUTDOWN

If the die temperature exceeds the thermal shutdown temperature of 160°C (Typ.) then the device will shutdown, and the sink currents are shut off for all channels. After a thermal shutdown event, the IS32LT3181 will not try to restart until its temperature has reduced to less than 145°C (Typ.). The fault register is triggered and FAULTB pin will be asserted low after delay time.

OUTPUT CURRENT SLEW RATE CONTROL

To minimize the effects of EMI, the output current rise and fall time is controlled. The slew rate control circuitry is designed to control the rise time, 10% to 90% and fall time 90% to 10% at 5mA/μs (Typ.).

OPEN LED DETECTION

Each of the outputs of the IS32LT3181 is monitored for an output voltage of less than 450mV (Typ.). If any of the output voltages drops below the threshold voltage, the fault register is triggered and the FAULTB pin is asserted low after delay time.

During normal operation, it is possible that current may still be flowing in the output LED string even if the output voltage of the IC falls below the OC detect threshold – for example, if the LED string remains intact, but the supply voltage dips momentarily (the duration is longer than t_D which is configured by the DELAY pin) and UVLO pin remain higher than threshold. In this case, the FAULTB pin would assert then de-assert when the output voltage returns to the nominal value.

OUTPUT DISABLE DETECTION

As IS32LT3181 powers up, the device will check OUTx pin of each channel to see if it is connected to GND. If any channel is connected to GND (disable typical threshold is 100mV), the fault diagnostic function will

ignore the fault of this channel. To prevent a trigger fault assertion, when less than 6 channels are used, the unused OUTx pins must be connected to GND to disable these channels.

Table 1 I_{OUT} and FAULTB State at Different PWM

6V< V_{CC} <16V (V_{UVLO}>1.2V)			
PWM Pin	**LED String**	**I_{OUT}**	**FAULTB**
> 2.2V	Normal	$100\times\frac{1.08}{R_{STOP}}$	De-asserted
	Open	0A	Asserted
<0.7V	Normal	$100\times\frac{1.08}{R_{STOP}}\times D_{cycle}$	De-asserted
	Open	0A	Asserted

D_{cycle} = Duty cycle of PWM as set by R_{TAIL}.

EXTERNAL REGULATOR CONTROL PIN

An external PMOS can be used to protect the IS32LT3181 and the LED strings from damage due to large voltage variation on the supply input voltage. The external PMOS is used as a linear voltage regulator to help minimize the power dissipated in the IS32LT3181 device.

Two modes of operation can be selected by external connection of the FB pin as described below.

1) The first mode of operation is selected by connecting the FB pin to VCC through a 10kΩ (as shown in the Figure 2 typical operating schematic). In this mode, the linear voltage regulator is disabled and the total LED V_F should be close to the supply voltage (V_{CC} – V_{OUTx}) for minimal IS32LT3181 package thermal dissipation.

2) The second mode of operation is selected by connecting a resistive voltage divider to the FB pin (as shown in the Figure 1 typical operating schematic). This enables the ERC pin output to linearly drive the PMOS FET and regulate the V_{STRING} voltage so the FB voltage is maintained at 1.05V (Typ.).

FEEDBACK VOLTAGE SETTING

V_{STRING} should be set to a level to allow proper operation of the IC without detecting an open LED (0.6V max on OUTx) and to keep power to the IC at reduced levels below the 160°C (Typ.) thermal shutdown threshold limit. Reducing die temperature will depend on printed circuit board composition, PCB size, thermal via number and placement, module component placement, and air flow.

V_{STRING} can only be adjusted with an external PMOS FET and it is set using resistors R_{FB1} and R_{FB2} (refer to Figure 1) as following Equation (3):

$$V_{STRING}=V_{FB}\times\left(\frac{R_{FB1}}{R_{FB2}}+1\right) \qquad (3)$$

This simplifies to an Equation (4) for R_{FB1}.

$$R_{FB1}=\frac{R_{FB2}\left(V_{STRING}-V_{FB}\right)}{V_{FB}} \qquad (4)$$

Where V_{FB} = 1.05V (Typ.)

And, $$V_{STRING}=V_{OUTx}+V_{LED} \qquad (5)$$

The recommended R_{FB2} is 1kΩ. V_{LED} is the total LED string forward voltage drop, V_F. V_{OUTx} should be selected for optimal current sink operation. Please refer to Figure 22 and 23 to set a proper V_{OUTx}.

FAULTB OUTPUT OPERATION

The FAULTB pin is an open drain structure. When a fault is asserted, the pin will change from high impedance to pull low state. If it is externally connected to a pull-up resistor, it will be at the pull-up voltage after fault is released. The FAULTB pin is also an input pin. When the voltage of this pin is pulled up to exceed V_{FAULT_H}, all the outputs will be enabled. To shutdown the output, the FAULTB pin voltage has to drop lower than V_{FAULT_L}. Several devices with their FAULTB pins connected in parallel act to turn off all the interconnected devices. Any device which encounters a fault will turn off all the other devices. Please refer to Figure 3 schematic.

A FAULTB pin assertion can be delayed. This fault delay time consists of T1 and T2. T1 is the built-in deglitch time. If an open LED fault occurs, T1 is about 4μs. If R_{STOP} pin over current fault or thermal shutdown occurs, T1 is about 100ns. T2 can be set by connecting a capacitor from the DELAY pin to GND. The device internally sources a 2μA (I_{DELAY}) current to charge this capacitor and monitor the voltage of this pin. Once it reaches the threshold voltage of 1.2V (V_{DELAY}), the FAULTB pin will be asserted. So the delay time t_D can be calculated by the following Equation (6):

$$t_D=\frac{V_{DELAY}\times C_{DELAY}}{I_{DELAY}} \qquad (6)$$

Note: The minimum value of this delay capacitor C_{DELAY} is 10pF. The DELAY pin CANNOT be left floating.

In all fault cases, if the device is powered down during the time when the FAULTB signal is asserted, the FAULTB pin is reset. Reapplying power to the circuit after this has occurred will cause the FAULTB pin to operate as normal in accordance with the conditions described below.

The LED(s) open fault reporting is enabled by UVLO pin voltage exceeding the UVLO threshold. A resistive voltage divider from VCC to GND is used for

preventing false triggering during power up. The fault UVLO voltage could be set by the following equation (7):

$$V_{UVLO} = V_{UVLO\_TH} \times \left(\frac{R_1}{R_2} + 1 \right) \qquad (7)$$

To disable the FAULTB reporting, the UVLO pin voltage has to drop more 100mV lower than V_{UVLO_TH}.

When the voltage of UVLO pin exceeds V_{UVLO_TH}, any channel which encounters an open LED condition (the voltage of the OUTx pin falls lower than 0.6V) will remain on state, turn off all the other channels and be asserted by the FAULTB pin after delay time. Typically this condition is encountered during a STOP or TAIL condition then the fault condition will be detected and the fault signal asserted after delay time. When the IS32LT3181 is in neither STOP nor TAIL condition, the circuit is powered down, and the signal is cleared. Upon re-entering either the STOP or TAIL condition, the fault signal will reassert after delay time and the output will remain off, if the fault condition still exists. If the fault condition has been cleared, FAULTB pin will not re-assert and all the other channels will be turned on.

Exceeding the STOP pin current limiting 1mA will turn off all the channels and the FAULTB pin will assert after delay time (refer to Figure 28). This fault assertion will be reset after fault condition cleared.

Table 2 Fault Assertion

Fault Type	Test Condition	Output Driver Action	FAULTB Pin Output	Fault Logic Decision	Fault Recovering
LEDs Open (1 to 6 LED string)	V_{OUT}<0.45V, V_{UVLO}> 1.2V	Keeping the open channel on and turning the other channels off.	Pulled Low	For stop mode, Fault state will be reported after fault delay time t_D.	V_{OUT} exceeds 0.45V.
				For Tail mode, Fault state can be reported due to fault delay time t_D and PWM signal. (See Figure 28)	
	V_{OUT}<0.45V, V_{UVLO}<1.2V	All channels turn on	High impedance	NA	NA
RSTOP PIN Over Current	I_{RSTOP}>1mA	All channels shutdown	Pulled Low	Fault state will be reported after fault delay time t_D.	I_{RSTOP} falls lower than 1mA.
Thermal shutdown	T_J>160°C	All channels shutdown	Pulled Low	Fault state will be reported after fault delay time t_D.	The junction temp falls lower than 145°C.

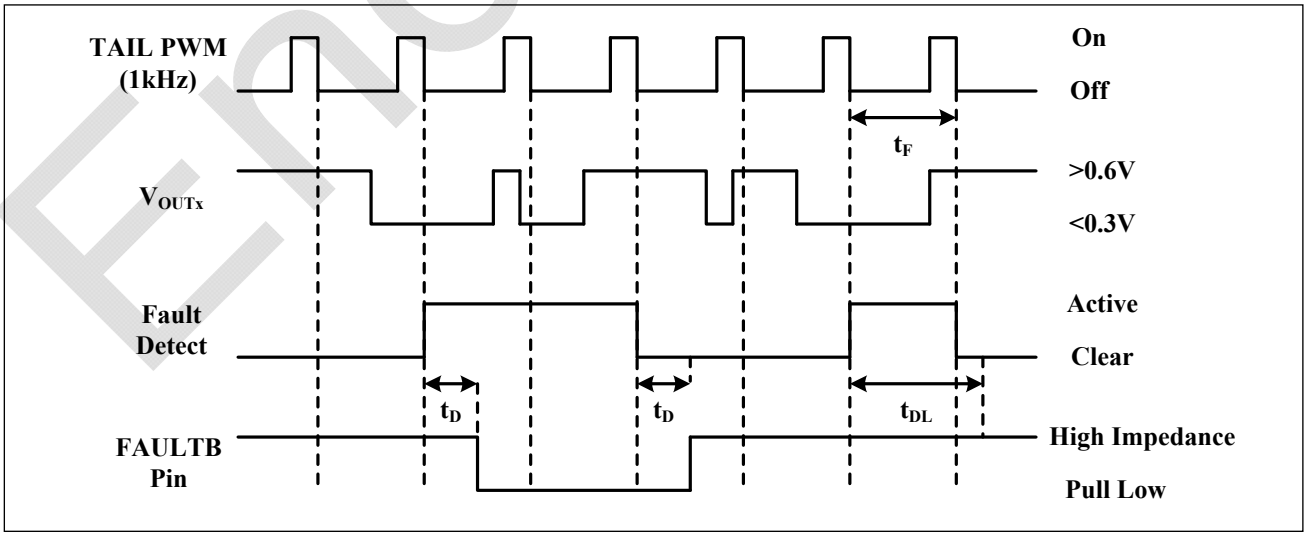


Figure 28 Fault detect during TAIL mode

Note 1: In TAIL mode, the fault detection is implemented only at the PWM falling edge.

Note 2: t_{DL} means a long fault delay time. t_F means the fault detect state change time. If t_{DL} is longer than t_F, the FAULTB pin will not report the fault.

THERMAL DISSIPATION

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation on IS32LT3181, P_{3181}, and the package thermal resistance, θ_{JA}, as in Equation (8):

$$P_{3181} = V_{CC} \times I_{CC} + \sum_{x=1}^{6} V_{OUTx} \times I_{OUTx} \qquad (8)$$

and,

$$T_J = T_A + \Delta T = T_A + P_{3181} \times \theta_{JA} \qquad (9)$$

Where, V_{CC} is the supply voltage, V_{OUTx} is the voltage across OUTx pin to GND, I_{OUTx} is the sink current of each LED string and T_A is the ambient temperature.

When operating the device at high ambient temperatures, or when driving high load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (10):

$$P_{D(MAX)} = \frac{150°C - 25°C}{\theta_{JA}} \qquad (10)$$

So, $$P_{D(MAX)} = \frac{150°C - 25°C}{39.9°C/W} \approx 3.1W$$

Figure 29, shows the power derating of the IS32LT3181 on a JEDEC board (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

When the junction temperature, T_J, exceeds the absolute maximum temperature 150°C (Typ.), the optional external linear voltage regulator configuration should be implemented in order to withstand unwanted dissipation.

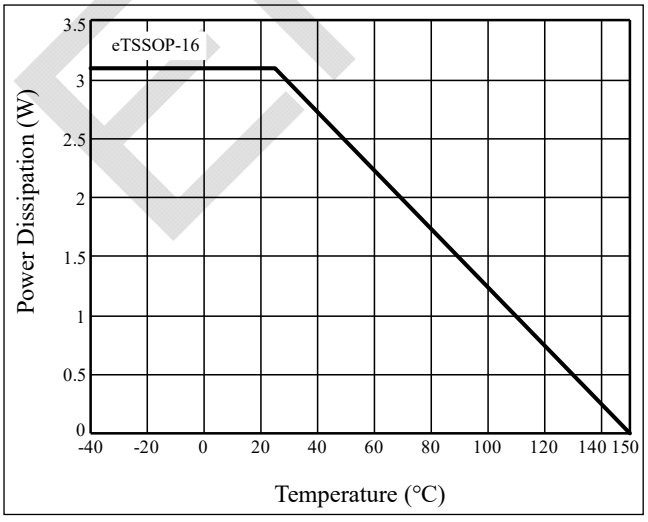


Figure 29 Dissipation Curve

With the linear voltage regulator, IS32LT3181 will regulate the PMOS FET to keep V_{STRING} voltage constant, that can be set by resistor divider R_{FB1} and R_{FB2}. So even though the supply voltage V_{CC} has some variation, the power dissipation on IS32LT3181 will be constant.

$$V_{OUTx} = V_{STRING} - V_{LEDSx} \qquad (11)$$

And, $$P_{3181} = V_{CC} \times I_{CC} + \sum_{x=1}^{6} V_{OUTx} \times I_{OUTx} \qquad (12)$$

Where, V_{LEDSx} is the total forward voltage of each LED string.

The power dissipation on the external PFET MOS can be calculated by the following Equation (13):

$$P_{FET} = \sum_{x=1}^{6} (V_{CC} - V_{STRING}) \times I_{OUTx} \qquad (13)$$

When designing the Printed Circuit Board (PCB) layout, double-sided PCB with a copper area of a few square millimeters on each side of the board directly under the IS32LT3181 (eTSSOP-16 package) and PMOS FET must be used. Multiple thermal vias will help to conduct heat from the exposed pad of the IS32LT3181 and PMOS FET to the copper on each side of the board. The thermal resistance can be further reduced by using a metal substrate or by adding a heat sink.

The thermal resistance is achieved by mounting the IS32LT3181 on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the IS32LT3181. Multiple thermal vias, as shown in Figure 30, help to conduct the heat from the exposed pad of the IS32LT3181 to the copper on each side of the board. The thermal resistance can be reduced by using a metal substrate or by adding a heatsink.

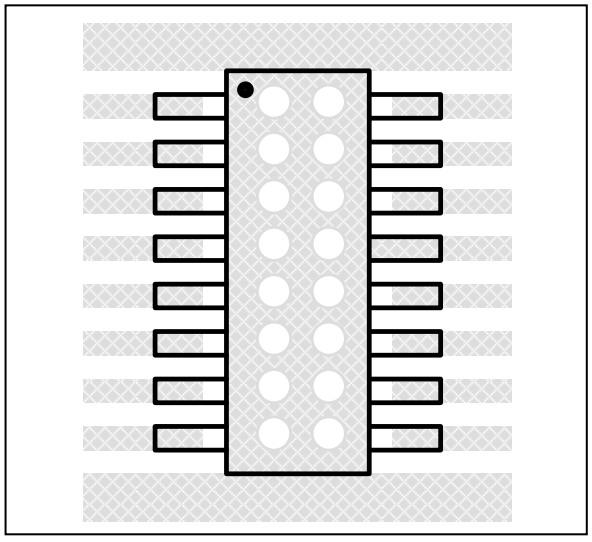


Figure 30 Board Via Layout For Thermal Dissipation

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

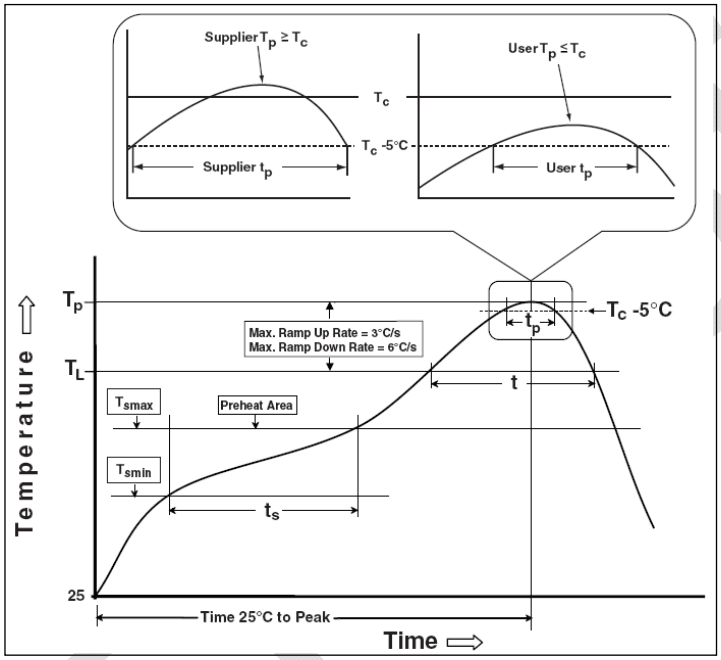
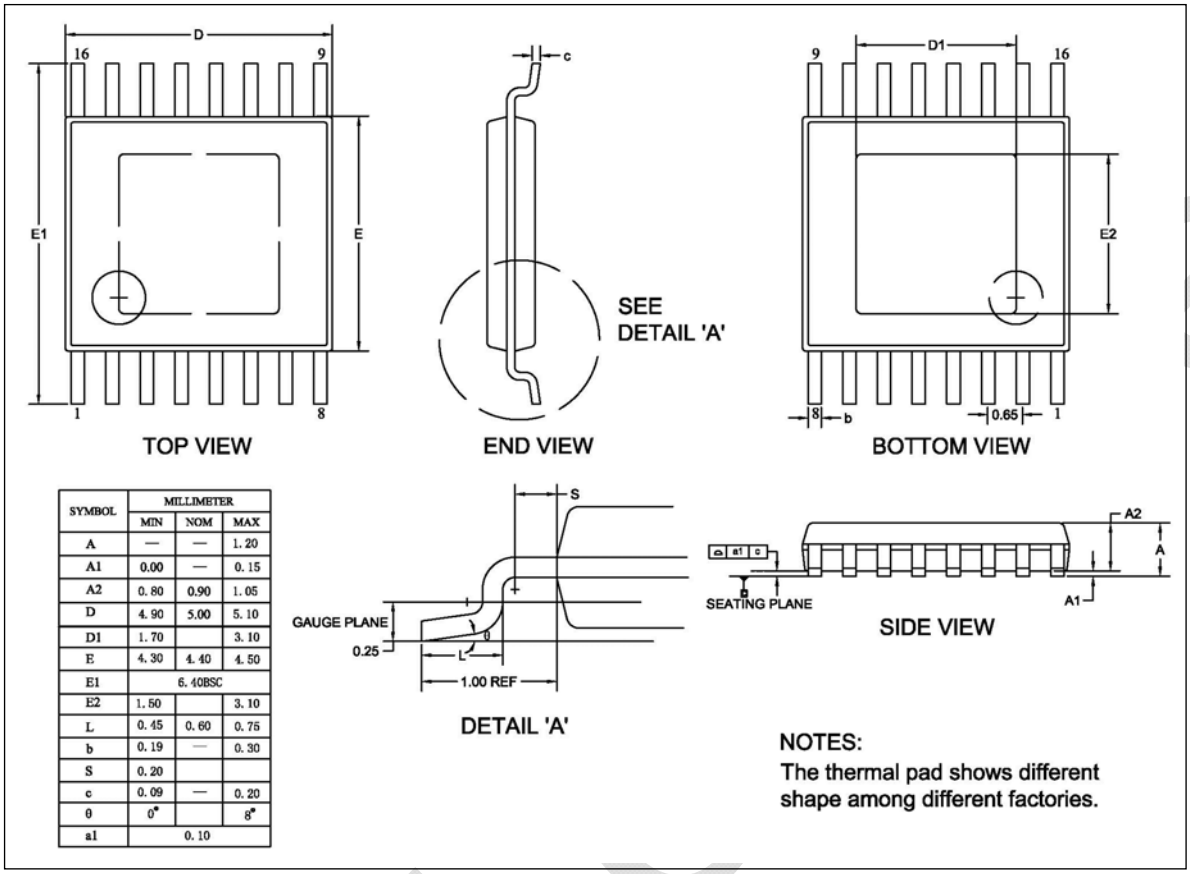


Figure 31 Classification Profile

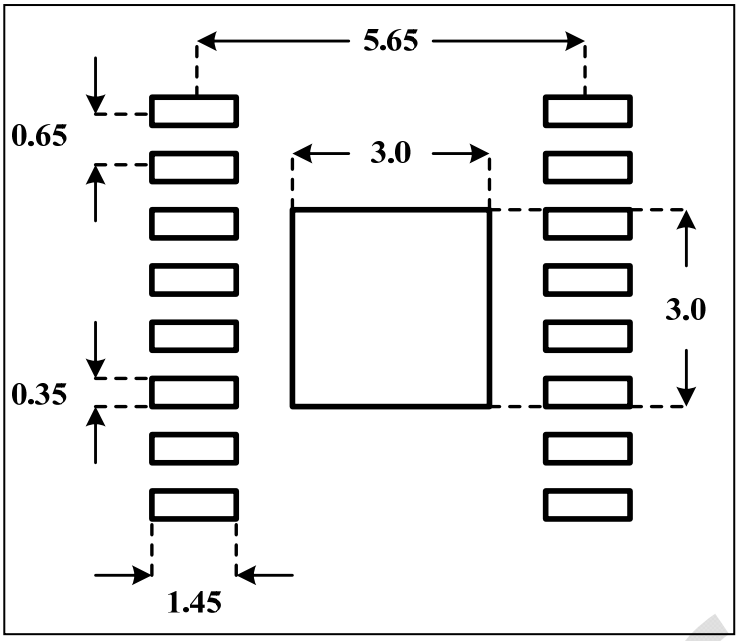
PACKAGE INFORMATION

eTSSOP-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	4.90	5.00	5.10
D1	1.70		3.10
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50		3.10
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2016.03.11
0B	1. Update EC table 2. Update the temperature range of figure 7, 9, 11, 13, 15, 17, 19 to 150°C	2016.09.02
A	AEC-Q100 qualification released.	2016.11.17
B	Correct I_{OUTACC} condition error in EC table: T_J = -40°C ~+150°C change to T_J = -40°C ~+125°C	2017.04.20
C	Add NRND watermark	2022.06.14
D	Change watermark to EOL	2022.08.26