ClampZero Family

Active Clamp IC with Integrated High-Voltage Switch
Pairs with InnoSwitch4 Family of Offline Switcher ICs

Product Highlights

Highly Integrated, Compact Footprint

- Eliminates switching losses in InnoSwitch4 primary switch
- Captures and recycles leakage inductance energy
- Dramatically improves power supply efficiency
- Interfaces seamlessly with InnoSwitch4
- Powered directly from InnoSwitch4 BYPASS pin
- Self-biased at start-up
- Operates in both DCM and CCM modes
- Robust 750 V PowiGaN switch (CPZ1075M / CPZ1076M)

Advanced Protection / Safety Features

- Integrated temperature sensing and hysteretic thermal shutdown

Green Package

- Halogen free and RoHS compliant

Applications

- High density flyback designs up to 220 W

Description

The ClampZero™ IC pairs with the InnoSwitch™4 family of ICs to eliminate energy wasted due to switching losses in the clamp and primary switch. This dramatically improves power supply efficiency – easily exceeding 95% - while maintaining the flexibility and low component count of the flyback architecture.

The ClampZero IC is an active clamping circuit which recycles otherwise wasted leakage inductance energy. The ClampZero incorporates a high-side power switch and level shifted self-biased controller which receives communication from a low-side transceiver connected to the InnoSwitch4 primary controller

By ensuring zero voltage switching across all line and load conditions and in both CCM and DCM operating modes, ClampZero combines with InnoSwitch4 to implement a highly flexible active clamp flyback solution. In a typical application paired with the InnoSwitch4 IC, the low switching losses permit use of a high switching frequency, minimizing the physical size of the transformer and resulting in an extremely small PCB footprint.

Zero-voltage switching is achieved by precise timing between the turn-off of the ClampZero and turn-on of the InnoSwitch4 power switch, which completely removes turn-on losses. The overall effect of this synchronized switching, along with the InnoSwitch4 PowiGaN switch with zero turn-off losses, is a flyback converter with zero primary clamp losses and zero power switch switching losses enabling high density, heat sinkless flyback designs up to 220 W.

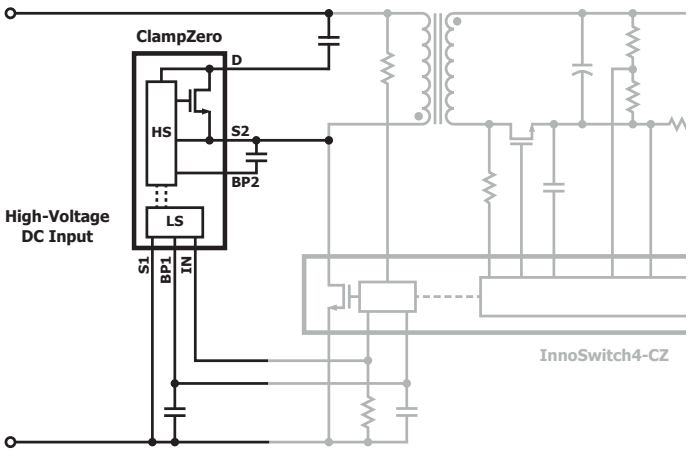


Figure 1. Typical Application schematic.

Figure 2. MinSOP-16A Package with Creepage for High-Side Driver.

ClampZero + InnoSwitch4 Output Power Table

Product[3,4]	Adapter[1]	Open Frame[2]
CPZ1061M	70 W	75 W
CPZ1062M	90 W	100 W
CPZ1075M	135 W	145 W
CPZ1076M	200 W	220 W

Table 1. Output Power Table.

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient. Max output power is dependent on the design. With condition that package temperature must be < 125 °C.
2. Minimum peak power capability.
3. Package: MinSOP-16A.
4. CPZ1061M / CPZ1062M – 650 V MOSFET.
   CPZ1075M / CPZ1076M – 750 V PowiGaN Switch.

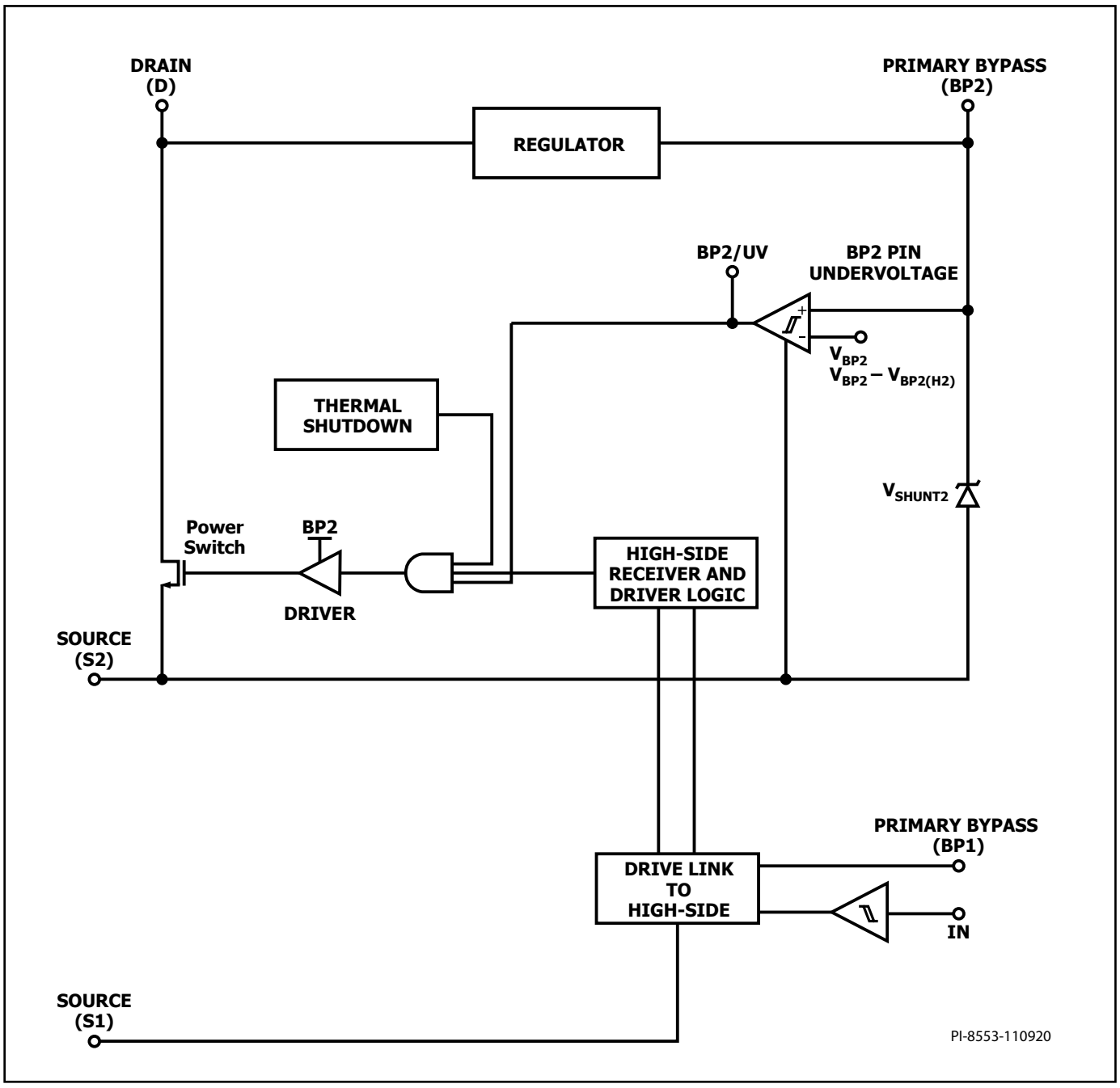


Figure 3. Block Diagram.

Pin Functional Description

Not Connected (NC) Pin (Pins 1-2, 4-5)
These pins are not electrically connected. Pin 5 must connect to S1 pin.

LOW-SIDE SOURCE (S1) Pin (Pins 3 and 6)
Source connection of low-side controller.

LOW-SIDE RECEIVER (IN) Pin (Pin 7)
Receiver for Clamp Zero trigger; connects to HSD pin of InnoSwitch4.

LOW-SIDE BYPASS (BP1) Pin (Pin 8)
Supply voltage for low side controller. Needs to be connected to BPP of InnoSwitch4 primary to draw power from auxiliary winding.

HIGH-SIDE BYPASS (BP2) Pin (Pin 9)
Supply voltage for high-side controller.

HIGH-SIDE SOURCE (S2) Pin (Pins 10-12)
Source connection of high-side switch.

DRAIN (D) Pin (Pin 16)
Drain of high-side switch.

ClampZero Functional Description

The ClampZero integrates low-side and high-side controller, plus a high-side power switch with gate driver.

The ClampZero is the partner IC with InnoSwitch4 to provide zero voltage switching (ZVS) functionality to the main power switch of flyback power converter. The ClampZero IC operates as an active clamping circuit in a flyback power supply that has the ability to operate in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The ClampZero incorporates a high-side power switch and self-biasing controller with integrated thermal protection, low-to-high side communication and low-side transceiver to receive a clamp turn-on signal from the InnoSwitch4 primary controller.

Figure 3 shows the functional block diagram of the controller, highlighting the most important features.

LOW-SIDE BYPASS Pin
Low-side controller receives its bias for BP1 from InnoSwitch4 BPP pin. When BP1 voltage is $V_{BP1(RESET)1}$ or greater, low-side controller is functional and able to receive an HSD pulse from InnoSwitch4 and communicate the drive instruction to the high-side driver stage.

LOW-SIDE RECEIVER Pin
The ClampZero low-side controller receives signal from InnoSwitch4 HSD pin. During the rising edge of the signal, the low-side controller communicates the drive instruction to turn on the high-side switch when HSD signal is above $V_{IN(R)}$. During the falling edge of the signal, the low-side controller communicates the drive instruction to turn off the high-side switch when HSD signal is below $V_{IN(F)}$.

HIGH-SIDE BYPASS Pin Regulator
High-side BYPASS pin has an internal regulator that charges the BP2 to V_{BP2} by drawing current from the DRAIN pin whenever the power switch is off. The amount of charge current available for BP2 is important in order to have fast start-up from initial switching of

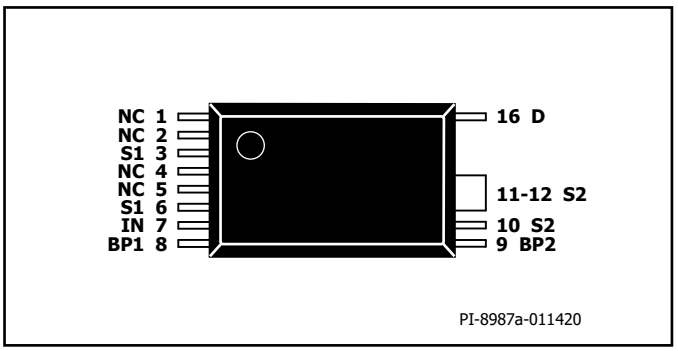


Figure 4. Pin Configuration.

InnoSwitch4. Thus the BP2 capacitor value is limited to 150 nF (min 100 nF/max 220 nF). Higher value BP2 capacitor is undesirable as this would cause too much delay in start-up and cause possible overshoot of primary clamp voltage.

HIGH-SIDE BYPASS Pin Undervoltage Threshold
The BP2 pin undervoltage circuitry disables the power switch when the BP2 pin voltage drops below ~4.4 V ($V_{BP2} – V_{BP2(H2)}$) in steady-state operation. Once the BP2 pin voltage falls below this threshold, it must rise to VBP2 to re-enable turn-on of the power switch.

In addition, a shunt regulator clamps BP2 pin voltage to V_{SHUNT2} when current is provided to the BP2 through external bias winding or boot strap circuit. This removes the excessive dissipation from Drain to BP2 charge current during steady-state operation.

Over-Temperature Protection
The thermal shutdown circuitry senses the die temperature. If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

Zero Voltage Switching (ZVS)
InnoSwitch4 will achieve ZVS operation both in CCM and DCM operation with ClampZero providing extra high side switch. The operation of the converter is as:

- InnoSwitch4, after receiving the Flux Link pulse, does not immediately turn on primary switch.
- InnoSwitch4 primary controller first generates a fixed duration pulse on the HSD pin. This pulse will control the power switch inside ClampZero, and the switch will be turned on when HSD pulse is high. ClampZero starts recycling clamp capacitor energy to output and also building up energy on transformer magnetizing inductance and leakage inductance which are used later for ZVS.
- After InnoSwitch4 terminates the HSD pulse, it waits for additional delay and then turns on the primary switch. This delay is programmable by InnoSwitch4. During this delay, the energy built up at magnetizing inductance and leakage inductance will help discharge C_{OSS} of primary switch in InnoSwitch4 to achieve ZVS.

Applications Example

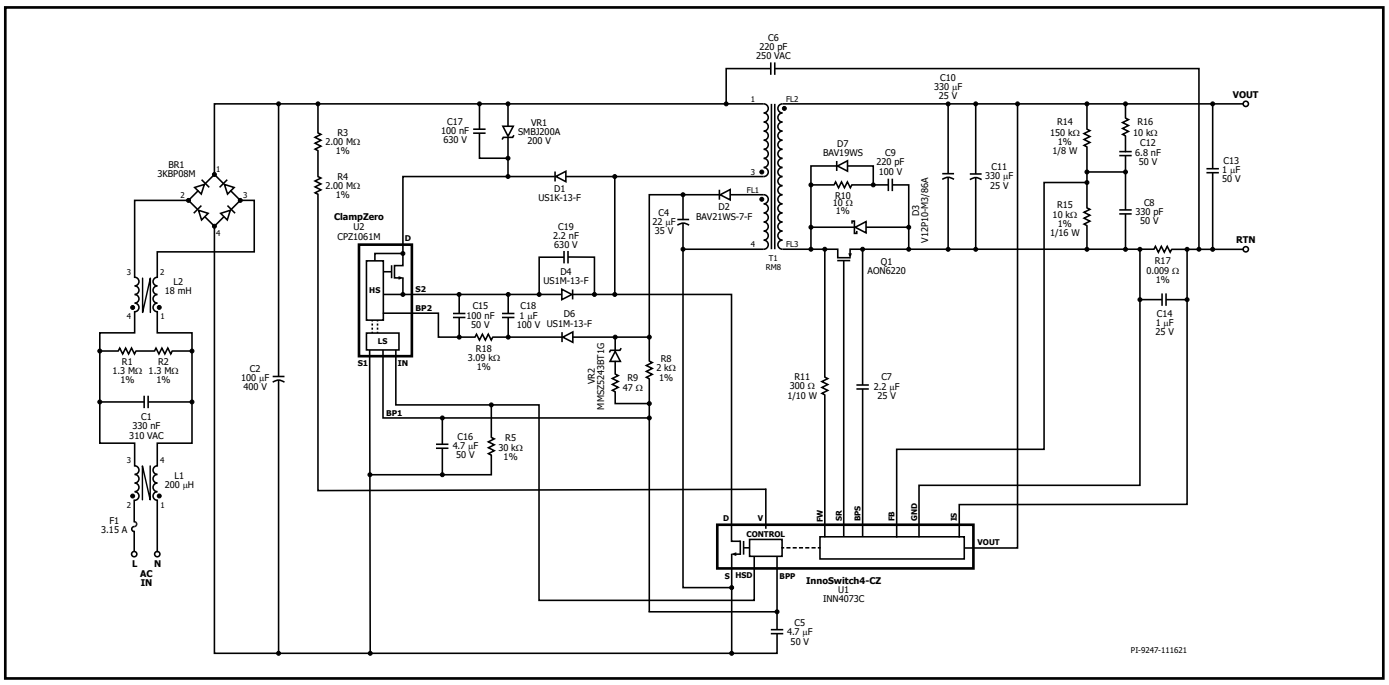


Figure 5. Schematic 20 V / 3.25 A Notebook Adapter Power Supply.

The circuit shown in Figure 5 is a 20 V, 3.25 A single output power supply using INN4073C and CPZ1061M. This single output design is DOE Level 6 and EC CoC v5 compliant.

Input fuse F1 isolates the circuit and provides protection from component failure, and the common mode choke L1 and L2 with capacitor C1 attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitor C2. Y capacitor C6 connected between the power supply output and input helps to reduce common mode EMI.

Resistors R1 and R2 along with U2 discharge capacitor C1 when the power supply is disconnected from AC mains.

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch4 IC (U1). Resistors R3 and R4 provide input voltage sense protection for undervoltage and overvoltage conditions.

The primary clamp formed by diode D1 and capacitor C17 limits the peak drain voltage of U1 at the instant of turn-off of the switch inside U1. The energy stored in the leakage inductance of transformer T1 will be transferred to capacitor C17. Part of the magnetizing energy will also get transferred to C17 depending on the capacitance value used. VR1 is used to protect the InnoSwitch4 from excessive drain voltages if there is any malfunction of the power supply.

When the FluxLink™ signal is received from the secondary-side, the InnoSwitch4 generates an HSD signal to turn on the ClampZero device. When the ClampZero IC (U2) turns on, to achieve soft switching of the InnoSwitch4 primary switch, clamp capacitor C17 starts to charge the leakage inductance of the transformer in the case of CCM operation and both the leakage and the magnetizing inductance of the transformer in the case of DCM operation. Ultrafast diodes D1 and D4 are used to divert the transformer current from the body diode of ClampZero's high-side switch to minimize the reverse-recovery energy. Those diodes (D1 and D4) and capacitor C19 are not required for the CPZ107xM. A small delay is provided from the instant the high-side switch turns off in order to achieve zero voltage switching on the primary switch. This delay is programmable by different resistor values of R5. Capacitor C19 will help reduce the voltage on the ClampZero IC (U2) to provide soft turn-on.

Capacitor C16 is used to provide local decoupling at the BP1 pin. Capacitor C15 provides the decoupling for BP2 pin. Diode D6 and capacitor C18 form a bootstrap circuit to provide the bias for the high-side BP2 pin. Resistor R18 limits the current flowing into the BP2 pin.

The InnoSwitch4 IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C5) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C4. Resistor R8 limits the current being supplied to the PRIMARY BYPASS pin of InnoSwitch4 IC (U1).

Output regulation is achieved using modulation control, where the frequency and ILIM of switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled for a high value of ILIM in the selected ILIM range, and at light load or no-load, most cycles are disabled, and the ones enabled have a low value of ILIM in the selected ILIM range. Once a cycle is enabled, the switch remains on until the primary current ramps to the device current limit for the specific operating state.

The latch-off/auto-restart primary-side overvoltage protection is obtained using Zener diode VR2 with current limiting resistor R9. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at the output of the converter, the auxiliary winding voltage increases and causes breakdown of VR2, which then causes a current to flow into the BPP pin of InnoSwitch4 IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the U1 controller latches off to prevent any further increase in output voltage.

The secondary-side of the InnoSwitch4 IC provides output voltage, output current sensing, and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by SR FET Q1/D3 and filtered by capacitors C10 and C11. Capacitor C13 is used to reduce the high-frequency output voltage ripple. High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced via RCD snubber R10, C9, and D7. Diode D7 minimizes the dissipation in resistor R10.

The gate of Q1 is turned on by the secondary-side controller of IC U1, based on the winding voltage sensed via resistor R11 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR MOSFET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off, when the voltage drop across the MOSFET falls below a threshold of approximately $V_{SR(TH)}$ mV.

The secondary side of the IC U1 is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C7 connected to the BPS pin of IC U1 provides decoupling for the internal circuitry.

Below the CC threshold, the device operates in constant voltage mode. During constant voltage mode operation, output voltage regulation is achieved through sensing the output voltage via divider resistors R14 and R15. The voltage across R15 is fed into the FEEDBACK pin with an internal reference voltage threshold of 1.265 V. The output voltage is regulated so as to achieve a voltage of 1.265 V on the FEEDBACK pin. Capacitor C8 provides noise filtering of the signal at the FEEDBACK pin.

During CC operation, when the output voltage falls, the device directly powers itself from the secondary winding. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C7 via resistor R11 and an internal regulator. This allows output current regulation to be maintained down to ~3.4 V. Output current is sensed by monitoring the voltage drop across resistor R17 between the IS and SECONDARY GROUND pins. A threshold of approximately 35 mV reduces losses. C14 provides filtering on the IS pin from external noise. Once the internal current sense threshold is exceeded, the device regulates the number of switch pulses to maintain a fixed output current.

Layout Example

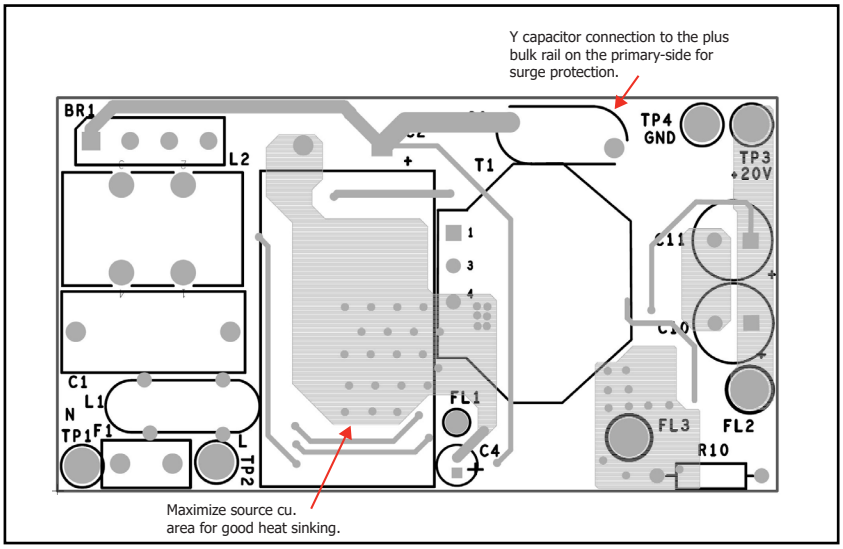


Figure 6. PCB Layout Top Side.

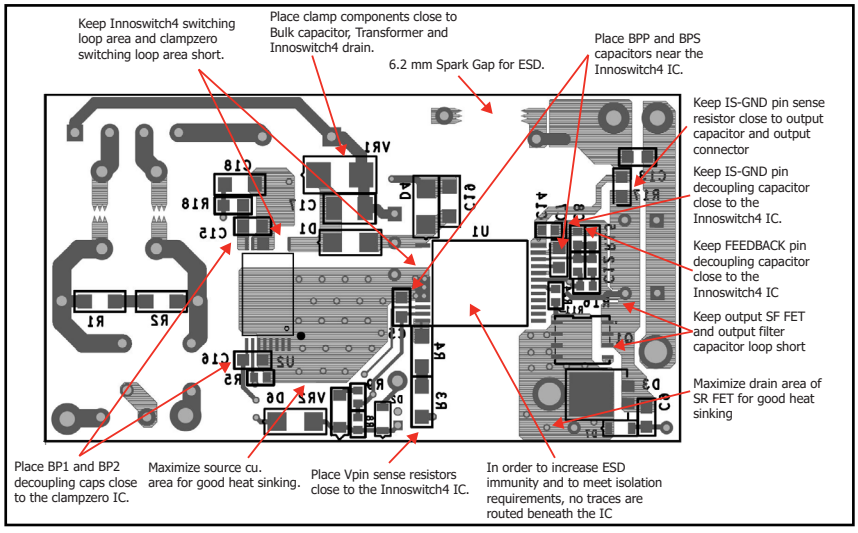


Figure 7. PCB Layout Bottom Side.

Applications Example 2

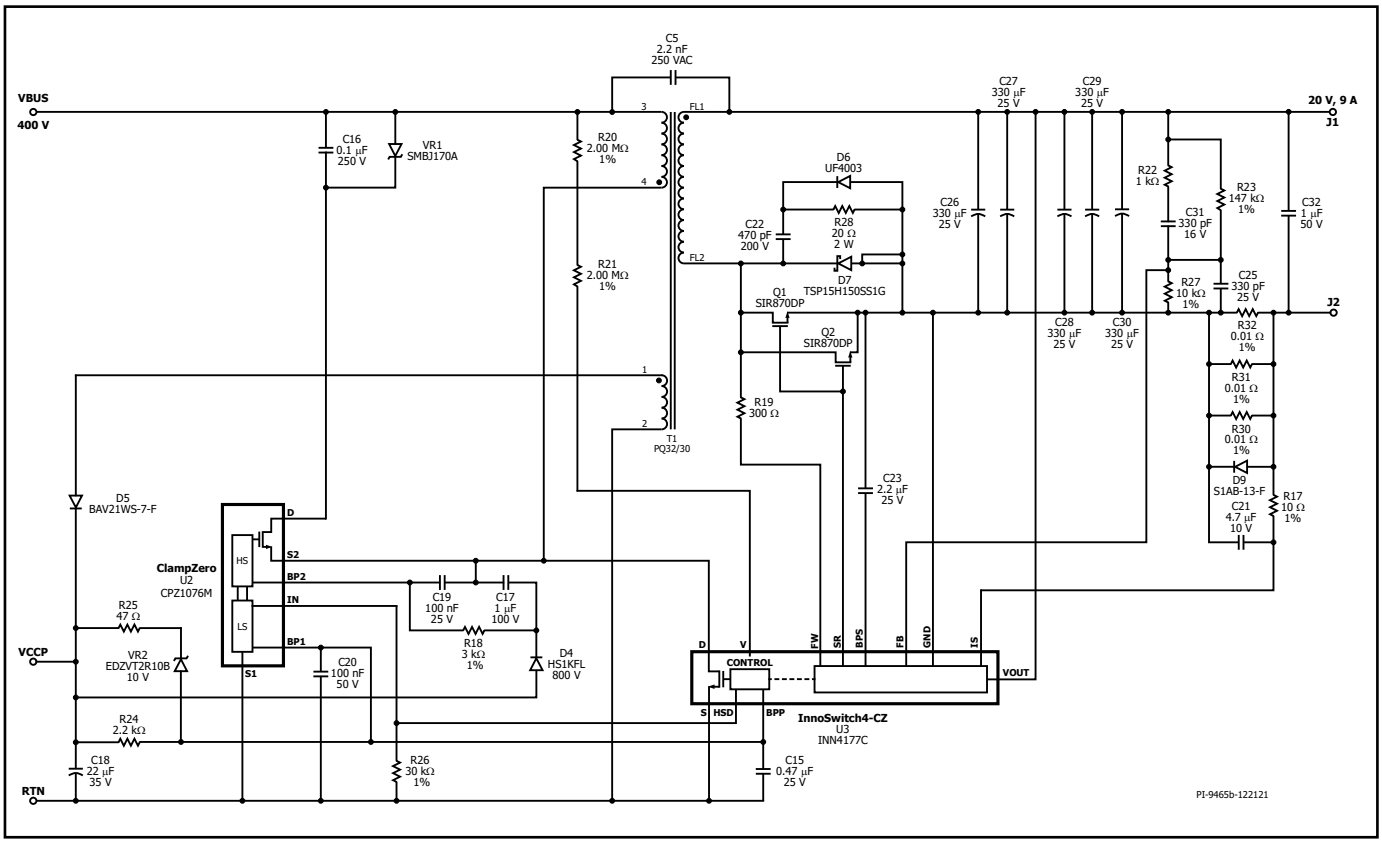


Figure 8. Schematic 20 V / 9 A Power Supply.

The circuit shown in Figure 8 is a DC/DC stage 20 V, 9 A single output power supply using INN4177C and CPZ1076M. This single output design exceed requirement for DOE Level 6 and EC CoC v5 compliant.

Y capacitor C5 is connected between the power supply output and input helps to reduce common mode EMI.

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch4 IC (U3). Resistors R20 and R21 provide input voltage sense protection for undervoltage and overvoltage conditions.

The primary clamp formed by switch of U2 and capacitor C16 limits the peak drain voltage of U3 at the instant of turn-off of the switch inside U3. The energy stored in the leakage inductance of transformer T1 will be transferred to capacitor C16. Part of the magnetizing energy will also get transferred to C16 depending on the capacitance value used. VR1 is used to protect the InnoSwitch4 from excessive drain voltages if there is any malfunction of the power supply.

When the FluxLink signal is received from the secondary side, the InnoSwitch-4 generates an HSD signal to turn on the ClampZero device. When the ClampZero IC (U2) turns on, to achieve soft switching of the InnoSwitch4 primary switch, clamp capacitor C16 starts to charge the leakage inductance of the transformer in the case of CCM operation and both the leakage and the magnetizing inductance of the transformer in the case of DCM operation. A small delay is provided from the instant the high-side switch turns off in order to achieve zero voltage switching on the primary switch. This delay is programmable by different resistor values of R26.

Capacitor C20 is used to provide local decoupling at the BP1 pin. Capacitor C19 provides the decoupling for BP2 pin. Diode D4 and capacitor C17 form a bootstrap circuit to provide the bias for the high-side BP2 pin. Resistor R18 limits the current flowing into the BP2 pin.

The InnoSwitch-4 IC is self-starting, using an internal high-voltage current source to charge the PRIMARY BYPASS pin capacitor (C15) when input AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D5 and filtered using capacitor C18. Resistor R24 limits the current being supplied to the PRIMARY BYPASS pin of InnoSwitch4 IC (U3).

Output regulation is achieved using modulation control, where the frequency and ILIM of switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled for a high value of ILIM in the selected ILIM range, and at light load or no-load, most cycles are disabled, and the ones enabled have a low value of ILIM in the selected ILIM range. Once a cycle is enabled, the switch remains on until the primary current ramps to the device current limit for the specific operating state.

The latch-off/auto-restart primary-side overvoltage protection is obtained using Zener diode VR2 with current limiting resistor R25. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at the output of the converter, the auxiliary winding voltage increases and causes

breakdown of VR2, which then causes a current to flow into the BPP pin of InnoSwitch4 IC U3. If the current flowing into the BPP pin increases above the ISD threshold, the U3 controller latches off to prevent any further increase in output voltage.

The secondary-side of the InnoSwitch4 IC provides output voltage, output current sensing, and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by SR FET's Q1, Q2 and diode D3 and filtered by capacitors C26 – C30. Capacitor C32 is used to reduce the high-frequency output voltage ripple. High-frequency ringing during switching transients that would otherwise create radiated EMI is reduced via RCD snubber R28, C22, and D6. Diode D6 minimizes the dissipation in resistor R28.

The gate of Q1 and Q2 is turned on by the secondary-side controller of IC U3, based on the winding voltage sensed via resistor R19 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR MOSFET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off, when the voltage drop across the MOSFET falls below a threshold of approximately $V_{SR(TH)}$ mV.

The secondary-side of the IC U3 is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C23 connected to the BPS pin of IC U3 provides decoupling for the internal circuitry.

Below the CC threshold, the device operates in constant voltage mode. During constant voltage mode operation, output voltage regulation is achieved through sensing the output voltage via divider resistors R23 and R27. The voltage across R27 is fed into the FB pin with an internal reference voltage threshold of 1.265 V. The output voltage is regulated so as to achieve a voltage of 1.265 V on the FB pin. Capacitor C25 provides noise filtering of the signal at the FB pin. Resistor R22 together with C31 forms a feed forward circuit and reduces the output triple.

During CC operation, when the output voltage falls, the device directly powers itself from the secondary winding. During the on-time of the primary-side power switch, the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C23 via resistor R19 and an internal regulator. This allows output current regulation to be maintained down to ~3.4 V depending on the trim configuration. Output current is sensed by monitoring the voltage drop across resistor R30 – R32 between the IS and SECONDARY GROUND pins. A threshold of approximately 35 mV reduces losses. Resistor R17 and capacitor C21 provides filtering on the IS pin from external noise. Once the internal current sense threshold is exceeded, the device regulates the number of switch pulses to maintain a fixed output current.

Key Application Considerations

No-load Consumption

The ClampZero device draws energy from the BP1 pin decoupling capacitor, which is supplied by the internal tap of InnoSwitch4. The InnoSwitch4 IC can start in self-powered mode, drawing energy from the BYPASS pin capacitor charged through an internal current source. Use of a bias winding, however, is required to provide supply current to the PRIMARY BYPASS pin, once the InnoSwitch4 IC has started switching. An auxiliary (bias) winding provided on the transformer serves this purpose. The high-side BP2 pin decoupling capacitor of the ClampZero device draws energy from the internal tap, once the power supply starts switching. In order to minimize the no-load consumption, a bootstrap diode D6 is recommended. Resistors R8 and R18 shown in Figure 5 should be adjusted to achieve the lowest no-load input power. ClampZero typically consumes ~35 µA from the BP1 pin and ~50 µA from the BP2 pin at no-load, adding only a few mW to total system losses.

Critical Components Selection

BP2 Pin Decoupling Capacitor

The high-side BYPASS pin has an internal regulator that charges BP2 to VBP2 by drawing current from the DRAIN pin whenever the power switch is off. The amount of charge current available for BP2 is important in order to have fast start-up from initial switching of InnoSwitch4. Thus, the BP2 capacitor value is set to 150 nF. A higher value BP2 capacitor is undesirable, because too much start-up delay may cause overshoot of the primary clamp voltage. A 100 nF to 220 nF capacitor may be used. At least 10 V, 0603 or larger size rated X5R or X7R dielectric capacitors are recommended to ensure that minimum capacitance requirements are met. The ceramic capacitor type designations, such as X7R or X5R from different manufacturers or different product families, do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0402 rated MLCC, because this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

Bias Winding and External Bias Circuit

The internal regulator connected from the DRAIN pin of the switch to the PRIMARY BYPASS pin of the InnoSwitch4 primary-side controller charges the capacitors connected to the InnoSwitch4 BPP pin and ClampZero BP1 pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can be used to supply current to the BPP and BP1 pins. The turns ratio for the bias winding should be selected such that a minimum of ~8 V is developed across the bias winding at the lowest rated output voltage of the power supply at the lowest load condition. If the voltage is lower than this, no-load input power increases.

The bias current from the external circuit should be set to $I_{S1(MAX)}$ to achieve lowest no-load power consumption when operating the power supply at 230 VAC input, (V_{BPP} > 5 V). An aluminum capacitor of at least 22 µF with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended. Highest voltage is typically developed across this capacitor when the supply is operated at the highest rated output voltage and load with the lowest input AC supply voltage.

Clamp Capacitor

It is recommended to choose the value of the clamp capacitor such that ~0.25 times the resonant period of the C_{CLAMP} and L_{LKG} equals the HSD pulse width. Capacitance in the range of 10 nF to 100 nF may be used depending on the design. At least 200 V, 1206 or larger size rated X7R dielectric capacitors are recommended.

$$\text{HSD Pulse Width} \backsim \frac{\pi}{2}\sqrt{L_{LKG}C_{CLAMP}}$$

Layout Considerations

The following layout considerations are specifically for the ClampZero components. For placement and layout of InnoSwitch4 specific and power components, check the InnoSwitch4 data sheet.

1. The ClampZero BP1 pin is supplied and regulated by the InnoSwitch4 internal BPP regulator. A separate decoupling capacitor needs to be placed very close to the BP1 pin of the ClampZero device.
2. The high-side BP2 pin is supplied by the internal drain tap during startup until the external bias is available from an external bootstrap circuit. A decoupling capacitor should be placed very close to the BP2 pin of the ClampZero IC.
3. Even though ClampZero conducts only for a short period and dissipates a small amount of power, some amount of PCB copper heat sinking on the source pin of the ClampZero device is required to minimize the thermals.
4. It is recommended to place the bootstrap components close to the BP2 and SOURCE pins of the ClampZero device to minimize the noise coupling into other parts of the circuit.
5. Place the ClampZero IC as close as possible to the clamp capacitor and transformer to minimize the clamp loop area.

Figure 2 shows the ClampZero layout used for the design in Figure 5 following the recommendations stated above.

Quick Design Checklist

Aside from the verification of the functionality of the InnoSwitch4 IC, proper operation of the ClampZero IC must also be checked. At the minimum, the following verification tests must be performed.

1. Maximum Drain Voltage – Verify that VDS of ClampZero does not exceed 90% of the breakdown voltage at the highest input voltage and peak (overload) output power in normal operation and during start-up.
2. Maximum Drain Current – Under all conditions, the maximum drain current for the ClampZero switch should be below the specified absolute maximum rating.
3. Thermal Check – Verify that the ClampZero IC does not cause an OTP fault when operating at maximum load throughout the whole input range. Sufficient bias current needs to be supplied to the BP2 pin of the ClampZero device; otherwise, operating with the internal tap can result in higher dissipation on the ClampZero device and eventually reach extreme operating conditions. Triggering OTP of the ClampZero device can cause additional thermal stress on the InnoSwitch4 device and the TVS device used across the clamp capacitor because of loss of zero voltage switching. This can also increase voltage stress on the DRAIN pin of the InnoSwitch4 and ClampZero devices.

Absolute Maximum Ratings[1,2]

DRAIN to S2 Pin Voltage: CPZ1061M & CPZ1062M..... -1.8 V[8] to 650 V
CPZ1075M & CPZ1076M.....-4.2 V[8] to 750 V[6]
DRAIN Pin Peak Current: CPZ1061M .....±3.26 A[3]
CPZ1062M .....±3.87 A[3]
CPZ1075M ..... ±3.2 A[7]
CPZ1076M ..... ±6.5 A[7]
BP1 to S1 Pin Voltage.....-0.3 V to 6 V
IN to S1 Pin Voltage.....-0.3 V to 6 V
BP2 to S2 Pin Voltage.....-0.3 V to 6 V
S2 to S1 Pin Voltage.....-0.3 V to 650 V
Storage Temperature .....-65 to 150 °C
Operating Junction Temperature[4] ..... -40 to 150 °C
Ambient Temperature .....-40 to 105 °C
Lead Temperature[5] ..... 260 °C

Notes:
1. All voltages referenced to low-side or high-side source, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Please refer to Figure 9 about maximum allowable voltage and current combinations.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.
6. Maximum drain voltage (non-repetitive pulse) 750 V, maximum continuous voltage 650 V.
7. Please refer to Figure 17 about maximum voltage and current combinations.
8. Minimum drain voltage (non-DC).

Thermal Resistance

Thermal Resistance: CPZ106xM
(θ_{JA})..... 82 °C/W[2], 76 °C/W[3]
(θ_{JC}).....19 °C/W[1]
CPZ107xM
(θ_{JA})..... 126 °C/W[2], 115 °C/W[3]
(θ_{JC}).....36 °C/W[1]

Notes:
1. Case termperature measured at top center of package body.
2. Solder to 0.36 sq. in (232 mm^2), 2 oz. (610 g/m^2) copper clad.
3. Solder to 1 sq. in (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
BP2 Supply Current	$I_{S1(2)}$	VBP2 = VBP2 + 0.1 V (Switch not Switching) T_J = 25 °C		35	47	55	µA
	$I_{S2(2)}$	VBP2 = VBP2 + 0.1 V (Switch Switching at f_{OSC} = 180 kHz) T_J = 25 °C	CPZ1061M	400	580	800	µA
			CPZ1062M	600	760	950	
			CPZ107xM		1490	1700	
BP2 Pin Charge Current	$I_{CH1(2)}$	VBP2 = 0 V T_J = 25 °C		4.2	5.2	6.2	mA
	$I_{CH2(2)}$	VBP2 = 4 V T_J = 25 °C		4.2	5.2	6.2	
BP2 Pin Voltage	V_{BP2}			4.8	5	5.2	V
BP2 Pin Voltage Hysteresis	$V_{BP2(H2)}$			0.38	0.6	0.8	V
BP2 Shunt Voltage	V_{SHUNT2}	IBP2 = 2 mA		5.2	5.45	5.7	V
BP2 Power-Up Reset Threshold voltage	$V_{BP2(RESET)2}$	T_J = 25 °C	CPZ1061M CPZ1062M	3	3.23	3.45	V
			CPZ1075M CPZ1076M		3.1	3.45	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Control Functions (cont.)						
BP1 Power-Up Reset Threshold voltage	$V_{BP1(RESET)2}$	T_J = 25 °C	3.4	3.8	4.2	V
BP1 Supply Current (Load)	$I_{S1(1)}$	Non Switching, VBP1 = 5.1 V IN: 0 V T_J = 25 °C	20	30	50	µA
	$I_{S2(1)}$	Switching, IN: 500 ns Pulse at 180 kHz V_{BP1} = 5.1 V T_J = 25 °C	60	80	100	µA
IN Pin Voltage Rising Threshold	$V_{IN(R)}$		2.75	2.93	3.25	V
IN Pin Voltage Falling Threshold	$V_{IN(F)}$		1.6	1.82	2.1	V
Delay from HSD High to ClampZero ON	$D_{HSD(ON)}$	CPZ1061M; CPZ1062M	30	57	100	ns
		CPZ1075M; CPZ1076M		54	100	
Delay From HSD Low To ClampZero OFF	$D_{HSD(OFF)}$	CPZ1061M	35	55	80	ns
		CPZ1062M	42	62	90	
		CPZ1075M		67	100	
		CPZ1076M		72	100	
Circuit Protection						
Thermal Shutdown	T_{SD}		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$			70		°C

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Electrical Characteristics							
Off-State Drain Leakage Current	I_{DSS1}	V_{BP2} = V_{BP2} + 0.1 V V_{DS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	V_{BP2} = V_{BP2} + 0.1 V V_{DS} = 325 V T_J = 25 °C			15		µA
On-State Resistance	$R_{DS(ON)}$	CPZ1061M	I_D = 300 mA T_J = 25 °C		3.20	3.68	Ω
			I_D = 300 mA T_J = 100 °C		4.96	5.70	
		CPZ1062M	I_D = 300 mA T_J = 25 °C		1.95	2.24	
			I_D = 300 mA T_J = 100 °C		3.02	3.47	
		CPZ1075M	I_D = 2 A T_J = 25 °C		0.85	1.20	
			I_D = 2 A T_J = 100 °C		1.35	1.80	
		CPZ1076M	I_D = 4 A T_J = 25 °C		0.52	0.78	
			I_D = 4 A T_J = 100 °C		0.78	1.17	

Typical Performance Curves

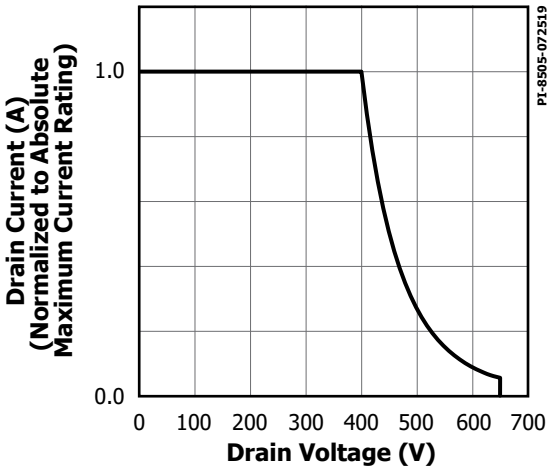


Figure 9. Maximum Allowable Drain Current vs. Drain Voltage.

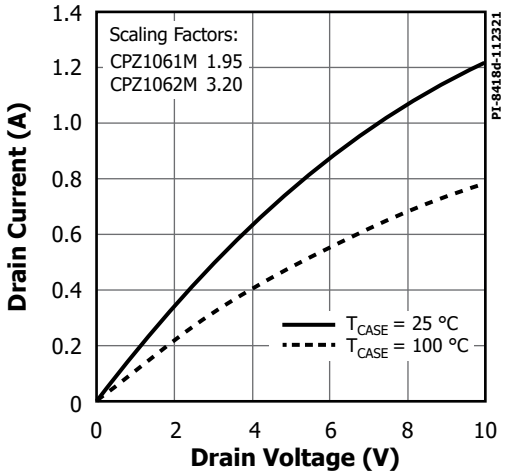


Figure 10. Output Characteristics.

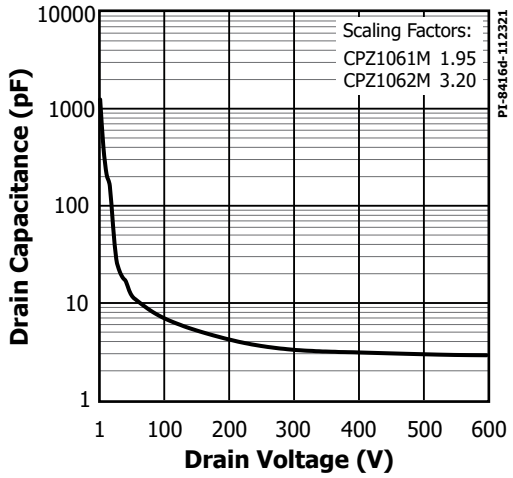


Figure 11. C_{OSS} vs. Drain Voltage.

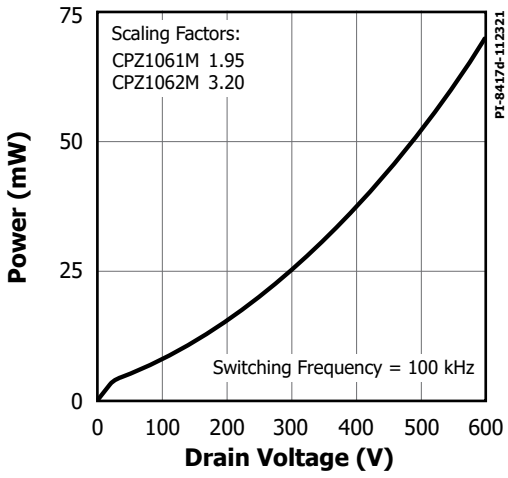


Figure 12. Drain Capacitance Power.

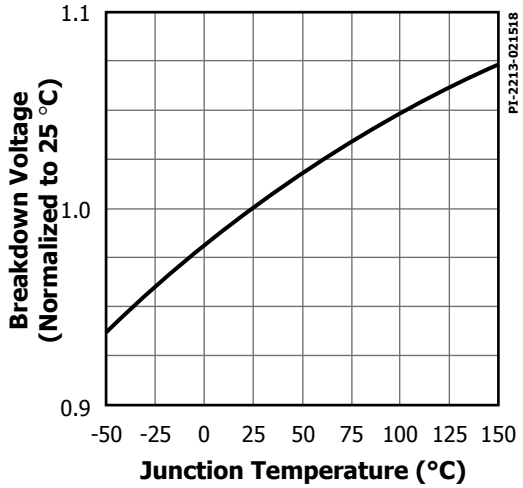


Figure 13. Breakdown vs. Temperature.

Typical Performance Curves

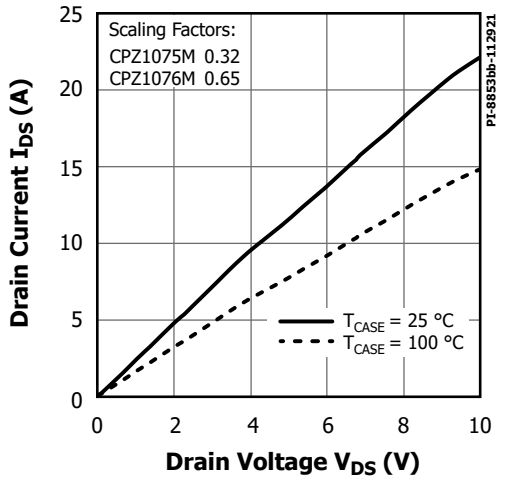


Figure 14. Optional Characteristics.

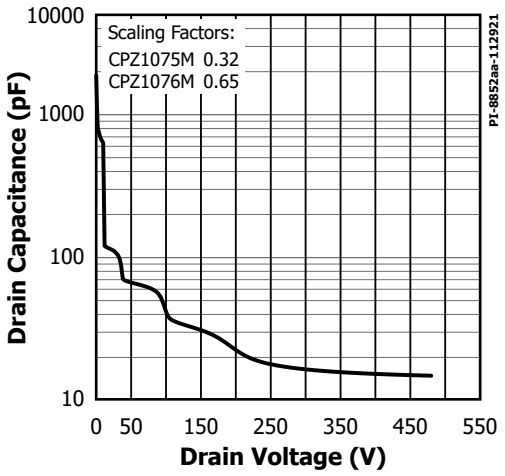


Figure 15. C_{OSS} vs. Drain Voltage.

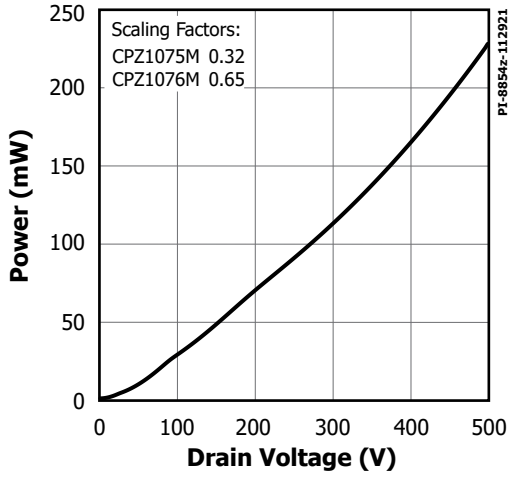


Figure 16. Drain Capacitance Power.

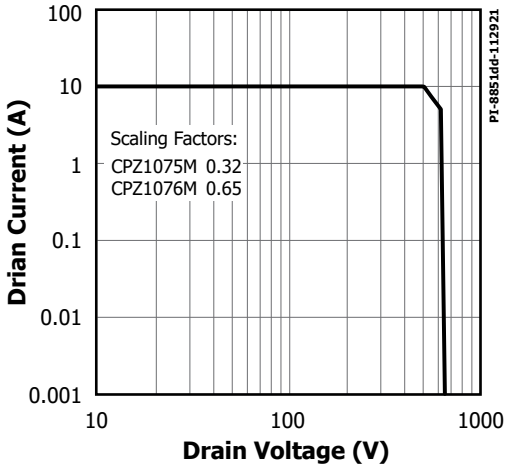
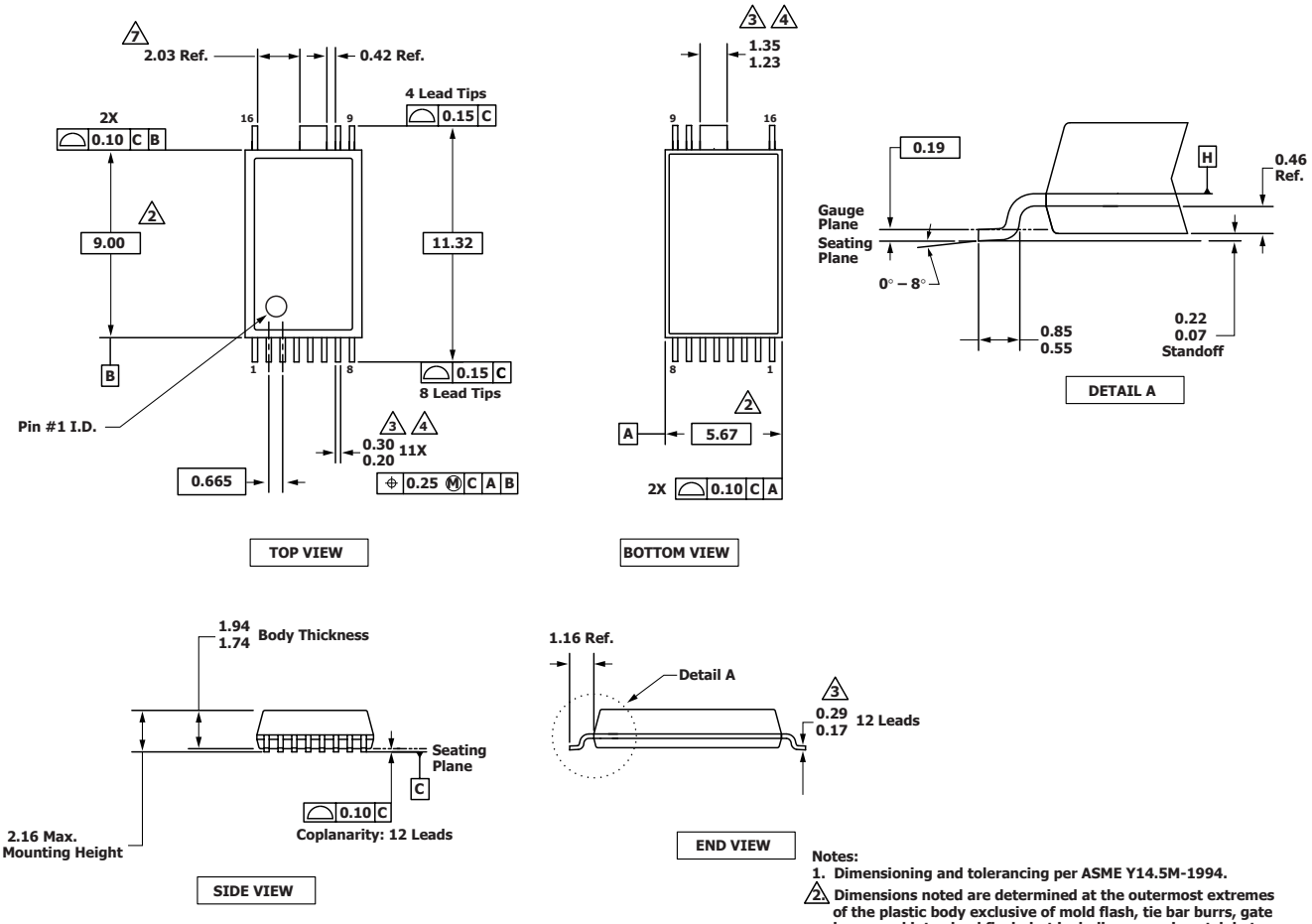


Figure 17. Maximum Allowable Drain Current vs. Drain Voltage.

MinSOP-16A (M Package)



Notes:

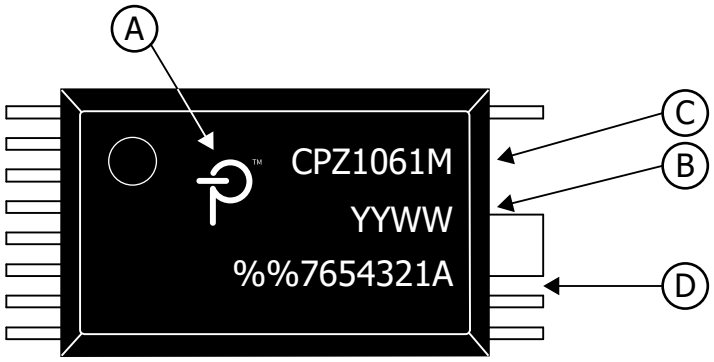
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters.
6. Datums A and B to be determined at Datum H.
7. This dimension is the nominal dimension between leadtips, not including plating, and not including metal protrusions. Metal-to-metal distance (Creepage) is 1.85 mm minimum.

POD_MinSOP-16A_E_042922

PI-8833-051622

PACKAGE MARKING

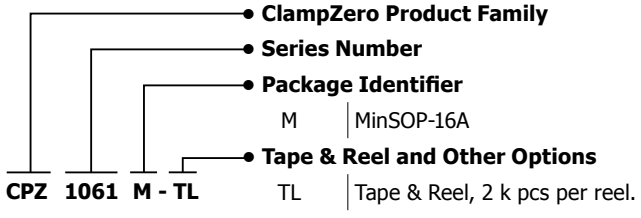
MinSOP-16A



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-9220a-111720

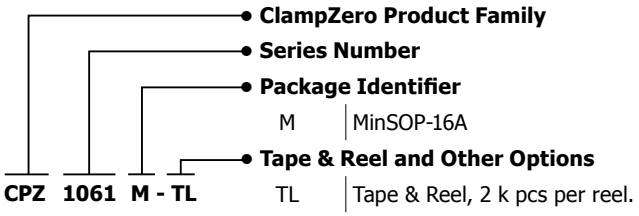
Part Ordering Information



MSL Table

Part Number	MSL Rating
CPZ1061M	3
CPZ1062M	3
CPZ1075M	3
CPZ1076M	3

Part Ordering Information



Revision	Notes	Date
C	Production release.	11/20
D	Introduction of part numbers CPZ1075M, CPZ1076M.	01/22
E	Production release of PowiGaN devices and update the $D_{HSD(ON)}$, $D_{HSD(OFF)}$ and $R_{DS(ON)}$.	03/22
F	Updated MinSOP-16A (M package) drawing.	05/22
G	Updated DRAIN Pin Voltage and Peak Current values in Abs Max Ratings table.	07/22

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