CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7164
Multi Mode Modem

DATASHEET

## 7164FI-1.x, 7164FI-2.x, 7164FI-4.x and 7164FI-6.x Multi Mode Modem

Features

- Half-duplex modem supports multiple modulations and channel spacings
- 7164FI-1.x
  - GMSK/GFSK with BT=0.5, 0.3, 0.27 or 0.25
  - Over-air compatible with FX/MX909B and CMX7143FI-1.x
  - Two frame sync detectors
  - Automatic frame sync detect
  - Rx carrier frequency correction
  - Receive signal quality measurement
- 7164FI-2.x
  - 2/4/8/16-FSK up to 10ksymbols/s in 25kHz e.g. 40kbps for 16-FSK
  - Compatible FEC for CMX7143 and FX/MX919B 4-FSK (not 2-FSK)
  - Over-air compatibility with CMX969 for RD-LAP Tx/Rx
  - Two frame sync detectors
  - Automatic frame sync detect
  - Rx carrier frequency correction
  - Receive signal quality measurement
- 7164FI-4.x
  - 4/16/32/64 QAM up to 96kbps in 25kHz
  - Adaptive Coded Modulation (ACM) features allowing over-the-air commands and on-the-fly changes to modulation rates
  - Different rate, robust FEC choices
  - Channel estimation and equalisation
  - Two frame sync detectors
  - Automatic frame sync detect
  - Rx carrier frequency and phase correction
  - Receive signal quality measurement
- 7164FI-6.x
  - V.23 modulation
  - Two frame sync detectors
  - Automatic frame sync detect
  - Rx carrier frequency correction
  - Receive signal quality measurement
- High Performance I/Q Radio Analogue Interface
  - Tx and Rx: 'direct connect' to zero IF transceiver
  - Simple external RC filters
  - Digital IF filter reconfigures for multiple RF channel spacings (Rx)
  - Deviation control without manual trim (Tx)
  - I/Q trims

- C-BUS host Serial Interface
  - SPI-like with register addressing
  - Read/Write 128-byte FIFOs and data buffers streamline transfers and relax host service latency
- Auxiliary Functions
  - Four 10-bit DACs
  - Autonomous RAMDAC sequencer
  - Automatic support for dc calibration of CMX998
  - Four 10-bit ADCs
  - ADC averaging and trip on high/low 'watch' modes
  - Four GPIO
  - Sequence GPIO on Tx or Rx trigger
  - Start Tx on digital trigger input
- Master C-BUS/SPI Serial Interface
  - For external slave devices e.g. RF transceiver and synthesiser
  - Pass-through mode expands host C-BUS/SPI capacity
- Two Synthesised Clock Generators
- Low Power 3.3V Operation with Powersave Functions
- Small 64-pin VQFN and LQFP Packages

Applications

- High Performance Narrowband Data Radio
  - Telemetry/SCADA/data modems
  - 6.25kHz to 25kHz RF channel spacing
  - Compatible worldwide e.g. ETSI, FCC, ARIB, etc.
  - FCC Part 90 per new spectral efficiency requirements
- Digital Software Defined Radio (SDR)
- High-speed Wireless Data
- Mobile Data over Fading Channels
- V.23 compatibility for interoperability with legacy equipment in the field
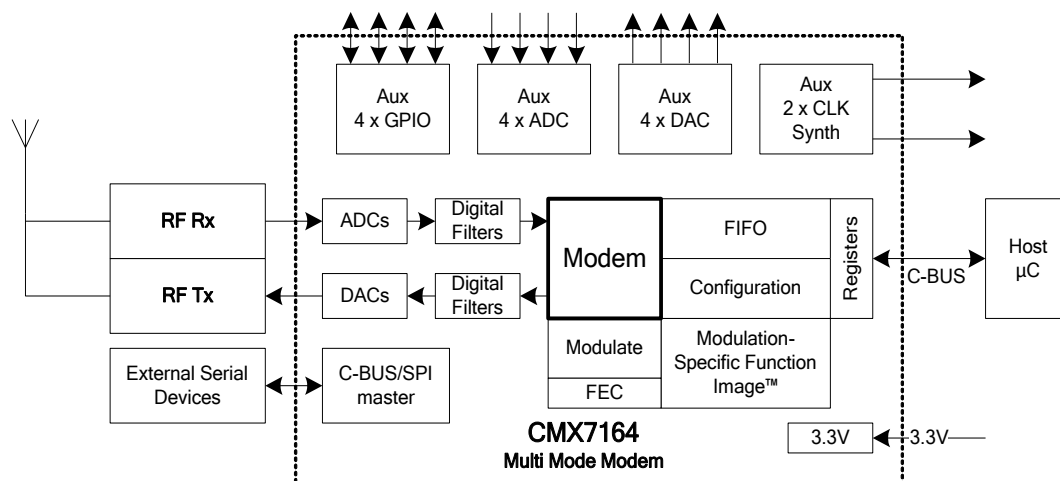
1   Brief Description

The CMX7164 Multi Mode Modem is a half-duplex device currently supporting GMSK/GFSK, 4/16/32/64-QAM, 2/4/8/16-Level FSK and V.23 modes in multiple channel spacings under host control. Its *Function Image (FI) is loaded to initialise the device and determine modulation types.

The 7164FI-1.x supports GMSK/GFSK modulation, with BT=0.5, 0.3, 0.27, or 0.25. User-programmable filters are also possible (contact CML Technical Support for further information). The 7164FI-1.x supports up to 20kbps. Flexible bit rates support a wide range of applications requiring a selectable bit rate and robustness. The 7164FI-1.x supports zero IF (I/Q) and two-point modulation (Mod1/2) transmit modes, with zero IF receive mode. The GMSK/GFSK data is over-air compatible with the FX/MX909B and the CMX7143FI-1.x.

The 7164FI-2.x supports 2-FSK, 4-FSK, 8-FSK, and 16-FSK modulations, root raised cosine filtered with α=0.2 with optional sinc filtering. User-programmable filters are also possible (contact CML Technical Support for further information). The 7164FI-2.x supports up to 10ksymbols/s in a 25kHz channel. Flexible bit rates support a wide range of applications requiring a selectable bit rate and robustness. The 7164FI-2.x supports zero IF (I/Q) and two-point modulation (Mod1/2) transmit modes, with zero IF receive mode. The data is over-air compatible with the FX/MX919B and the (CMX)7143FI-2.x. Additionally, 4-FSK coded mode also supports RD-LAP channel coding which is over-air compatible with CMX969.

The 7164FI-4.x supports 4-, 16-, 32- and 64-QAM modulations, root raised cosine filtered with α=0.2, 0.35 or a user programmable filter (contact CML Technical Support for further information). The 7164FI-4.x supports up to 96kbps in a 25kHz channel, with channel estimation and equalisation to provide robust performance under realistic channel conditions. The 7164FI-4.x supports zero IF (I/Q) transmit and receive. QAM data is over-air compatible with the CMX7163FI-4.x.

FI-2.x and FI-4.x include Adaptive Coded Modulation (ACM) features that add the following increased functionality and flexibility to the device:

- *Over The Air Commands* – A Tx CMX7164 host driver can effectively control an Rx terminal's CMX7164 via commands transported by the link. This enables a Tx terminal to dynamically select over air burst structure in response to application requirements and have bursts properly received by Rx terminals that do not have prior knowledge of the structure. The Rx host first commands the Rx CMX7164 to expect and treat a portion of the next received data payload as an Over The Air Command that is pushed into the front of the Rx CMX7164 Command FIFO for top priority execution.

- *Change FI-2.x RRC FSK or FI-4.x M-QAM Modulation Format* – allows the modulation format (4-, 8- or 16-FSK for FI-2.x formatted blocks, 2-, 4-, 8-, or 16-FSK for FI-2.x raw blocks, or 4-, 16-, 32- or 64-QAM for FI-4.x) of the next burst to be quickly changed without the device first having to enter Idle mode. This is achieved by writing an appropriate command that selects modulation format. The newly-configured modulation format will remain operational, in both transmit and receive modes, until the device is either reset or another modulation change selection is made.

- *Configurable Error Magnitude and RSSI Reporting Modes* – To better guide dynamic host selection of modulation type and coding, channel quality assessment modes synchronize Error Magnitude and RSSI measurements and support configuring their measurement period, selecting one-shot or repeating operation, and reporting both RSSI and AGC gain step at the time of Rx Frame Sync detection.

The 7164FI-6.x supports V.23 modulation at 1200 and 300 baud to provide half-duplex modem functionality for interoperability with legacy equipment in the field. The 7164FI-6.x supports 1 to 8 byte data blocks with start bit, stop bit and parity generation in transmit and start bit, stop bit and parity checking and removal in receive.

Within this Datasheet and the accompanying User Manual any reference to FI1-x, FI-2.x, FI-4.x or FI-6.x is intended to respectively refer to 7164FI1.x, 7164FI-2.x, 7164FI-4.x, or 7164FI-6.x.

Forward error correction and raw modes are available and support user-defined packet structures to support a range of applications. For greater flexibility FI-2.x and FI-4.x support different rate FEC modes and user defined block formats via configurable payload size, CRC size and FEC overhead. Receive signal quality measurement is supported to assess channel conditions.

High-performance digital IF filters may be reconfigured to support multiple channel spacings via host command. This feature may eliminate the need to switch between multiple, discrete IF filters.

An integrated analogue interface supports 'direct connection' to zero IF I/Q radio transceivers with few external components; no external codecs are required.

Intelligent auxiliary ADC, DAC and GPIO sub-systems perform valuable functions and minimise host interaction and host I/O resources. Two synthesised system clock generators develop clock signals for off-chip use. The C-BUS/SPI master interface expands host C-BUS/SPI ports to control external devices.

Function Image™. The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™ data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from a host µC over the C-BUS serial interface or from an external memory device. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

The CMX7164 operates from a 3.3V supply and includes selectable powersaving modes. It is available in 64-VQFN and 64-LQFP packages.

Note that text shown in pale grey indicates features that will be supported in future versions of the device.

This Data Sheet is the first part of a two-part document.

CONTENTS

Information in this datasheet should not be relied upon for final product design. It is recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

1.1   History

Version	Changes	Date (D/M/Y)
29	• Section 13.2.6 added 300 baud option to FI-6 using P4.2:b0	12/05/21
28	• Section 13.2.5 changed the default tail lengths for FI-1 and FI-2 to 7 and 6 respectively.	14/01/20
27	• Section 14.4 corrected and clarified P5.20 High Gain Step Name description • Section 13.1.15 – AGC Control $65 write register description updated to include new functionality controlled by b11-13 • Section 13.2 clarified, made more complete and corrected to indicate that Reg Done Select - $69 write register PRG bit b0 must be set to enable Reg Done handshaking on writes to the Programming Register - $6A write register • Section 13.2.6 amended to include description of P4.1-selectable Tx I/Q lowpass filter • Section 13.2.6 – P4.5 – added new alternate I/Q tracking algorithm (FI-2 only), improving 8- and 16-FSK operation.	18/12/19
26	• Section 7.6.1 – clarification to description for transmit path levels and modulation envelope ramping • Section 10.1 - Updated Figure 82 (QAM Mappings) • Section 13.1.4 – Clarification to description for FIFO Control $50 register • Section 13.2.13 – for FI-2.x changed P11.1 Receiver Response Equaliser Training Gain default value from 6000 to 150	03/04/19
25	• Section 13.1.11 – Maximum supported Thru-Port SPI Mode read and write transaction length increased to 32 bits • Section 13.2.3 – Corrected small rounding error in calculated default AuxADC sample rate • Section 13.2.8 – New rules have been created for defining SSP Macros. This enhances SSP Macros to support both longer macro sequences and SPI Mode transactions as long as 32 bits. This feature enhancement changes the associated SSP Macro definition API. • Section 13.1.19 – In FI-2.x added AutoModMode Rx with Automatic modulation type detection for Formatted Data • Section 13.1.14 – New feature: Writing to GPIO control C-BUS register $64 with Forced Set b15 set to 1 will override any automatic or manual control of GPIO pins set using program block 5. • Section 13.2.5 – New feature: the initial value of the RD-LAP 6 bit CRC register can be set using a new program register P3.18. • Section 13.2.6 – Clarified description of Transmit Modulation Envelope Ramping • Section 13.2.9 – New feature: For designs that use fewer than 8 total AGC gain steps (7-0), P7.18 limits the minimum AGC gain step used. • Sections 7.4.22 and 13.2.6 – New feature: AGC Observe diagnostic mode to enable external observation of internal AGC state • Section 7.6.1 – Transmit path levels and modulation envelope ramping description clarified and enhanced. • Section 13.1.13 – Added SPI ThruPort Data Write2 - $67 register	05/02/18

| 24 | • Section 1 – corrected Over the Air Commands description and added description of Configurable Error Magnitude and RSSI Reporting Modes
• Sections 7.4.21, 7.4.21.1, 13.1.11, 13.2.8, and 13.2.9 – added and expanded descriptions of SPI Thru-Port operation and managing Thru-Port contention
• Sections 7.4.22 SPI/C-BUS AGC and 13.1.15 AGC Control – expanded AGC function description
• Section 9.3 FI-2.x new coding rate tables for 4-, 8- and 16-FSK native format
• Section 13.1.3 FI-2.x
    o new Change Modulation command to change Tx modulation between bursts, while keeping modem in Tx mode
    o removed command for 8-, 16-FSK high rate FEC
    o new reset CRC command
    o new Over the Air Command feature
    o new coding rate tables for native format
• Section 13.1.19 – Modem Mode and Control – Clarified the SSP Macro and Rx mode operation descriptions
• Section 13.2.5 FI-1.x – added P3.0 and P3.1 detailed descriptions
• Section 13.2.5 FI-2.x – added user defined CRCs and corrected Tail Pattern example description
• Section 13.2.6 FI-1.x , FI-2.x P4.3 – new EM and RSSI reporting mode and period
• Section 13.2.6 FI-2.x and FI-4.x – P4.6 Maximum Rx FEC Effort mode added
• Section 13.2.6 FI-1 , FI-2.x and FI-4.x – P4.11 Automatic Gain Control Debug added
• Section 13.2.8 FI-1, FI-2 – added SSP Thru-Port Macros
• Section 13.2.13 FI-2.x
    o corrected and expanded table that maps user defined formatted blocks and the default formatted blocks that they replace
    o corrected and clarified descriptions
    o added user defined formatted block sizes and coding rates
• Section 14.11 FI-2.x and FI-4.x – added application note section on measuring Rx Delay with Maximum Rx FEC Effort enabled
• Various editorial corrections | 01/06/16 |

23	• Section 10.1: FI-4.x - added 32-QAM as a new modulation option.
	• Section 10.3: 32-QAM coding rate added to Table 8
	• Section 13.1.3: FI-4.x - New Command FIFO commands to enable:
	    ○ 8,16 or 32 bit CRCs in formatted blocks,
	    ○ change QAM modulation type between bursts without the need to enter Idle Mode,
	    ○ the first N bytes in the next received data block are FIFO commands sent over the air (Over the Air Command Expected feature).
	• Section 13.1.3 – description of Over the Air Command Expected feature added.
	• Section 13.1.19: FI-4.x - added new SPI Macro field to Modem Mode and Control register.
	• Section 13.1.3, Table 18: coding rate for 32-QAM added
	• Section 13.1.27: FI-4.x - new Receive FIFO commands for reporting when 32-QAM is automatically detected and new FIFO commands for automatically reporting the Error Magnitude and RSSI when frame sync was detected.
	• Section 13.2.5: FI-4.x - new program blocks for 8, 16 or 32 bit user defined CRCs.
	• Section 13.2.6: FI-4.x - new program blocks to set Error Magnitude and RSSI reporting period and behaviour.
	• Section 13.2.8: FI-4.x - new program blocks to enable SSP Macros.
	• Section 13.2.13: FI-4.x - new program block 12 enabling user defined formatted block sizes and coding rates.
		24/02/16

22	• Added information covering 7164FI-6.x • Section 7.4.22: AGC control algorithm can now be used to control a second device using one of the available GPIO pins. • Section 10.1 Updated Figure 82 (QAM Mappings) • Section 12.2: Original C-BUS timing diagram replaced by latest version • Section 13.1.22:Register $B3 – changed reserved bit 9 set value and added example settings • Section 13.1.32: description for register $77: b11-0 description corrected to describe RSSI averaging period set by P4.3 • Section 13.2.6 (Prog Block 4 – Modulation Control): P4.5 entry corrected to indicate that the parameter also supports FI-1.x • Section 13.2.6: Added description for P4.3 • Section 13.2.7: Transmit sequence – added description for minimum pulse period on GPIOA to trigger transmission and corrected the explanation of DC Calibration Sequence delays for default values • Sections 13.1.8, 13.1.9, 13.1.10, and 13.1.15: Descriptions for registers $5D, $5E, $5F, $60, $61, $65 – added note regarding delay between successive writes • Section 13.2.9: Added Program Block 7.17 for AGC control of external device via GPIO pins. • Section 14.10: App Note updated for clarification • Section 12: Performance figures replace TBDs	11/05/15

21	• Section 13.1.22: $B3 register table corrected and note added describing correct settings for the I/Q output drivers • Section 0: Table for P0.0, b11-0 corrected to show value of 1 as invalid • Section 13.2.5: Table showing new program registers P3.3 to P3.6 and associated description • Section 13.2.6: Summary table, and subsequent description, Program Block 4, P4.5 corrected to say that two of the values apply also to FI-1.x. • Section 13.2.6: Summary table for Program Block 4, P4.8:b15-2 corrected to say "reserved, set to 1" • Section 14.10: New Application Note - Aborting Rx and Restarting Frame Sync Search • Miscellaneous typographical and editorial improvements	02/09/14
20	• Section 13.2.4: Clarification to description on frame sync detection and error tolerance. • Section 13.2.6: Entries and descriptions for P4.8 to P4.10 which offer additional control	19/06/14
19	• Added 16-FSK operation • Section 11: Performance figures replace TBDs • Section 12.2.4: Entire section rewritten to improve clarity	12/05/14
18	• Described the state of GPIO pins after reset and before a Function Image is loaded • Added voltage differential between power supplies to section 11 specification • Added description of RAMDAC ramp profile scaling • Added description of modulation envelope ramp control • Added control method for narrower channel filter options in FI-1.x • Added information on 8/16 FSK, channel coding • Figure 5 replaced by new drawing showing removal of unused components • Miscellaneous typographical and editorial improvements	12/02/14
16/17	• Update of graphs to improve datasheet clarity in v14. Datasheet becomes v16.	21/10/13
14/15	• Added details of FI-2 Equaliser operation • Added programming register control for I/Q dc offset acquisition • Added corrections to frame sync programming register description • Added power connection to pin 37 in Figure 7 • Enhancements for custom filter support • Added payload byte lengths to Tables 3, 4, 5 and 6 • Document formatting corrected and typos/clarifications	01/08/13
11/12/13	• Added RD-LAP channel coding block types in FI-2.x • Clarification of FI-1.x channel coding	15/03/13
10	• Add 8-FSK and 16-FSK operation in FI-2.x	10/01/13
9	• Add GMSK/GFSK operation in FI-1.x	30/4/12
8	• Added details of FI-4 Equaliser operation and control: Mode register, programming block • Added details of programming block read mechanism (Available for selected programming registers only) • Updated receive performance curves for FI-4 • Added description of soft decision output bits for FI-2 only • Added details of bus hold function for unused inputs • Added details of Core regulator select • Corrected conditions under which current measurements were made • Changed reference to input impedance of I/Q INPUTs • Typos/clarifications	9/1/12

7	• Remove constraint on use of document with FI-2.x, as the latter is now updated.	21/09/11
6	• Advice in section 5.5 greyed out as not implemented in current FI.	22/08/11
5	• Added advice about terminating unconnected GPIO pins in section 5.5	17/8/11
4	• Added details of default and inverting gains to the description of the I/Q Output Control - $5D, $5E registers • Pointed out correct use of handshaking when using signal control (Register $61) to select I and Q offset measurements (Registers $75 and $76) • Clarified behaviour of the I and Q offset registers (Rx dc offset correction) when using automatic Rx IQ dc mode • Clarified behaviour and scaling of RSSI measurements • Documented further AGC controls added in FI-4.0.5.4, and described AGC operation in detail • Documented the Pll On bit added to the mode register in FI-4.0.5.4, which provides a fast idle mode for programming register modifications without powersave, but with improved speed • Added parameters in Program Block 1 to reduce delay when transitioning from Idle to Tx or Rx modes • Added information about receive dynamic range • Corrected and clarified scaling of Tx output fine control.	3/8/11
3	• Remove information indicating that a reset with no FI load is possible. See sections 11.1.1 Reset Operations, 7.3 Function image loading • FIFO level interrupts to the host require re-arming using $50 FIFO control. See 11.1.4 FIFO Control $50 • Include description for "I/Q Input dc correction loop gain". See 11.1.10 Signal control $61 • Spectrum figure ACP mislabeled as for 25kHz when it is for 12.5kHz. See fig 58 • Expand description of FI-2 4-FSK deviation configuration. See 11.1.10 Signal control $61 • Include over-air symbol sequence for FI-2 (2-FSK and 4-FSK) and FI-4 data. See 7.4.15, 11.1.3 and 11.1.26. Specifically this matters for bit wise transfers, indicating which bits are valid • Default values in 11.1.9 to be changed: $07FF becomes $0400; $0801 becomes $0C00 • Addition of "Tx Done flag set on completion of DC Calibration" to 7.4.11, 11.1.18 and 11.1.36. Also indicate that AuxADC paths, etc in 7.4.11 are fixed permanently, by changing the description "assumed" to "required" • Figure 34 to show "Main PLL out" sourced directly from the Xtal in Idle mode • Update Figure 3 and correct minor typographical errors (Fig 43)	15/4/11
2	• Clarify text at the end of section 12.3.2 • Change b11 to b9 in section 11.1.14 • Remove FI Load Activation Block references and describe default states in section11.1.2 and Table 5 • Clarify bit names in section 11.1.20, to avoid duplication • Add missing action #20 in section 11.2.1	22/3/11
1	• Original document, prepared for first alpha release of FI.	24/2/11

2   Block Diagrams

Transmit Functions

- Tx Data Buffer
- Channel Coder (FI-1.x, FI-2.x & FI-4.x)
- Data Modulator FI-1.x, FI-2.x & FI-6.x: I/Q or 2-point modulation FI-4.x: I/Q output
- IOUTPUTP / IOUTPUTN
- QOUTPUTP / QOUTPUTN

Receive Functions

- IINPUTP / IINPUTN
- Channel Filter
- QINPUTP / QINPUTN
- Channel Filter
- Data Demodulator
- Channel Decoder (FI-1.x, FI-2.x & FI-4.x) Frame Sync Detect (FI-6.x)
- Rx Data Buffer

Auxiliary Functions

- MUX
- ADC 1 / Thresholds / Averaging
- ADC 2 / Thresholds / Averaging
- ADC 3 / Thresholds / Averaging
- ADC 4 / Thresholds / Averaging
- AUXADC1
- AUXADC2
- AUXADC3
- AUXADC4
- Auxiliary Multiplexed ADCs

- Command FIFO
- Rx Data FIFO
- Registers
- C-BUS Interface
- IRQN
- RDATA
- CSN
- CDATA
- SCLK

- GPIOA
- GPIOB
- GPIOC
- GPIOD
- GPIO with O/P Sequencer
- FI Configured I/O

- System Clock Div 1
- System Clock Div 2
- System Clock PLL
- Main Clock PLL
- Crystal Oscillator
- System Clocks
- SYSCLK1
- SYSCLK2
- XTAL/ CLOCK
- XTALN

- AUXDAC1
- DAC 1
- Ramp-profile RAM
- AUXDAC2
- DAC 2
- AUXDAC3
- DAC 3
- AUXDAC4
- DAC 4
- Auxiliary DACs

- Power control

- MOSI
- CLK
- MISO
- SPI Thru-Port (SSP)
- Single Host Thru-Port Commands (R/W)
- SSP Macro Thru-Port Commands (W)
- AGC Controller
- SSOUT0
- SSOUT1
- SSOUT2
- CMX998 DC Cal Controller
- Flash Boot
- SPI Thru-Port Control

- Device Reset
- Bias
- Reg.
- Boot Control

- RESETN
- AVDD
- VBIAS
- AVSS
- ADCREF
- DVDD3V3
- DVCORE
- DVSS
- DACREF
- BOOTEN1
- BOOTEN2

Figure 1 Overall Block Diagram

Figure 1 illustrates the overall functionality of the CMX7164, detailing the auxiliary functions. The following figures expand upon the transmit and receive functions.
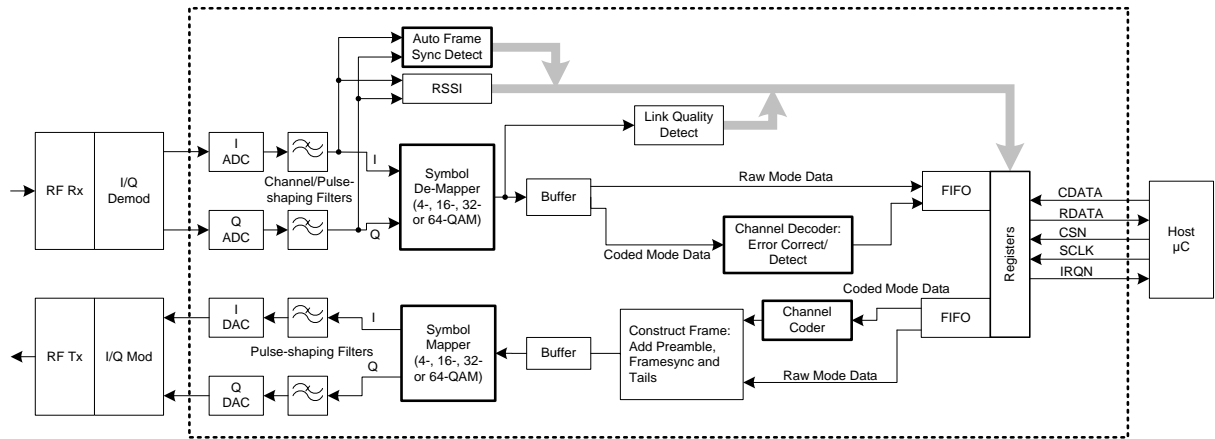
Figure 2 FI-4.x Block Diagram – I/Q Tx and Rx
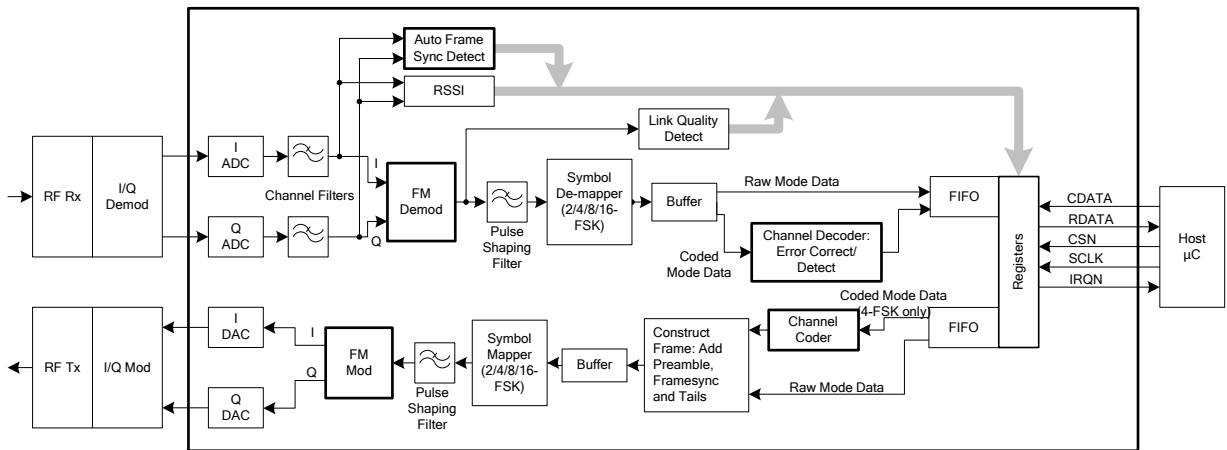
Figure 3 FI-1.x / FI-2.x Block Diagram – I/Q Tx and Rx
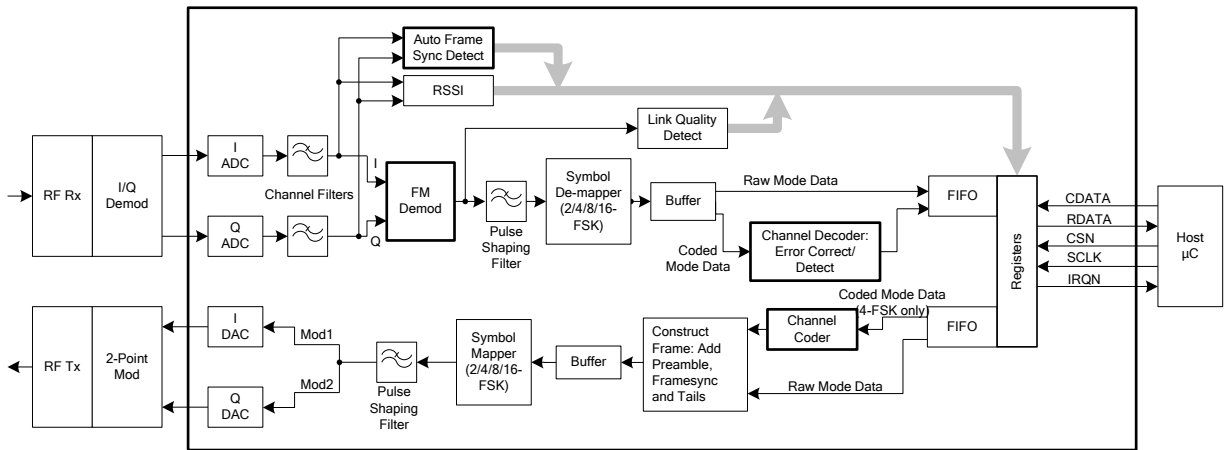
Figure 4 FI-1.x / FI-2.x Block Diagram – two-point Tx with I/Q Rx
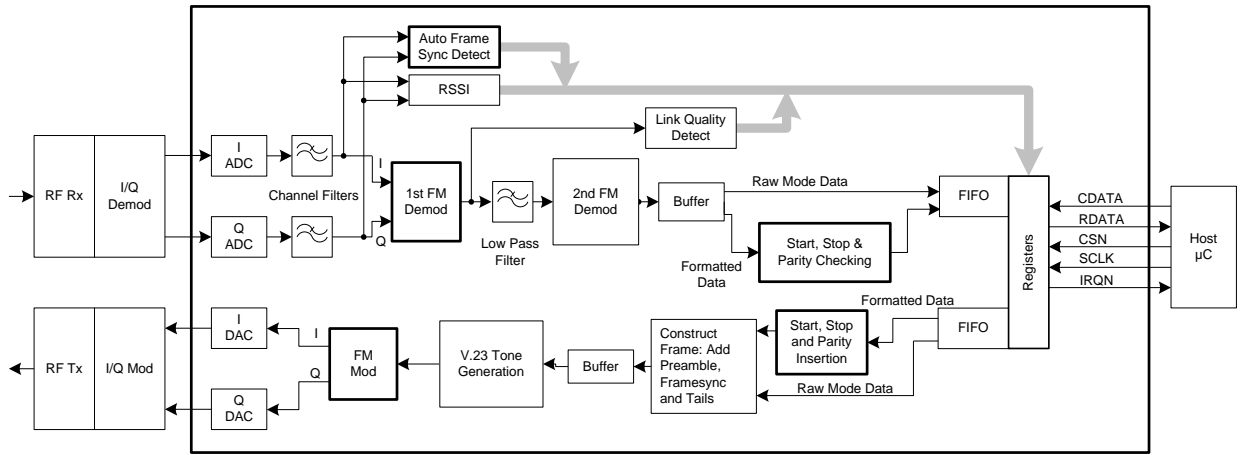
Figure 5 FI-6.x Block Diagram - I/Q Tx and Rx
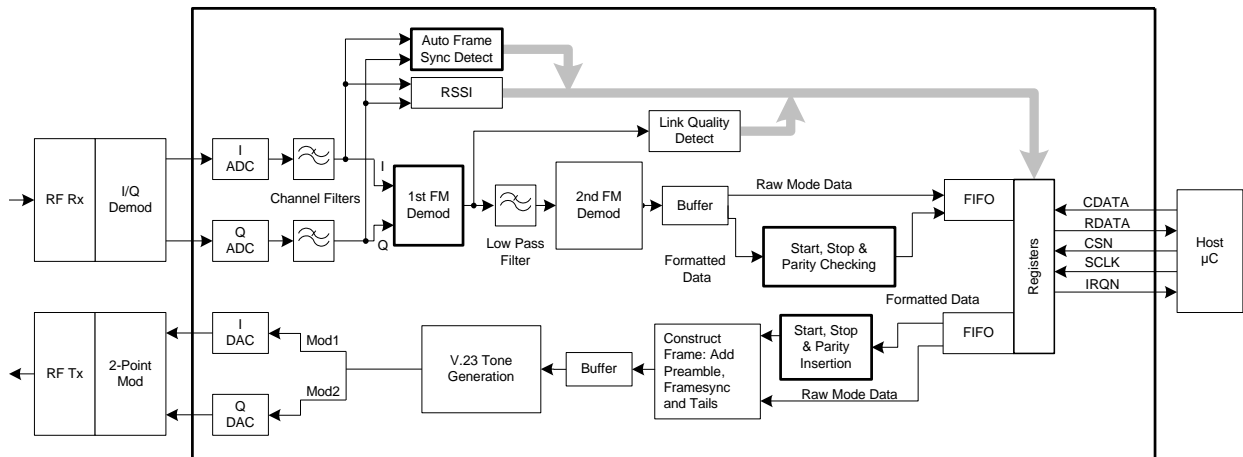
Figure 6 FI-6.x Block Diagram - Two-point Tx with I/Q Rx

3   Signal List

64-pin Q1/L9	Pin		Description
Pin No.	Name	Type	
1	GPIOB	BI	General Purpose I/O
2	BOOTEN1	IP+PU	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determine the Function Image™ load interface
3	BOOTEN2	IP+PU	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determine the Function Image™ load interface
4	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
5	DVDD 3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DVSS by capacitors mounted close to the supply pins.
6	SSOUT2	OP	SPI: Slave Select Out 2
7	RESETN	IP	Logic input used to reset the device (active low)
8	GPIOC	BI	General Purpose I/O
9	GPIOD	BI	General Purpose I/O
10	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
11	NC	NC	Do not connect
12	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVSS by capacitors mounted close to the device pins.
13	NC	NC	May also be connected to AVSS
14	NC	NC	Do not connect
15	NC	NC	Do not connect
16	NC	NC	May also be connected to AVDD
17	IOUTPUTP	OP	Differential outputs for I channel; 'P' is positive, 'N' is negative. Together these are referred to as the I Output. When the 7164 FI-1 or FI-2 is in two-point modulation mode the I Output is used as 'Mod 1'.
18	IOUTPUTN	OP	
19	QOUTPUTP	OP	Differential outputs for Q channel; 'P' is positive, 'N' is negative. Together these are referred to as the Q Output. When the 7164 FI-1 or FI-2 is in two-point modulation mode the Q Output is used as 'Mod 2'.
20	QOUTPUTN	OP	
21	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits
22	DACREF		DAC reference voltage, connect to AVSS
23	NC	NC	Do not connect
24	NC	NC	Do not connect
25	NC	NC	Do not connect

64-pin Q1/L9	Pin		Description
Pin No.	Name	Type	
26	NC	NC	Do not connect
27	VBIAS	OP	Internally generated bias voltage of approximately $AV_{DD}/2$. If V_{BIAS} is powersaved this pin will be connected via a high impedance to AV_{DD}. This pin must be decoupled to AV_{SS} by a capacitor mounted close to the device pins.
28	IINPUTP	IP	Differential inputs for I channel signals; 'P' is positive, 'N' is negative. Together these are referred to as the I Input.
29	IINPUTN	IP	
30	ADCREF		ADC reference voltage; connect to AV_{SS}
31	QINPUTP	IP	Differential inputs for Q channel signals; 'P' is positive, 'N' is negative. Together these are referred to as the Q Input.
32	QINPUTN	IP	
33	AUXADC1	IP	Auxiliary ADC input 1
34	AUXADC2	IP	Auxiliary ADC input 2
35	AUXADC3	IP	Auxiliary ADC input 3
36	AUXADC4	IP	Auxiliary ADC input 4
37	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.
38	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits
39	AUXDAC1	OP	Auxiliary DAC output 1 (Optionally the RAMDAC output)
40	AUXDAC2	OP	Auxiliary DAC output 2
41	AUXDAC3	OP	Auxiliary DAC output 3
42	AUXDAC4	OP	Auxiliary DAC output 4
43	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
44	DVCORE	PWR	Internally generated digital core voltage of approximately 1.8V. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins
45	DVDD3V3	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DV_{SS} by capacitors mounted close to the supply pins.
46	NC	NC	Do not connect
47	NC	NC	May also be connected to DVSS
48	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
49	XTALN	OP	Output of the on-chip Xtal oscillator inverter
50	XTAL/CLOCK	IP	Input to the oscillator inverter from the Xtal circuit or external clock source
51	SYSCLK1	OP	Synthesised digital clock output 1

64-pin Q1/L9	Pin		Description
Pin No.	Name	Type	
52	SYSCLK2	OP	Synthesised digital clock output 2
53	SCLK	IP	C-BUS serial clock input from the µC
54	RDATA	TS OP	3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
55	CDATA	IP	C-BUS serial data input from the µC
56	CSN	IP	C-BUS chip select input from the µC
57	IRQN	OP	'wire-Orable' output for connection to the Interrupt Request input of the µC. This output is pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor is required.
58	DVCORE	PWR	Internally generated digital core voltage of approximately 1.8V. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins
59	MOSI	OP	SPI: Master Out Slave In
60	SSOUT1	OP	SPI: Slave Select Out 1
61	MISO	IP	SPI: Master In Slave Out
62	SSOUT0	OP	SPI: Slave Select Out 0
63	CLK	OP	SPI: Serial Clock
64	GPIOA	BI	General Purpose I/O
EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on the Q1 package only) may be electrically unconnected or, alternatively, may be connected to Analogue ground (AVss). **No other electrical connection is permitted.**

Notes:

IP	=	Input (+ PU/PD = internal pull-up / pull-down resistor of approximately 75kΩ)
OP	=	Output
BI	=	Bidirectional
TS OP	=	3-state Output
PWR	=	Power Connection
NC	=	No Connection - should NOT be connected to any signal

4   PCB Layout Guidelines and Power Supply Decoupling
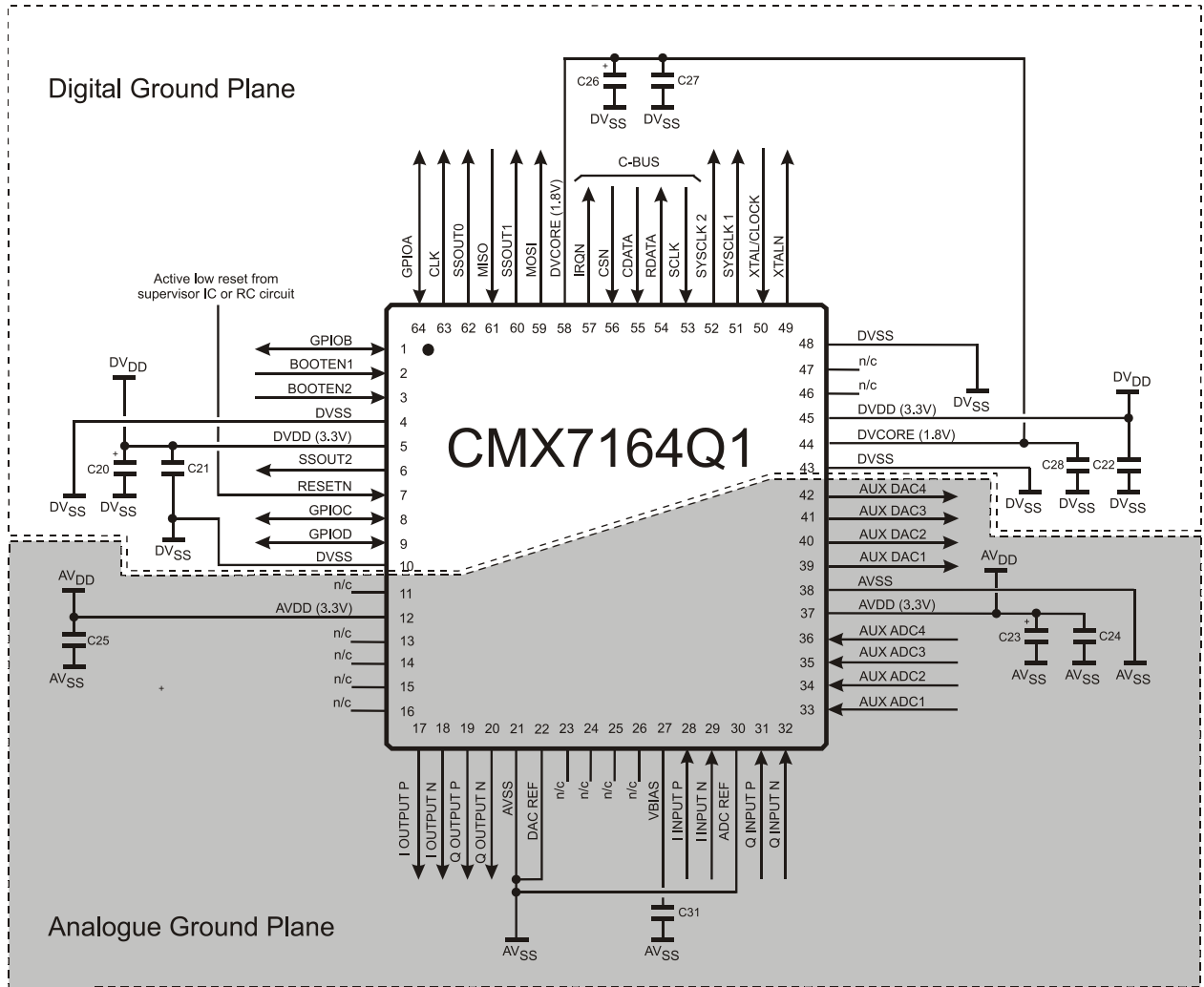
C20	10µF	C26	22µF
C21	10nF	C27	10nF
C22	10nF	C28	10nF
C23	10µF	C31	100nF
C24	10nF		
C25	10nF		

Figure 7 CMX7164 Power Supply and De-coupling

Notes:

To achieve good noise performance, AV_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals is very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX7164 analogue area to provide a low impedance connection between the AVSS pins and the AV_{DD} and V_{BIAS} decoupling capacitors.

5   External Components

5.1   Xtal Interface
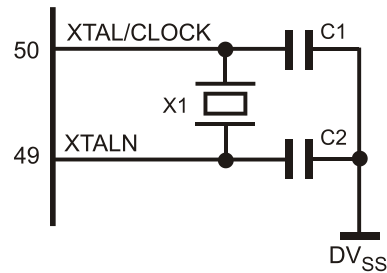
X1   For frequency range see
        12.1.2 Operating Limits
C1   22pF Typical
C2   22pF Typical

Figure 8   Recommended External Components – Xtal Interface

Notes:
The clock circuit can operate with either a Xtal or external clock generator. If using an external clock generator it should be connected to the XTAL/CLOCK pin and the xtal and other components are not required. For external clock generator frequency range see 12.1.2 Operating Limits. When using an external clock generator the Xtal oscillator circuit may be disabled to save power, see 13.2.3 Program Block 1 – Clock Control for details. Also refer to section 7.1 Xtal Frequency.

The tracks between the Xtal and the device pins should be as short as possible to achieve maximum stability and best start up performance. It is also important to achieve a low impedance connection between the Xtal capacitors and the ground plane.

The DV_{SS} to the Xtal oscillator capacitors C1 and C2 should be of low impedance and preferably be part of the DV_{SS} ground plane to ensure reliable start up. For correct values of capacitors C1 and C2 refer to the documentation of the Xtal used.

5.2   C-BUS Interface
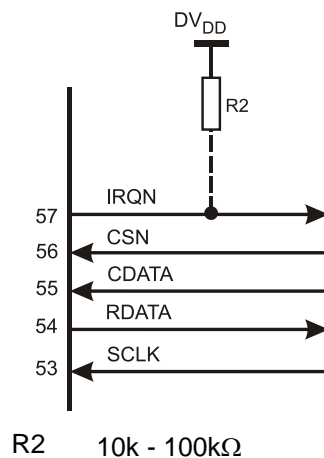
R2   10k - 100kΩ

Figure 9   Recommended External Components – C-BUS Interface

Note: If the IRQN line is connected to other compatible pull-down devices only one pull-up resistor is required on the IRQN node.

5.3 I/Q Output Reconstruction Filter

The CMX7164 I/Q Outputs provide internal reconstruction filtering with four selectable bandwidths (-3dB point shown in section 13.1.22). The bandwidth of the internal reconstruction filter may be selected using the I/Q Output Configuration - $B3 write or Signal Control - $61 write registers.

To complete the I/Q output reconstruction filter one of the following external RC networks should be used for each of the differential outputs. The external RC network should have a bandwidth that matches the bandwidth of the selected internal reconstruction filter.

Bandwidth (kHz)	R3-R6 (kOhms)	C9-C10 (pF)
100	22	33
50	20	75
25	22	150
12.5	22	270
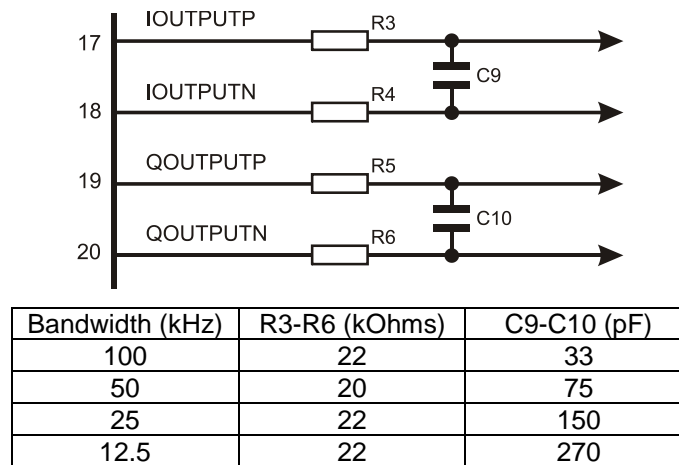
Figure 10 Recommended External Components – I/Q Output Reconstruction Filter

When transmitting an I/Q signal, each I/Q output will produce a signal with bandwidth half the channel bandwidth. A reconstruction filter with a –3dB point close to half the channel bandwidth will therefore have significant roll off within the channel bandwidth – which is undesirable. An appropriate choice for channels occupying up to a 25kHz bandwidth (channel bandwidth/2 = 12.5kHz) would be a reconstruction filter of 25kHz bandwidth.

5.4 I/Q Input Antialias Filter

The device has a programmable antialias filter in the I/Q input path, which is controlled using the I/Q Input Configuration - $B0 write or Signal Control - $61 write registers. This should be sufficient for most applications, however if additional filtering is required it can be done at the input to the device.

The input impedance of the I/Q Input pins varies with the input gain setting, see section 12.1.3 Operating Characteristics.

5.5 GPIO Pins

All GPIO pins are configured as inputs with an internal bus-hold circuit, after the Function Image™ has been loaded. This avoids the need for users to add external termination (pullup/pulldown) resistors onto these inputs. The bus-hold is equivalent to a 75kΩ resistor either pulling up to logic 1 or pulling down to logic 0. As the input is pulled to the opposite logic state by the user, the bus-hold resistor will change, so that it also pulls to the new logic state. The internal bus-hold can be disabled or re-enabled using programming register P1.20 in Program Block 1 – Clock Control.

If the device is reset (either by asserting RESETN pin 7, issuing a C-BUS General RESET or by triggering an internal power on reset) all GPIO pins will be immediately configured as inputs. Any GPIO pins not being pulled either up or down by an external load will be left in a floating state until the Function Image™ is loaded. To avoid GPIO floating input states that may somewhat elevate supply current between a RESET and Function Image™ load, it will be necessary to connect pull up or pull down resistors of 220kΩ to these pins.

6   General Description

6.1   CMX7164 Features

The CMX7164 is intended for use in half-duplex modems. Transmission takes the form of a data burst consisting of preamble, frame sync and data payload, followed by a tail sequence. Reception may utilise the preamble to assist with signal acquisition[1], but is then followed by frame sync detection and data decoding.

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a Xtal clock generator, with phase locked loop and buffered output, to provide a System Clock output, if required, for other devices.

Block diagrams of the device are shown in section 2, Block Diagrams.

Tx Functions:
- Automatic preamble and frame sync insertion simplifies host control
- I/Q analogue outputs (7164FI-4), I/Q or two-point modulation analogue outputs (7164 FI-1 or FI-2)
- Pulse shape filtering
- RAMDAC capability generates PA power ramping control signal
- Tx trigger feature allowing precise control of burst start time
- Tx burst sequence for automatic RAMDAC ramp and Tx hardware switching
- Transmit modulation envelope ramping
- Carrier sense for "listen before talk" operation
- Raw and formatted (channel coded) data modes, with multiple blocks supported in a single burst
- Flexible Tx coded data block size, up to: 416 bytes (7164FI-4), 48 bytes (7164FI-2 4/8/16-FSK), 18 bytes (7164FI-1)

Rx Functions:
- Automatic frame sync detection simplifies host control
- I/Q analogue inputs
- Rx channel filtering and pulse shape filtering
- Channel estimation and equalisation
- Tracking of symbol timing and input I/Q dc offsets
- AGC using SPI Thru-Port
- Raw and formatted (channel coded) data modes, with multiple blocks supported in a single burst
- Flexible Rx coded data block size, up to: 416 bytes (7164FI-4), 48 bytes (7164FI-2 8/16-FSK), 18 bytes (7164FI-1)

Auxiliary Functions:
- Two programmable system clock outputs
- Four auxiliary ADCs with six selectable input paths
- SPI Thru-Port for interfacing to synthesisers, Cartesian loop IC (CMX998), direct conversion receiver (CMX994/A/E), and other external serial interface devices
- In-build calibration routine to support CMX998 Cartesian loop transmitter IC
- Four auxiliary DACs, one with built-in programmable RAMDAC

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[1] The frame sync detection algorithm of the CMX7164 is capable of detecting a frame sync without having bit synchronisation, so preamble is not required for obtaining bit sync. Some preamble is still needed to ensure that the beginning of the frame sync is transmitted and received without distortion. Preamble may also be used to provide a known signal on which to acquire I/Q dc offset corrections.

Interface:

- Optimised C-BUS (4-wire, high speed synchronous serial command/data bus) interface to host for control and data transfer, including streaming C-BUS for efficient data transfer
- Open drain IRQ to host
- Four GPIO pins
- Tx trigger input (Provided by GPIOA)
- Serial memory or C-BUS (host) boot mode

Both transmit and receive data can be raw or coded data blocks. FI-4.x provides a variety of coding rates for flexibility and very large block sizes having the potential to improve performance in fading conditions considerably. FI-2.x provides coding compatible with CMX7143FI-2.x. . FI-1.x provides coding compatible with CMX7143FI-1.x.

6.2   Signal Interfaces (I/Q Tx and Rx)

FI-4.x produces QAM modulation. The transmitted signal is provided as an I/Q baseband, for mixing up onto an RF carrier, with amplification. For reception an I/Q baseband signal should be interfaced into the 7164FI-4.x. 7164FI-2.x produces 2-FSK, 4-FSK, 8-FSK, and 16-FSK modulation and can be configured to produce I/Q modulation, in which case the signal interfaces are the same as for FI-4.x. 7164FI-1.x produces GMSK/GFSK modulation and can also be configured to produce I/Q modulation, in which case the signal interfaces are the same as for FI-4.x.

In receive, the I/Q interface provides amplitude information, so the RSSI signal is calculated internally. It is averaged in order to produce the RSSI measurement and to support the carrier sense decision whether to transmit.
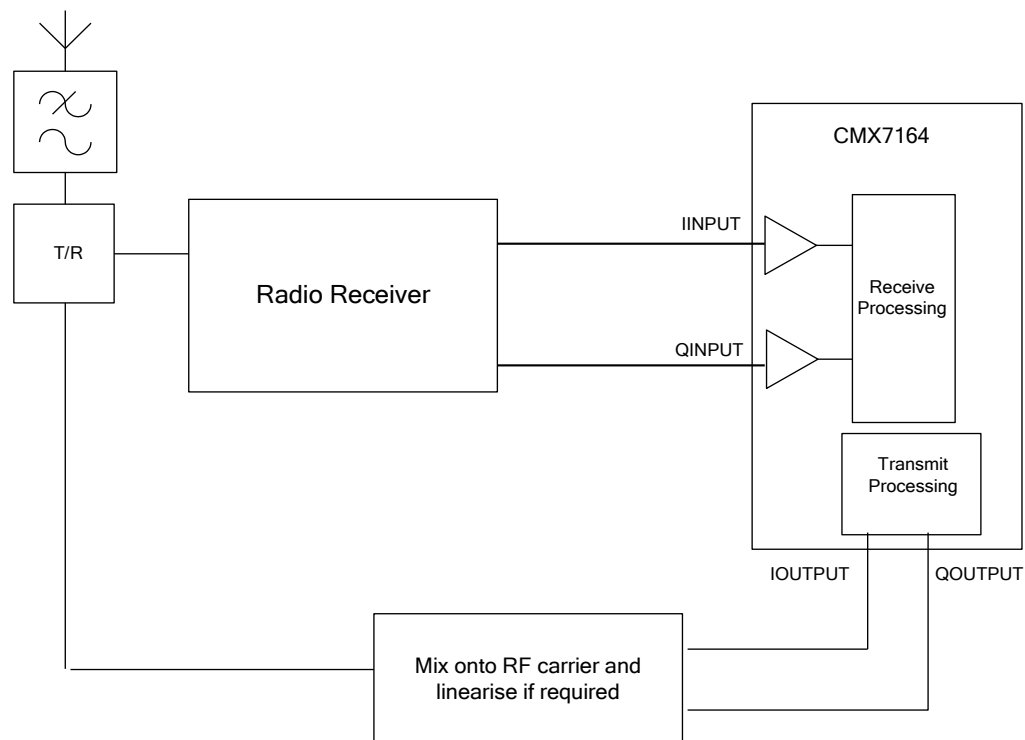
Figure 11   CMX7164 I/Q Tx, I/Q Rx

6.3   Signal Interfaces (Two-point Tx and I/Q Rx)

FI-2.x produces 4-FSK modulation and can be configured to produce two-point modulation. FI-1.x produces GMSK/GFSK modulation and can also be configured to produce two-point modulation. This option is not applicable for FI-4.x. Receive supports only the I/Q interface type.
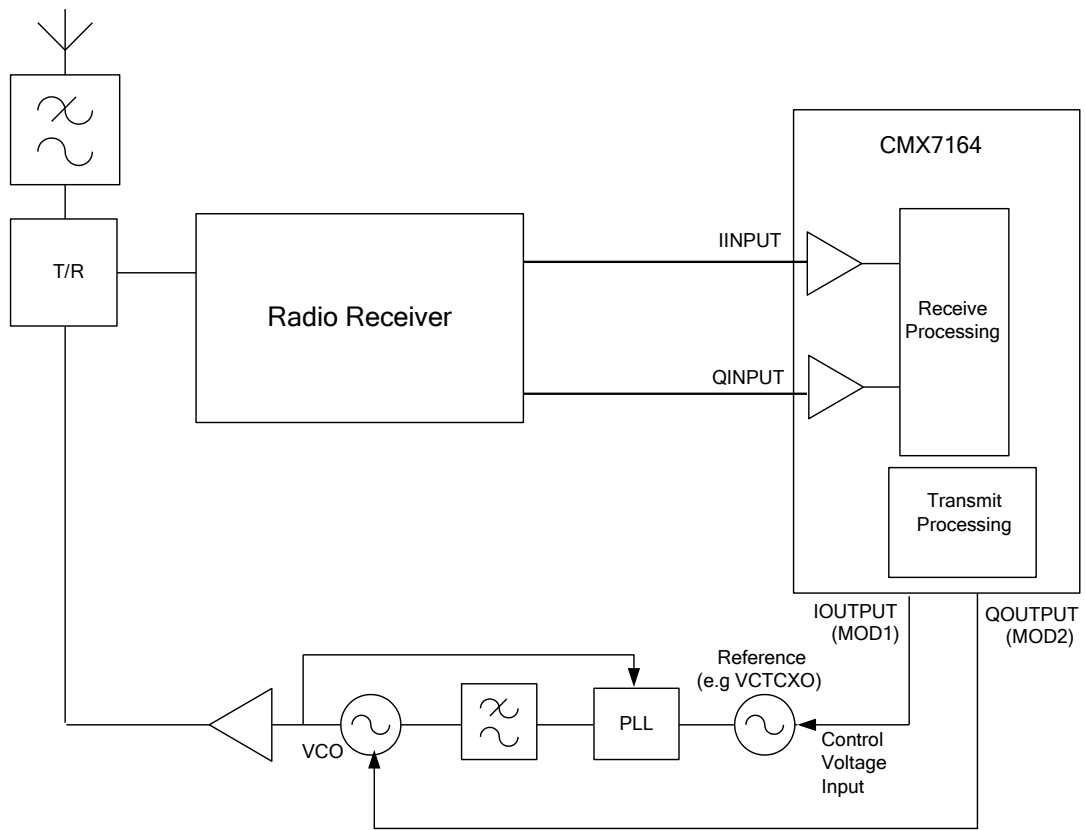
Figure 12 CMX7164 Two-point Tx, I/Q Rx

7   Detailed Descriptions

7.1   Xtal Frequency

The CMX7164 is designed to work with a Xtal, or an external frequency oscillator within the ranges specified in section 12.1.3 Operating Characteristics. Program Block 1 (see User Manual) must be loaded with the correct values to ensure that the device will work to specification with the user selected clock frequency. A table of configuration values can be found in Table 19 supporting baud rates up to 20ksymbols/s when the Xtal frequency is 9.6MHz or the external oscillator frequency is 9.6 or 19.2 MHz. Rates other than those tabulated (within this range) are possible, see section 13.2.3 Program Block 1 – Clock Control. Further information can be provided on request. The modem can operate with a clock or Xtal input frequency tolerance of 50ppm. The receive performance will be compromised as the system tracks, so a maximum tolerance of 20ppm is recommended.

7.2   Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7164 and the host µC; this interface is compatible with Microwire™, SPI™ and other similar interfaces. Interrupt signals notify the host µC when a change in status has occurred; the µC should read the IRQ Status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set, see Interrupt Operation.

7.2.1   C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7164 internal registers and the host µC over the C-BUS serial bus. Single register transactions consist of a single register address byte sent from the µC, which may be followed by a data word sent from the µC to be written into one of the CMX7164's write-only registers, or a data word read out from one of the CMX7164's read-only registers. Streaming C-BUS transactions consist of a single register address byte followed by many data bytes being written to or read from the CMX7164. All C-BUS data words are a multiple of 8 bits wide, the width depending on the source or destination register. Note that certain C-BUS transactions require only an address byte to be sent from the µC, no data transfer being required. The operation of the C-BUS is illustrated in Figure 13.

Data sent from the µC on the CDATA (command data) line is clocked into the CMX7164 on the rising edge of the SCLK input. Data sent from the CMX7164 to the µC on the RDATA (reply data) line is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Section 12.2 C-BUS Timing gives detailed C-BUS timing requirements.

Note that, due to internal timing constraints, there may be a delay of up to 60µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS single byte command (no data)

CSN

SCLK

CDATA

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

MSB   Address   LSB

RDATA   Hi-Z
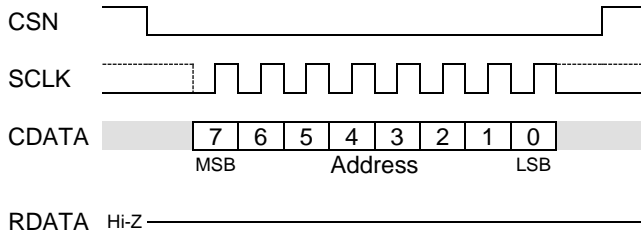
Note:
The SCLK line may be high or
low at the start and end of each
transaction.

C-BUS n-bit register write

CSN

SCLK

CDATA

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

MSB   Address   LSB

| n-1 | n-2 | n-3 | | 2 | 1 | 0 |

MSB   Write data   LSB

RDATA   Hi-Z

C-BUS n-bit register read

CSN

SCLK

CDATA

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

MSB   Address   LSB

RDATA   Hi-Z

| n-1 | n-2 | n-3 | | 2 | 1 | 0 |

MSB   Read data   LSB
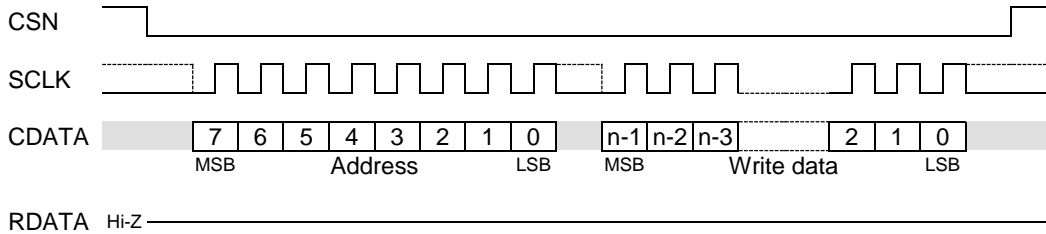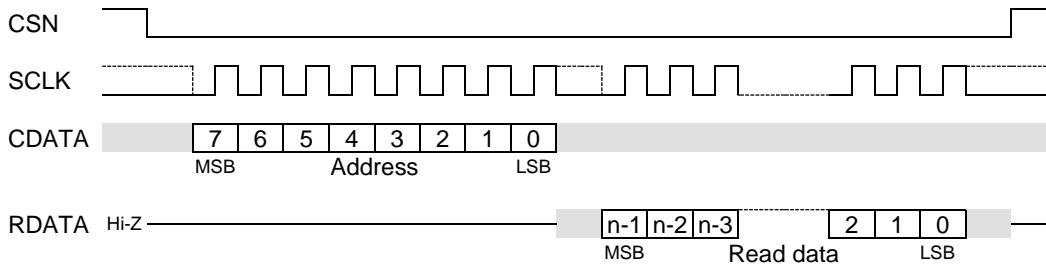
Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 13 Basic C-BUS Transactions

To increase the data bandwidth between the µC and the CMX7164, certain of the C-BUS read and write registers are capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 14.

Example of C-BUS data-streaming (8-bit write register)

Example of C-BUS data-streaming (8-bit read register)

Figure 14 C-BUS Data Streaming Operation

Notes:
1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset)
2. For single byte data transfers only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The address byte determines the data direction for each C-BUS transfer.
4. The SCLK can be high or low at the start and end of each C-BUS transaction
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.3 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration and authorisation. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external serial memory. The Function Image™ size can never exceed 128 kbytes, although a typical FI will be considerably less than this. Note that the BOOTEN1/2 pins are only read at power-on, when the RESETN pin goes high, or following a C-BUS General Reset, and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN1/2 pins are ignored by the CMX7164 until the next power-up or Reset.

The BOOTEN1/2 pins are both fitted with internal low current pull-up devices.

For serial memory load operation, BOOTEN2 should be pulled low by connecting it to DV_{ss} either directly or via a 47k resistor (see Table 1).

Whilst booting, the boot loader will return the checksum of each block loaded in the C-BUS Rx Data FIFO. The checksums can be verified against the values provided with the FI to ensure that the FI has loaded correctly.

Once the FI has been loaded, the CMX7164 performs these actions:

(1) The product identification code ($7164) is reported in the C-BUS Rx Data FIFO
(2) The FI version code is reported in C-BUS Rx Data FIFO.

Table 1 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS host load	1	1
reserved	1	0
Serial Memory load	0	1
reserved	0	0

Note: Once the Function Image™ is loaded then the device can be configured. That may be required before changing device mode or engaging certain device functions. See Section 7.4 Device Control for more details.

7.3.1   FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7164 at power-up over the C-BUS interface, using the Command FIFO. For Function Image™ load, the FIFO accepts raw 16-bit Function Image™ data (using the Modem Command FIFO Word) - $49 write register, there is no need for distinction between control and data fields. The BOOTEN1/2 pins must be set to the C-BUS load configuration, the CMX7164 powered or Reset, and then data can then be sent directly over the C-BUS to the CMX7164.

If the host detects a brownout, the BOOTEN1/2 pins should be set to re-load the FI. A General Reset should then be issued or the RESETN pin used to reset the CMX7164 and the appropriate FI load procedure followed.

Streaming C-BUS may be used to load the Modem Command FIFO Word - $49 write register with the Function Image™, and the IRQ Mask - $6C write register.

Each bit in the Interrupt Mask register corresponds to a bit in the IRQ Status - $7E read register. Setting a bit in the Interrupt Mask register enables the corresponding bit in the IRQ Status register to cause an external interrupt. All external interrupts are disabled if the IRQ bit is cleared.

The Modem Command FIFO Level - $4B read register is used to ensure that the FIFO is not allowed to overflow during the load process.

The download time is limited by the clock frequency of the C-BUS; with a 5MHz SCLK it should take less than 250ms to complete even when loading the largest possible Function Image™.

BOOTEN2 = 1
BOOTEN1 = 1

Power-up or
write General Reset to CMX7164

Read the RxFIFO Level - $4F until 3 device check words appear in RxFIFO Word - $4D. Read and discard them

Block number **N** =1

Write Block 1 Length (DB**N**_len) to CmdFIFO Word - $49

Write Start Block N Address (DB**N**_ptr) to CmdFIFO Word - $49

Check CmdFIFO Level - $4B

Write up to "128-FIFO fill level" words to CmdFIFO Word - $49

End of Block?   No

Yes

Read and verify 32-bit checksum words from RxFIFO Word - $4D

N = **N**+1

Is the next block the Activation Block?

Yes   No - load next block

Write Start Block **N** Length (ACTIVATE_len) to CmdFIFO Word - $49

Write Start Block **N** Address (ACTIVATE_ptr) to CmdFIFO Word - $49

Poll Status -$7E until Reg Done b14 = 1 (PRG Flag is unmasked in Reg Done Select register - $69 by default and indicates when the FI is loaded)

Read the Product ID Code and the FI version code from the RxFIFO Word -$4D

CMX7164 is now ready for use

BOOTEN1 and BOOTEN2 may be changed once it is clear that the CMX7164 has comitted to C-BUS boot - i.e. when a word has been read from the C-BUS command FIFO

V_{DD}

BOOTEN1

BOOTEN2

Figure 15 FI Loading from Host

7.3.2   FI Loading from Serial Memory

The FI must be converted into a format for the serial memory programmer (normally Intel Hex) and loaded into the serial memory either by the host or an external programmer. The serial memory should contain the same data stream as written to the Command FIFO shown in Figure 15. The most significant byte of each 16-bit word should be stored first in serial memory.

The serial memory should be interfaced to the CMX7164 SPI Thru-Port using SSOUT0 as the chip select. The CMX7164 needs to have the BOOTEN pins set to Serial Memory Load, and then on power-on, following the RESETN pin becoming high, or following a C-BUS General Reset, the CMX7164 will automatically load the data from the serial memory without intervention from the host controller.
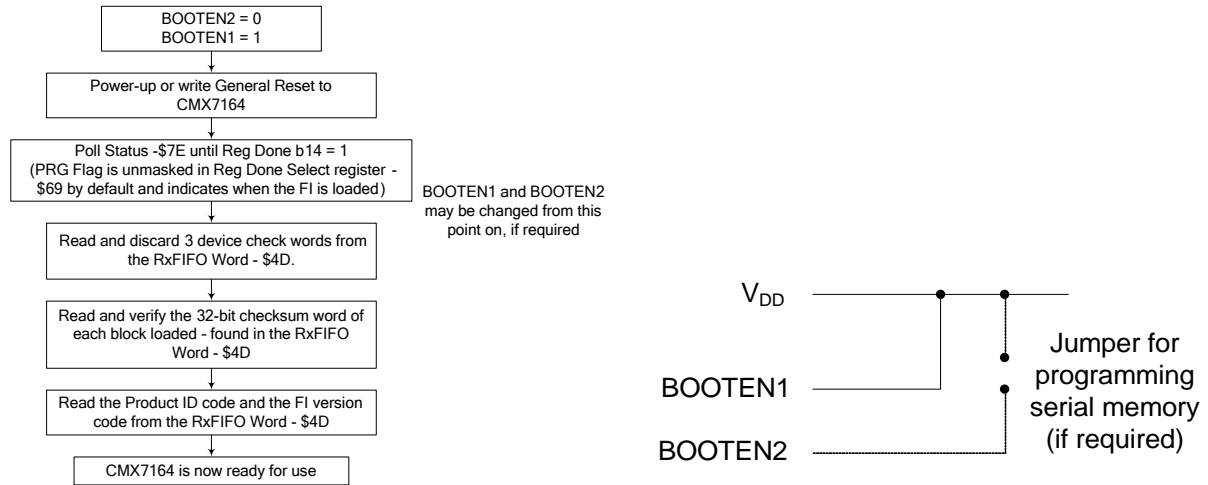
Figure 16 FI Loading from Serial Memory

The CMX7164 has been designed to function with the AT25F1024 serial flash device, however other manufacturers' parts may also be suitable.

7.4   Device Control

Once the Function Image™ is loaded, the CMX7164 can be set into one of four main modes using the Modem Mode and Control - $6B write register:

- Idle mode – for configuration or low power operation
- Transmit mode – for transmission of raw or formatted data
- Receive mode – for detection and reception of bursts containing raw or formatted data
- Carrier sense mode – for attempting to transmit if the channel is free, otherwise continuing to receive.

These four modes are described in the following sections. All control is carried out over the C-BUS interface: either directly to operational registers in transmit, receive and carrier sense modes or, for parameters that are not likely to change during operation, using the Programming Register - $6A write in Idle mode.

To conserve power when the device is not actively processing a signal, place the device into Idle mode. Additional power-saving can be achieved by disabling unused hardware blocks, however, most of the hardware power-saving is automatic. Note that V_{BIAS} must be enabled to allow any of the Input or Output blocks to function. It is only possible to write to the Programming register whilst in Idle mode. See:

- 13.1.18 Programming Register - $6A write
- 13.1.19 Modem Mode and Control - $6B write
- 13.2 Programming Register Operation
- 13.1.24 VBIAS Control - $B7 write.

7.4.1   Normal Operation Overview

In normal operation (after the CMX7164 is configured) the appropriate mode must be selected and data provided in transmit or retrieved in receive. This process is carried out by selecting the mode (Tx, Rx or Carrier Sense), selecting the frame sync to use (Frame Sync 1 or 2) and selecting formatted or raw data. Such a selection is required to initiate transmission or reception of a burst.

In transmit (or following a carrier sense period where no signal is detected on channel) the CMX7164 will begin by switching GPIO signals as configured by the transmit sequence. The RAMDAC can also be configured to ramp up its output signal at this point. Transmission then begins with preamble and the selected frame sync. The main payload of user data comes next, ending with selectable tail bits. The burst ends with the transmission sequence ramping the RAMDAC output signal down and/or switching GPIO signals.

In receive (or following a carrier sense period where signal is detected on channel) the CMX7164 will begin by searching for either or both of the configured frame sync patterns. On detection of a frame sync, reception and delivery of Rx data will begin. Reception continues until the CMX7164 is switched into a different mode, determined by the host.

During the burst, data must be transferred into or out of the CMX7164. Transfers use the Command FIFO to transfer data and commands about data type into the CMX7164, and the Rx FIFO to transfer data out of the CMX7164. The IRQ Status register is used to indicate that the data has been dealt with. The CMX7164 can be configured to interrupt the host when a specified data block has been transferred, or on FIFO fill level.

The CMX7164 offers internal buffering of data in addition to the Command and Rx FIFOs in both receive and transmit directions. The amount of buffering offered is dependant on the mode in which the device is operating. In the process of burst transmission or reception the most significant registers are:

- 13.1.19 Modem Mode and Control - $6B write
- 13.1.38 IRQ Status - $7E read
- 13.1.25 IRQ Mask - $6C write
- 13.1.3 Modem Command FIFO Data/Control - $48, $49 and $4A write
- 13.1.27 Receive FIFO Data/Control - $4C, $4D, $4E read
- 13.1.26 Modem Command FIFO Level - $4B read
- 13.1.28 Receive FIFO Level - $4F read

7.4.2   Basic Tx and Rx Operation

The CMX7164 has many features that provide a great deal of flexibility, but basic data transmission and reception can be carried out fairly easily by understanding the operation of just a few registers. There are other ways of controlling signal transmission and reception but basic examples are given below:

Basic Transmit Operation

Transmission of raw data bytes uses the following procedure:

C-BUS Operation	Action	Description
Write $0080 to FIFO Control - $50 write	Flush the Command FIFO	To ensure that no data is remaining from previous transmissions
Write $18 to the Modem Command FIFO Control Byte (see Modem Command FIFO Data/Control - $48, $49 and $4A write)	Select 8 byte data blocks	Selects blocks of data bytes to be transmitted – 8 bytes in each, after which the CMX7164 will request more data from the host
Write 8 data bytes to the Modem Command FIFO Data Byte - see Modem Command FIFO Data/Control - $48, $49 and $4A write	Pre load the Command FIFO with data to transmit	This provides a buffer of 8 data bytes before transmission starts, so that the host does not need to write data as promptly for the rest of the burst
Write $0042 to Modem Mode and Control - $6B write	Start transmission	Initiates a transmission with preamble, Frame Sync 1 and then the pre loaded data
Poll the IRQ Status - $7E read register for bit 8 – Cmd Done = 1	Wait until the data block has been read from the FIFO	When this is complete a further 8 data bytes may be written to the Modem Command FIFO Data Byte (see Modem Command FIFO Data/Control - $48, $49 and $4A write) and the IRQ Status - $7E read register polled again. This step may be repeated as many times as needed.
Write $F000 to the Modem Command FIFO Word (see Modem Command FIFO Data/Control - $48, $49 and $4A write)	Indicate burst end is intended	Indicate that no more data is to follow – so when the data loaded into the Command FIFO is modulated the CMX7164 will terminate the burst with tail bits
Poll the IRQ Status - $7E read register for bit 9 – Tx Last Tail = 1	Wait until the burst ends	The burst has completed, with all data and tail bits having been modulated. It is now possible to transition to other modes, or transmit another burst using the Modem Mode and Control - $6B write register.

The procedure described above can be adapted, making transmission of different numbers of bytes, bits or coded blocks possible.

Basic Receive Operation

Reception of raw data bytes uses the following procedure:

C-BUS Operation	Action	Description
Write $8000 to FIFO Control - $50 write	Flush the Command FIFO	To ensure that no data is remaining from previous data reception
Write $1400 to the Modem Command FIFO Word (see Modem Command FIFO Data/Control - $48, $49 and $4A write)	Select 4 byte data block reception – repeat forever	Selects blocks of data bytes to be received (after frame sync is detected) – 4 bytes in each, at which point the host will be notified. This will continue until the mode is changed.
Write $0033 to Rx Tracking - $66 write	Select tracking modes	Selects automatic I/Q dc offset correction and symbol timing tracking
Write $0401 to Modem Mode and Control - $6B write	Start reception	Initiates a frame sync search, searching for Frame Sync 1. Once it is detected then Rx data will be made available.
-	Apply input signal	The input signal should contain preamble, Frame Sync 1 and then raw data. The frame sync should be detected and Rx data made available
Poll the IRQ Status - $7E read register for bit 8 – Cmd Done = 1	Wait for data	This indicates that the 4 data bytes requested have been received and are available
Read the Receive FIFO Data Byte (see Receive FIFO Data/Control - $4C, $4D, $4E read) 4 times	Retrieve the received data	Data is read from the Receive Data FIFO. Once 4 data bytes are read the IRQ Status register may be polled again to check if more data is available if required, and then those data bytes read. This step may be repeated as many times as needed
-	End of reception	Once enough data has been received a mode change (using the Modem Mode and Control - $6B write register) will stop reception or start searching for another frame sync.

The procedure described above can be adapted, making reception of different numbers of bytes, bits or coded blocks possible. The registers used for basic transmission and reception are:

- 13.1.19 Modem Mode and Control - $6B write
- 13.1.38 IRQ Status - $7E read
- 13.1.3 Modem Command FIFO Data/Control - $48, $49 and $4A write
- 13.1.27 Receive FIFO Data/Control - $4C, $4D, $4E read
- 13.1.4 FIFO Control - $50 write
- 13.1.16 Rx Tracking - $66 write

7.4.3   Device Configuration (Using the Programming Register)

While in Idle mode the Programming register becomes active. The Programming register provides access to the Program Blocks. Program Blocks allow configuration of the CMX7164 during major mode change. Features that can be configured include:

- Flexible selection of Baud rates, from 2k to 20k baud
- Pre-amble and frame syncs to be using in transmit and receive
- Selection of Automatic control of 4 x GPIO and the RAMDAC during transmission
- Configuration of RAMDAC profile
- Configuration of RSSI averaging
- Configuration of the carrier sense window and thresholds
- Configuration of System Clock outputs
- Configuration of SPI Thru-Port rate and word format
- Configuration of AGC commands using the SPI Thru-Port

Full details of how to configure these aspects of device operation are given in section 13.2 in the User Manual.

7.4.4   Device Configuration (Using dedicated registers)

Some device features may be configured using dedicated registers. This allows for configuration outside of Idle mode. Configuration of the following features is possible:

- Auxiliary ADC detect thresholds
- Auxiliary ADC input selection and averaging mode
- Output gain
- Output dc offsets
- Selection of AGC mode, or manual control of the gain level.

The registers that allow configuration of these features are:

- 13.1.8 I/Q Output Control - $5D, $5E write
- 13.1.9 I/Q Input Control - $5F, $60 write
- 13.1.21 I/Q Input Coarse Gain - $B1, $B2 write
- 13.1.23 I/Q Output Coarse Gain - $B4, $B5 write
- 13.1.22 I/Q Output Configuration - $B3 write
- 13.1.20 I/Q Input Configuration - $B0 write
- 13.1.5 AuxADC1-4 Control - $51 to $54 write
- 13.1.6 AuxADC1-4 Threshold- $55 to $58 write
- 13.1.10 Signal Control - $61 write
- 13.1.15 AGC Control - $65 write

7.4.5   Interrupt Operation

The CMX7164 can produce an interrupt output when various events occur. Examples of such events include detection of a frame sync, an overflow of the internal data buffering in receive, or completion of transmission whilst in transmit.

Each event has an associated IRQ Status register bit and an IRQ Mask register bit. The IRQ Mask register is used to select which status events will trigger an interrupt on the IRQN line. All events can be masked using the IRQ mask bit (bit 15) or individually masked using the IRQ Mask register. Enabling an interrupt by setting a mask bit (0→1) after the corresponding IRQ Status register bit has already been set to 1 will also cause an interrupt on the IRQN line. The IRQ bit (bit 15) of the IRQ Status register reflects the IRQN line state.

All interrupt flag bits in the IRQ Status register are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the IRQ Status register. See:

- 13.1.38 IRQ Status - $7E read
- 13.1.25 IRQ Mask - $6C write

7.4.6   Signal Control

The CMX7164 offers two signal inputs (I Input, Q Input), and two modulator outputs (I Output, Q Output). The analogue gain/attenuation of each input and output can be set individually.

During I/Q modulation transmit, I Output and Q Output will output in-phase and quadrature output signals. They may be independently inverted and their gains changed. During I/Q modulation receive, I Input and Q Input will accept in-phase and quadrature modulated signals. They may be independently inverted and their gains changed.

During two-point modulation transmit the 7164FI-2.x or 7164FI-1.x will output two signals that may be used to drive VCOs in order to create FM modulation. The two signals are provided on the I and Q Outputs, they may be independently inverted and their gains changed.

Note: When transmitting (or receiving) in I/Q mode it may be necessary to swap the I and Q signals. This effect can be achieved by negating either the I or Q signals.
See:
- 13.1.8 I/Q Output Control - $5D, $5E write
- 13.1.9 I/Q Input Control - $5F, $60 write
- 13.1.10 Signal Control - $61 write
- 13.1.23 I/Q Output Coarse Gain - $B4, $B5 write
- 13.1.22 I/Q Output Configuration - $B3 write
- 13.1.20 I/Q Input Configuration - $B0 write

7.4.7   Tx Mode

In typical Tx operation, the preamble and FS1 or FS2 are transmitted automatically, and then data from the Command FIFO is transmitted directly until a TxEnd command is processed, or the mode is changed to Rx or Idle. Data may be written to the Command FIFO prior to starting transmission, enabling the host to create a buffer of data and therefore avoiding risk of the data running out during transmission. Further buffering is provided to expand the amount of data that may be absorbed by the CMX7164.

The host should write the initial data to the Command FIFO and then set modem control to the required transmit type with the Mode bits as Tx. As soon as the data has been read from the C-BUS TxData registers the Cmd Done IRQ and/or Command FIFO IRQ will be asserted (when configured correctly). More data should be loaded into the Command FIFO at this stage before data buffered in the CMX7164 runs out, otherwise an under-run will occur. To end the burst the host should send a TxEnd command, signalling to the CMX7164 that the burst is to end, and the imminent data under-run is intentional.

It is possible to define a transmission sequence with defined RAMDAC ramp up/down, and GPIO on/off events. The transmission sequence is configured using Program Block 5. For precise control of the instant that transmission starts it is possible to trigger a transmission using GPIOA as an input. Selecting a Tx mode with GPIOA configured as an "automatic input" places the device into a "Tx pending" state, where it is neither receiving nor transmitting, just waiting for a trigger on GPIOA to begin transmission.

In general Figure 17 describes operation when a transmit sequence is defined by the host by:

- Removing the need for the host to provide a ramp up – instead the configured Tx sequence will deal with this
- Inserting GPIO on/off events before ramp up and after ramp down as specified by the transmit sequence.

Tx_Process ----------note:--------→ This assumes that:
The transmit control sequence and frame syncs have been configured using the programming register

Load data to Command FIFO

Set Modem Control toTxPreamble, Frame sync and required data mode, Mode = Tx

Here the device is waiting for a GPIO trigger to start the transmission attempt. As no carrier sense is selected it is not receiving and is committed to transmit

Tx triggered on GPIO? --Yes→ Wait for Tx Trigger --note:--

No

GPIO Tx Trigger

Yes

The Modem will transmit the preamble, frame sync and data The host should ensure that any external hardware is also set into Tx mode (if not automatically controlled by the GPIO pins).

----------note:----------

Ensure that RAMDAC speed is fast enough to allow for hardware and internal processing delays ←--note:----

Execute RAMDAC rampup

No

IRQ = CmdDone or Cmd FIFO?

yes

IRQ=Error, Modem status = Underflow may occur at this point, if enabled. --note:--

No← more data to send? --yes→ Load data to Command FIFO

Load TxEnd Command

No

IRQ = TxDone? ----------note:----------→ Due to internal processing delays in the filters etc, the host should wait for IRQ=TxDone or implement its own delay to ensure all data has been transmitted.

Yes

Execute RAMDAC rampdown

Set Modem Control to Idle: Mode = Idle

See Rx_Process flow diagram ←--note:-- Goto Rx_Process

The host should ensure that any external hardware is also set into Idle mode (if not automatically controlled by the GPIO pins).

----------note:----------→

Goto Idle Mode

Figure 17 Host Tx Data Flow (No Tx Sequence/Carrier Sense)

7.4.8 Rx Mode

In Rx mode a frame sync must be detected, then data is supplied to the host through the Rx Data FIFO. Data should be read in response to a "Cmd Done"/"Rx Data FIFO" IRQ or status indication. The CMX7164 will continue decoding the input waveform until the host sets the mode bits to either Tx or Idle, as required. Once initial timing is established, timing corrections can be derived from the data to track the received signal. The Rx Tracking register allows selection of the tracking mode used to track the signal level, I/Q dc offset and symbol timing of the input signal as required. Use of the automatic tracking modes is recommended.
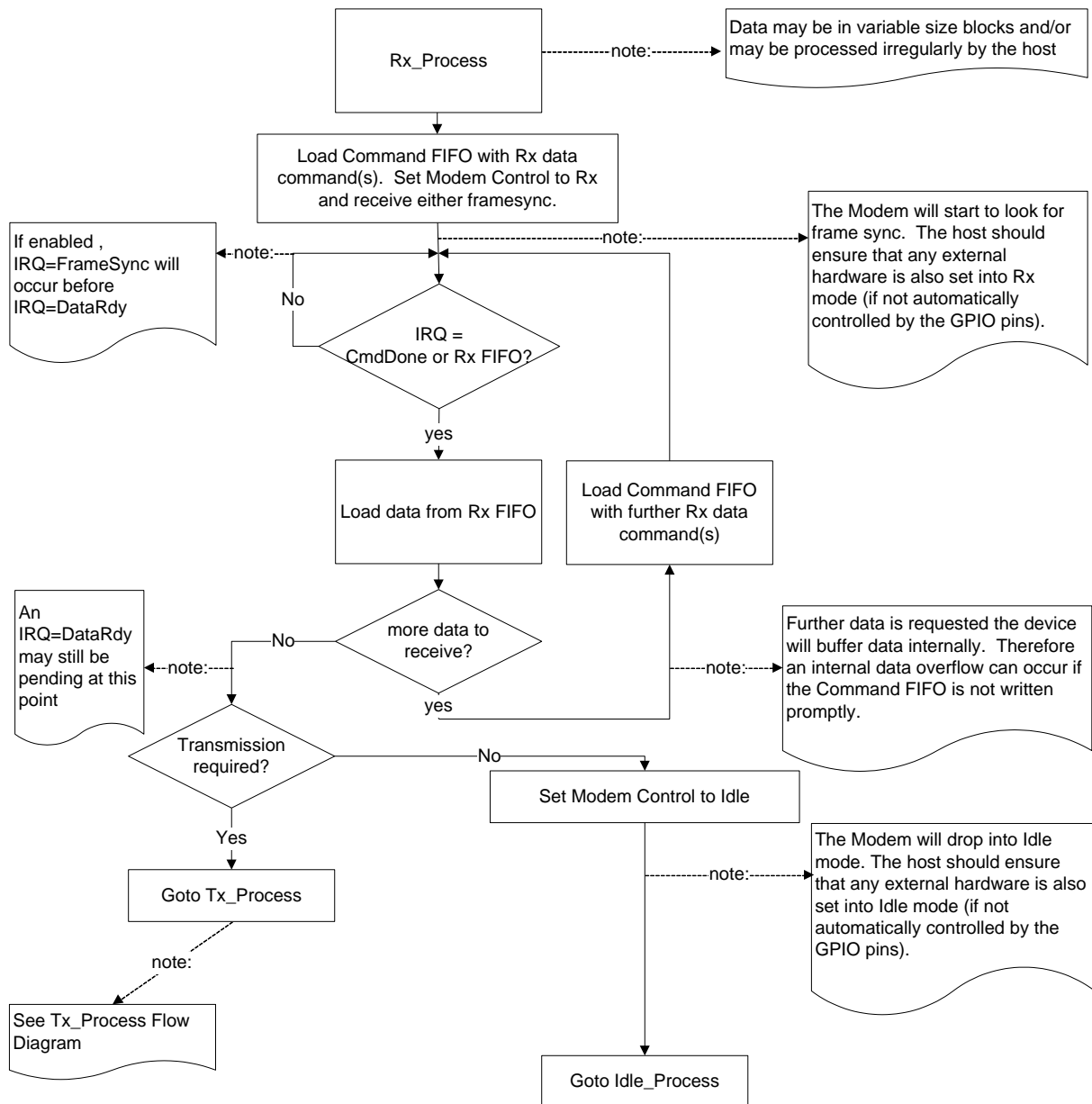
Figure 18 Host Rx Data Flow

7.4.9   Carrier Sense Mode

Carrier sense mode is a receive mode, pending a transmission. A carrier sense period, averaging window length and threshold must be defined in the Program Blocks prior to entering this mode. The signal strength is calculated internally – as the I/Q signal contains amplitude information.

On entry to Carrier Sense mode, reception will begin (or continue if the previous mode was receive) with an attempt to search for a frame sync. During the defined carrier sense period average RSSI will be computed over a moving window. Three outcomes are possible:

1. If during the carrier sense period the average RSSI is above the carrier sense threshold then transmission will be aborted, and search for frame sync will continue. The device reverts to receive.
2. There is a possibility that a valid frame sync will be detected during the carrier sense period. If this is the case, the transmission will be aborted immediately and the device will revert to receive.
3. If the RSSI average remains below the carrier sense threshold then transmission will proceed.

In each of the three possible cases, status bits will be used to indicate the result of the carrier sense period.

If the carrier sense mechanism is used in conjunction with GPIOA as a Tx trigger, operation is as follows: the device is put in receive, searching for a frame sync. If frame sync is found during this period then it is indicated to the host via the status bits and normal reception resumes. No carrier sense happens until GPIOA is used to start the transmit process, at which point carrier sense begins and operation is as described above.

Note: The Command FIFO and Command Buffer will automatically be flushed when a carrier sense attempt to transmit results in the CMX7164 reverting to receive mode. This is to avoid accidentally processing transmit commands pre-loaded by the host as receive commands. This is the only situation in which the FIFOs or buffers will be flushed other than by direct host instruction.
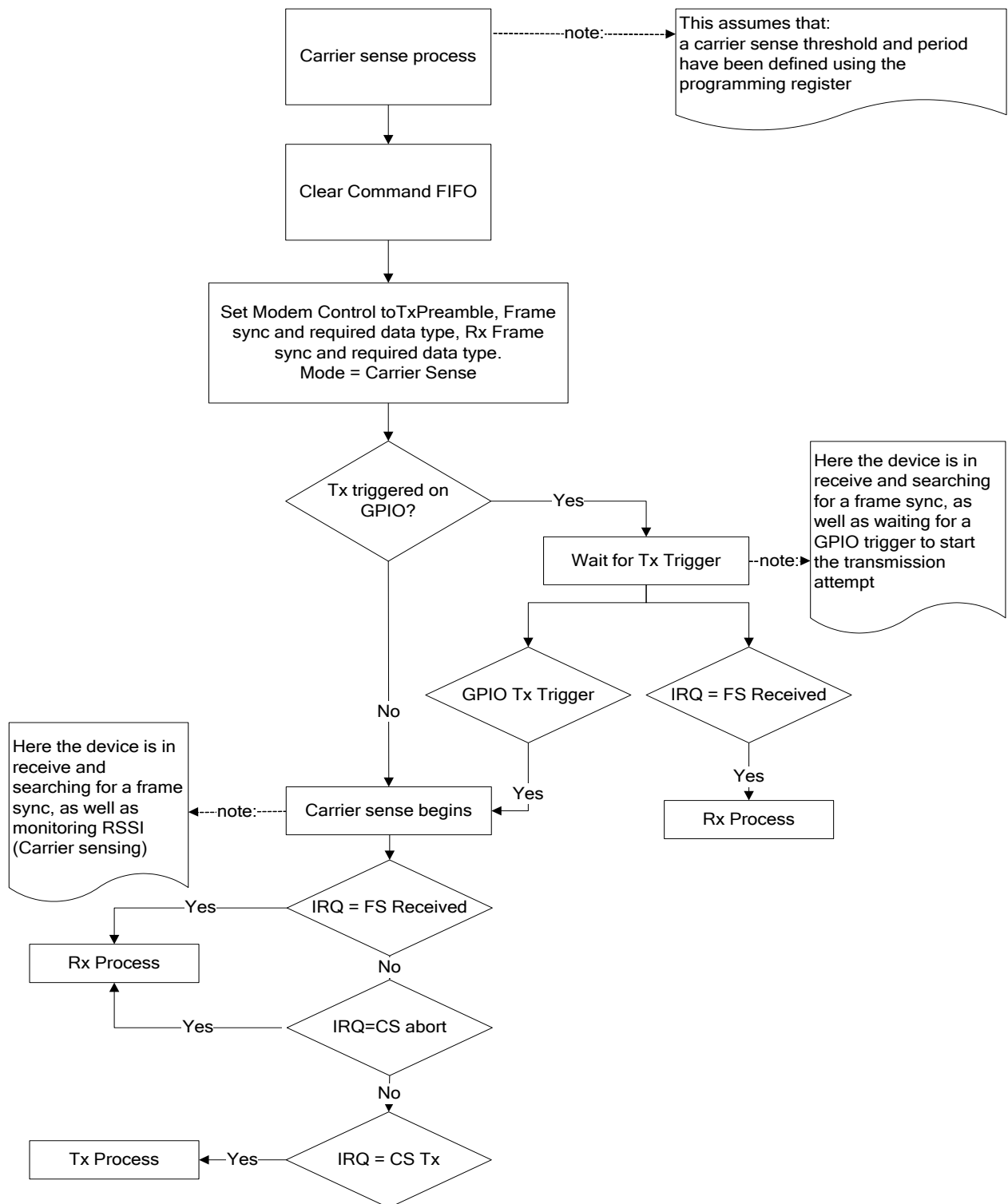
Figure 19 Carrier Sense

7.4.10 The Transmit Sequence

The CMX7164 is capable of being configured to provide the following features:

1. Selecting Tx mode results in transmission starting directly on entry to Tx mode or is delayed until GPIOA is used as an input trigger
2. Selecting carrier sense mode will result in behaviour as in point 1, followed by a carrier sense period, where transmission is delayed (reception continues) until a carrier sense period is completed and no activity is sensed on the channel
3. Selecting Tx calibration will cause CMX998 cartesian loop dc calibration to be carried out prior to transmission, as part of the programmable transmit sequence. See section 7.4.11 CMX998 DC Offset Calibration for details.
4. Once started, transmission can be configured to be a simple modulation output or can include a programmable sequence of events including RAMDAC ramp up/down and GPIO On/Off.

Each of these operations can be selected independently of the others. The following diagram illustrates transmit operation.
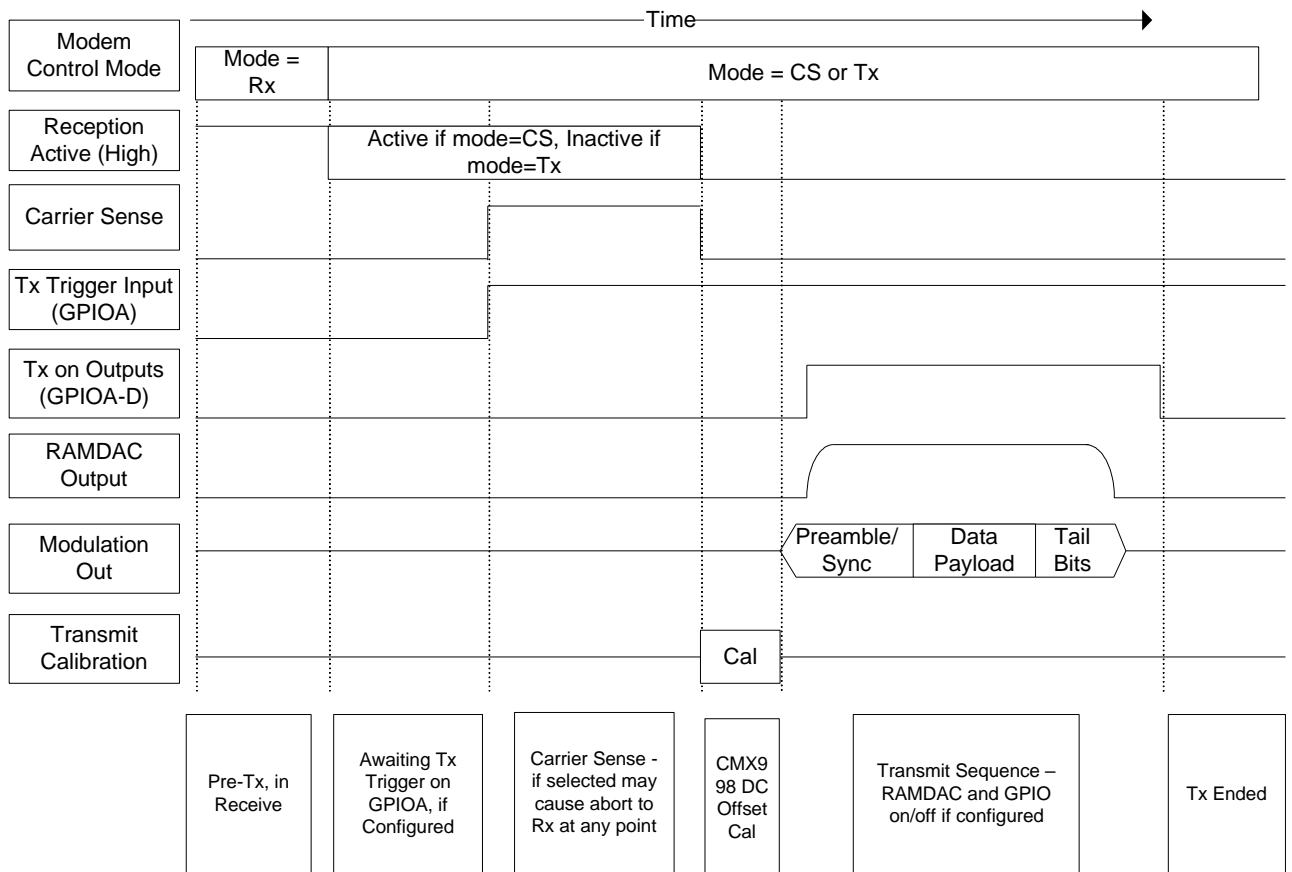
Figure 20 Transmit Sequence

7.4.11 CMX998 DC Offset Calibration (I/Q Transmit Only)
When transmitting in I/Q mode, the CMX7164 may be interfaced to a CMX998 Cartesian Loop IC. The CMX998 is used to provide linearisation of the power amplifier used to transmit the modulation produced

by the CMX7164. If the signal produced by the CMX7164 when no modulation is present does not exactly match the dc reference of the CMX998, carrier leakage will result. This worsens the transmitted signal quality. DC offset calibration is intended to significantly reduce the carrier leakage.

The CMX998 Cartesian Feed-back Loop Transmitter datasheet and an application note "CMX998 Cartesian Feedback Loop DC Calibration" are both available from the CML website (www.cmlmicro.com) and should be referred to for a more in-depth understanding of the need for dc offset calibration.

The CMX7164 performs automatic dc offset calibration as either part of a transmit sequence or in a separate calibration stage. DC offset calibration determines the dc offset that should be applied to the I Output and Q Output signals by the CMX7164 to minimise carrier leakage. The results of calibration will be held by the CMX7164 for use in later transmissions and are made available to the host. The interface is required to be as shown in Figure 21 CMX998 DC Calibration Interfaces.
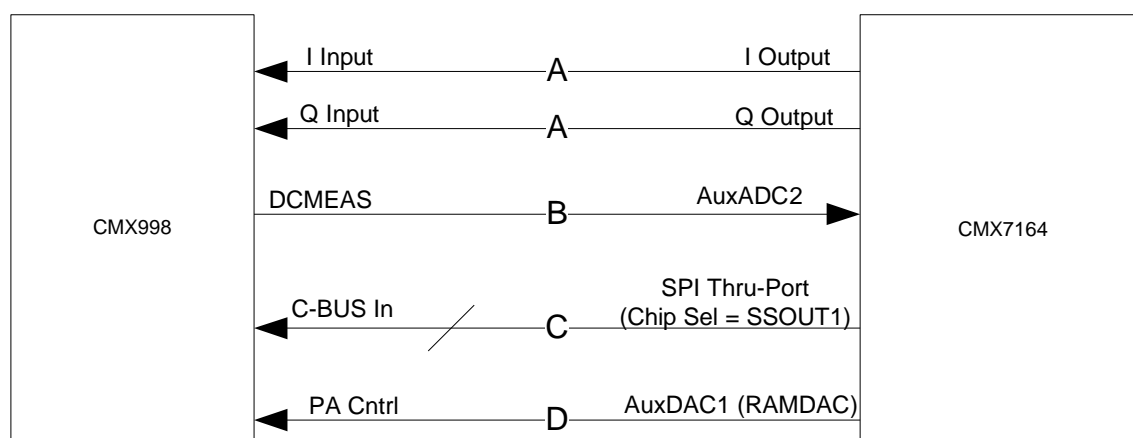
A. The CMX7164 I and Q Outputs are used to provide dc levels, which are adjusted to make the error I/Q measurements equal to the Reference I/Q measurements

B. AuxADC2 is used to sample DCMEAS – To measure Reference signals and error signals

C. The SPI Thru-Port is used to control the CMX998 – selecting Reference I/Q and Error I/Q as measurements, as well as high gain/low gain modes of the CMX998

D. The RAMDAC is typically used to ramp-up the PA Control voltage after calibration is complete. This is not a part of the calibration sequence, but may be active as part of the transmit sequence.

Figure 21 CMX998 DC Calibration Interfaces

During calibration the CMX998 is controlled by the CMX7164 using the SPI Thru-Port chip select SSOUT1 to select one of the following to be output at the CMX998 DCMEAS pin:

I Reference   The CMX998 dc reference for the in-phase signal path
Q Reference   The CMX998 dc reference for the quadrature signal path
I Error (Low/high gain[2]) The CMX998 measure of the dc produced by the input signal on the in-phase signal path
Q Error (Low/high gain)   The CMX998 measure of the dc produced by the input signal on the quadrature signal path.

---

[2] The low and high gain states are created by adjusting the gain of the error amplifiers in the CMX998, see the CMX998 datasheet for more information.

During calibration the CMX7164 uses AuxADC2 to measure Reference I and Reference Q. It then puts (outputs) a dc level on the I Output, Q Output signals. AuxADC2 is used to measure the DCMEAS I and Q Error and I Output, Q Output are adjusted to make the DCMEAS I and Q errors equal to the DCMEAS I Reference and Q Reference measurements.

There are three complications to this process:

1. The total gain of the feedback loop I Output to CMX998 DCMEAS Error signal to AuxADC is unknown – so the adjustment to the I Output signal may not be calculated completely accurately from a single measurement. Therefore the gain applied to the calculated adjustment may be programmed and a number of iterations selected, resulting in a damped feedback loop.
2. The dc error to be corrected is usually large enough that if measured with the CMX998 in high gain mode the DCMEAS output would saturate. This makes calculation of the magnitude of error impossible. Therefore low gain mode should be used initially.
3. When changing from low to high gain modes the circuit changes (see dc calibration Application Note "CMX998 Cartesian Feedback Loop DC Calibration"), therefore the correction needed changes. However the low gain correction should at least be close to bringing the high gain measurement out of saturation. The relationship between correction computed using low gain and high gain is consistent – so may be noted and applied as an offset.

The calibration sequence implemented in the CMX7164 has the following stages:

Setup   Initialise the SSP port, AuxADC and select RefI as DCMEAS output from the CMX998
RefI   Read RefI, select DCMEAS = RefQ
RefQ   Read RefQ, select DCMEAS = ErrorI
ErrorILo   Read ErrorI assuming Low gain and adjust the I Output accordingly
ErrorQLo   Read ErrorQ assuming Low gain and adjust the Q Output accordingly
               Iterate – go to ErrorILo after a delay for corrected signals to settle
HighGain   Select High gain mode of the CMX998, apply Low to High gain mode correction
ErrorQHi   Read ErrorQ assuming High gain and adjust the Q Output accordingly
ErrorIHi   Read ErrorI assuming High gain and adjust the I Output accordingly
               Iterate – go to ErrorQHi after a delay for corrected signals to settle
Tidyup   Restore the CMX998, to its stage pre-calibration – ready to output modulation.

Note: Despite no modulation being produced, the Tx Done flag of the IRQ Status - $7E read register will be set at the completion of the CMX998 DC Offset Calibration task.

The timings of each calibration step can be configured using Program Block 5 – Burst Tx Sequence. To reduce calibration time, a calibration sequence may be configured that omits some stages of the calibration process. However there must always be a Setup and TidyUp stage, and if ErrorQHi and ErrorIHi are included then the high gain stage must be included as well.

The registers used during Tx dc offset calibration are:

- 13.1.19 Modem Mode and Control - $6B write
- 13.2.7 Program Block 5 – Burst Tx Sequence
- 13.1.31 I/Q Offset - $75, $76 read
- 13.1.8 I/Q Output Control - $5D, $5E write

7.4.12 Other Modem Modes

Tx Preamble
In Tx mode, a transmit preamble feature is provided to aid setup – the preamble may be programmed to any useful repeating 8-bit pattern.

Tx PRBS
In Tx mode, a fixed PRBS (pseudo random bit sequence) or a repeated preamble transmission is provided and may be used for test and alignment. A 511 bit PRBS conforming to ITU-T O.153 (Paragraph 2.1) is used to generate the PRBS.

The output created by transmitting a PRBS (using 7164FI-4.x in 16-QAM mode) is shown in Figure 22. The 16 constellation points are just visible on the plot. Likewise the transmitted eye diagram when using 7164FI-2.x in two-point modulation 4-FSK mode is shown in Figure 23, and the transmitted eye diagram when using 7164FI-1.x in two-point modulation GMSK/GFSK mode is shown in Figure 24.
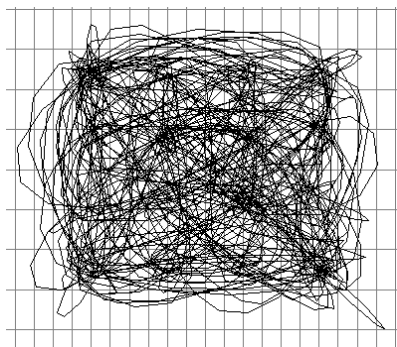
Figure 22 Transmit Constellation (7164FI-4.x)
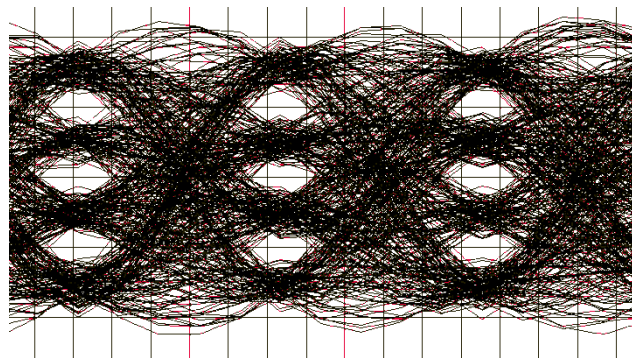
Figure 23 Transmit Eye Diagram (7164FI-2.x)
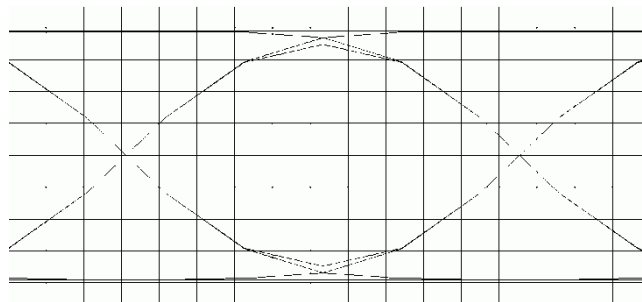
Figure 24 Transmit Eye Diagram (7164FI-1.x)

Rx Constellation (7164 FI-4.x only)
A test mode to examine the Rx constellation diagram is also provided, this utilises the IOUTPUTP/N and QOUTPUTP/N pins to produce a diagnostic signal where the RRC filtered I/Q signals are output. This produces a two-dimensional constellation diagram which may be displayed on an oscilloscope in X-Y mode. Note that best results are often obtained with an analogue oscilloscope.
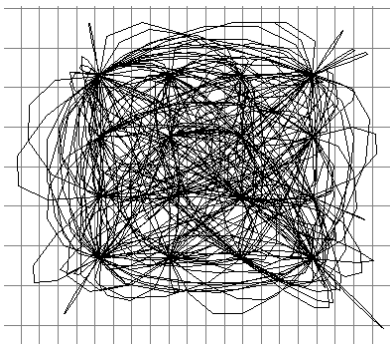
Figure 25 Constellation Diagram – no frequency or phase error
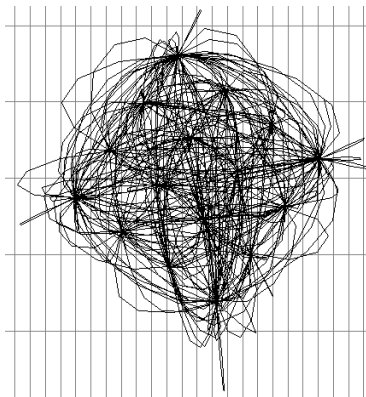
Figure 26 Constellation Diagram – phase error
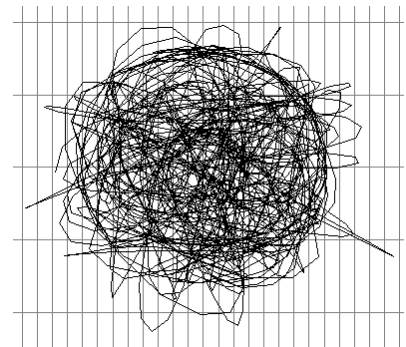
Figure 27 Constellation Diagram – frequency error

As shown in the third plot, if there is any frequency error between transmitting and receiving CMX7164 devices then the diagram will spin and be difficult to interpret. Therefore other diagnostic modes are provided as described below.

Any of the GPIO signals can be configured to produce a pulse train at the nominal symbol rate of the receiving CMX7164 to aid triggering whilst viewing the constellation diagram (I Output or Q Output alone vs time) or other diagnostic modes in receive. In some cases it is advisable to obtain a trigger pulse that is synchronised to the transmitting modem symbol rate, for example if the transmitted signal comes from a signal generator.

Rx Eye (7164FI-1.x and FI-2.x only)

A test mode to examine the Rx eye diagram is provided. This utilises the IOUTPUTP/N pins to produce a diagnostic output signal that may be used to create an eye diagram. The diagnostic signal is produced by channel filtering the I/Q input signals, FM demodulating the result and applying an Rx pulse shaping filter. This produces a one-dimensional eye diagram when displayed on an oscilloscope. One of the CMX7164 GPIO pins may be used as an oscilloscope trigger signal that is locked to the nominal Rx symbol rate, in order to display an eye diagram. For details on how to select the GPIO that produces a nominal symbol rate output clock signal and also the specific diagnostic mode see section 13.1.10 Signal Control - $61 write, Select b15-12=0011. Note that best results are often obtained with an analogue oscilloscope.
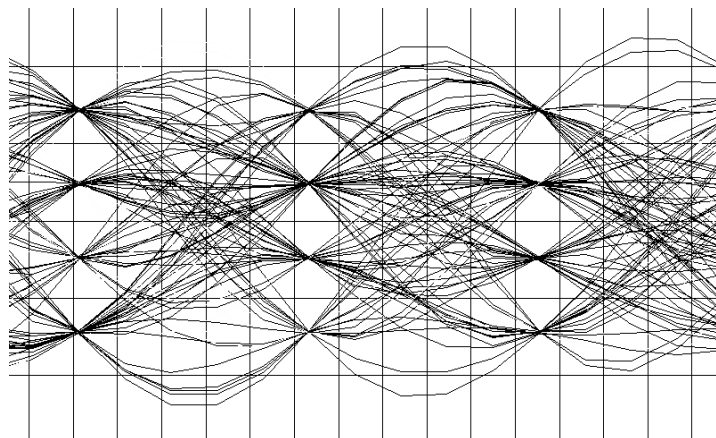
Figure 28 Received Eye Diagram7164 FI-2.x (4-FSK mode)
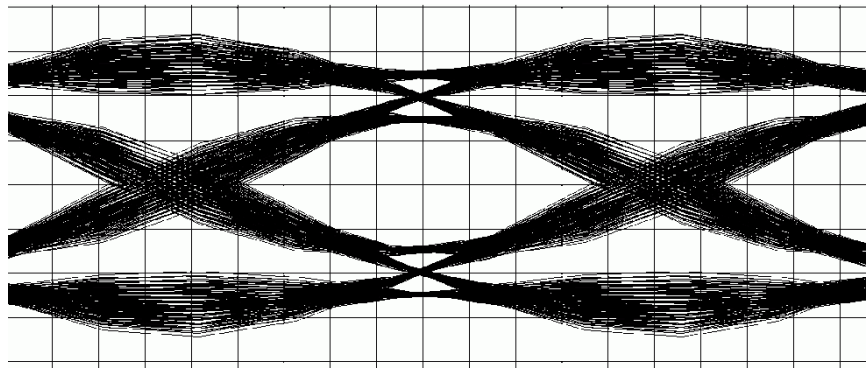
Figure 29 Received Eye Diagram7164 FI-1.x

Rx Diagnostics (7164FI-4.x only)
A diagnostic mode is provided that produces channel filtered I/Q signals and an optional dc offset correction indication. This aids in diagnosing reception issues that may be related to I/Q dc offsets in the CMX7164 input signal. This diagnostic mode can still be of use when there is a frequency error present in the received signal. As shown in Figure 30 and Figure 31, the estimated I/Q dc offset correction is an extra dot in the centre of the constellation.
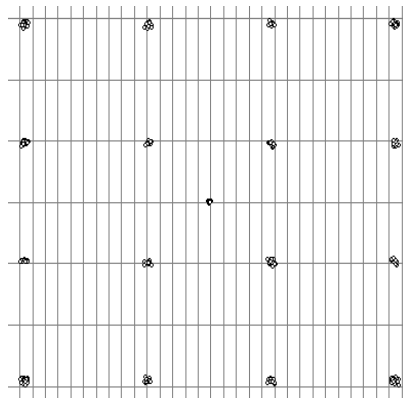
Figure 30 Sample at Symbol Timing with I/Q DC Offset Diagnostic Mode (no frequency error)
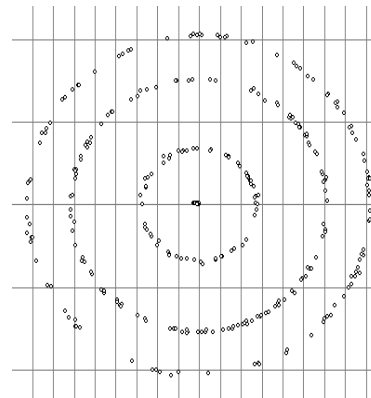
Figure 31 Sample at Symbol Timing with I/Q DC Offset Diagnostic Mode (with frequency error)

A normalised received constellation diagnostic output is provided. It relies on having detected a frame sync and therefore being able to output the signal level measured at the symbol timing instant, with the frequency error removed and amplitude corrected. So long as the CMX7164 remains locked to a suitable signal the normalised constellation output will remain static regardless of frequency error and amplitude of the input signal (within limits – see section 12.1.5 7164FI-2.x Parametric Performance). If the signal becomes noisy or its amplitude small then the constellation points will spread as shown in Figure 32 and Figure 33.
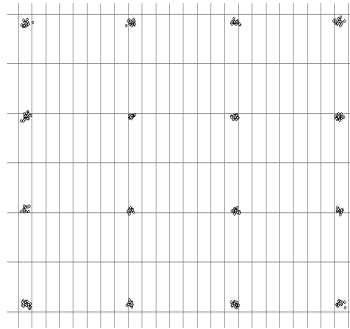
Figure 32 Normalised Constellation (even with a frequency or phase error)
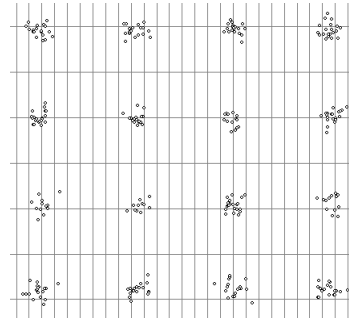
Figure 33 Normalised Constellation (noisy received signal)

Rx Diagnostics (7164 FI-1.x, FI-2.x and FI6.x only)

A diagnostic mode is provided that produces channel filtered I/Q signals and an optional dc offset correction indication. This aids in diagnosing reception issues that may be related to I/Q dc offsets in the CMX7164 input signal. As shown in Figure 34 and Figure 35, the estimated I/Q dc offset correction is an extra dot in the centre of the constellation.
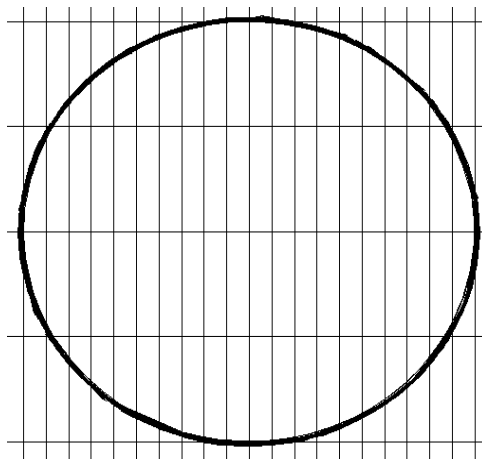
Figure 34 Channel Filtered I/Q Signals
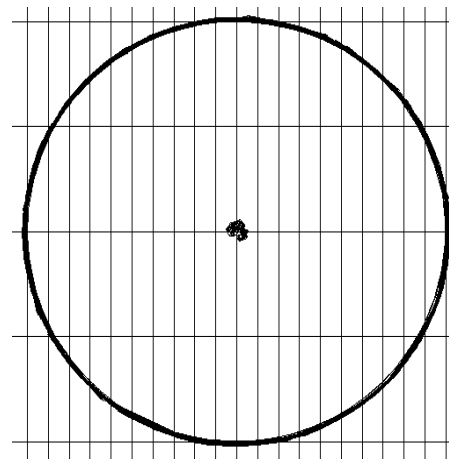
Figure 35 Channel Filtered I/Q Signals with I/Q DC Offset Estimate

Note: The images of receive diagnostic modes shown above are idealised. In practice when using the I Output and Q Output signals to view diagnostics the transitions between constellation point are not instantaneous. Using an analogue oscilloscope is the best way to observe these diagnostic signals.

See:

- 13.1.19 Modem Mode and Control - $6B write
- 13.1.10 Signal Control - $61 write.

First FM Demodulator output (7164FI-6.x only)
A test mode to examine the FM demodulated signal is provided, this utilises the IOUTPUTP/N pins to produce a diagnostic output signal. The diagnostic signal is produced by channel filtering the I/Q input signals, FM demodulating the result and applying a low pass filter. This reproduces the FSK tones.
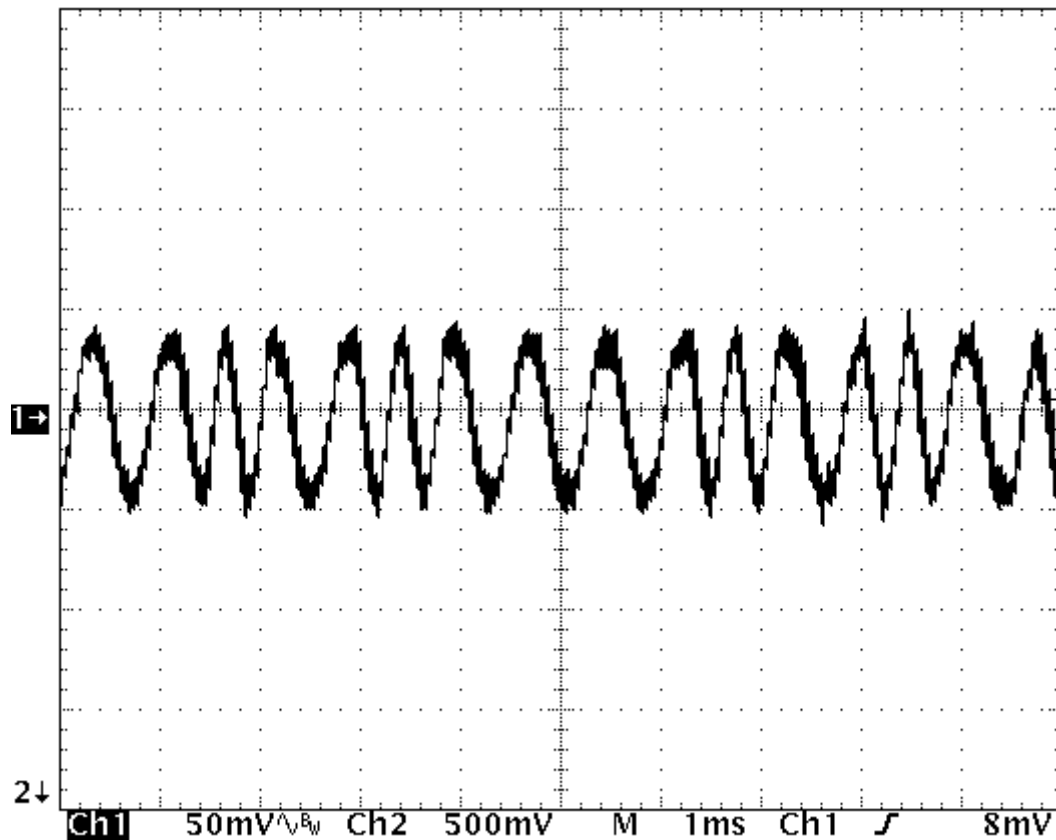
Figure 36 Received Signal (First FM Demodulator) 7164FI-6.x

Rx Eye Diagram (Second FM Demodulator output) (7164FI-6.x only)
A test mode to examine the second FM demodulated signal is provided, this utilises the QOUTPUTP/N pins to produce a diagnostic output signal. The diagnostic signal is produced by FM demodulating the FSK tones from the first FM Demodulator output.
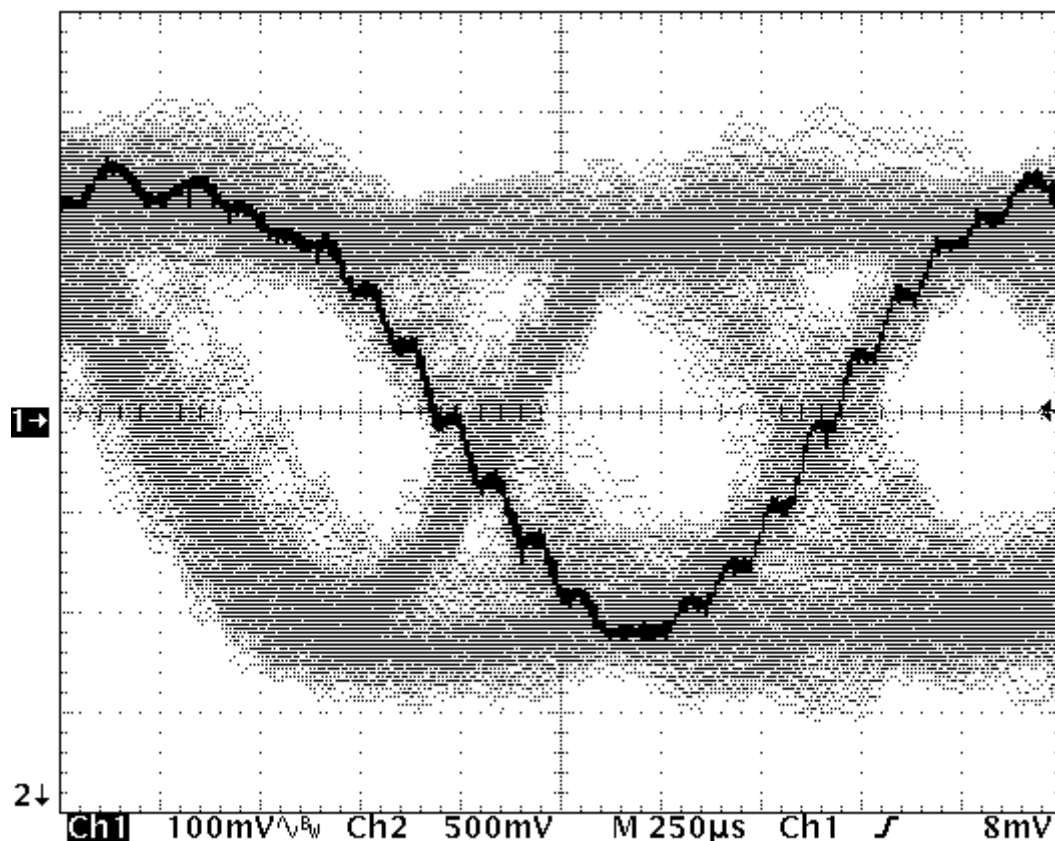
Figure 37 Received Signal (Second FM Demodulator) 7164FI-6.x

7.4.13 Data Transfer

The payload data is transferred to and from the host via the C-BUS Command and Rx Data FIFOs, each of which provide efficient streaming C-BUS access. FIFO fill level can be determined by reading the Receive FIFO Level and Modem Command FIFO Level and controlled using FIFO Control - $50 write register. Interrupts may be provided on FIFO fill thresholds being reached, or successful transfer of a block of host requested FIFO data between CMX7164 modem and FIFOs.

Each FIFO word is 16 bits, with the least significant byte (LSByte) containing data, and the most significant (MSByte) containing control information. The control information indicates to the CMX7164 what type, or how much data is in the LSByte, for example if the byte belongs to a header block or contains only 4 valid bits. The control and data bytes may be written or read together using the Receive FIFO Word and Modem Command FIFO Word registers, or individually using their byte-wide registers.

Word wide FIFO writes involve writing 16-bit words to the Modem Command FIFO Word register using either a single write or streaming C-BUS. The whole word written is put into the Command FIFO, with the upper byte interpreted as control and the lower byte as data. This causes the control byte to be held in the Command FIFO Control Byte register.

Byte wide FIFO writes involve writing to the Modem Command FIFO Data Byte register using either single access or streaming C-BUS. This causes the Modem Command FIFO Control Byte (MSByte) and data written to the Modem Command FIFO Data Byte (LSByte) registers to be put into the command FIFO as one word. The control byte can be written separately as a single byte (this does not result in anything being added to the FIFO) or is preserved from a previous 16-bit Modem Command FIFO Data Byte write.

Likewise a word read from the Rx Data FIFO will return the Receive FIFO Control Byte in the MSByte and the Receive FIFO Data Byte at the top of the FIFO in the LSByte. Both registers will be updated so that when read next time they will provide details of the next item in the FIFO. Reading the Receive FIFO Control Byte only will not change the FIFO content. Reading the Receive FIFO Data Byte only will provide the data and remove the item from the FIFO – updating both control and data registers.
In summary:

Operation	Effect
write Modem Command FIFO Control Byte register	Cmd FIFO control word updated, nothing added to Cmd FIFO
write Modem Command FIFO Data Byte register	Cmd FIFO control word + data byte written are added to Cmd FIFO
write Modem Command FIFO Word register	data word (control and data bytes) is added to Cmd FIFO. Cmd FIFO control word updated for future writes.
read Receive FIFO Control Byte register	Rx FIFO control word is returned, no effect on Rx FIFO contents
read Receive FIFO Data Byte register	Oldest Rx FIFO data byte is removed from FIFO and returned, Rx FIFO Word updated
read Receive FIFO Data Word register	Oldest Rx FIFO data word (control and data bytes) is removed from FIFO and returned, Rx FIFO control word updated.
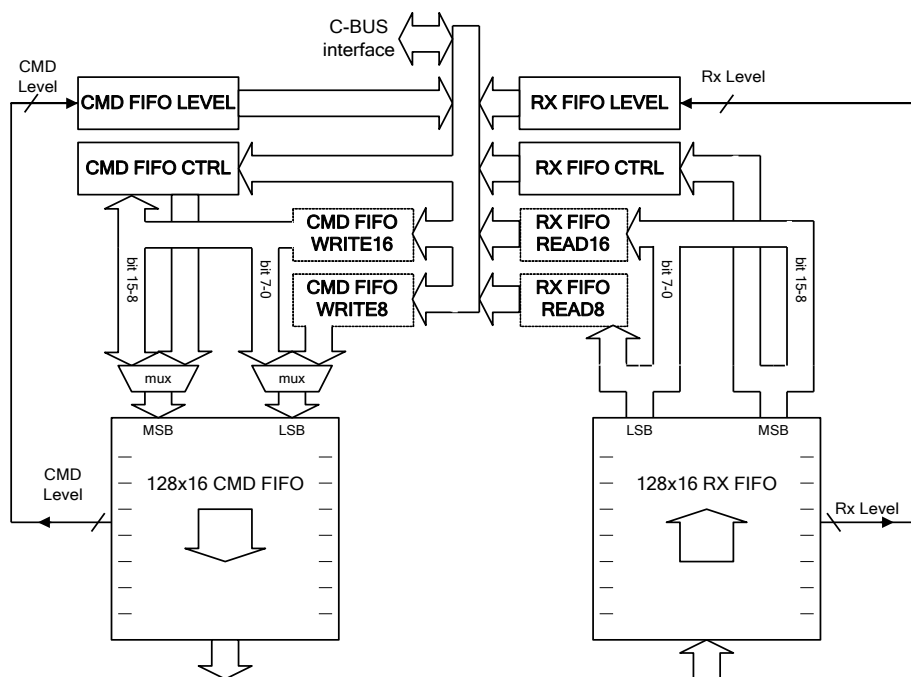
Figure 38 Command and Rx Data FIFOs

Raw or formatted data may be transmitted with the CMX7164 adding preamble, frame sync and tail bits. Raw or formatted transmission/reception is selected using the Modem Mode and Control - $6B write register, each whole transmission/reception must continue in the selected mode. Relevant registers are:

- Modem Mode and Control - $6B write
- Modem Command FIFO Data/Control - $48, $49 and $4A write
- Receive FIFO Data/Control - $4C, $4D, $4E read
- Receive FIFO Level - $4F read
- FIFO Control - $50 write

Note: The Command FIFO and Command Buffer will automatically be flushed when a carrier sense attempt to transmit results in the CMX7164 reverting to receive mode. This is to avoid accidentally processing transmit commands pre-loaded by the host as receive commands. This is the only situation in which the FIFOs or buffers will be flushed other than by direct host instruction.

7.4.14 Data Buffering
To expand the buffering capabilities of the CMX7164 two internal buffers are provided:

A Command buffer which buffers commands from the control FIFO which are yet to be processed.
An Rx data buffer which buffers received data yet to be loaded into the Rx data FIFO.

Transfer between the FIFOs and their respective buffers will occur during transmission, reception and Idle mode. Such transfer is not instantaneous so the FIFO fill levels should be used to indicate how much data the host may read or write at any time.

The Internal Buffer Fill Level - $70 read register allows the buffer fill levels to be read; their contents will be flushed when the respective FIFO is flushed.

See:
- 13.1.4 FIFO Control - $50 write
- 13.1.29 Internal Buffer Fill Level - $70 read.

Note: The Command FIFO and Command Buffer will automatically be flushed when a carrier sense attempt to transmit results in the CMX7164 reverting to receive mode. This is to avoid accidentally processing transmit commands pre-loaded by the host as receive commands. This is the only situation in which the FIFOs or buffers will be flushed other than by direct host instruction.

7.4.15 Raw Data Transfer
When transferring raw data the FIFO Control byte indicates the amount of data that will be transferred in a block before the CMX7164 interrupts the host. Byte and bit-wise transfers are possible, providing the facility to transmit or receive a burst of arbitrary length, not just a whole number of bytes. It is suggested that data is transferred in the maximum size blocks possible until the end of a burst – where the remaining bits, or bytes can be transferred in a single transaction of the required size.

When using byte wise or bit wise transfers the most significant bit of the data byte is transmitted (or received) first. When using bit wise transfers with a bit count of less than 8 the most significant bits are used. In all cases the bits are combined into symbols according to the selected modulation type.

It is also possible to ignore the concept of blocks of data whilst in raw mode. Instead, a transmission can just be treated as a series of bytes to transmit and FIFO levels/level IRQs used to manage the data flow. Likewise in receive the host can request continual data reception and the resulting bytes will be placed in the Rx Data FIFO. FIFO levels and level IRQs may be used to manage the data flow. This mode provides the ability to simply stream (using streaming C-BUS if desired) multiple bytes into or out of the CMX7164 as FIFO content allows.

7.4.16 Formatted Data Transfer
When the transfer of formatted data is selected by the Modem Mode and Control - $6B write register the FIFO Control byte indicates the block type to use in either sending or decoding the data. The block type dictates the format or quantity of data transferred, including how error detection and correction bits are added to the over air data stream.

7.4.17 Pre-loading Commands
It is advisable to pre-load data into the Command FIFO before transmission begins, or to pre-load receive data commands into the Command FIFO prior to frame sync reception.

7.4.18 GPIO Pin Operation
The CMX7164 provides four GPIO pins, each pin can be configured independently as automatic/manual, input/output and rising/falling (with the exception of the combination automatic + input function which is only allowed for GPIOA).

Pins that are automatic outputs become part of a transmit sequence and will automatically switch, along with the RAMDAC – AuxDAC1 (if it is configured as automatic) during the course of a burst. Pins that are manual are under direct user control. When automatic, a rising or a falling event at the start or end of transmission will cause the specified GPIO to be switched high or low accordingly.

GPIOA may be configured as an automatic input. This means that any attempted transmission will wait until GPIOA input is high (if rising is selected) or low (if falling is selected).

See:
- 13.2.7 Program Block 5 – Burst Tx Sequence
- 13.1.14 GPIO Control - $64 write
- 13.1.34 GPIO Input - $79 read.

7.4.19 Auxiliary ADC Operation

The inputs to the four Auxiliary ADCs can be independently routed from any of four dedicated AuxADC input pins or the two main inputs. AuxADCs can be disabled to save power. BIAS in the VBIAS Control - $B7 write register must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC1-4 Control - $51 to $54 write registers. This is a rolling average system such that a proportion of the current data will be added to the last value. The proportion is determined by the value of the average counter in the AuxADC1-4 Control - $51 to $54 write registers. Setting the average counter to zero will disable the averager, for an average value of 1; 50% of the current value will be applied, for a value of 2 = 25%, 3 = 12.5%, continuing up to the maximum useful value of 11 = 0.0488%.

High and low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when an input exceeds the high or low threshold, or on every sample as required. The thresholds are programmed via the AuxADC1-4 Threshold- $55 to $58 write register.

Auxiliary ADC data is read back in the AuxADC1-4 Read - $71 to $74 read registers and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

The AuxADC sample rate is selected using Program Block 1 – Clock Control.

See:
- 13.1.5 AuxADC1-4 Control - $51 to $54 write
- 13.1.6 AuxADC1-4 Threshold- $55 to $58 write
- 13.1.30 AuxADC1-4 Read - $71 to $74 read
- 13.2.3 Program Block 1 – Clock Control
- 13.1.24 VBIAS Control - $B7 write.

7.4.20 Auxiliary DAC/RAMDAC Operation

The four auxiliary DACs are programmed via the AuxDAC1-4 Control - $59 to $5C write registers. AuxDAC1 may also be programmed to operate as a RAMDAC which will autonomously output a pre-programmed profile at a programmed rate. The RAMDAC may be configured as automatic or manual using Program Block 5 – Burst Tx Sequence. The AuxDAC1-4 Control - $59 to $5C write register, with b12 set, controls the RAMDAC mode of operation when configured as a manually triggered RAMDAC. The RAMDAC ramp rate is controlled by the Internal system clock rate, which changes between active CS/Tx/Rx modes and Idle mode. Therefore it is inadvisable to return to Idle mode prior to RAMDAC ramp completion.

The default profile is a Raised Cosine (see Table 17 in the user manual), but this may be over-written with a user defined profile by writing to Program Block 0. The current profile may be scaled using the Signal Control - $61 write register. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero.

See:
- 13.1.7 AuxDAC1-4 Control - $59 to $5C write
- 13.2.2 Program Block 0 – RAMDAC
- 13.2.3 Program Block 1 – Clock Control
- 13.2.7 Program Block 5 – Burst Tx Sequence
- 13.1.10 Signal Control - $61 write.

7.4.21 SPI Thru-Port (SSP)

The CMX7164 provides an SPI Thru-Port synchronous serial port (SSP) master interface that can perform transactions with up to three external slave SPI/C-BUS devices (0, 1 and 2) respectively selected via CMX7164 SSOUT0, SSOUT1 and SSOUT2 chip select output signals. In addition to those chip select signals the interface includes clock out (CLK), data out (MOSI) and receiving data in (MISO) signals shared by all connected slaves.

The Thru-Port supports independent, slave-specific operating characteristics via three configuration parameter sets in Program Block 6 – SPI Thru-Port Configuration. Some of the configurable characteristics are clock speed, inter-frame guard period, clock phase/polarity, and C-BUS/SPI transaction format. The CMX7164 automatically applies each slave's Program Block 6 Thru-Port Configuration characteristics in response to whichever external slave device will be selected by CMX7164 SSOUT0, SSOUT1 or SSOUT2 chip select pins.

7.4.21.1 *SPI Thru-Port (SSP) configuration conflicts*

Note: Once a Thru-Port transaction with an external device has been initiated it must be allowed to complete before Thru-Port Configuration characteristics are changed otherwise the ongoing transaction may be corrupted. Accordingly the CMX7164 host driver must not cause a Thru-Port transaction to be initiated if that would cause a configuration conflict i.e. select a slave having a different Thru-Port Configuration characteristic than that of an ongoing transaction.

SPI Thru-Port transactions may be initiated by the following methods.

1. Host Single Thru-Port Commands – The CMX7164 host writes a C-BUS command to the SPI Thru-Port Control - $62 write register (section 13.1.11) after having optionally written associated data to the SPI Thru-Port Data Write1 - $63 write (section 13.1.12) register. If this initiates a Thru-Port read transaction then when that completes any returned data read is reported in the CMX7164 SPI Thru-Port Data Read - $78 read (section 13.1.33) register, from where the host may read it via C-BUS transaction. This Thru-Port transaction method executes a single Thru-Port transaction with one serial slave. The host driver must pace when it issues Host Single Thru-Port Commands so they do not cause a Thru-Port configuration conflict.

2. SSP Macro Thru-Port Commands – SSP macros each comprising a sequence of one or more SPI Thru-Port write transactions may be configured in Program Block 6 – SPI Thru-Port Configuration (section 13.2.8). An SSP macro may include Thru-Port transactions with multiple slave devices that have different SPI Thru-Port Configuration characteristics, in which case SSP macro execution automatically paces its own Thru-Port Configuration characteristic changes so they do not cause configuration conflicts amongst themselves. Execution of an SSP macro's Thru-Port transactions is initiated by writing to the Modem Mode and Control - $6B write with specific bits set; see section 13.1.19 for details.

3. Autonomous CMX998 Tx DC Calibration – While the CMX7164 modem is in Tx mode the device can optionally perform Tx DC Calibration of an external CMX998 transmitter device connected as the SPI Thru-Port slave selected by SSOUT1. The calibration process and its associated Thru-Port transactions are initiated by writing to the CMX7164 Modem Mode and Control - $6B write register; see section 13.1.19 for details.

4. Autonomous AGC Using SPI Thru-Port – As described in section 7.4.22 SPI/C-BUS AGC, while the CMX7164 modem is in Rx mode the device may autonomously perform Thru-Port transactions under the control of the CMX7164 AGC function in its Auto mode. In addition, while the AGC function is in its Manual mode and the CMX7164 modem is in any of Rx, Tx or Idle modes then a host C-BUS write that manually selects an AGC function gain step will initiate an associated Thru-Port transaction. Individual AGC Thru-Port transactions are configured in Program Block 7 – AGC Configuration (section 13.2.9) and could include multiple external slave devices having different Thru-Port Configuration characteristics. Accordingly, the configured timing of the AGC function and its associated Thru-Port transactions, whether associated with autonomous or manual AGC gain changes, must be arranged not to cause a Thru-Port configuration conflict.

The SSP Macro Thru-Port Commands, Autonomous CMX998 Tx DC Calibration and Autonomous AGC Using SPI Thru-Port methods initiate Thru-Port transactions by a host C-BUS write to the same CMX7164 Modem Mode and Control - $6B write register. The latter two require the CMX7164 modem to be in mutually exclusive modes (Tx and Rx) and so cannot be simultaneously initiated to mutually cause a Thru-Port configuration conflict. However, SSP Macro Thru-Port Commands and either Autonomous CMX998 Tx DC Calibration or Autonomous AGC Using SPI Thru-Port methods can be simultaneously initiated by the same C-BUS write to the Modem Mode and Control - $6B write register, which could cause a configuration conflict. The SSP Macro Wait feature, enabled on the same write to the Modem Mode and Control - $6B write register, avoids such a conflict by causing resulting Thru-Port transactions to sequence with the SSP Macro Thru-Port Commands performed first.

7.4.21.2 *SPI Thru-Port C-BUS and SPI Transaction Modes*

In order to offer a simpler, more convenient interface, a slave device's Thru-Port configuration can be designated C-BUS, rather than SPI. This means that data read/written is assumed to be in the format:

> Address byte, data byte1 (optional), data byte 2 (optional)

In each case the CMX7164, as the master, drives the address and data for a write operation, or drives the address and receives the data for a read operation. Commands can be called 0, 1 or 2 byte reads or writes – with a 0 byte write typically being a reset command. As the word format is known, then for convenience only the desired read data is returned to the host.

SPI mode is more general and makes no assumption about the SPI word format or that its data field length is a whole number of bytes.

See:
- 13.1.11 SPI Thru-Port Control - $62 write
- 13.1.12 SPI Thru-Port Data Write1 - $63 write
- 13.1.33 SPI Thru-Port Data Read - $78 read
- 13.2.8 Program Block 6 – SPI Thru-Port Configuration.

7.4.22 SPI/C-BUS AGC

Using the SPI Thru-Port, the CMX7164 provides an AGC function that can control an external C-BUS or SPI device capable of implementing variable gain steps in the receive signal path. The state of a GPIO output can also optionally be configured to change with AGC function gain state and thereby control additional external hardware. The function's Auto modes act autonomously only while the modem is in Rx mode; when in manual mode the function acts in response to manual gain step selection while the modem is in any of Rx, Tx and Idle modes.

During receive the AGC function can provide fast response gain reduction to large signals that cause clipping and gain increase when the signal becomes too small. Controlling the external device requires the host to program a table of eight SPI/C-BUS commands that the CMX7164 stores and outputs when a specific gain step is required. In conjunction with each gain step that is output, a second external device can also be enabled using one of the four available GPIO pins. This feature is intended for use with RF systems using an external LNA or other stages prior to a SPI/C-BUS controlled device. The commands may be produced by the AGC function, or the CMX7164 can be commanded to output them manually if required. Commands are programmed using Program Block 7 – AGC Configuration.

By default the AGC function range is 8 gain selection steps, 0 to 7 with 0 being the lowest gain and 7 being the highest. If a range of fewer steps is desired then Program Block 7 – AGC Configuration can be used to set the lowest gain step that the AGC is allowed to select. For example, if the lowest allowed gain step is set to 4 the AGC will select AGC function gain steps 4 to 7 only.

AGC function state is controlled by sensing over-range in the CMX7164 received input signal – in which case the external gain is backed off. While searching for a frame sync the gain will also be backed off when the signal is considered "large" – this ensures that after frame sync is detected there is headroom for the amplitude to increase a little. If the signal is sensed to be small for a period of time the gain can also be increased. The signal magnitude low or high threshold considered to require a gain change, the time for which it should remain low before making a change and the time to allow a gain adjustment to take effect are all programmable. The overall system is shown in Figure 39.
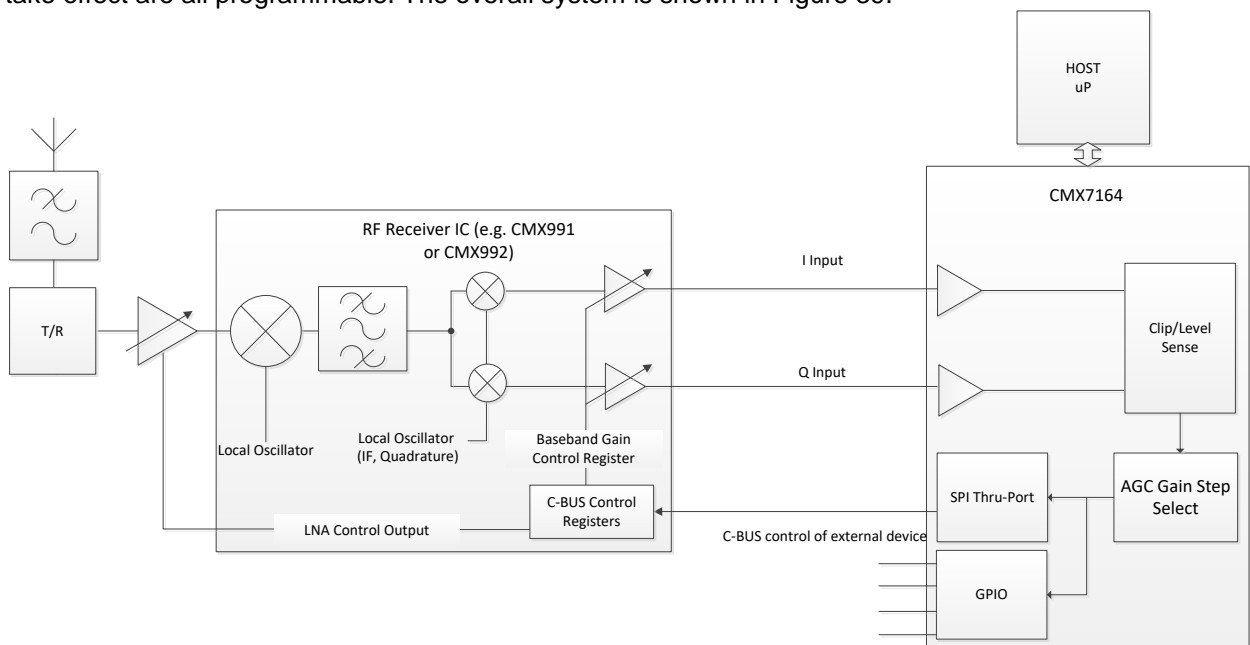
Figure 39 AGC using SPI Thru-Port
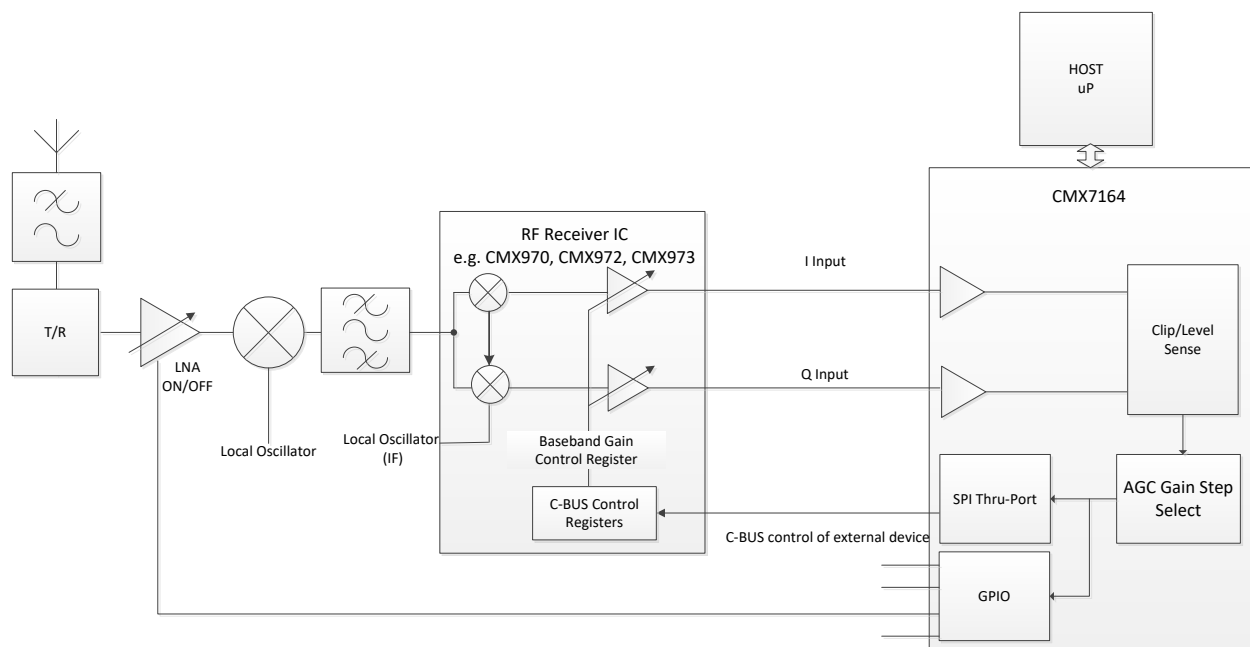
Figure 40 AGC using SPI Thru-Port and external LNA

Note: The external LNA control feature of the CMX7164 may be useful where an RF device does not provide an LNA control output like that available in the CMX991 or CMX992. An example of where CMX7164 control would be necessary is a receiver using the CMX994/A/E but not using the IC's internal LNA; in order to achieve the maximum operating dynamic range of a direct conversion receiver, like the CMX994/A/E, the signal level to mixers must be controlled in order to minimise the chance of local oscillator pulling hence the need for LNA control.

Controlling the external device as shown in Figure 39 causes the gain to step suddenly. This in itself may cause a short burst of errors, so once signal is being received it may be desirable to ensure that the gain is not changed unnecessarily. This is typically the case with short bursts of data, where it is likely that the signal amplitude will remain constant throughout the burst. To help achieve this, various AGC automatic modes are provided:

- Manual Gain – Controlled manually always, allowing user control and for control during latching in of I/Q dc corrections
- Full Auto – Gain can increase and decrease during the search for frame sync and during burst reception
- AGC lock on FS – Gain can increase and decrease during the search for frame sync but once a frame sync is detected its level will be fixed
- AGC down after FS – Gain can increase and decrease during the search for frame sync but once a frame sync is detected its level will only decrease.

AGC gain changes made during the frame sync section of the input signal introduce a signal amplitude distortion that can cause CMX7164 frame sync detection to fail. To avoid this the CMX7164 compares the incoming on-channel signal to a Signal Detect Threshold that when first exceeded is interpreted to indicate the start of an arriving burst i.e. the burst's preamble field. This event, the amplitude of the CMX7164 input signal before and after AGC gain changes and whether a frame sync is detected within a certain time causes the AGC function to change states according to configured AGC level and timing settings. State changes include reducing gain by one step, increasing it by one step, not changing gain for a certain time (e.g. immediately after a gain change or when the frame sync field is expected to arrive),

and returning to the original starting state (e.g. if after the detect threshold was first exceeded no frame sync was detected within the maximum expected time). Some AGC behaviour is illustrated in Figure 41.
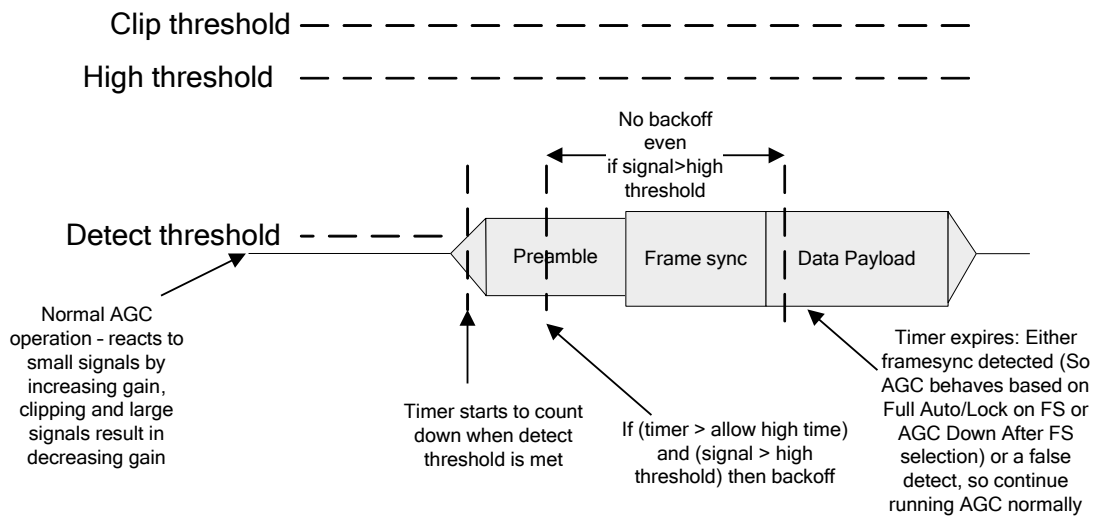
Figure 41 AGC Behaviour During Burst Reception

A general issue with I/Q receivers is that of dc offsets. Offsets are generated by the receiver hardware and typically vary with channel selection, but depending on receiver architecture can also change with gain. The CMX7164 is capable of calculating I/Q dc offset corrections but, if the gain steps suddenly and therefore the dc offset changes suddenly, errors may occur. Once again this may only be an issue for longer bursts when it is necessary to change gain during reception.

To overcome the dc offset issue, the CMX7164 allows an I/Q dc offset correction to be latched-in for each AGC gain step. When a gain step other than maximum gain is selected the tabulated dc offset correction will become active and tracking will be suspended. Additionally, in receivers with large dc offsets present, a gain change may result in a sufficiently large step in dc offset that the signal will look small/large to the AGC algorithm resulting in unwanted gain changes

AGC thresholds and parameters are controlled using the Signal Control - $61 write register and may be changed during reception for ease of setup. All times are measured in units of 6/5 of a symbol period. All levels or thresholds are compared to the magnitude of signed 16 bit samples, with max range therefore being 32767 to -32768.

AGC Observe (FI-1, FI-2 and FI-4 only)
The CMX7164 AGC function described above has several states. The current state is not externally observable during normal operation. It is determined by AGC function configuration in combination with the CMX7164 input signal history. Different states allow or prevent AGC function actions to change gain. To help users properly configure the AGC function, an AGC Observe function is provided and makes AGC function state and behaviour externally observable. AGC Observe indicates current AGC function state as a code value in an Aux ADC C-BUS register or a code voltage on an Aux DAC output pin. (While AGC Observe is enabled, the Aux DAC or Aux ADC C-BUS register selected for its use is not available for normal Aux DAC or ADC operation thus AGC Observe is intended to be used as a configuration design tool, not enabled during regular modem operation.) AGC Observe is activated and its Aux DAC or ADC output mode selected using Program Block 4 – Modulation Control. The table below lists AGC function states and their AGC Observe codes.

	AGC Function State	Preamble detected	Frame sync detected	AGC Observe Code (value written to selected Aux ADC C-BUS register or instead to Aux DAC, which sets its output voltage)	Input Signal Case That Causes AGC Action		
					ADC clipping	Above high threshold	Below low threshold
1.	Waiting for burst - active, with AGC function timers reset			$000	x	x	x
2.	Rx burst start detected	x		$100	x	x	x
3.	Preamble detected, no high threshold action thereafter option	x		$200	x		x
4.	Frame sync detected, no AGC action thereafter option	x	x	$300			
5.	Frame sync detected, only AGC gain reduction action thereafter option	x	x	$380	x	x	
6.	Frame sync detected, any AGC action thereafter option	x	x	No update	x	x	x

Note: There is a short delay between when a signal is applied to the CMX7164 input pins and when it is sensed by the AGC. There is a longer delay (caused by the CMX7164 channel filter) before the frame sync is detected by the preamble and frame sync detectors.
See:
- 13.2.8 Program Block 6 – SPI Thru-Port Configuration
- 13.2.9 Program Block 7 – AGC Configuration
- 13.2.6 Program Block 4 – Modulation Control
- 13.1.15 AGC Control - $65 write
- 13.1.10 Signal Control - $61 write
- 14.3.1 Effect of AGC on DC Offsets

7.5   Digital System Clock Generators
The CMX7164 includes a two-pin Xtal Oscillator circuit. This can either be configured as an oscillator, as shown in section 4, or the XTAL/CLK input can be driven by an externally generated clock. The crystal (Xtal) source frequency is typically 9.6MHz and if an external oscillator is used, the input frequency is typically 9.6 or 19.2 MHz. For both cases reference frequencies in the range specified in 12.1.2 Operating Limits may be used.

7.5.1   Main Clock Operation
A digital PLL is used to create the main clock for the internal sections of the CMX7164. The configuration of the main clock and the internal clocks derived from it is controlled using Program Block 1 – Clock Control.

The CMX7164 defaults to settings appropriate for a 19.2MHz externally generated clock with a baud rate of 9.6ksymbols/s, however if a different reference frequency is to be used, or a different baud rate required, then Program Block entries P1.1 to P1.6 will need to be programmed appropriately at power-on. A table of preferred values is provided in Table 19 along with details of how to calculate settings for other baud rates and crystal frequencies.
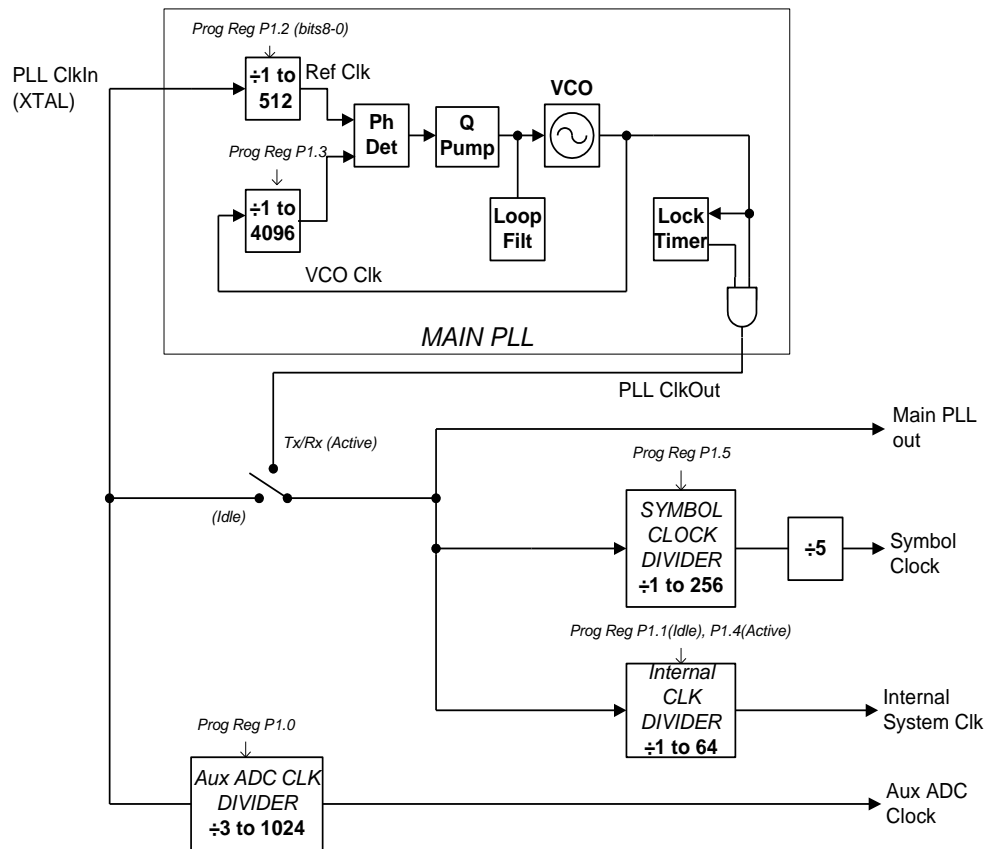
Figure 42 Main Clock Generation

See:
- 13.2.3 Program Block 1 – Clock Control.

7.5.2   System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. The System Clock circuitry is shown in Figure 43 Digital System Clock Generation Schemes.

Having chosen the input frequency source, system clock generation may be by simply dividing the input frequency source, or via its own phase locked loop. The system clock PLL does not affect any other internal operation of the CMX7164 – so if a frequency that is not a simple fraction of the Xtal is required, it can be used with no side effects. There is one phase locked loop, with independent output dividers to provide phase locked output signals.
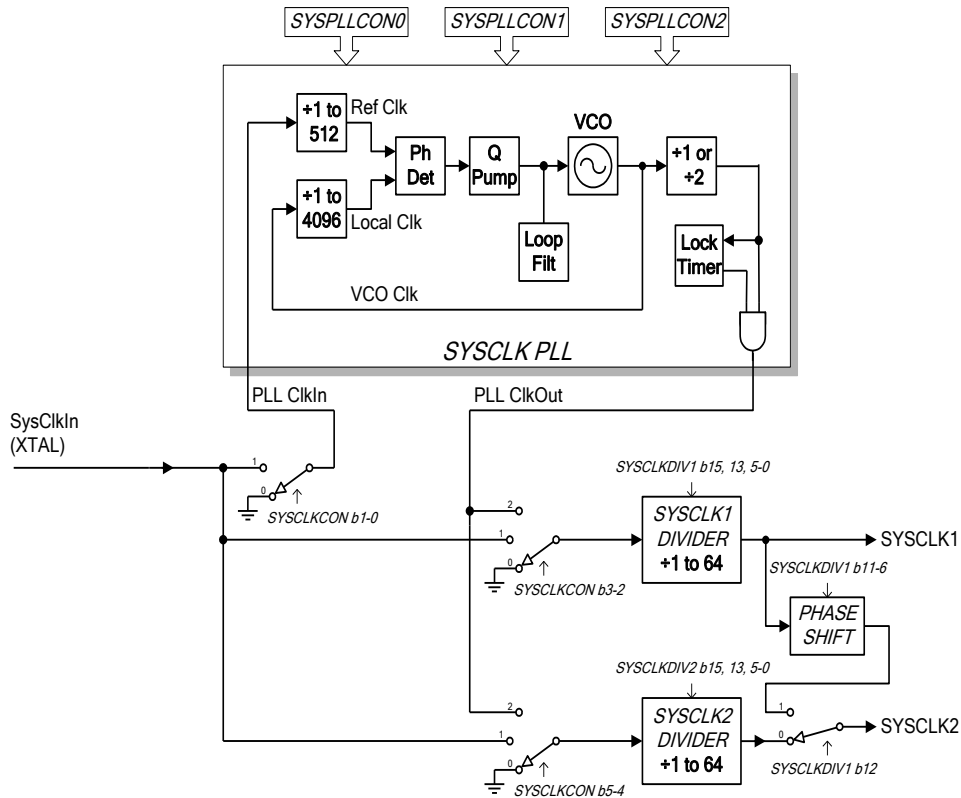
Figure 43 Digital System Clock Generation Schemes

See:
- 13.2.3 Program Block 1 – Clock Control.

7.6   Signal Level Optimisation

The internal signal processing of the CMX7164 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V supply, the signal range which can be accommodated without distortion is specified in 12.1.3 Operating Characteristics. Signal gain and dc offset can be manipulated as follows:

7.6.1   Transmit Path Levels and Modulation Envelope Ramping

For the maximum signal out of the I/Q Outputs, the signal level at the output of the modem block is set to be 0dB, the Fine Output adjustment has a maximum attenuation of 6dB and no gain, whereas the Coarse Output adjustment has a variable attenuation of up to 14.2dB and 6dB gain.

The signals output from I Output and Q Output may be independently inverted. Inversion is achieved by selecting a negative value for the (linear) Fine Output adjustment. When transmitting I/Q format signals inverting one of the I/Q pair has a similar effect to swapping I with Q.

DC offsets may be added to the signal, however care must be taken that the combination of gain and dc offset does not cause the signal to clip at any point in the signal processing chain, which is: Fine gain followed by dc offset addition, followed by coarse gain.

The transmit I/Q output signal represents instantaneous modulation signal power, which determines the modulation envelope. For a given transmit burst, how quickly the I/Q signal envelope rises at burst start and declines at burst end can influence the resulting modulation signal spectrum; if the I/Q envelope makes a rapid step change the bandwidth associated with that transient step may be wider than desired.

The inherent nature of FI-4.x QAM modulation makes its modulation envelope ramp, not step, its transmit I/Q signal modulation envelope up at the start and down at the end of each a transmission. This has the effect of reducing each FI-4.x transmit burst's modulation on/off transients, especially when using the CMX998 Cartesian Feedback Loop IC.

The FSK modulations produced by FI-1.x, FI-2.x and FI-6.x are constant envelope so, by default, at burst start and end their transmit I/Q signal modulation envelope respectively steps from 0% to 100% and from 100% to 0%, without any inherent ramping effect. When using FI-1.x, FI-2.x or FI-6.x the modulation envelope can be optionally ramped up and down at beginning and end of a transmission. To select and configure this option see:

- 13.1.8 I/Q Output Control - $5D, $5E write
- 13.1.23 I/Q Output Coarse Gain - $B4, $B5 write
- 13.2.6 Program Block 4 – Modulation Control

7.6.2   Receive Path Levels

The Coarse Input has a variable gain of up to +22.4dB and no attenuation. With the lowest gain setting (0dB), the maximum allowable input signal level at the I Input or Q Input pins is specified in section 12.1.3 Operating Characteristics.

A Fine Input level adjustment is provided, although the CMX7164 should operate correctly with the default level selected. The primary purpose of the Fine Input level adjustment is to allow independent inversion of the I/Q Input signals. Inversion is achieved by selecting a negative value for the (linear) Fine Input gain adjustment. When receiving I/Q format signals, inverting one of the I/Q pair has a similar effect to swapping I with Q.

DC offsets can be removed by the CMX7164, the offset to remove can be selected by the host or calculated automatically by the CMX7164.

It should be noted that if the maximum allowable signal input level is exceeded, signal distortion will occur regardless of the internal dc offset removal or attenuation.

See:

- 13.1.9 I/Q Input Control - $5F, $60 write
- 13.1.20 I/Q Input Configuration - $B0 write

7.7 C-BUS Register Summary

Table 2 C-BUS Registers

ADDR. (hex)	Read/ Write	REGISTER	Word Size (bits)
$01	W	C-BUS General Reset	0
$48	W	Modem Command FIFO Data Byte	8
$49	W	Modem Command FIFO Word	16
$4A	W	Modem Command FIFO Control Byte	8
$4B	R	Modem Command FIFO Level	8
$4C	R	Receive FIFO Data Byte	8
$4D	R	Receive FIFO Word	16
$4E	R	Receive FIFO Control Byte	8
$4F	R	Receive FIFO Level	8
$50	W	FIFO Control	16
$51 to $54	W	AuxADC1-4 Control	16
$55 to $58	W	AuxADC1-4 Threshold	16
$59 to $5C	W	AuxDAC1-4 Control	16
$71 to $74	R	AuxADC1-4 Read	16
$5D	W	I Output Control	16
$5E	W	Q Output Control	16
$5F	W	I Input Control	16
$60	W	Q Input Control	16
$61	W	Signal Control	16
$65	W	AGC Control	16
$66	W	Rx Tracking	16
$69	W	Reg Done Select	16
$70	R	Internal Buffer Fill Level	16
$75	R	I Offset	16
$76	R	Q Offset	16
$77	R	AGC Gain and RSSI	16
$7A	R	Rx Error Magnitude	16
$7B	R	Frequency Error	16
$62	W	SPI Thru-Port Control	16
$63	W	SPI Thru-Port Write	16
$64	W	GPIO Control	16
$78	R	SPI Thru-Port Read	16
$79	R	GPIO Input	16
$6A	W	Programming	16
$6B	W	Modem Mode and Control	16
$6C	W	IRQ Mask	16
$7D	R	Programming Register Read	16
$7E	R	IRQ Status	16
$7F	R	Modem Mode and Control Readback	16
$B0	W	I/Q Input Configuration	16
$B1	W	I Input Coarse Gain	16
$B2	W	Q Input Coarse Gain	16
$B3	W	I/Q Output Configuration	16
$B4	W	I Output Coarse Gain	16
$B5	W	Q Output Coarse Gain	16
$B7	W	V_{BIAS} Control	16

All other C-BUS addresses are reserved and must not be accessed.

8   7164FI-1.x Features

The 7164FI-1.x uses a GMSK/GFSK modulation scheme with a configurable over-air bit rate up to 20kbps. The modulating signal is Gaussian filtered with a filter BT selectable from 0.5, 0.3, 0.27 or 0.25. Raw data can be transferred, in addition to formatted data blocks. Formatted data blocks may be of variable length (up to 18 bytes) and support 16-bit CRC for error detection, plus hamming coding for error correction. The modulation scheme and coding are designed to produce a signal that is over-air compatible with the CML FX/MX909B and CMX7143 (7143FI-1.x) modems.

8.1   7164FI-1.x Modulation

The GMSK/GFSK modulation running at 8kbps with BT of 0.3 (or less) can be accommodated within a 12.5kHz channel bandwidth, A rate of 9.6kbps with BT=0.5 is typical in 25kHz bandwidth channels while meeting the transmit and receive requirements of international standards such as EN 300 113. Channel bandwidth is dependent on the deviation that the modulating signal causes the carrier to deviate by as well as the data rate and the BT. As a result, the user can choose to configure the device to suitable settings for a particular application.

8.2   7164FI-1.x Radio Interface

The transmit radio interface of the 7164FI-1.x can be set to two-point modulation or I/Q. When the 7164FI-1.x is in two-point modulation mode the I Output is used as 'Mod 1', and the Q Output is used as 'Mod 2'. The receive signal must come from an I/Q radio receiver.

8.2.1   I/Q Transmit and I/Q Receive Interfaces

The 7164FI-1.x can produce an I/Q modulated signal, taking a baseband modulating signal and using it to frequency modulate an I/Q baseband signal, with a user-programmable deviation.

In receive the 7164FI-1.x will accept an I/Q input signal and provide significant channel filtering digitally. It will then frequency demodulate the resulting signal, which is treated as a limiter discriminator output signal would be internally. An overview of how the CMX7164 might use the CMX992[3] for reception and the CMX998[4] for transmission is shown in Figure 44. The internal functions of the CMX7164 when operating in this mode are shown in Figure 3.

Note that the transmit and receive interfaces are identical to those used for QAM modulation in Figure 83, facilitating multi-mode modem operation.   However no linearisation is required when transmitting GMSK/GFSK.

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[3] CMX992 is an RF Quadrature/IF Receiver

[4] CMX998 is a Cartesian Feedback Loop Transmitter which is designed primarily for non-constant envelope modulations such as QAM although it will also support GMSK/. Conventional I/Q vector modulators such as the CMX993 would be more typical of solutions for GMSK/ modulation.
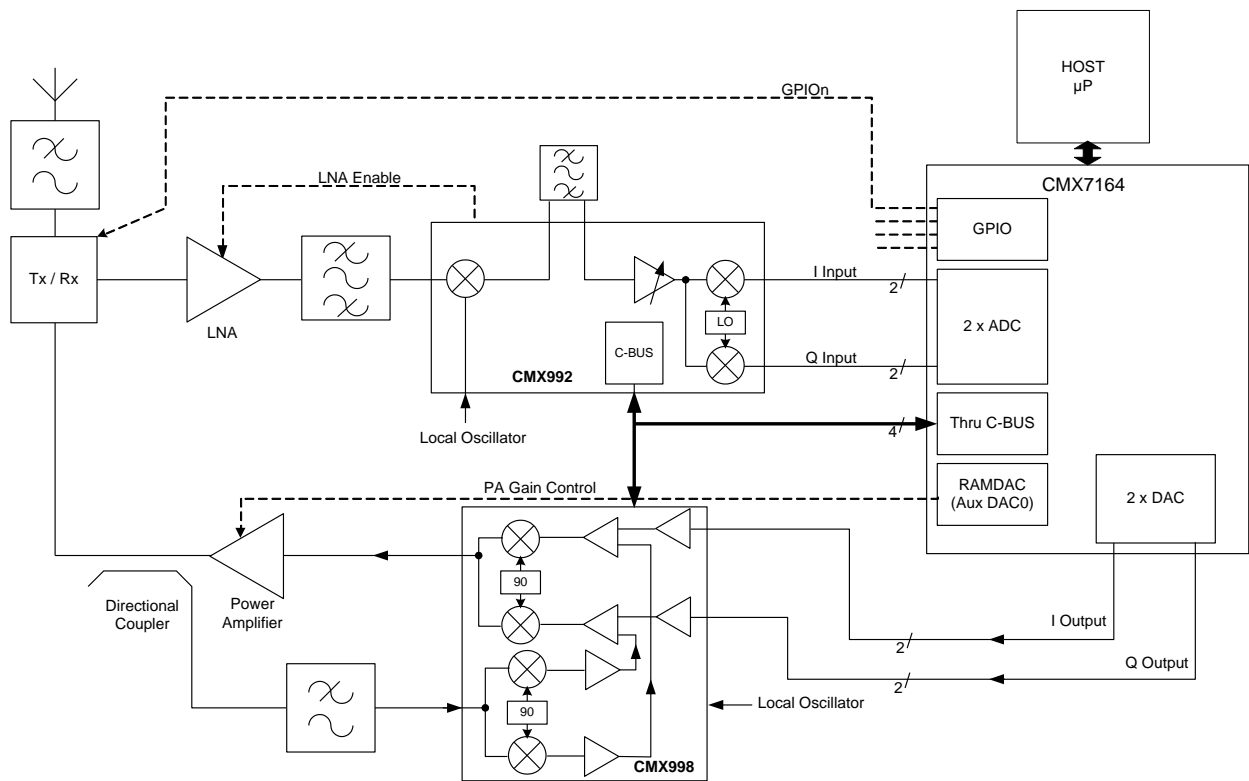
Figure 44 Outline Radio Design (I/Q in/out for GMSK/GFSK)

Use of I/Q receive mode introduces the problem of I/Q dc offsets. There are dc offsets caused by the radio receiver – resulting in the signal into the CMX7164 having a dc offset other than BIAS. The offset needs to be removed prior to demodulation. Offsets typically remain constant for a particular radio frequency selected, but will vary if that frequency is changed. Gain within the radio receiver may also affect the dc offset seen by the CMX7164.

I/Q dc offset effects are a radio issue which is beyond the control of the CMX7164. However the CMX7164 does provide dc offset calculation and removal. These are described in detail in the application note (Section 14.3 DC Offsets in I/Q Receivers).

8.2.2 Two-point Modulation Transmit with I/Q Receive Interface

An overview of how the CMX7164 might integrate with an I/Q receiver, and two-point modulation transmitter is shown in Figure 45. The internal functions of the CMX7164 when operating in this mode are shown in Figure 4.
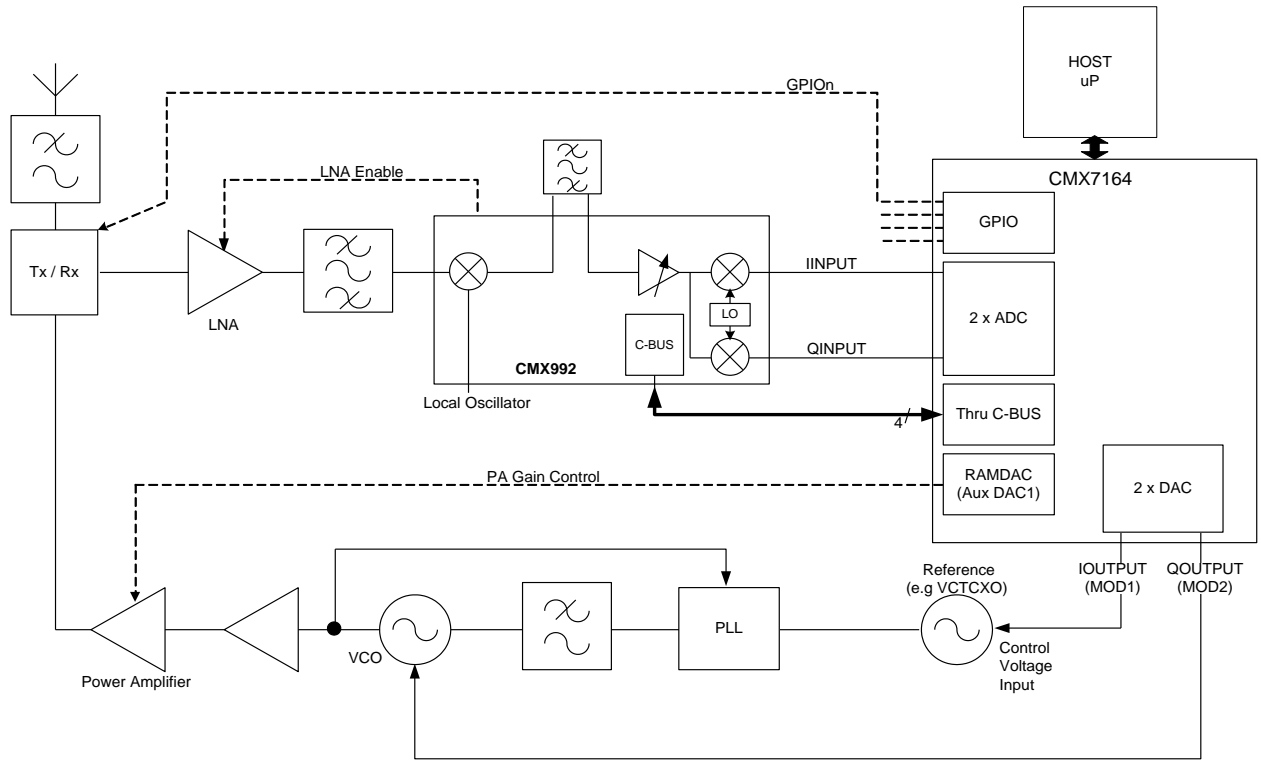
Figure 45 Outline Radio Design (GMSK/GFSK – I/Q in, two-point mod out)

8.3   7164FI-1.x Formatted Data

The 7164FI-1.x supports formatted data, which provides the ability to channel code blocks of data using hamming coding and CRCs. The frame structure as used in a formatted data system is illustrated in Figure 46. Typically it comprises a frame head consisting of a 16-bit sync word, followed by a 16-symbol frame sync pattern, control and data bytes, and then one or more data blocks.
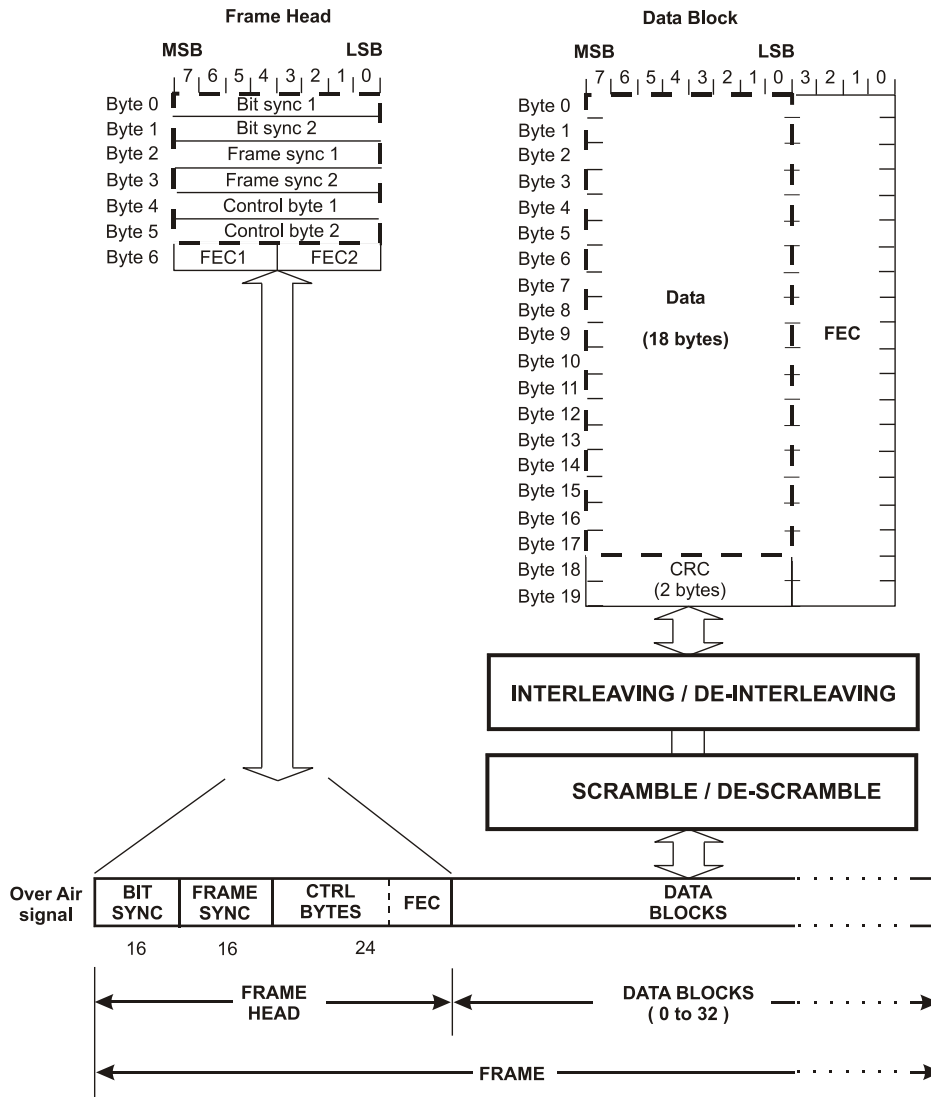
Figure 46 Formatted Data Over Air Signal Format

The 'Frame head' may be used to contain addressing and control flag information.

The 'Data' block(s) contain user data, and an optional checksum.

The CMX7164 performs all of the block formatting and de-formatting, the binary data transferred between the modem and its µC being that enclosed by the thick dashed rectangles near the top of Figure 46. When receiving data blocks with CRCs the CMX7164 will indicate CRC success or failure and will provide the data regardless.

In Figure 46 the size of data block illustrated is 20 bytes when user bytes and CRC bytes are counted together. The CMX7164 adds further flexibility by supporting block sizes of 4, 6, 12 or 18 user bytes, with an optional 2-byte CRC. The resulting data content is:

Table 3 Formatted Block Types and Sizes (FI-1.x)

Block type	User bytes	CRC bytes	FEC bytes	Total bytes
Frame Head (With bit/frame sync)	2	0	1	3
Frame Head (User data/CRC only)	6	0	1	7
4 byte data block without CRC	4	0	2	6
6 byte data block without CRC	6	0	3	9
12 byte data block without CRC	12	0	6	18
18 byte data block without CRC	18	0	9	27
4 byte data block with CRC	4	2	3	9
6 byte data block with CRC	6	2	4	12
12 byte data block with CRC	12	2	7	21
18 byte data block with CRC	18	2	10	30

8.4   7164FI-1.x Typical Transmit Performance

Using the test system shown in Figure 47 the 7164FI-1.x internal PRBS generator was used to modulate the RF vector signal generator. Some typical results are shown in the following figures. The desired deviation was achieved by adjusting the CMX7164 peak deviation using register $61.
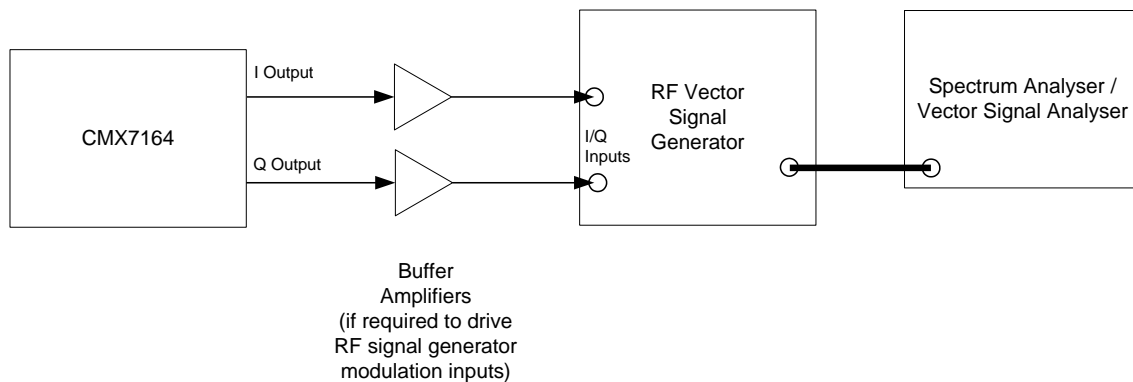
Figure 47 Tx Spectrum and Modulation Measurement Configuration for I/Q Operation

Modulation Spectrum

EN 300 113 Adjacent Channel measurement for 25kHz channel:

ACP < -81dB (limit is –60dB)

(Integration window = 16kHz)

Peak deviation (+1 symbol) = 2.4kHz

Eye Diagram

(Deviation for +1 symbol = 2.4 kHz)
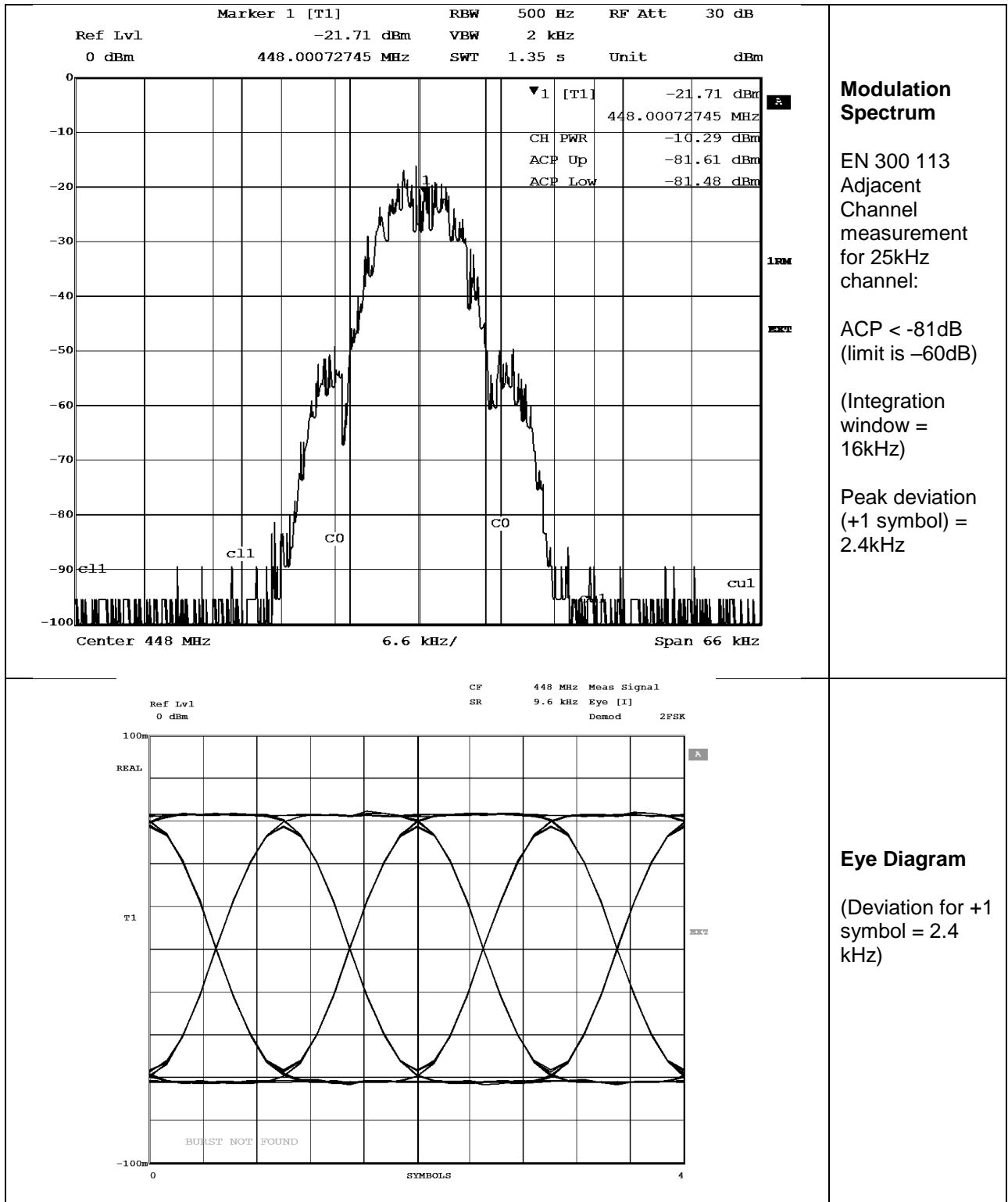
Figure 48 Tx Modulation Spectra (GMSK), 9.6kbps (BT=0.5), I/Q Modulation
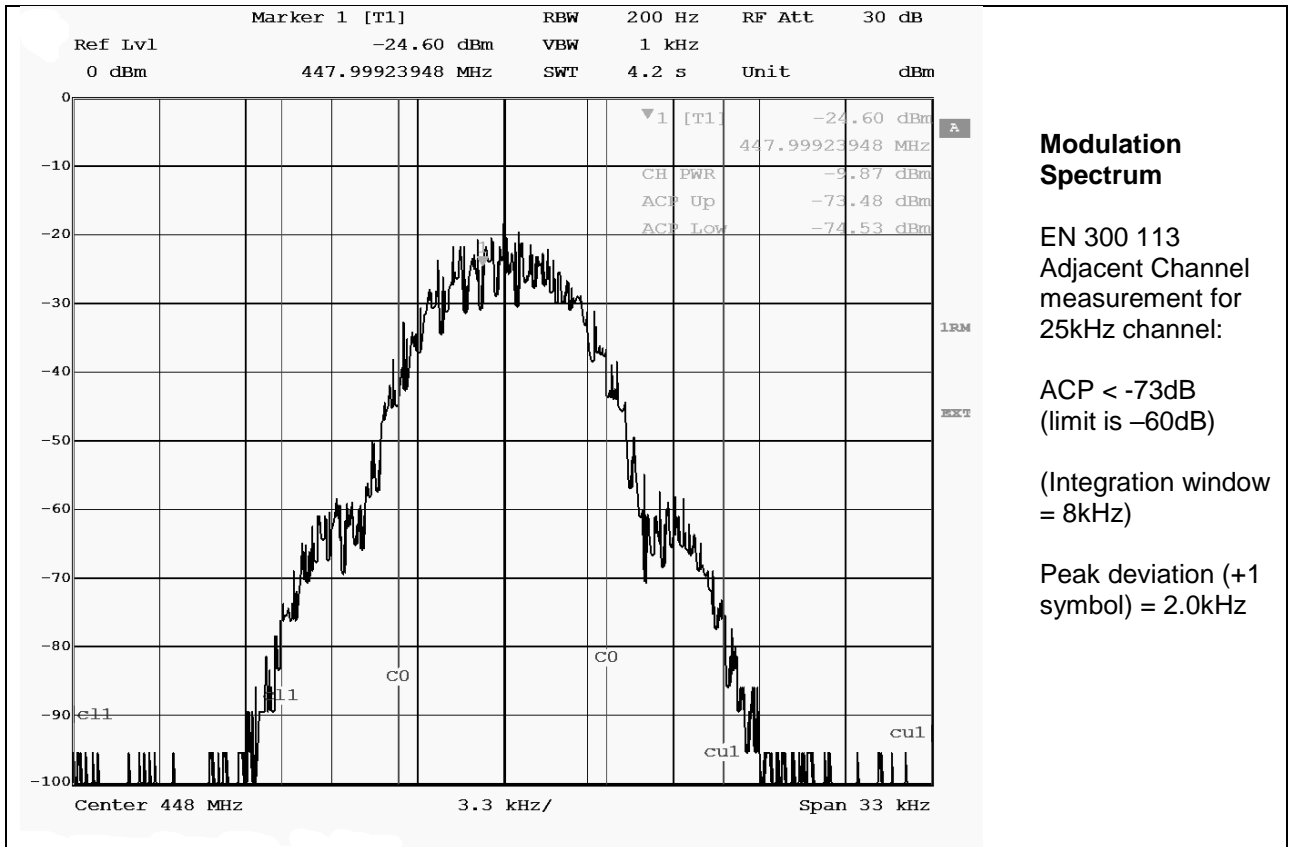
Modulation Spectrum

EN 300 113 Adjacent Channel measurement for 25kHz channel:

ACP < -73dB (limit is −60dB)

(Integration window = 8kHz)

Peak deviation (+1 symbol) = 2.0kHz
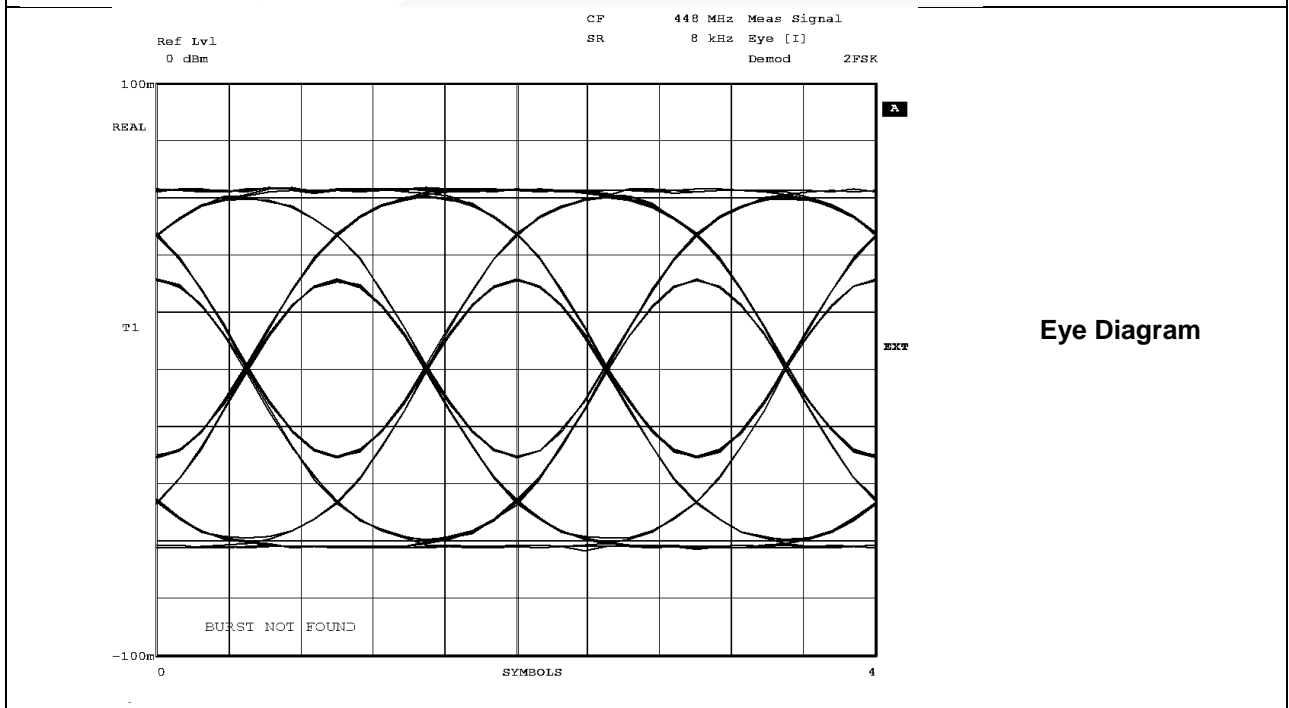
Eye Diagram

Figure 49 Tx Modulation Spectra (GMSK), 8kbps, BT=0.3 I/Q Modulation
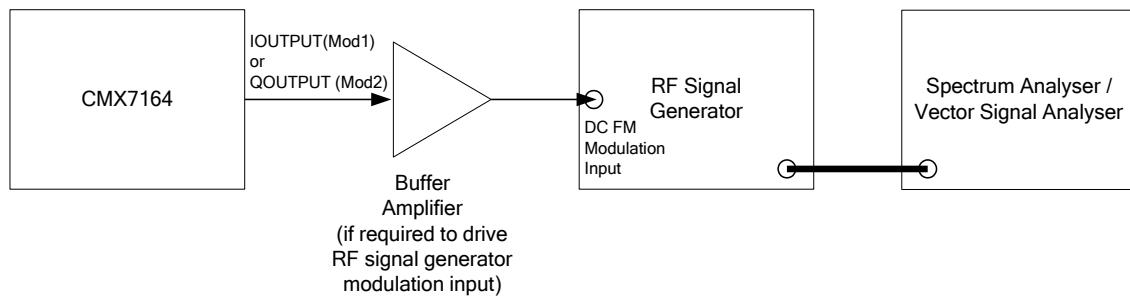
Figure 50 Tx Spectrum and Modulation Measurement Configuration for Two-point Modulation

Using the test system shown in Figure 50 the 7164FI-1.x internal PRBS generator was used to modulate the RF FM signal generator. Some typical results are shown in the following figures. The desired deviation was achieved by adjusting the deviation control in the RF signal generator.

Marker 1 [T1]		RBW	200 Hz	RF Att	20 dB
Ref Lvl	−22.95 dBm	VBW	1 kHz	Mixer	−20 dB
0 dBm	448.00095892 MHz	SWT	4.2 s	Unit	dB

▼1 [T1]   −22.95 dBm
               448.00095892 MHz
CH PWR   −9.76 dBm
ACP Up   −69.50 dBm
ACP Low   −70.51 dBm

Center 448 MHz   3.3 kHz/   Span 33 kHz

Modulation Spectrum

EN 300 113 Adjacent Channel measurement for 12.5kHz channel:

ACP = -69dB

(Integration window = 8kHz)

Peak deviation (+1 symbol) = 2.0kHz

CF   448 MHz Meas Signal
SR   8 kHz   Eye [I]
                  Demod   2FSK

Ref Lvl
0 dBm

BURST NOT FOUND
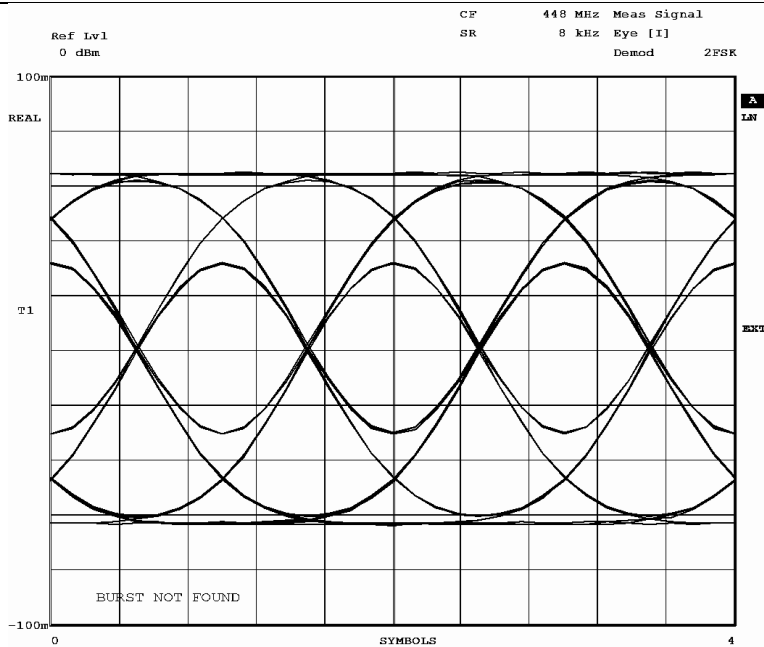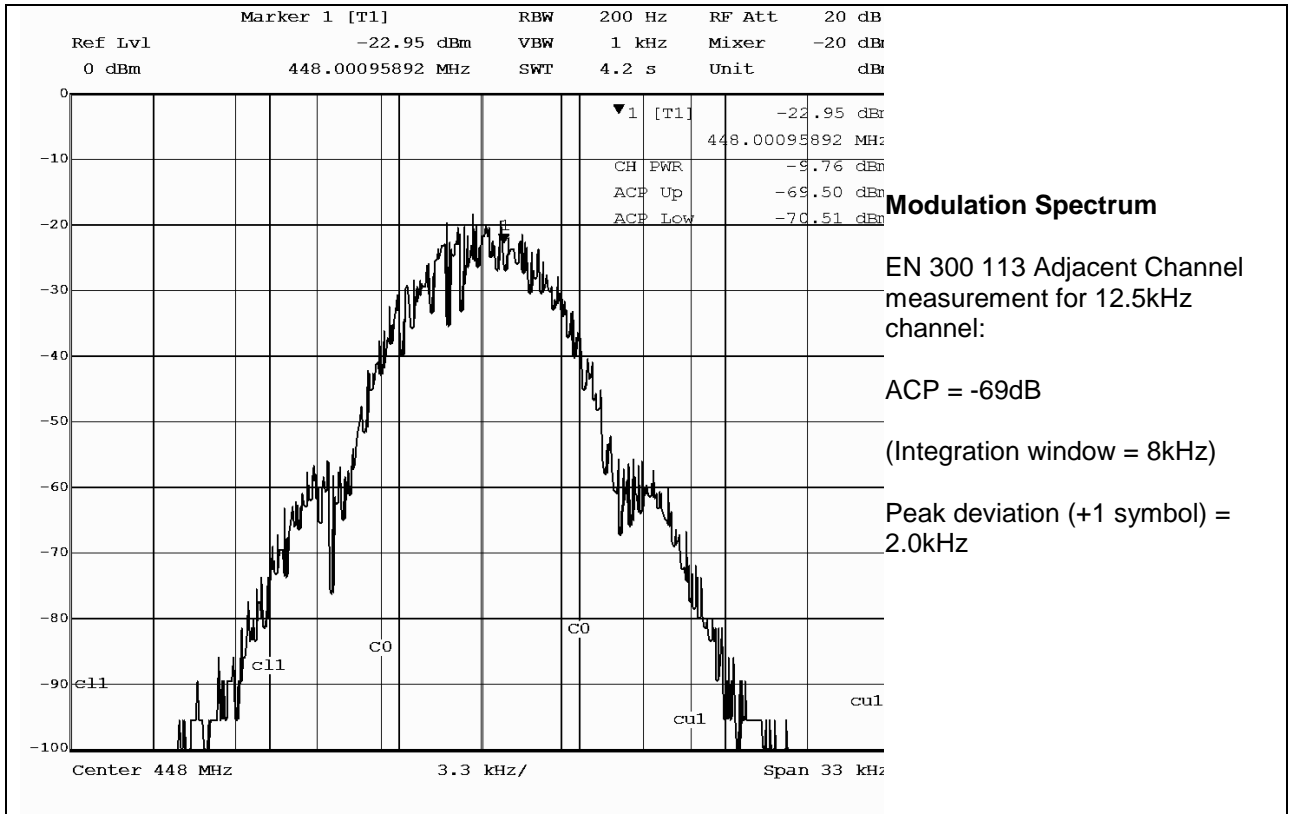
Eye Diagram

Figure 51 Tx Modulation Spectra (GMSK), 8kbps, BT=0.3 Two-point Modulation

8.5   7164FI-1.x Typical Receive Performance

The performance of the receiver will be different for any combination of bit rate and deviation. To aid the designer, some typical performance data has been measured using a realistic I/Q receiver.

8.5.1   Signal-to-Noise and Co-channel Performance

The performance of the 7164FI-1.x, when receiving, is illustrated by the graphs shown in Figure 52, Figure 53 and Figure 54. It should be noted that error rate performance depends on the modulation rate deviation and BT; results have been taken for typical channel bandwidths. The 7164FI-1.x supports multiple combinations of these factors but it is beyond the scope of this document to provide data for every combination. Data is provided, showing a selection of representative cases ranging from best case performance (with coding) to worst case where no coding is used (raw mode) plus the effect of using different BT values.

In the following graphs, the modulation is GMSK and the data rate is dependent on channel bandwidth. The 25kHz channel data rate is 9.6ksymbols/s, the 12.5kHz channel data rate is 8ksymbols/s, which is typical of the rate that may be achieved in each RF channel. The signal-to-noise ratio is calculated as:

SNR = Mean signal power -174 + NF + 10 $\log_{10}$(RxBW)

Where:

NF = receiver noise figure in dB
RxBW = receiver noise bandwidth
Mean signal power is in dBm
SNR = Signal-to-Noise Ratio in dB.

The graph in Figure 52 compares the raw sensitivity performance of data transfer using a 12.5kHz and a 25kHz channel. Pulse shaping was achieved using a Gaussian filter with BT=0.5 in the 25kHz channel, and BT=0.3 in the 12.5kHz channel. The modulation parameters used in all of the figures that follow in this section are summarised below

Channel Bandwidth (kHz)	Baud Rate (Symbols/s)	Pulse Shaping Filter	Deviation (kHz)	Measured Tx ACP (dBc)	Receiver Noise Bandwidth (kHz)	Used in Figures
25	9600	Gaussian BT=0.5	2.4	81	16	Figure 52
12.5	8000	Gaussian BT=0.3	2.0	73	8	Figure 52 Figure 53 Figure 54
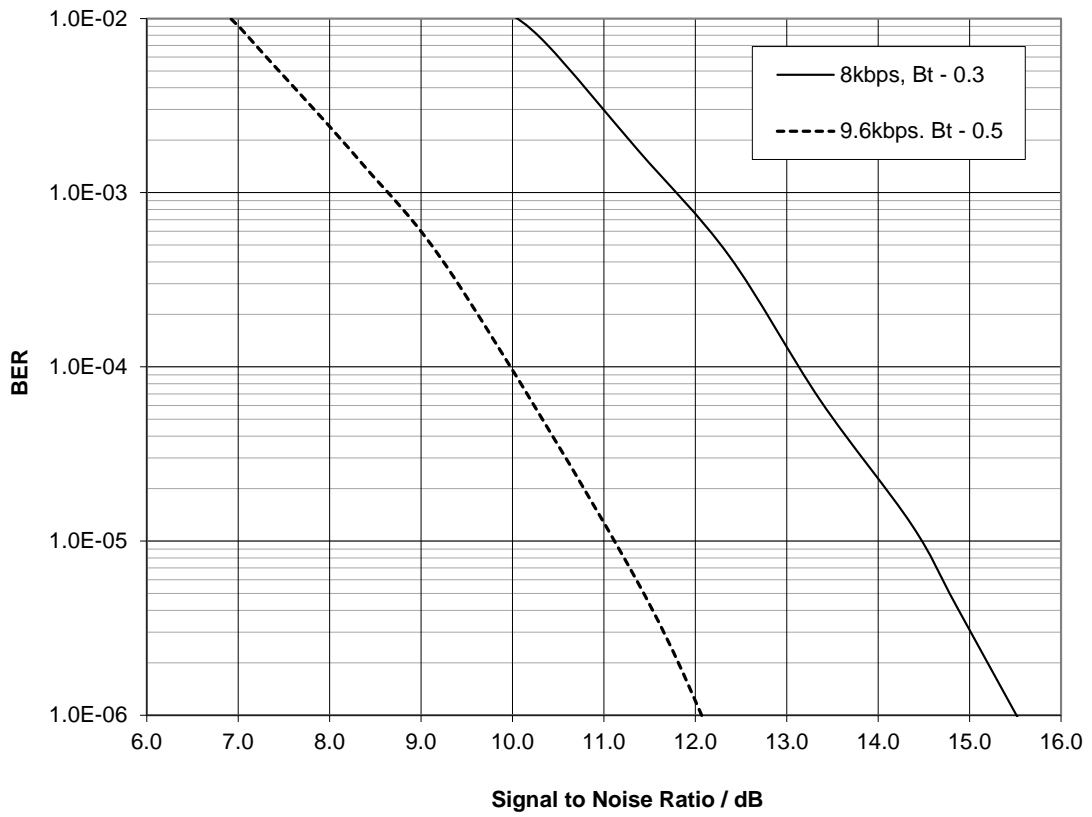
Figure 52 Modem Sensitivity Performance

Data transfer may have channel coding applied to it when GMSK/GFSK modulation is selected. The graph in Figure 53 shows the improvement due to channel coding in the 12.5kHz channel case (8ksymbols/s with Gaussian pulse shaping filter with BT=0.3).
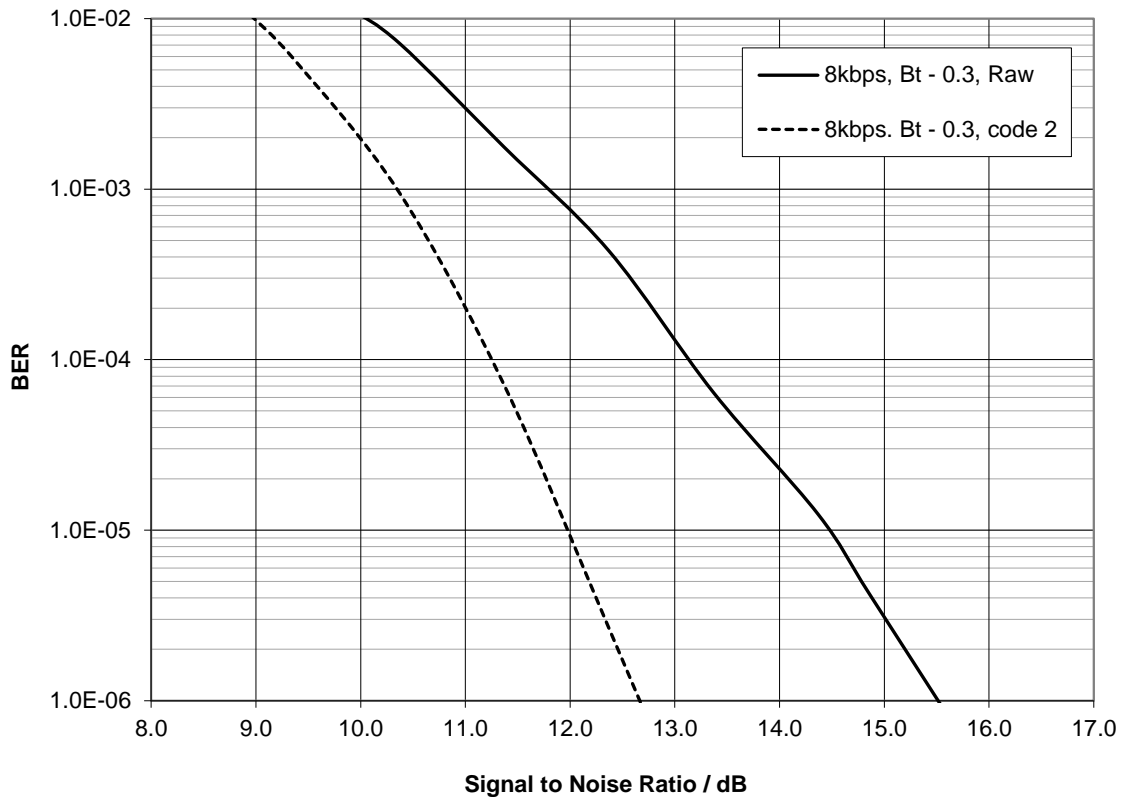
Figure 53 Sensitivity: 12.5kHz Channel, 8ksymbols/s With and Without Coding

The co-channel rejection ratio (Figure 54) is measured with an interferer modulated with 400Hz FM and having a deviation of 1.5kHz; which is 12% of the nominal 12.5kHz channel bandwidth. This particular interfering signal is used as it is specified in ETSI standard EN 300 113 for co-channel tests.
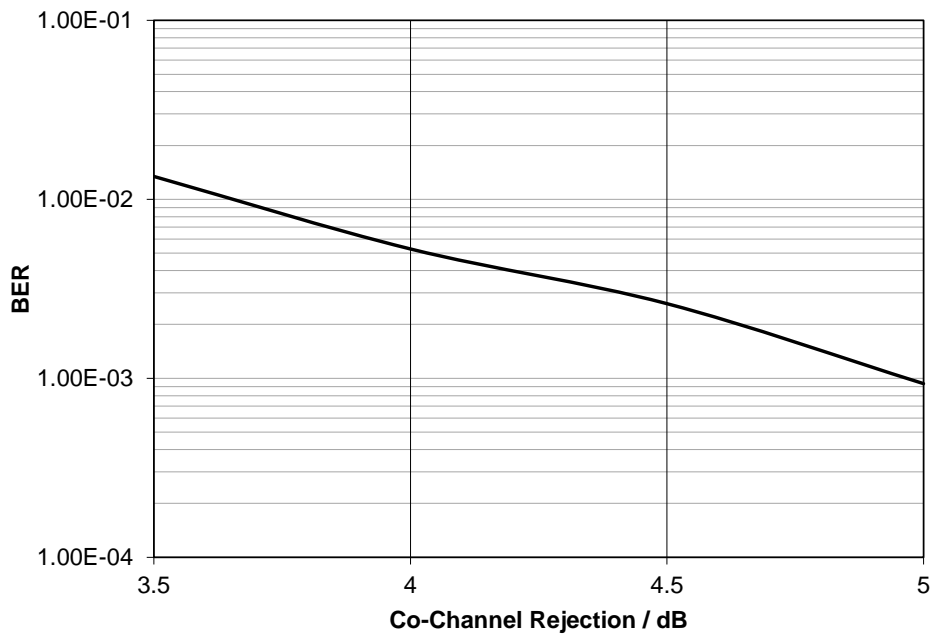
Figure 54 Modem Co-channel Rejection with FM Interferer (as EN 300 113)

9   7164FI-2.x Features

The 7164FI-2.x uses a 2, 4, 8 or 16 FSK modulation scheme with a configurable over-air symbol rate up to 10ksymbols/s, which corresponds to a maximum bit rate of 40kbps when using 16-FSK. In each case, the modulating signal is root raised cosine filtered with a filter alpha of 0.2. Raw data can be transferred and, in addition, formatted data blocks are supported and may be of variable length (up to 48 bytes) with a combination of 8-bit,16-bit or 32-bit CRC for error detection, plus error correction. In 4-FSK mode the modulation scheme and coding is designed to produce a signal that is over-the-air compatible with the CML FX/MX919B and CMX7143 (7143FI-2.x) modem devices. 4-FSK mode also supports RD-LAP coded block types that are over-air compatible with the CMX969 modem device.

9.1   7164FI-2.x Modulation

The 4-FSK scheme running at 2.4ksymbols/s (4.8kbps) can be used to fit inside a 6.25kHz channel bandwidth, a rate of 9.6ksymbols/s (19.2kbps) can be used in 25kHz bandwidth channels. Similarly the 2-FSK scheme running at 2.4ksymbols/s (2.4kbps) can be used to fit inside a 6.25kHz channel bandwidth, a rate of 9.6ksymbols/s (9.6kbps) can be used in 25kHz bandwidth channels. A 12.5kHz channel bandwidth is possible with data rates in between these extremes. Channel bandwidth is dependent on the peak deviation that the modulating signal causes the carrier to deviate by as well as the data rate.

The 7164FI-2.x can also transmit and receive 8-FSK and 16-FSK modulated signals.

When the device is in 4-, 8- or 16-FSK mode the preamble and the frame sync will always be transmitted using 4-FSK modulation. The following table shows the list of possible modulation types along with choices for their corresponding preamble and frame sync modulation types:

Payload modulation type (Controlled by programming register P4.2)	Applicable modulation type(s) for preamble and frame sync (Controlled by programming register P4.2)	FEC available for payload data? (Controlled by Modem Mode and Control - $6B write register)
2-FSK	2-FSK or 4-FSK	No
4-FSK	4-FSK	Yes
8-FSK	4-FSK	Yes
16-FSK	4-FSK	Yes

Normally, when receiving, the 7164FI-2.x can be programmed to receive data using a fixed modulation type. In this case it will search for Frame Sync1 and/or Frame Sync2 and then continue to receive data according to the modulation type defined using the programming register P4.2 in Program Block 4 – Modulation Control programming block. This is the case for both raw and formatted (coded) data reception.

Alternatively, the device can be used in its "AutoModMode", selected using the Modem Mode and Control - $6B write register. In this mode, the 7164FI-2.x will search for Frame Sync1 and Frame Sync2 with the particular frame sync detected dictating the type of modulation for the associated payload data. Programming register P4.4 in Program Block 4 – Modulation Control programming block defines the relationship between the particular detected frame sync and the modulation type for the payload data in "AutoModMode". The following table lists the programming register that controls the payload modulation type for each receive mode.

b11-8 of Modem Mode and Control - $6B write register	The 7164FI-2.x will search for:	Rx Payload modulation type is controlled by:
0010	Sync1 and Sync2	P4.2
0100	Sync1	P4.2
0101	Sync2	P4,2
1001	Sync1 and Sync2	P4.2
1010	Sync1	P4.2
1011	Sync2	P4.2
1101 (AutoModMode)	Sync1 and Sync2	P4.4

The bit to symbol mappings that this Function Image™ uses for 2-FSK and 4-FSK are:

2-FSK bit to symbol mapping	
Input Bit	Relative Symbol Level
0	-3
1	+3

4-FSK bit to symbol mapping	
Input Bit Pair	Relative Symbol Level
00	-1
01	-3
10	+1
11	+3

The bit to symbol mappings that this Function Image™ uses for 8-FSK and 16-FSK are:

8-FSK bit to symbol mapping	
Input tri-bits	Relative Symbol Level
000	-1
001	-3
010	-7
011	-5
100	+1
101	+3
110	+7
111	+5

16-FSK bit to symbol mapping	
Input quad bits	Relative Symbol Level
0000	-1
0001	-3
0010	-7
0011	-5
0100	-15
0101	-13
0110	-9
0111	-11
1000	+1
1001	+3
1010	+7
1011	+5
1100	+15
1101	+13
1110	+9
1111	+11

RRC filters are implemented in both Tx and Rx with a filter alpha of 0.2. Care has been taken to ensure that the maximum frequency deviation level is the same across all the different order modulations i.e. all of 2-FSK +1, 4-FSK +3, 8-FSK +7, and 16-FSK +15 symbols have the same frequency deviation.
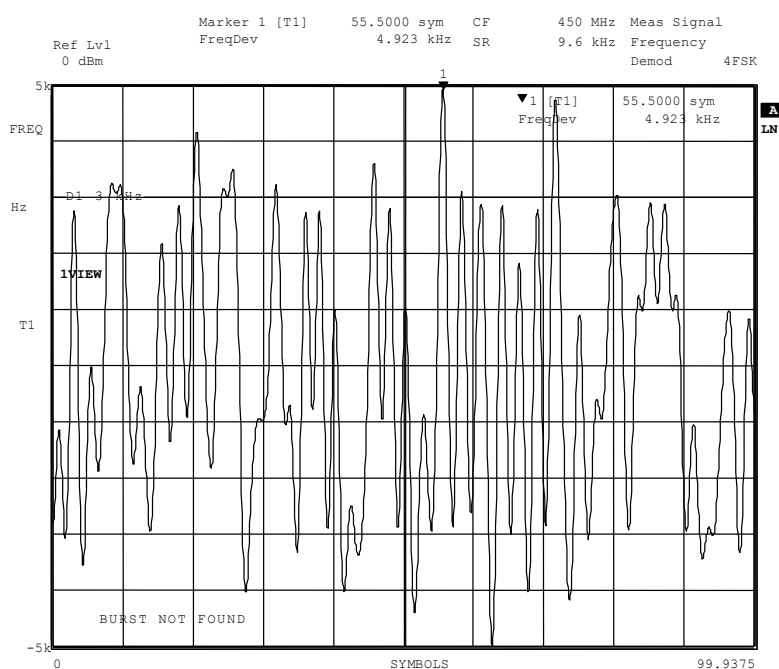
Figure 55 PRBS Waveform (Two-point Modulation)

When receiving 8 and 16-FSK signals the initial acquisition of I/Q dc offset correction is critical to good reception. The 7164FI-2.x is capable of calculating an I/Q dc offset correction, but performance will be improved by choice of preamble pattern. If the deviation is small then a typical +3,+3,-3,-3,… preamble pattern can have a large dc component in I or Q which will make dc offset calculation difficult. A +3,+3,+3,+3… pattern is a better choice, with particular benefit to 8 and 16-FSK reception. It is recommended that such a preamble pattern be chosen for 8- and 16-FSK reception, along with an alternate I/Q dc offset acquisition mode set using programming register P4.5 as described in section 13.2.6 Program Block 4 – Modulation Control.

9.2   7164FI-2.x Radio Interface
The transmit radio interface of the 7164FI-2.x can be set to two-point modulation or I/Q. When the 7164FI-2.x is in two-point modulation mode the I Output is used as 'Mod 1', and the Q Output is used as 'Mod 2'. The receive signal must come from an I/Q radio receiver.

9.2.1   I/Q Transmit and I/Q Receive Interfaces
The 7164FI-2.x can produce an I/Q modulated signal, taking a baseband modulating signal and using it to frequency modulate an I/Q baseband signal, with a user programmable deviation.

In receive the 7164FI-2.x will accept an I/Q input signal and provide significant channel filtering digitally. It will then frequency demodulate the resulting signal, which is treated as a limiter discriminator output signal would be internally. An overview of how the CMX7164 might use the CMX992[5] for reception and the

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[5] CMX992 is an RF Quadrature/IF Receiver

CMX998[6] for transmission is shown in Figure 56. The internal functions of the CMX7164 when operating in this mode are shown in Figure 3.

Note that the transmit and receive interfaces are identical to those used for QAM modulation in Figure 83, facilitating multi-mode modem operation. However no linearisation is required when transmitting 2/4-FSK.
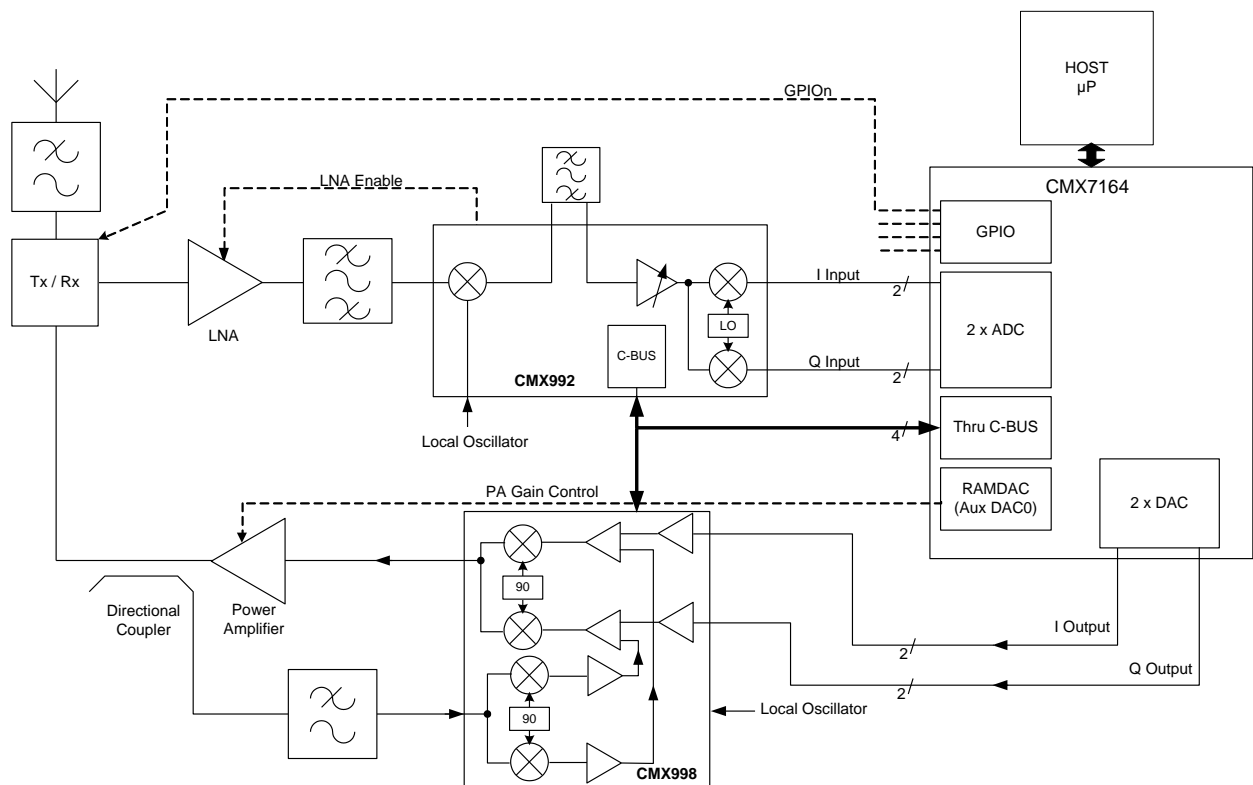
Figure 56 Outline Radio Design (I/Q in/out for 2 or 4-FSK)

Use of I/Q receive mode brings with it the problem of I/Q dc offsets. There are dc offsets caused by the radio receiver – resulting in the signal into the CMX7164 having a dc offset other than BIAS. The offset needs to be removed prior to demodulation. Offsets typically remain constant for a particular radio frequency selected, but will vary if that frequency is changed. Gain within the radio receiver may also affect the dc offset seen by the CMX7164.

I/Q dc offset effects are a radio issue which is beyond the control of the CMX7164. However the CMX7164 does provide dc offset calculation and removal. These are described in detail in the application note section 14.3 DC Offsets in I/Q Receivers.

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[6] CMX998 is a Cartesian Feedback Loop Transmitter which is designed primarily for non-constant envelope modulations such as QAM although it will also support GMSK/4-FSK; conventional I/Q vector modulators such as the CMX993 would be more typical of solutions for GMSK/4-FSK modulation.

9.2.2   Two-point Modulation Transmit with I/Q Receive Interface

An overview of how the CMX7164 might integrate with an I/Q receiver, and two-point modulation transmitter is shown in Figure 57. The internal functions of the CMX7164 when operating in this mode are shown in Figure 4.
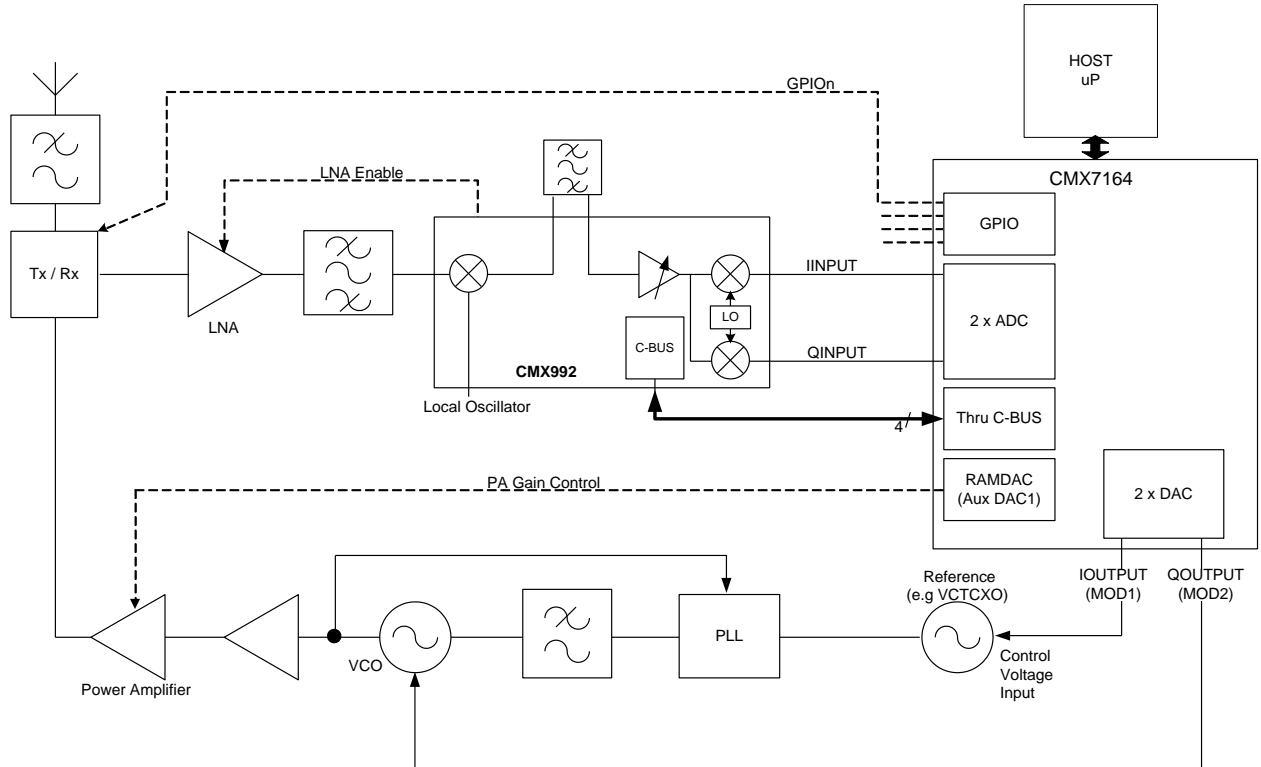
Figure 57 Outline Radio Design (2 or 4-FSK – I/Q in, two-point mod out)

9.3   7164FI-2.x Formatted Data

When transmitting/receiving 4-FSK the 7164FI-2.x supports two kinds of formatted data – native formatted data and RD-LAP formatted data, both of which provide the ability to channel code blocks of data using trellis coding and CRCs. RD-LAP formatted data is only available when 4-FSK is selected.

When transmitting/receiving 4-FSK, 8-FSK or 16-FSK the 7164FI-2.x supports native formatted data in a range of block sizes and with two channel code rates (high and low) for each modulation type; RD-LAP formatting is not available.

Native formatted data:
The frame structure as used in a formatted data system is illustrated in Figure 58. It typically consists of a 24-symbol frame sync pattern followed by a 'Header Block', one or more 'Intermediate Blocks and a 'Last Block'.
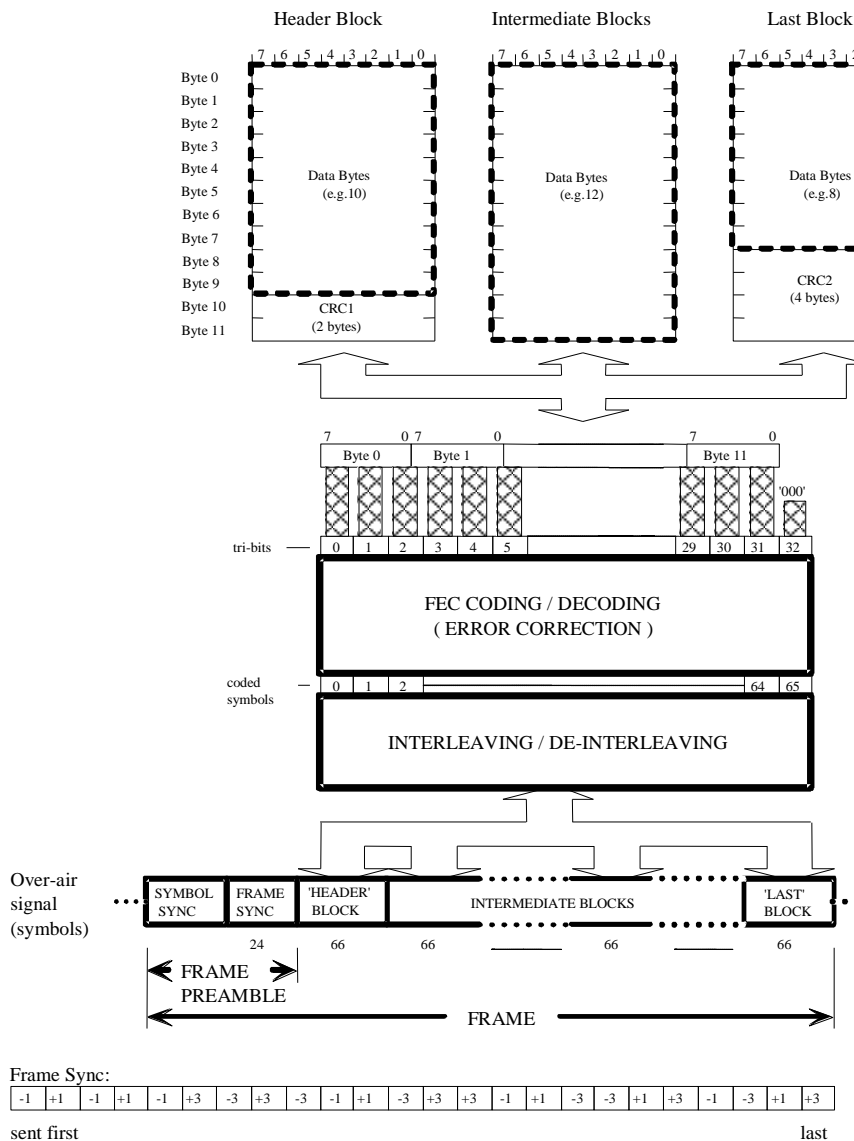
Figure 58 Native Formatted Data Over Air Signal Format

The 'Header' block is self-contained as it includes its own checksum (CRC1), and would normally carry information such as the address of the calling and called parties, the number of following blocks in the frame (if any) and miscellaneous control information.

The 'Intermediate' block(s) contain only data, the checksum at the end of the 'Last' block (CRC2) also checks the data in any preceding 'Intermediate' blocks. This checksum calculation should be reset as required using the "Reset CRC2" block type – so that any transmitted CRC2 contains the CRC of only the desired blocks. In receive it must be reset to match the expected input data block sequence. A variety of different frame formats are possible, some examples are illustrated in Figure 59.

Figure 59 Suggested Frame Structures

The CMX7164 performs all of the block formatting and de-formatting, the binary data transferred between the modem and its µC being that enclosed by the thick dashed rectangles near the top of Figure 58. When receiving header blocks and last blocks the CMX7164 will indicate CRC success or failure and will provide the data regardless.

In Figure 58 the size of data block illustrated is always 12 bytes when user bytes and CRC bytes are counted together. The CMX7164 adds further flexibility by supporting other block sizes depending on the modulation type in use. The reference to tri-bits, and symbol count for the 12-byte block in Figure 58 is specific to 4-FSK coded data. The 7164 FI-2-x provides the following predefined formatted block sizes.

Table 4 Native Formatted Block Types, Sizes and Rates for 4-, 8-, 16-FSK (FI-2.x)

Block Type (b11-8)	Block Size in bytes	Coding Rate 4-FSK	Coding Rate 8-FSK	Coding Rate 16-FSK	User (CRC) bytes for a Command (b15-12):		
					Header Block (Cmd 5)	Inter Block (Cmd 6)	Last Block (Cmd 7)
0	6	3/4	2/3	3/4	4(2)	6	2(4)
1	9	3/4	2/3	3/4	7(2)	9	5(4)
2	12	3/4	2/3	3/4	10(2)	12	8(4)
3	12	3/4 RDLAP – 4-FSK Only			10(2)	12	8(4)
4	12	3/4	2/3	3/4	10(2)	12	8(4)
5	24	3/4	2/3	3/4	22(2)	24	20(4)
6	36	3/4	2/3	3/4	34(2)	36	32(4)
7	48	3/4	2/3	3/4	46(2)	48	44(4)
8	12	9/16	1/2	9/16	10(2)	12	8(4)
9	24	9/16	1/2	9/16	24(2)	24	20(4)
10	36	9/16	1/2	9/16	34(2)	36	32(4)
11	48	9/16	1/2	9/16	48(2)	48	44(4)

User defined block sizes and coding rates can be set using Program Block 12 – see section 13.2.13.

RD-LAP formatted data:

The frame structure in RD-LAP mode is illustrated in Figure 60 RD-LAP Over Air Signal Format, and typically consists of a Frame Preamble (comprising a 24-symbol Frame Synchronisation pattern and Station ID block) followed by one or more 'Header' blocks, one or more 'Intermediate' blocks and a 'Last' block. Channel Status (S) symbols are included at regular intervals. The first frame of any transmission is preceded by a Symbol Synchronisation pattern.
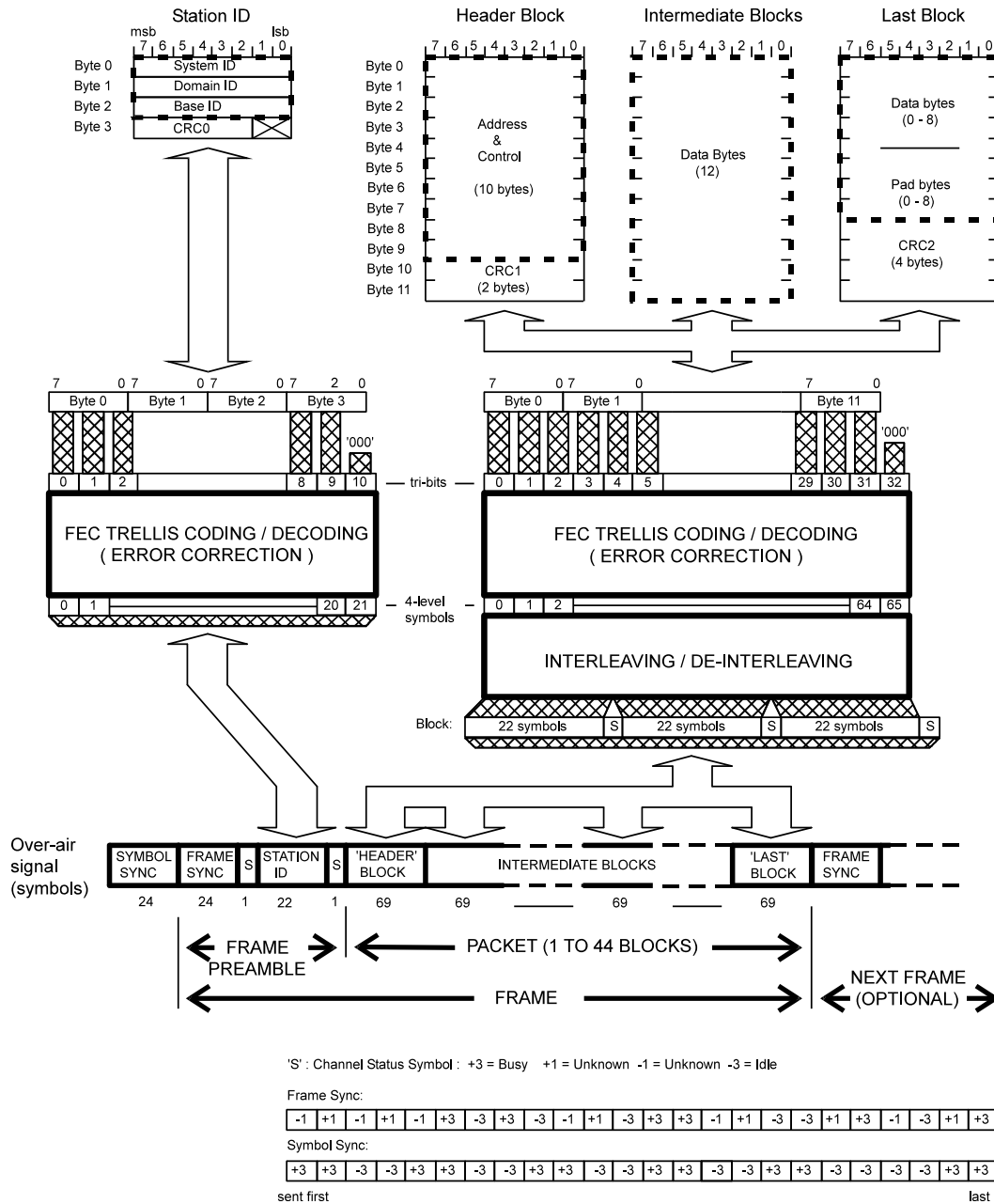

Figure 60 RD-LAP Over Air Signal Format

The 'Station ID' and the 'Header' block are self-contained as they include their own checksums – CRC0 (6-bit CRC) and CRC1 (16-bit CRC) respectively.

The 'Intermediate' block(s) contains only data, the checksum at the end of the 'Last' block (CRC2 – 32-bit CRC) also checks the data in any preceding 'Intermediate' blocks. This checksum calculation should be reset as required using the 'Reset CRC2' block type – so that any transmitted CRC2 contains the CRC of only the desired blocks. In receive it must be reset to match the expected input data block sequence.

The CMX7164 performs all of the block formatting and de-formatting, the binary data transferred between the modem and its µC being that enclosed by the thick dashed rectangles near the top of Figure 60. When receiving Station ID blocks, Header blocks and Last blocks the CMX7164 will indicate CRC success or failure and will provide the data regardless.

In Figure 60, except for the Station ID block, the size of data block illustrated is always 12 bytes when user bytes and CRC bytes are counted together. The channel status symbols must be packed in a byte and provided along with the payload data as shown in Table 12 and Table 13.

Table 5 RD-LAP Block Types, Sizes and Rates (FI-2.x)

Block Type	Block Size	Coding Rate (only)	Channel Status Byte + User(CRC) bytes for a:				Total bytes (excluding frame/symbol sync,)
			Header Block	Inter Block	Last Block	Station ID Block	
3	12 bytes + 3 channel status symbols	RD-LAP coding	1+10(2)	1+12	1+8(4)	-	17 bytes + 2 bits
0	30 bits + 1 channel status symbol	RD-LAP coding	-	-	-	1 + 3 (6-bits)	5 bytes + 6 bits

Note that in order to be compatible with CMX969 RD-LAP coding the CRC register initial values must be configured to 0 as shown in   Program Block 3 - Preamble/Tail/CRC.

9.4   7164FI-2.x Receiver Response Equaliser

When receiving signals using a radio receiver the signal provided to the CMX7164 is likely to be distorted. Considering the architecture of Figure 56 as typical, the distortion will largely be caused by the crystal filter – shown as a bandpass filter in the diagram. The crystal filter operates on the received signal at an intermediate frequency; its purpose is to attenuate unwanted signals such as those on adjacent channels before they get to the CMX7164.[7]

Typically the pass band of the crystal filter is not flat or perfectly linear phase, resulting in the wanted signal being distorted due to the amplitude/phase response of the filter. The result is usually a degraded receive signal which will result in poor receive performance for 8 or 16-FSK reception and a small degradation in 2 or 4-FSK reception.

Other radio architectures may provide baseband filtering in order to help reject unwanted adjacent channel signals. Such filtering may also have a pass band that is not flat, and therefore will degrade reception in a similar way.

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[7] Note that the CMX7164 provides significant channel filtering itself, but further rejection of unwanted signals is desirable in most applications to improve receiver dynamic range and prevent blocking or products generating intermodulation products reaching the low power 'back-end' of the receiver.

The CMX7164 provides a Receiver Response Equaliser that will compensate for the group delay and variation in gain of the crystal filter, or any other distortions present in the received signal. The equaliser must be trained with a clean, high level, 4-FSK signal in order to establish the receiver response and produce a filter which compensates for it. Once this filter is calculated it may be read from the CMX7164 and stored for later use. The CMX7164 can be configured with up to two previously stored Receiver Response Equaliser filters which may, for example, be used to compensate for two different crystal filters in a radio designed to receive in two channel bandwidths.

Although trained using a 4-FSK signal the resulting filter is suitable to compensate for the receiver response whilst receiving 2, 4, 8, or 16-FSK signals. A suitable training signal may either be produced using another CMX7164 or a signal generator using preamble, frame sync and pseudo-random data, along with pulse shaping filters that are compatible with the FI-2.x signal specification within this datasheet.

The Receiver Response Equaliser has two modes, single mode produces better results when correcting for receivers with a simple baseband roll off (for example in a direct conversion architecture). Dual mode produces better results when compensating for a radio receiver which includes a crystal filter. Program Block 11 – Receiver Response Equaliser (FI-2.x and FI-4.x) provides equaliser mode selection, allows adjustment of the gain used in the feedback path when training the equaliser and allows the training time to be altered. The same Program Block allows the filter resulting from training to be read for storage and to be programmed back in to the CMX7164 later for use when receiving.

Results when using the Receiver Response Equaliser are shown in section 9.6.4 Receiver Response Equaliser Performance.

See:
- 13.1.19 Modem Mode and Control - $6B write
- 13.2.13 Program Block 11 – Receiver Response Equaliser (FI-2.x and FI-4.x)

9.5   7164FI-2.x Typical Transmit Performance

Using the test system shown in Figure 61 the 7164FI-2.x internal PRBS generator was used to modulate the RF vector signal generator. Some typical results are shown in the following figures. The desired deviation was achieved by adjusting the CMX7164 peak deviation using register $61.
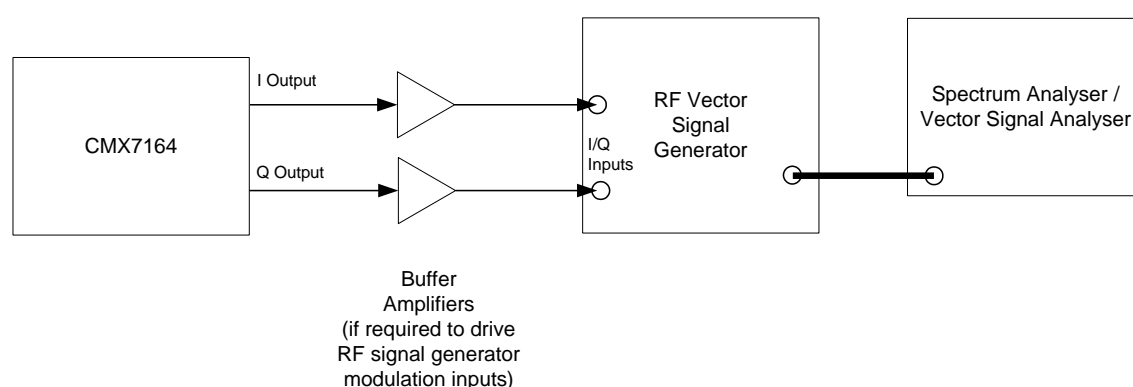
Figure 61 Tx Spectrum and Modulation Measurement Configuration for I/Q Operation
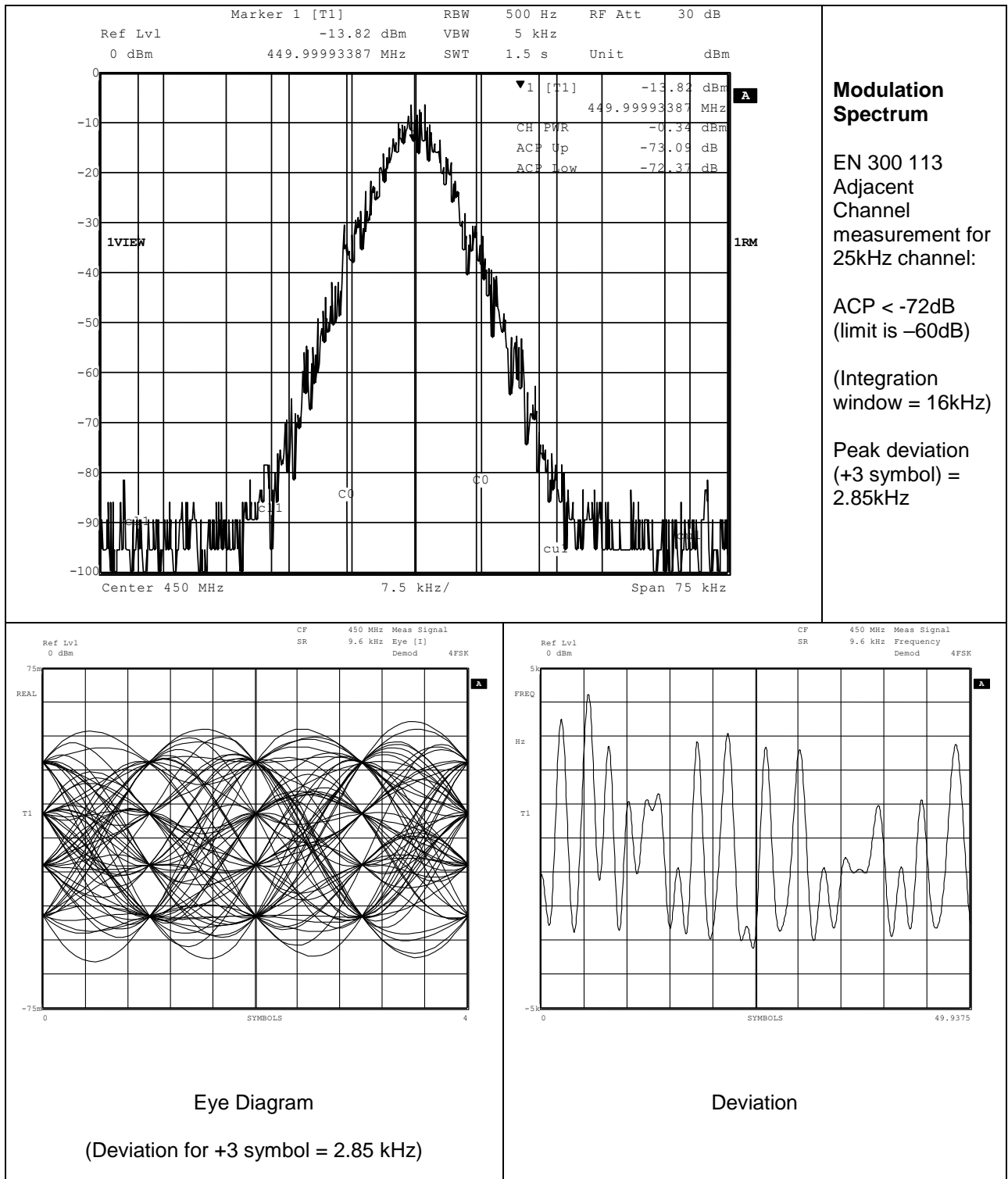
Figure 62 Tx Modulation Spectra (4-FSK), 9.6ksymbols/s (19.2kbps), I/Q Modulation
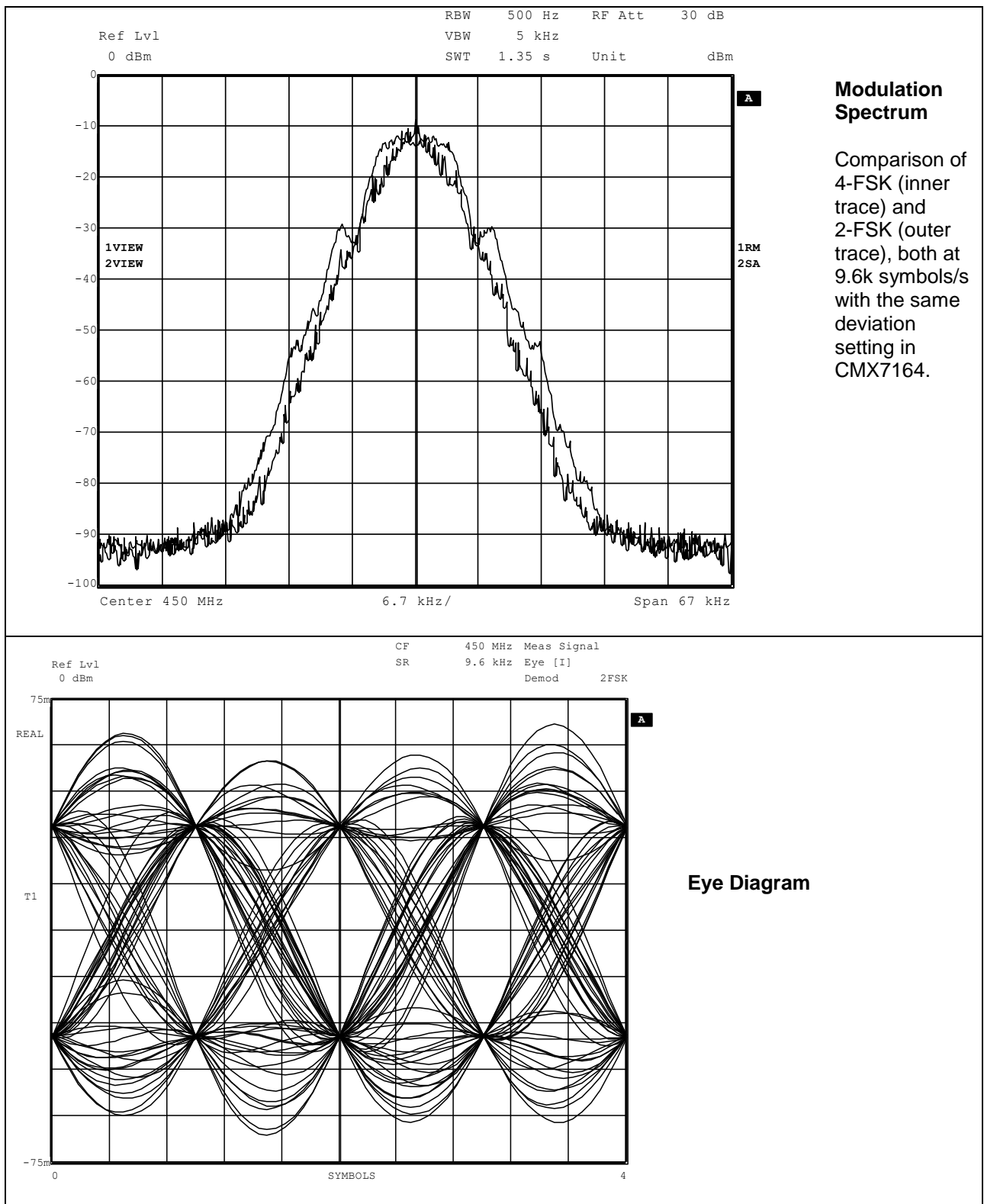
Figure 63 Tx Modulation Spectra (2-FSK), 9.6k symbols/s (9.6kbps), I/Q Modulation
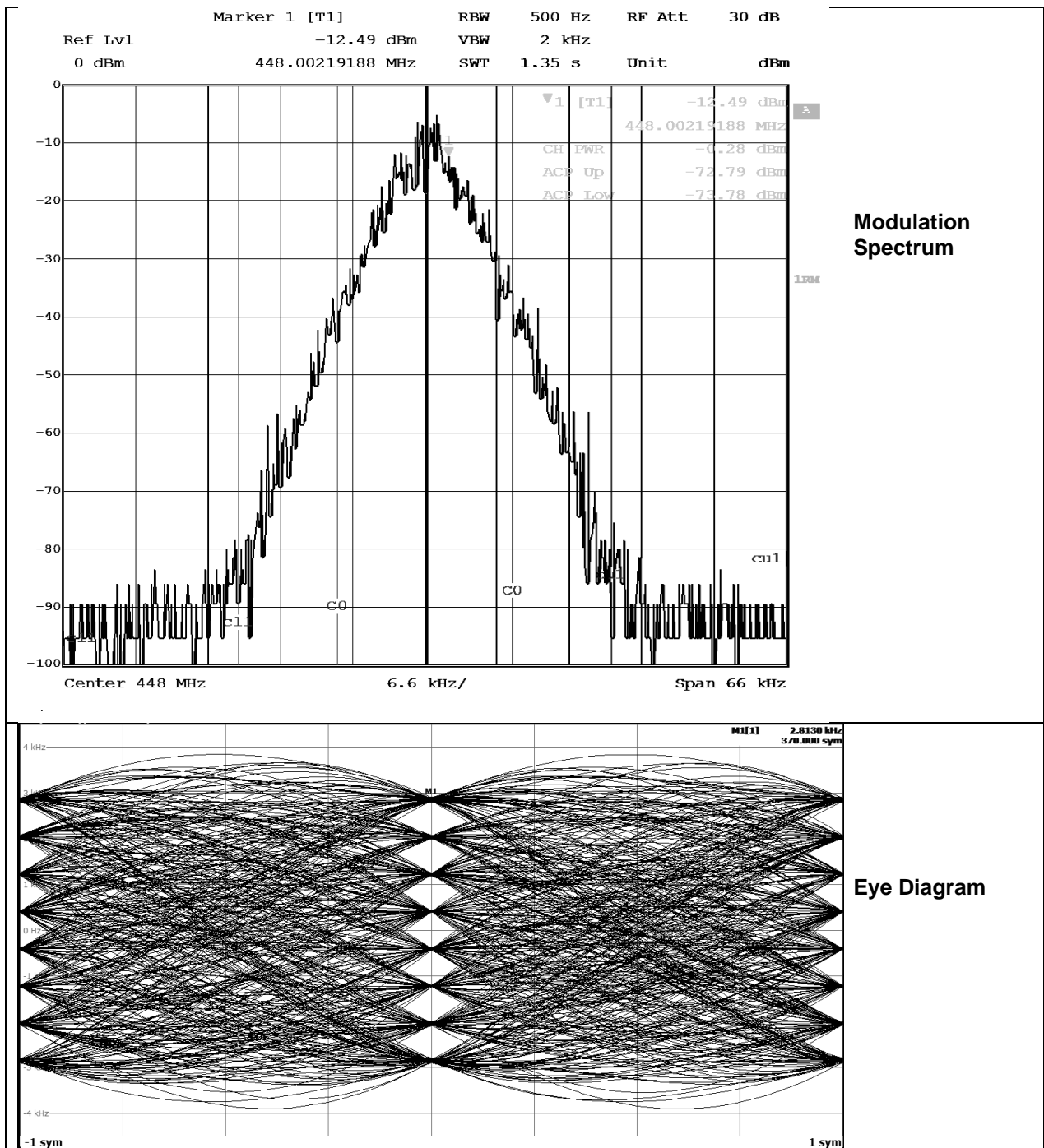
Figure 64 Tx Modulation Spectra (8-FSK), 9.6k symbols/s (28.8kbps), I/Q Modulation
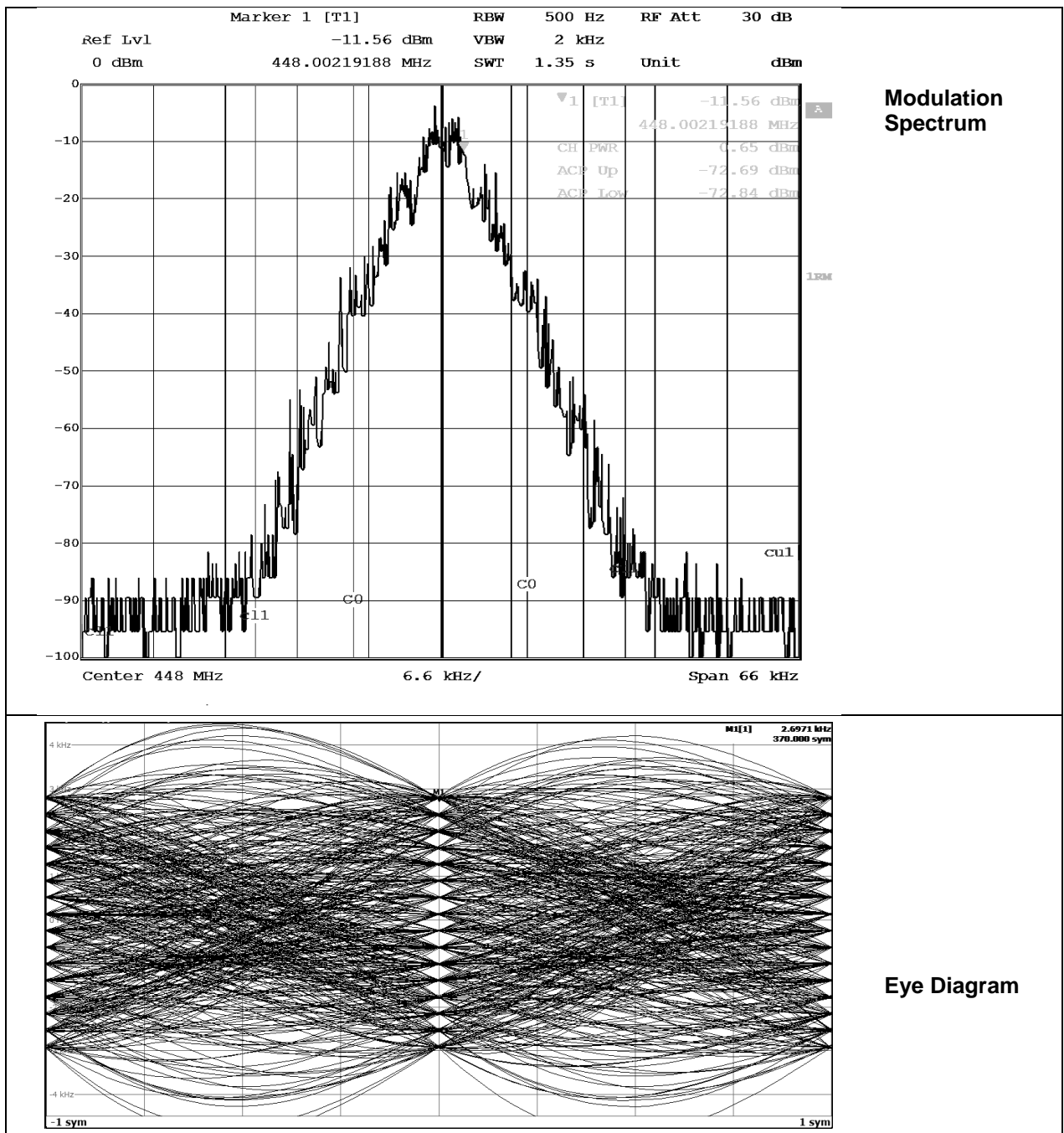
Figure 65 Tx Modulation Spectra (16-FSK), 9.6k symbols/s (38.4kbps), I/Q Modulation
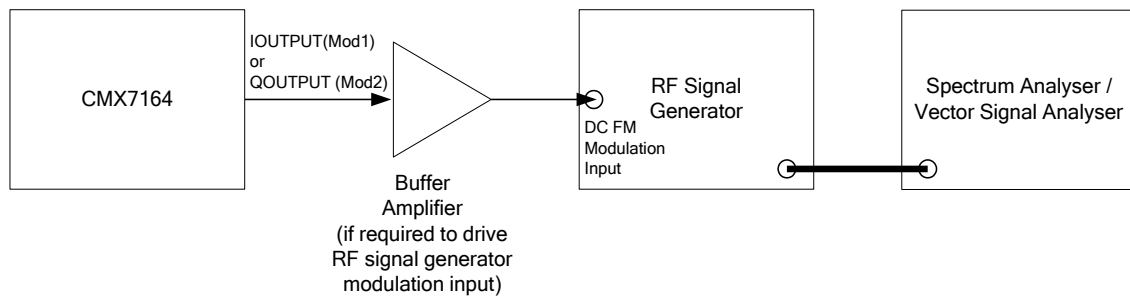
Figure 66 Tx Spectrum and Modulation Measurement Configuration for Two-point Modulation

Using the test system shown in Figure 66 the 7164FI-2.x internal PRBS generator was used to modulate the RF FM signal generator. Some typical results are shown in the following figures. The desired deviation was achieved by adjusting the deviation control in the RF signal generator.

Marker 1 [T1]   RBW   500 Hz   RF Att   30 dB
Ref Lvl   -40.77 dBm   VBW   5 kHz
0 dBm   450.00837836 MHz   SWT   1.35 s   Unit   dBm

Modulation Spectrum

EN 300 113 Adjacent Channel
measurement for 25kHz
channel:

ACP = -75dB

(Integration window = 16kHz)

Peak deviation (+3 symbol) =
2.85kHz

CF   450 MHz Meas Signal
SR   9.6 kHz Eye [I]
Demod   4FSK
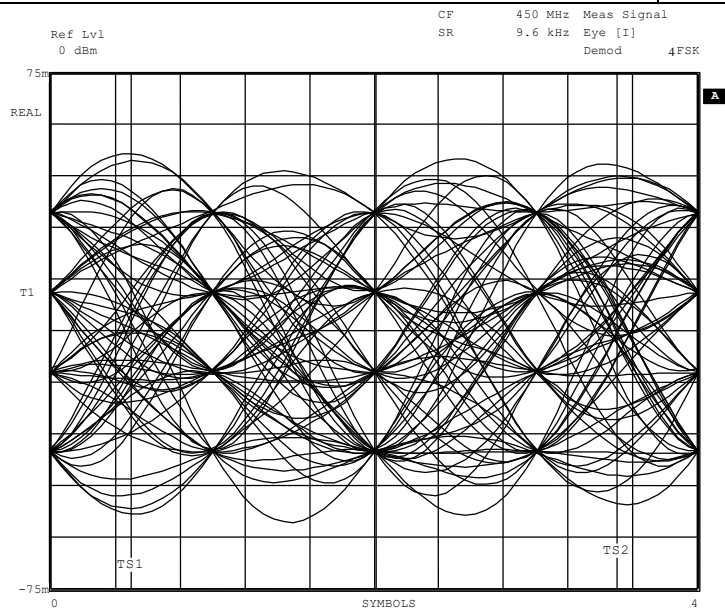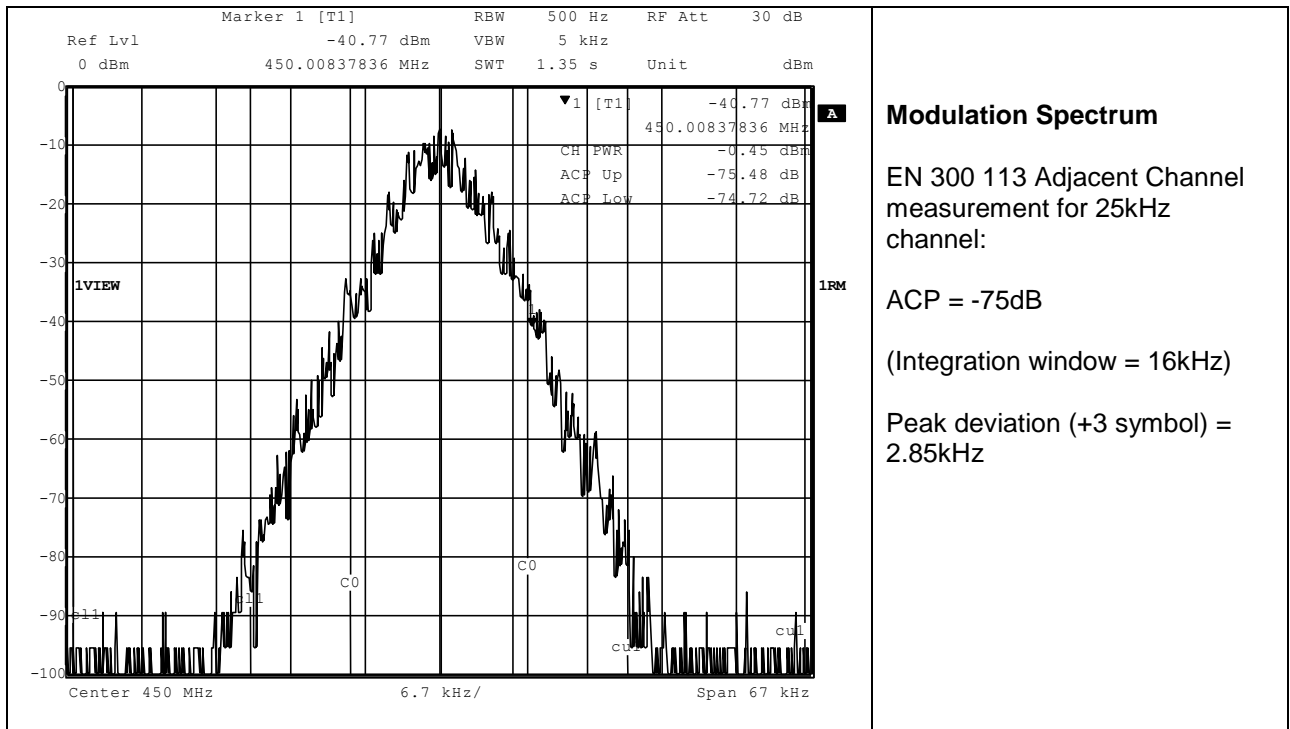
Eye Diagram

Figure 67 Tx Modulation Spectra (4-FSK), 19.2kbps, Two-point Modulation

9.6   7164FI-2.x Typical Receive Performance

The performance of the receiver will be different for any combination of nFSK modulation, bit-rate and deviation. To aid the user some typical performance data has been measured using a realistic I/Q receiver. This is provided to serve as guidance, however, each user must consider his own application requirements and then select both the receiver used and any coding (whether used and if so block size and code rate, where applicable).

9.6.1   4-FSK

9.6.1.1   *Signal-to-Noise and Co-channel Performance*
The performance of the 7164FI-2.x when receiving is shown in the following graphs. It should be noted that error rate performance depends on the modulation type, symbol rate and deviation; results have been taken for typical channel bandwidths. The 7164FI-2.x supports multiple combinations of these factors but it is beyond the scope of this document to provide data for every combination. Data is provided showing a selection of representative cases ranging from best case performance (maximum coding) to worst case where no coding is used (raw mode) plus the effect of using the two supported types of data pulse shaping: plain Root Raised Cosine (RRC) filtering or RRC plus sinc filter.

In the following graphs, the modulation is 4-FSK and the data rate is dependant on channel bandwidth. The 25kHz channel data rate is 9.6ksymbols/s, the 12.5kHz channel data rate is 4.8ksymbols/s and the 6.25kHz channel data rate is 2.4ksymbols/s, which is typical of the rate that may be achieved in each RF channel. The signal-to-noise ratio is calculated as:

$$SNR = \text{Mean signal power} -174 + NF + 10 \log_{10}(RxBW)$$

Where:

NF = receiver noise figure in dB
RxBW = receiver noise bandwidth
Mean signal power is in dBm
SNR = Signal-to-Noise Ratio in dB.

The graph in Figure 68 compares the raw sensitivity performance of data transfer using a 6.25kHz, a 12.5kHz and a 25kHz channel, in each case the deviation of the transmitted modulation has been adjusted to give a realistic Tx ACP, in the 6.25kHz and 12.5kHz case the Tx ACP was ~63dBc and in the 25kHz case the Tx ACP was ~73dBc. The pulse shaping filter used was an RRC with no sinc filter in place. The modulation parameters used in all of the figures that follow in this section are summarised below

Channel Bandwidth (kHz)	Baud Rate (Symbols/s)	Pulse Shaping Filter	Deviation (kHz)	Measured Tx ACP (dBc)	Receiver Noise Bandwidth (kHz)	Used in Figures
25	9600	RRC Only	2.85	72	18	Figure 68
12.5	4800	RRC + Sinc	2.45	63	9	Figure 69
12.5	4800	RRC Only	1.9	63	9	Figure 68 Figure 69 Figure 70 Figure 71 Figure 72
6.25	2400	RRC Only	0.95	63	4.5	Figure 68
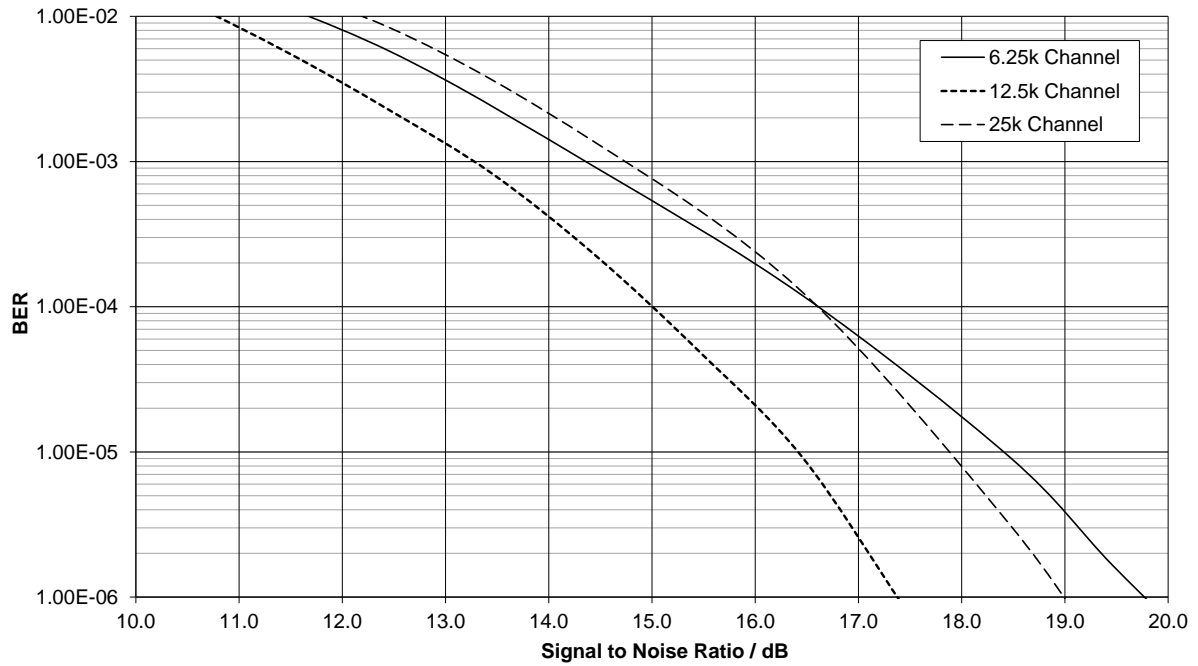
Figure 68 Modem Sensitivity Performance (Root Raised Cosine Pulse Shaping)

The 7164FI-2.x supports pulse shaping filters using an alternative RRC plus sinc filter option. Simply switching from a RRC Only filter to this filter reduces the bandwidth of the modulated signal – so an increased deviation was used to return the Tx ACP to ~63dBc. The graph in Figure 69 compares the performance of a 12.5kHz channel system with and without the sinc filtering included. It can be seen that the sinc filter degrades the sensitivity by less than 0.5dB.
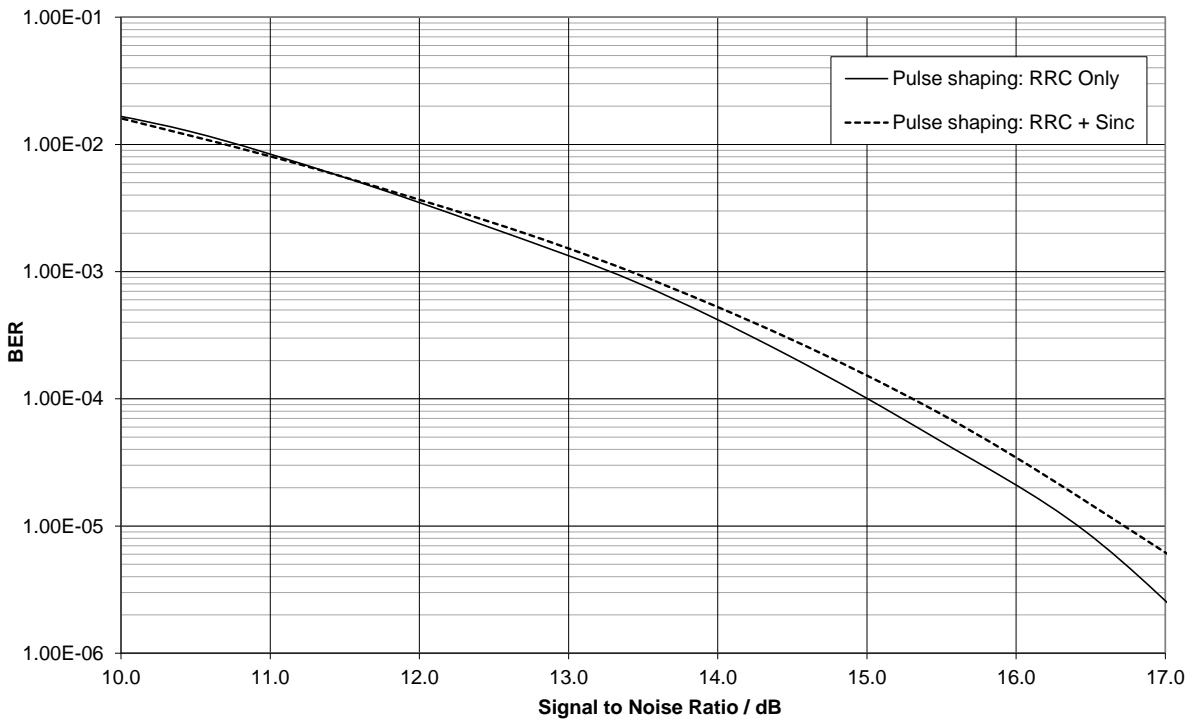
Figure 69 12.5kHz Channel Sensitivity With and Without Sinc Filter Comparison

Data transfer may have channel coding applied to it when 4-FSK modulation is selected. The graph in Figure 70 shows the improvement due to channel coding in the 12.5kHz channel case (4.8ksymbols/s with an RRC only pulse shaping filter).
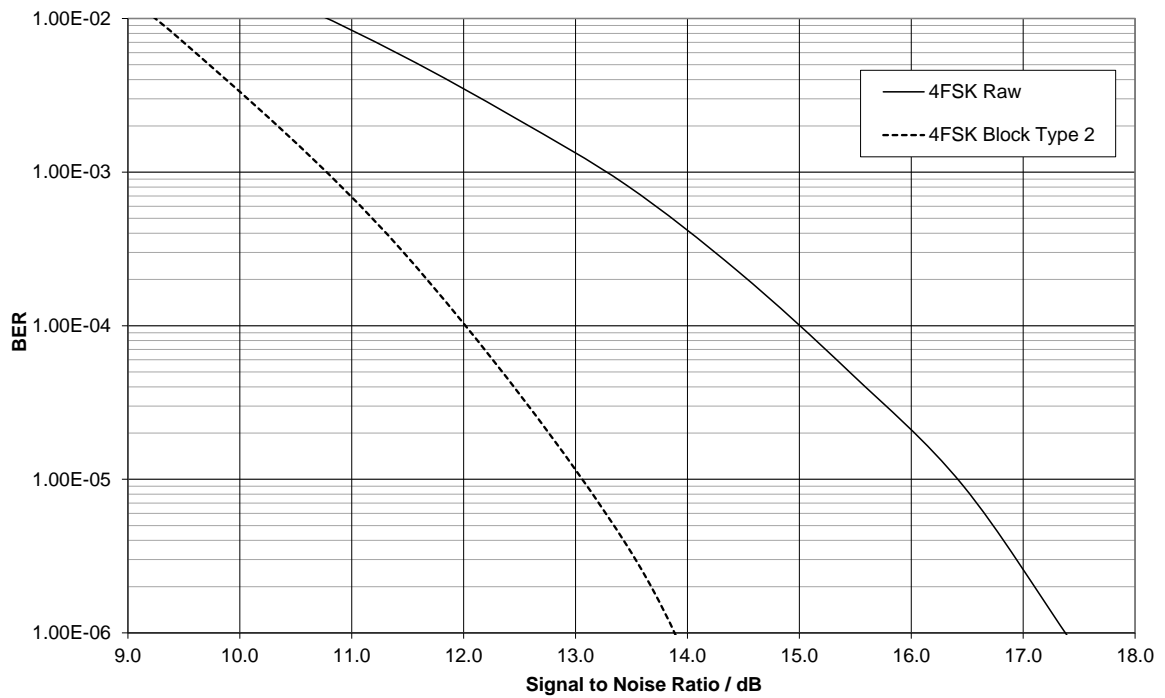
Figure 70 Sensitivity: 12.5kHz Channel, 4.8ksymbols/s With and Without Coding

The co-channel rejection ratio (Figure 71) is measured with an interferer modulated with 400Hz FM and having a deviation of 1.5kHz; which is 12% of the nominal 12.5kHz channel bandwidth. This particular interfering signal is used as it is specified in ETSI standard EN 300 113 for co-channel tests.
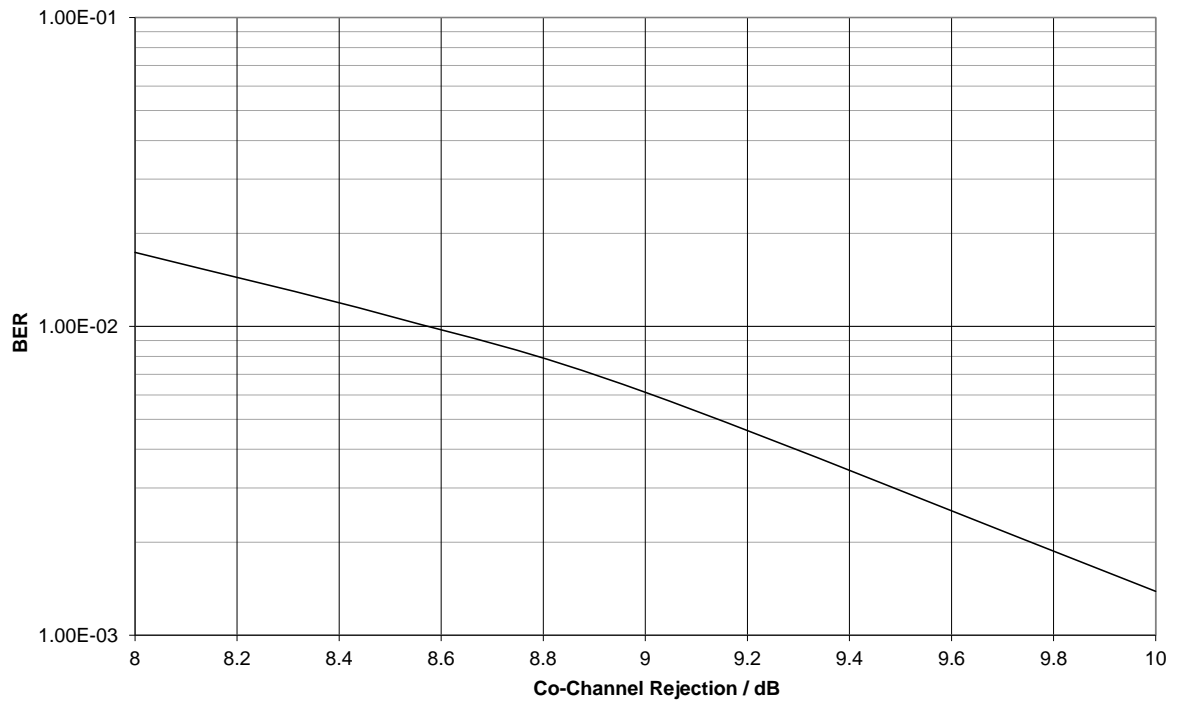
Figure 71 Modem Co-channel Rejection with FM Interferer (as EN 300 113)

9.6.1.2 Adjacent Channel Performance

The 7164 FI-2.x provides excellent rejection of adjacent signals present on the I/Q inputs. Assessment of the adjacent channel rejection (ACR) performance of the modem is normally made in terms of BER or PER for a given ratio between the wanted signal (on channel) and larger interferer on the adjacent channel. Detailed measurement methods vary depending on the standards in use, in particular whether the wanted signal is raised above the sensitivity limit and where the reference is taken. The figures quoted here are based on the measurement method from EN 300 113. The BER curve shown in Figure 72 is based on the difference between the interferer (400Hz FM modulation, 1.5kHz deviation) and the power of the wanted signal for 4.8ksymbols/s.
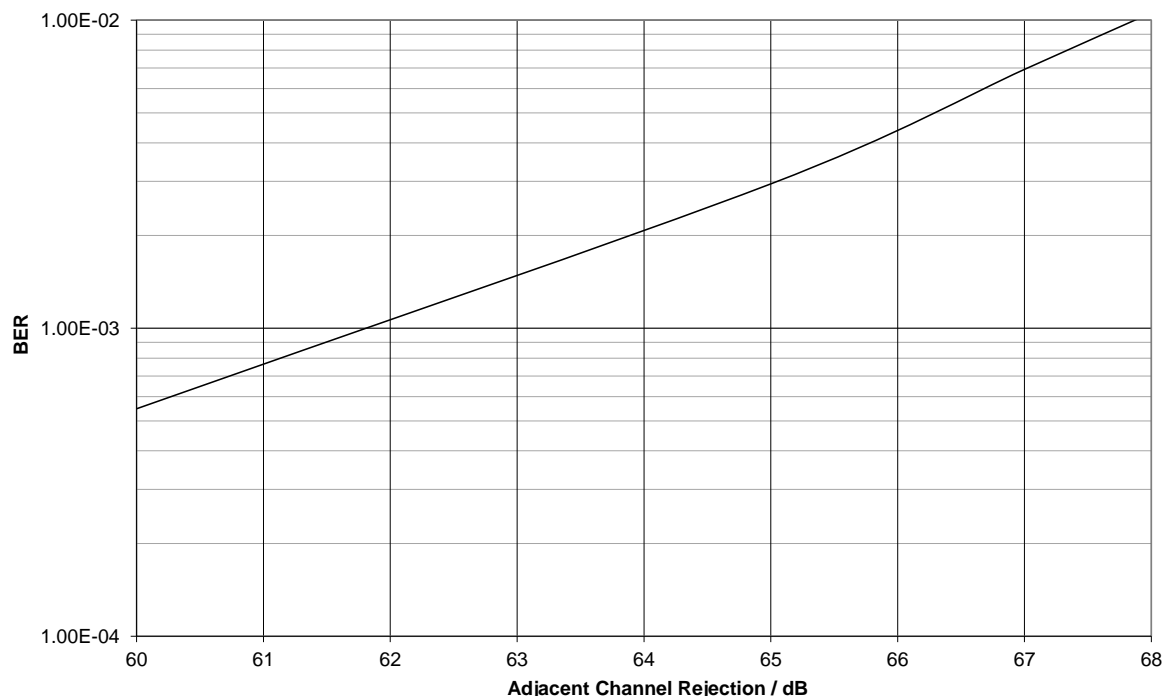
Figure 72 ACR Rejection Performance

The results in Figure 72 are typical of what may be achieved with 7164FI-2.x and a typical I/Q radio receiver with no adjacent channel selectivity in the radio circuits. In a more normal RF architecture, some adjacent channel selectivity will be provided making system results better than the measured values for the 7164FI-2.x alone. Furthermore, the results observed are not necessarily the maximum that the CMX7164 can achieve but are limited by the practical dynamic range of the CMX7164 combined with the system gain and noise figure of the receiver used in these tests.

9.6.2 8-FSK and 16-FSK

9.6.2.1 Signal-to-Noise

It should be noted that error rate performance depends on the modulation type, symbol rate and deviation. In the following graphs the modulation is 4-FSK, 8-FSK and 16-FSK and the data rate is 4.8ksymbols/s, which is typical of the rate that may be achieved in a 12.5kHz RF channel. The signal-to-noise ratio is calculated as:

$$SNR = \text{Mean signal power } -174 + NF + 10 \log_{10}(RxBW)$$

Where:

NF = receiver noise figure in dB
RxBW = receiver noise bandwidth
Mean signal power is in dBm
SNR = Signal-to-Noise Ratio in dB.
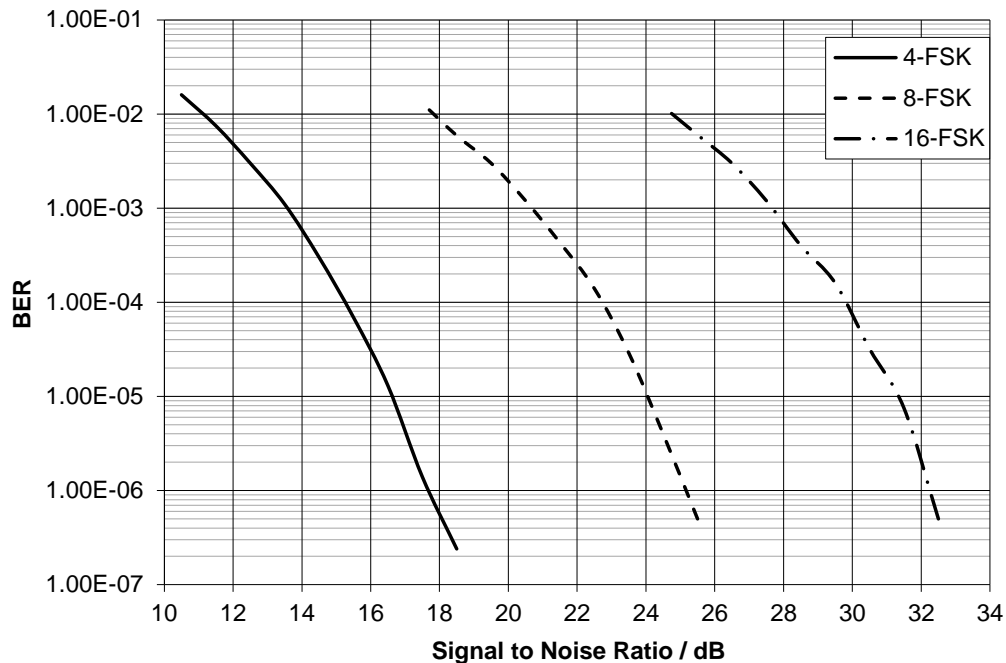
Figure 73 Signal to Noise Performance – Comparison of uncoded (raw) 4-FSK, 8-FSK and 16-FSK

9.6.2.2   Co-channel Performance

The co-channel rejection ratio (Figure 76) is measured with an interferer modulated with 400Hz FM and having a deviation of 1.5kHz; which is 12% of the nominal 12.5kHz channel bandwidth. This particular interfering signal is used as it is specified in ETSI standard EN 300 113 for co-channel tests. The measurement uses wanted signal levels of -95dBm (8-FSK) and -90dBm (16-FSK), as required by EN 300 113.

9.6.2.3   Coding Performance

The performance of the 8-FSK and 16-FSK coding modes is shown in Figure 74 and Figure 75. The high rate coding mode gives adequate performance in a static channel (AWGN) but the low rate code gives much better performance in a faded channel (Figure 75). Best performance, particularly in faded channels, is achieved with the largest block size (block size 3). Typical Block Error Rate with the smallest block size (12 bytes) is shown in Figure 77.
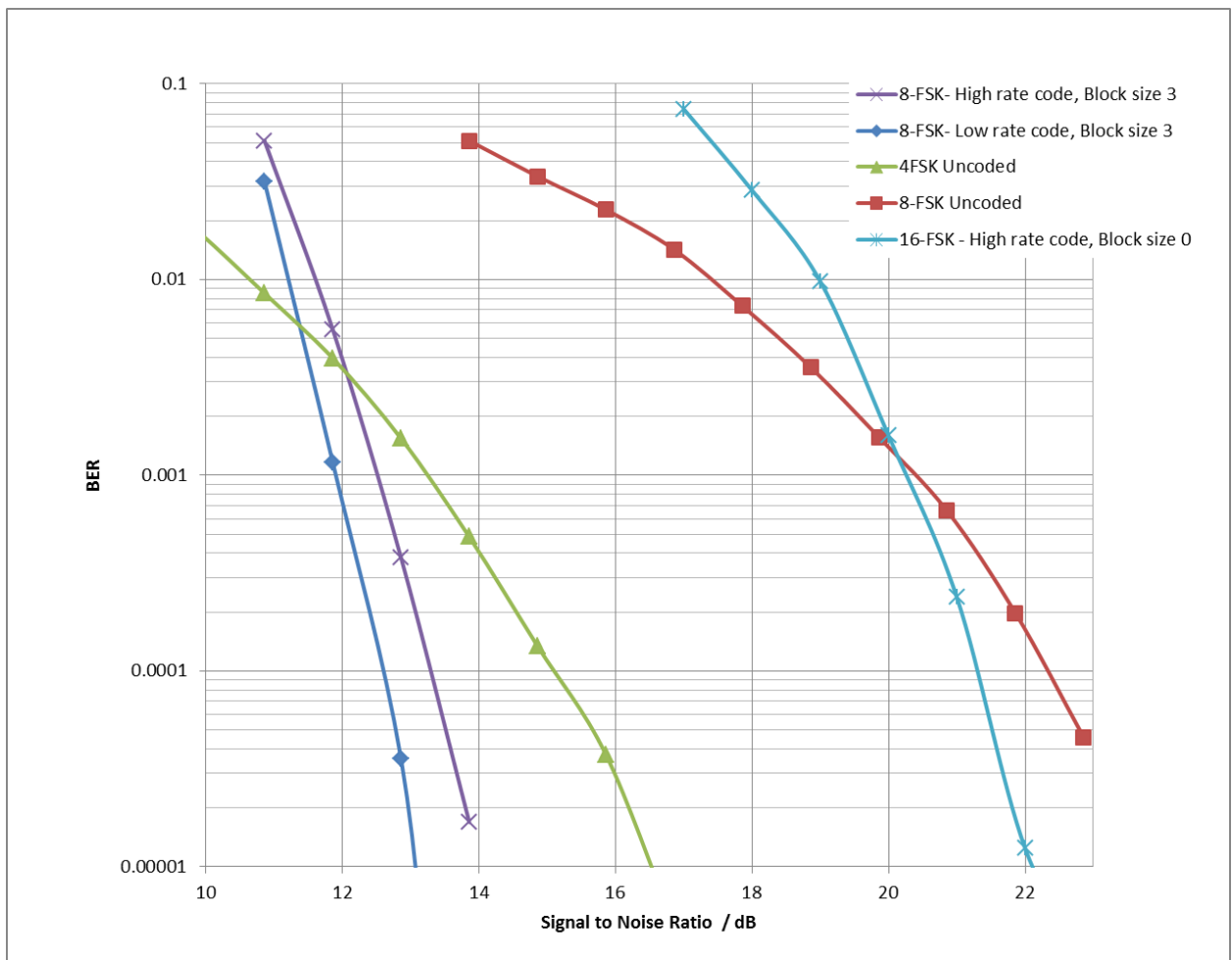
Figure 74 8-FSK and 16-FSK Coding Performance in Static Channel
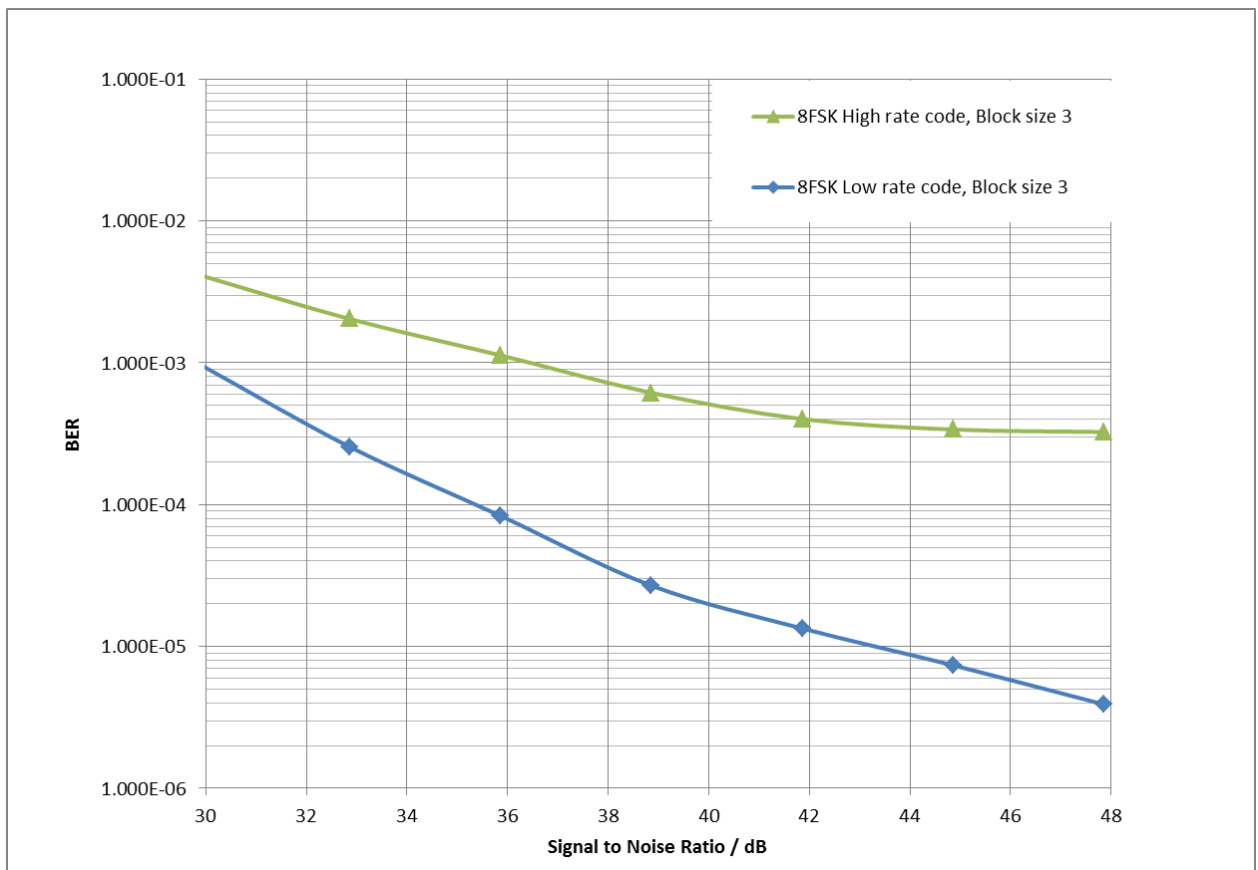
Figure 75 8-FSK Coding Performance in TU50 Fading Channel, 150MHz
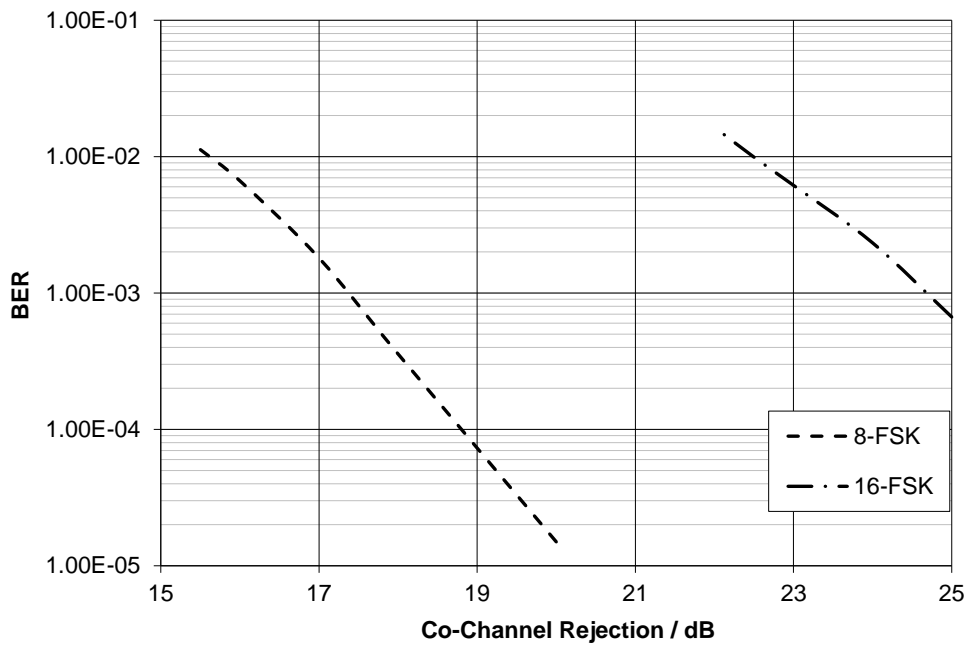
Figure 76 8-FSK and 16-FSK Co-channel Rejection with FM Interferer (as EN 300 113)
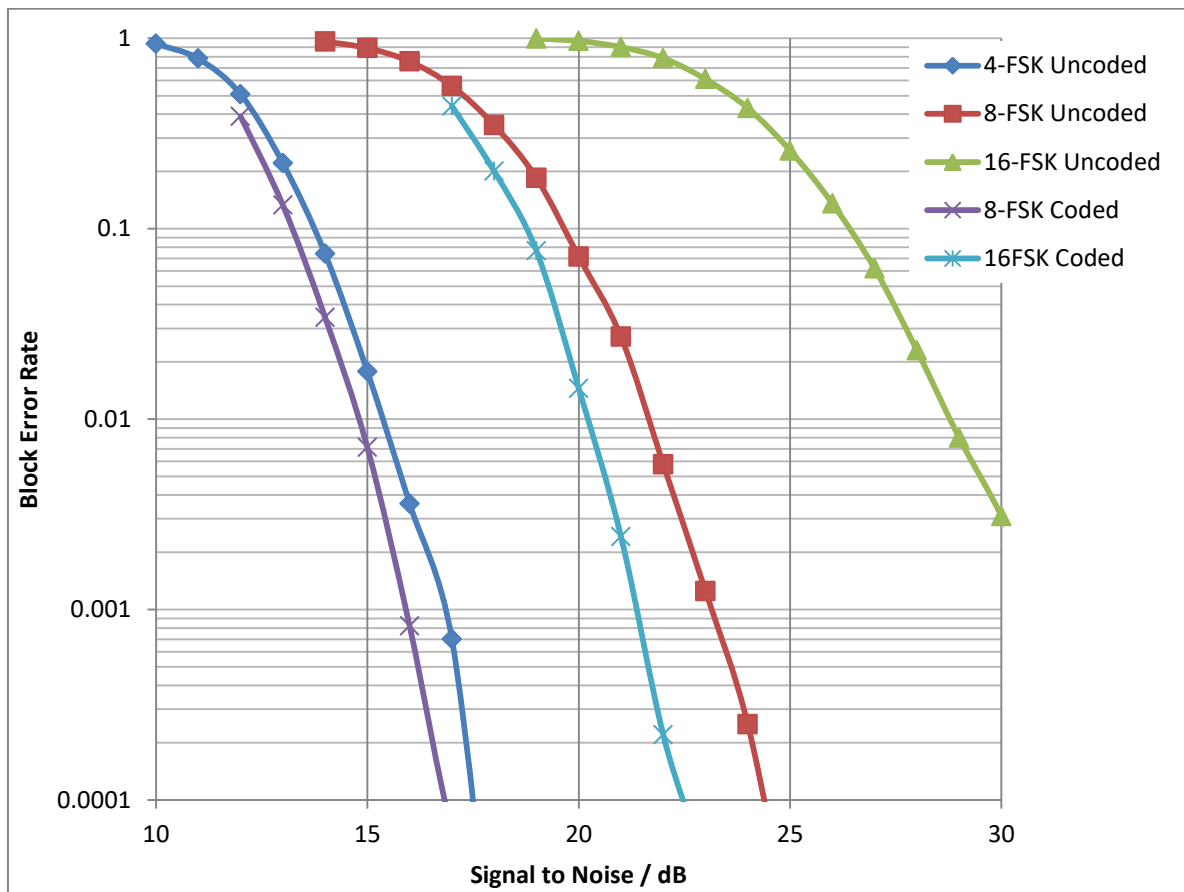
Figure 77 8-FSK and 16-FSK Block Error Rate, Block Size 0, High Rate Code, 12 Byte Blocks of Data in Uncoded Mode

9.6.3   Receiver Dynamic Range

The adjacent channel rejection results in section 9.6.1.2 also indicate that a wanted signal can be successfully received over the dynamic range shown in Figure 72 without any need for an AGC. Note that this is limited at the top end by the maximum allowed signal amplitude into the CMX7164, but performance at the bottom end is affected by noise added by the test receiver – so these figures are not the absolute limit of CMX7164 FI-1.x/2.x/4.x/6.x performance. Results for 8-FSK and 16-FSK operation should be corrected for the different Eb/No of the modulation.

9.6.4   Receiver Response Equaliser Performance

The performance of the 7164FI-2.x when receiving a signal using the EV9942 (CMX994/A/E with temperature compensated baseband filter) is shown in the following graphs. The EV9942 includes a baseband channel filter, the nominal bandwidth of which is 8kHz (-3dB)[8].

The following tests were carried out using a 4.8ksymbols/s, 8-FSK or 16-FSK signal and are representative for a typical 12.5kHz RF channel. Where the results are quoted as using no equalisation the Receiver Response Equaliser was disabled. Where the results are quoted as Equalised the Receiver

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[8] EV9942 with default components fitted and 'Mid' channel bandwidth selected Rx Control Register ($12), b4-b3 = '01'.

Response Equaliser was provided with a training sequence at a level of –70dBm, which produced 400mV (differential) on the I and Q inputs. Equaliser gain was set to 1000 and training lasted for 10000 symbol periods. While training, the received signal had less than 100Hz frequency error. Once trained, the resulting equaliser coefficients were used for the remaining tests.

Firstly the signal-to-noise performance of equalised and non-equalised received signals are compared. The test is similar to that described in 9.6.1.1 Signal-to-Noise and Co-channel Performance.
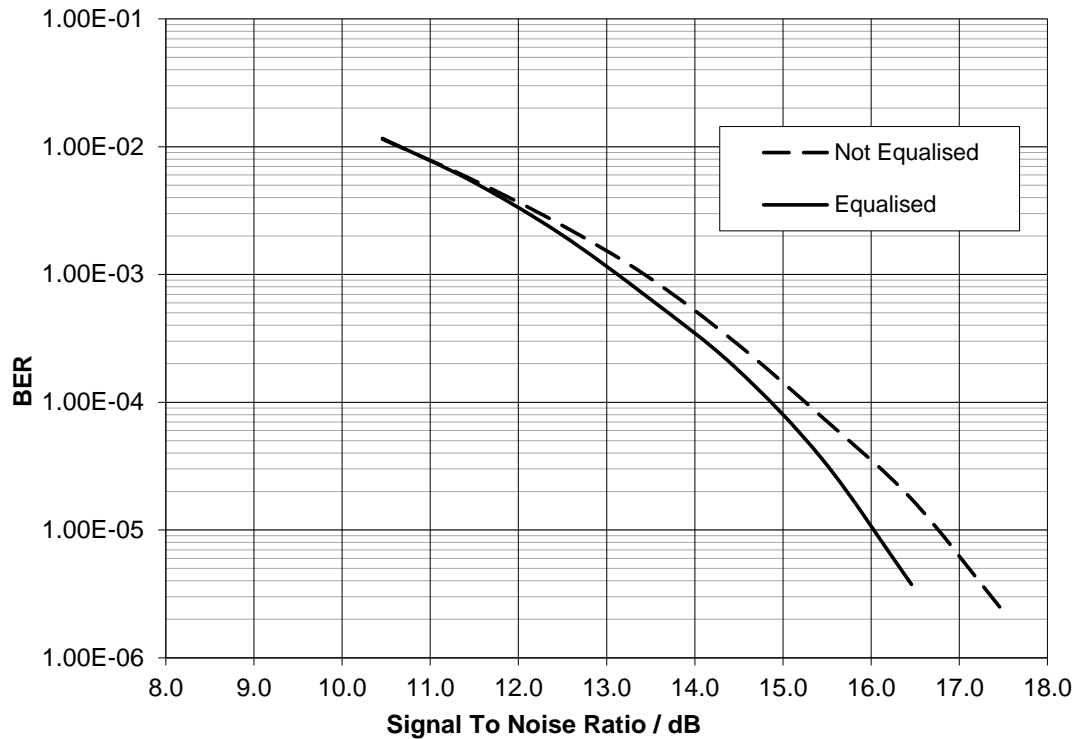
Figure 78 4-FSK Signal-to-Noise Performance, Equalised and Non-Equalised
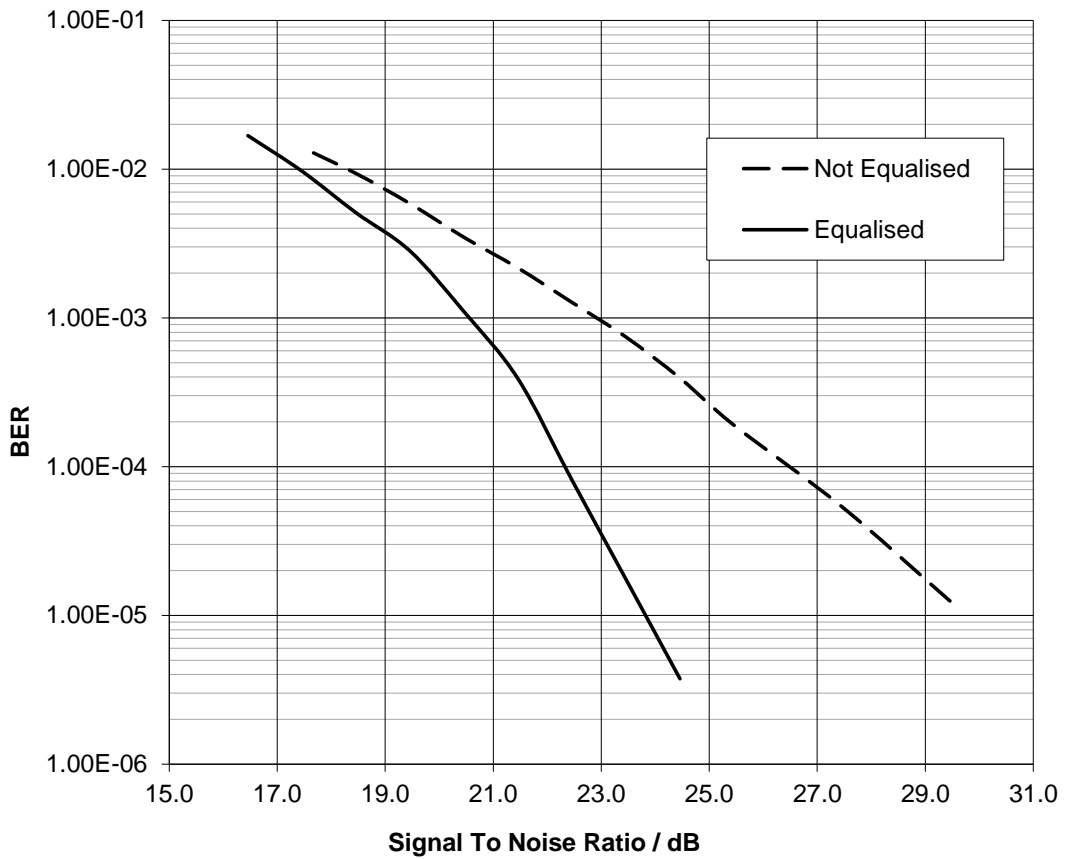
Figure 79 8-FSK Signal-to-Noise Performance, Equalised and Non-Equalised
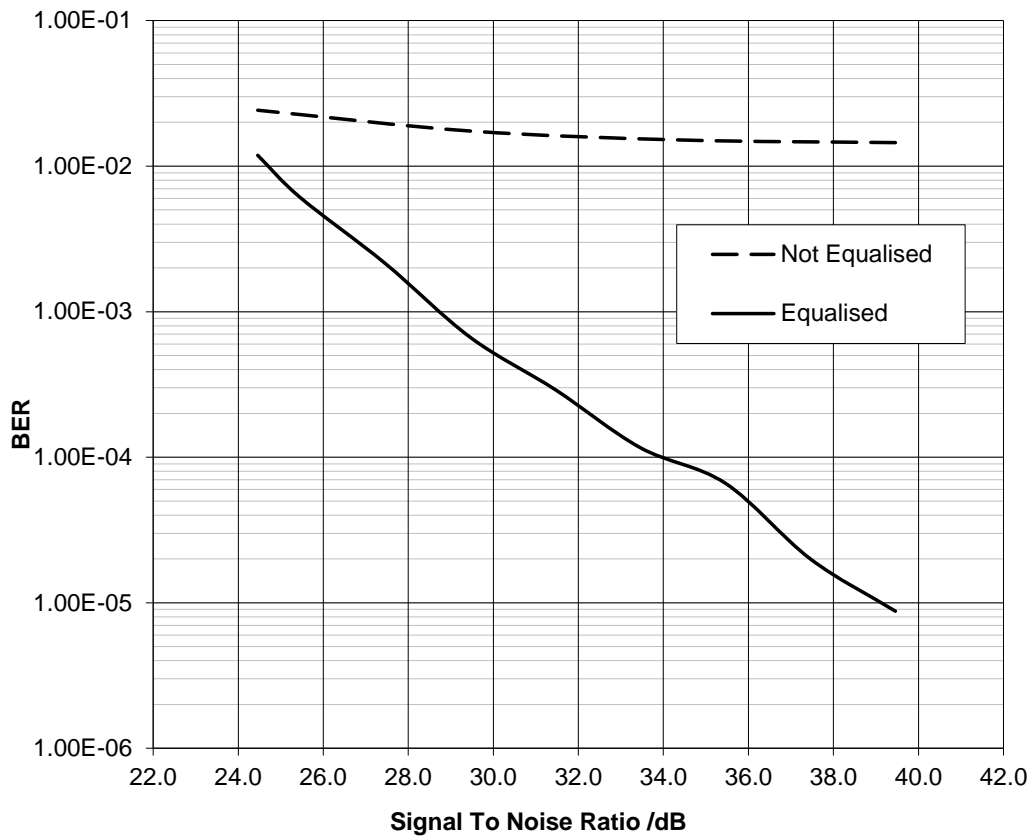
Figure 80 16-FSK Signal-to-Noise Performance, Equalised and Non-Equalised
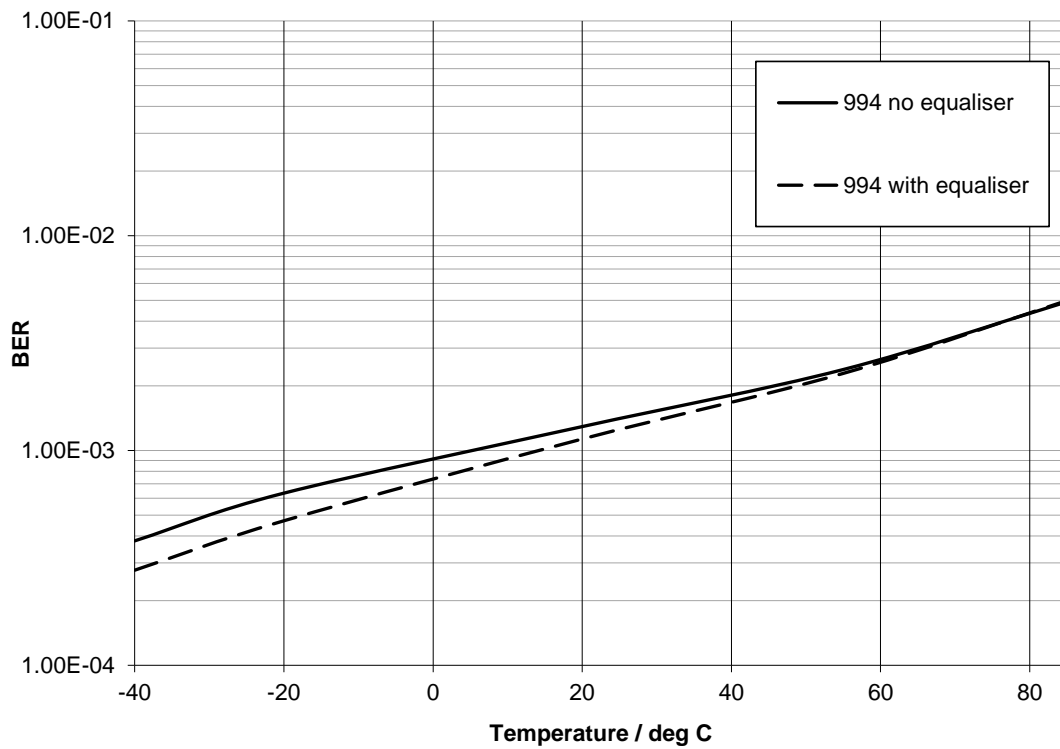
Figure 81 Performance of Equalised Signals with Temperature Variation

Tests were carried out using modulation with a signal to noise ratio of 13dB using the EV9942 (CMX994/A/E with temperature compensated baseband filter). BER performance was measured with and without equalisation being applied then the temperature was varied and the equalised and non-equalised bit error rate measurements repeated. The results are shown in Figure 81. The results show that equaliser performance is maintained across the full operating temperature range. For all results the frequency error between transmitter and receiver was less than 100Hz.

10 7164FI-4.x Features

The 7164FI-4.x uses a QAM modulation scheme, switchable between 4-, 16-, 32- and 64-QAM on a burst by burst basis. The symbol rate is configurable up to 20ksymbols/s resulting in 106 000 user bits per second maximum. Raw data can be transferred, in addition to formatted data blocks. Formatted data blocks may be of variable length – from 15 to 416 bytes and support a combination of 16-bit or 32-bit CRC for error detection, plus error correction.

10.1 7164FI-4.x Modulation

The 7164FI-4.x produces QAM modulation, with four options: 4-, 16-, 32- or 64-QAM, see Figure 82. In each case, the signal is Root Raised Cosine filtered. The same filter is applied in receive to remove inter-symbol interference. Due to the way the signal is produced, there is no deviation to select, instead only the baud rate may be altered. This has a direct effect on the signal bandwidth. A baud rate of 18ksymbols/s is typical of a 25kHz channel spacing and provides:

QAM Variant	Bits per Symbol	Base Over-air Bit Rate (18ksymbols/s)	Raw Mode Over-air Bit Rate (18ksymbols/s)
4-QAM	2	36kbps	32kbps
16-QAM	4	72kbps	64kbps
32-QAM	5	90kbps	80kbps
64-QAM	6	108kbps	96kbps

Q

01   00

4-QAM

Q

0111   0110   0010   0011

0101   0100   0000   0001

                                    I

1101   1100   1000   1001

11   10   1111   1110   1010   1011

16-QAM

Q

01111 01011 00011 00111

01110 01100 01101 00101 00100 00110

01010 01000 01001 00001 00000 00010   I

11010 11000 11001 10001 10000 10010

11110 11100 11101 10101 10100 10110

11111 11011 10011 10111

32-QAM

Q

101111 101101 100101 100111 000111 000101 001101 001111

101110 101100 100100 100110 000110 000100 001100 001110

101010 101000 100000 100010 000010 000000 001000 001010

101011 101001 100001 100011 000011 000001 001001 001011   I

111011 111001 110001 110011 010011 010001 011001 011011

111010 111000 110000 110010 010010 010000 011000 011010

111110 111100 110100 110110 010110 010100 011100 011110

111111 111101 110101 110111 010111 010101 011101 011111

64-QAM

Figure 82 QAM Mappings

The signal spectrum is identical in bandwidth when using 4-, 16-, 32- or 64-QAM, however the peak-to-mean of each modulation type does vary

4-QAM has a peak to mean of   5.2dB (α=0.2) or 3.8dB (α=0.35)
16-QAM has a peak to mean of 6.8dB (α=0.2) or 5.8dB (α=0.35)
32-QAM has a peak to mean of 7.3dB (α=0.2) or 6.4dB (α=0.35)
64-QAM has a peak to mean of 7.3dB (α=0.2) or 6.3dB (α=0.35)

Note: peak to mean figures are the measured crest factor for the specified modulation with PRBS test modes (PN9) i.e. register $6B set to $0032.

The difference between the base over air rate and the raw mode rate (which is the actual user data rate in raw mode at 18ksymbols/s) is due to some symbols being used internally by the modem to perform channel equalisation. A further implication of this is that any transmission must contain a multiple of 16 symbols, the CMX7164 will automatically pad as necessary.

10.2 7164FI-4.x Radio Interface

QAM modulation requires control of both phase and amplitude in the transmitter, and to measure both phase and amplitude in the receiver. Therefore the 7164FI-4.x offers I/Q transmit and I/Q receive interfaces. This is shown in Figure 83, using the CMX992[9] for reception and the CMX998[10] for transmit – with RF power amplifier linearisation. The internal functions of the CMX7164 when operating in this mode are shown in Figure 2.
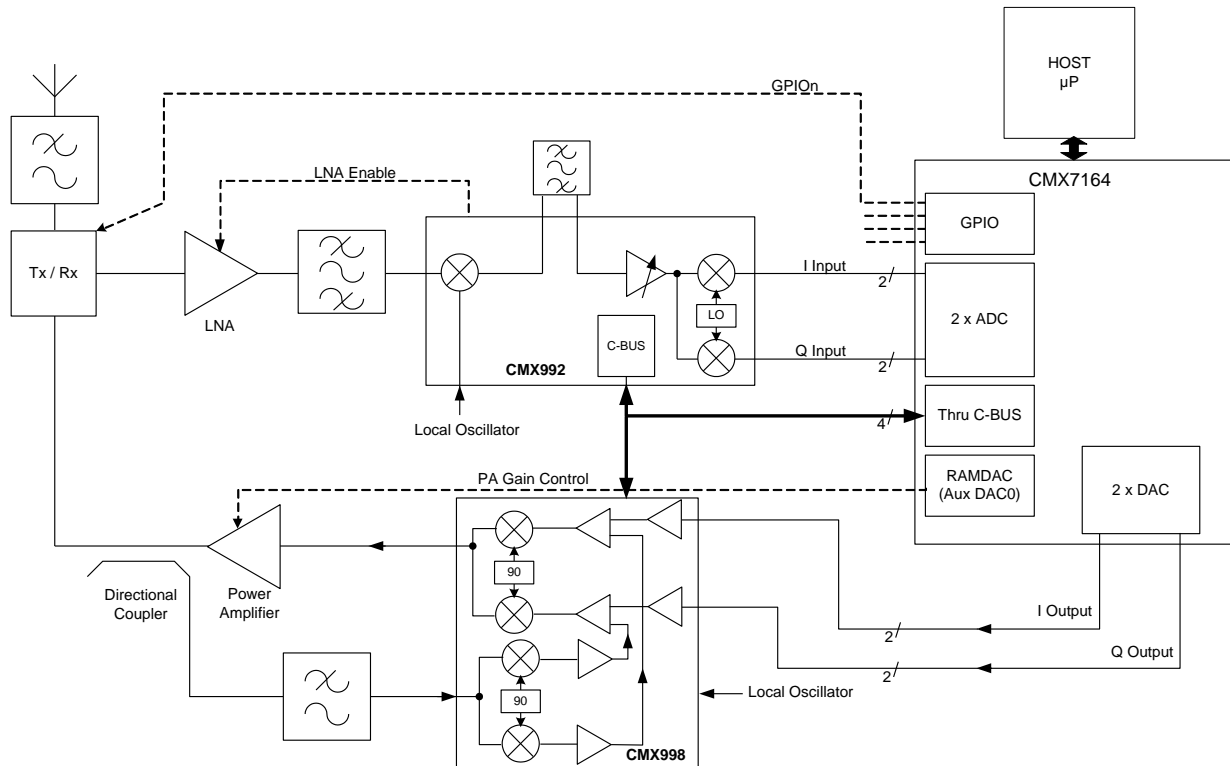
Figure 83 Outline Radio Design (I/Q in/out for QAM)

Use of I/Q receive mode brings with it the problem of I/Q dc offsets. There are dc offsets caused by the radio receiver – resulting in the signal into the CMX7164 having a dc offset other than V_{BIAS}. The offset needs to be removed prior to demodulation. Offsets typically remain constant for a particular radio frequency selected, but will vary if that frequency is changed. Gain within the radio receiver may also affect the dc offset seen by the CMX7164.

I/Q dc offset effects are a radio issue which is beyond the control of the CMX7164. However the CMX7164 does provide dc offset calculation and removal. These are described in detail in the application note section 14.3 DC Offsets in I/Q Receivers.

10.2.1 Control interfaces

As can be seen in Figure 83, the CMX7164 provides control interfaces to assist with controlling the radio transmitter and receiver. These include:

- A SPI Thru-Port– port which may be used to control radio ICs with C-BUS/SPI interfaces
- A RAMDAC which can be used to control PA ramp up and ramp down

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[9] CMX992 is an RF Quadrature/IF Receiver
[10] CMX998 is a Cartesian Feedback Loop Transmitter

- Four GPIO pins which may be used for Tx/Rx switching, LNA off and general device control.

10.3 7164FI-4.x Formatted Data

The 7164FI-4.x supports formatted data, which provides the ability to channel code blocks of data using a variety of coding rates and CRCs. A frame structure would typically consist of a 24-symbol frame sync pattern followed by a 'Header Block', one or more 'Intermediate Blocks and a 'Last Block'.

The 'Header' block is self-contained in that it includes its own checksum (CRC1), and would normally carry information such as the address of the calling and called parties, the number of following blocks in the frame (if any) and miscellaneous control information.

The 'Intermediate' block(s) contain only data, the checksum at the end of the 'Last' block (CRC2) also checks the data in any preceding 'Intermediate' blocks. This checksum calculation should be reset as required using the "Reset CRC2" block type – so that any transmitted CRC2 contains the CRC of only the desired blocks. In receive it must be reset to match the expected input data block sequence.

A variety of different frame formats are possible, some examples are illustrated in Figure 84.

Figure 84 Suggested Frame Structures

The CMX7164 performs all of the block formatting and de-formatting. When receiving header blocks and last blocks the CMX7164 will indicate CRC success or failure and will provide the data regardless. The size of the data block can be varied, as can the coding rate applied. A lower coding rate (more FEC bits) will improve performance in noisy or faded conditions but will reduce the user data rate available. Small data blocks provide the ability to produce a short burst or granularity in burst size. However to cope with fading conditions longer coded blocks are necessary. The 7164FI-4.x provides blocks with the following predefined formatted block sizes/rates:

Table 6 Formatted Block Types, Sizes and Rates (FI-4.x)

Block Type Code (b11-8)	Inter. Block size in bytes	Header block size (16-bit CRC)	Last block size (32-bit CRC)	Coding Rate (4,16-QAM)	Coding Rate (32-QAM)	Coding Rate (64-QAM)
0	15	13 (2)	11 (4)	0.75	0.8	0.83
1	60	58 (2)	56 (4)	0.75	0.8	0.83
2	33	31 (2)	29 (4)	0.55	0.57	0.61
3	37	35 (2)	33 (4)	0.62	0.64	0.69
4	44	42 (2)	40 (4)	0.55	0.58	0.61
5	176	174 (2)	172 (4)	0.55	0.58	0.61
6	73	71 (2)	69 (4)	0.52	0.55	0.58
7	292	290 (2)	288 (4)	0.52	0.55	0.58
8	88	86 (2)	84 (4)	0.55	0.58	0.61
9	352	350 (2)	348 (4)	0.55	0.58	0.61
10	104	102 (2)	100 (4)	0.65	0.69	0.72
11	416	414 (2)	412 (4)	0.65	0.69	0.72

User defined block sizes and coding rates can be set using Program Block 12 – see section 13.2.13.

10.4 7164FI-4.x Receiver Response Equaliser

When receiving signals using a radio receiver the signal provided to the CMX7164 is likely to be distorted. Considering the architecture of Figure 83 as typical, the distortion will largely be caused by the crystal filter – shown as a bandpass filter in the diagram. The crystal filter operates on the received signal at an intermediate frequency, its purpose is to attenuate unwanted signals such as those on adjacent channels before they get to the CMX7164.[11]

Typically the pass band of the crystal filter is not flat or perfectly linear phase, resulting in the wanted QAM signal being distorted due to the amplitude/phase response of the filter. The result is usually a significantly degraded receive signal and therefore poor receive performance.

Other radio architectures may provide baseband filtering in order to help reject unwanted adjacent channel signals. Such filtering may also have a pass band that is not flat, and therefore will degrade reception.

The CMX7164 provides a Receiver Response Equaliser that will compensate for the group delay and variation in gain of the crystal filter, or any other distortions present in the received signal. The equaliser must be trained with a clean, high level 4-QAM signal in order to establish the receiver response and produce a filter which compensates for it. Once this filter is calculated it may be read from the CMX7164 and stored for later use. The CMX7164 can be configured with up to two previously stored Receiver Response Equaliser filters which may, for example be used to compensate for two different crystal filters in a radio designed to receive in two channel bandwidths.

Although trained using a 4-QAM signal the resulting filter is suitable to compensate for the receiver response whilst receiving 4, 16, 32 or 64-QAM signals. A suitable training signal may either be produced using another CMX7164 or the training sequence described in section 14.9 FI-4.x Receiver Response Equaliser Training Sequence.

The Receiver Response Equaliser has two modes, single mode produces better results when correcting for receivers with a simple baseband roll off (for example in a direct conversion architecture). Dual mode produces better results when compensating for a radio receiver which includes a crystal filter. Program Block 11 – Receiver Response Equaliser (FI-2.x and FI-4.x) provides equaliser mode selection, allows adjustment of the gain used in the feedback path when training the equaliser and allows the training time to be altered. The same Program Block allows the filter resulting from training to be read for storage and to be programmed back in to the CMX7164 later for use when receiving.

An example of the effect of the receiver crystal filter on a 4 and 16-QAM signals is shown in Figure 85. Once the equaliser has been trained the resulting received signal was as shown in Figure 86. Each plot is gathered by using the Rx diagnostics mode of the 7164FI-4.x, see section 7.4.12 Other Modem Modes for details.

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[11] Note that the CMX7164 provides significant channel filtering itself, but further rejection of unwanted signals is desirable in most applications to improve receiver dynamic range and prevent blocking or products generating intermodulation products reaching the low power 'back-end' of the receiver.
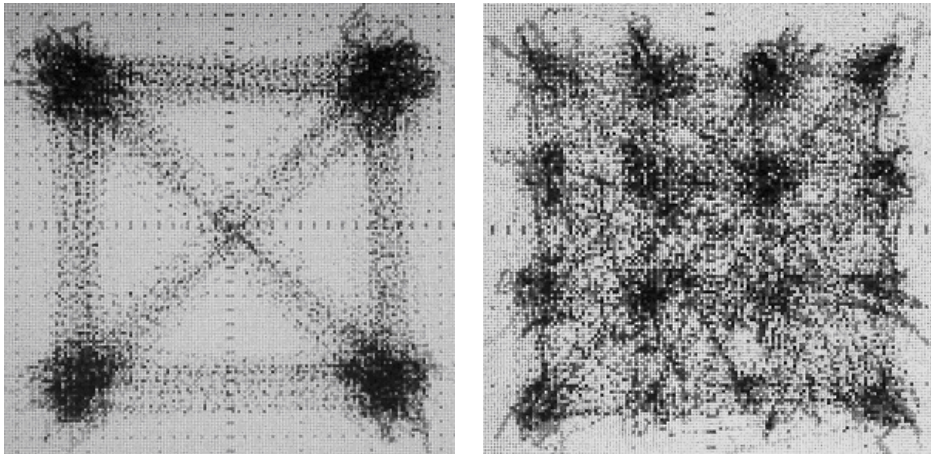
Figure 85 Received 4 and 16-QAM signals, no equalisation
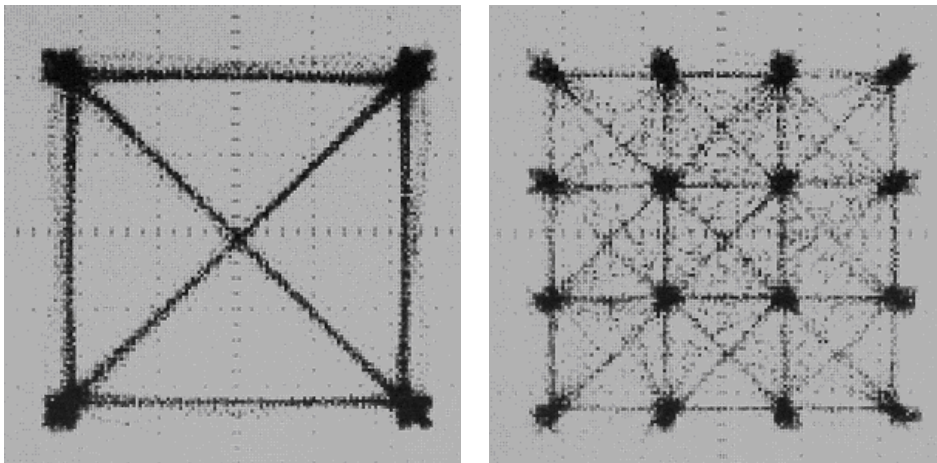
Figure 86 Received 4 and 16-QAM signals with equalisation

Results when using the Receiver Response Equaliser are shown in section 10.6.4 Receiver Response Equaliser Performance.

See:
- 13.1.19 Modem Mode and Control - $6B write
- 13.2.13 Program Block 11 – Receiver Response Equaliser (FI-2.x and FI-4.x)
- 14.9 FI-4.x Receiver Response Equaliser Training Sequence

10.5 7164FI-4.x Typical Transmit Performance

The 7164FI-4.x transmits QAM modulation using an I/Q interface. The modulation may be evaluated using a test system as illustrated in Figure 87 Tx Spectrum and Modulation Measurement Configuration for I/Q Operation.
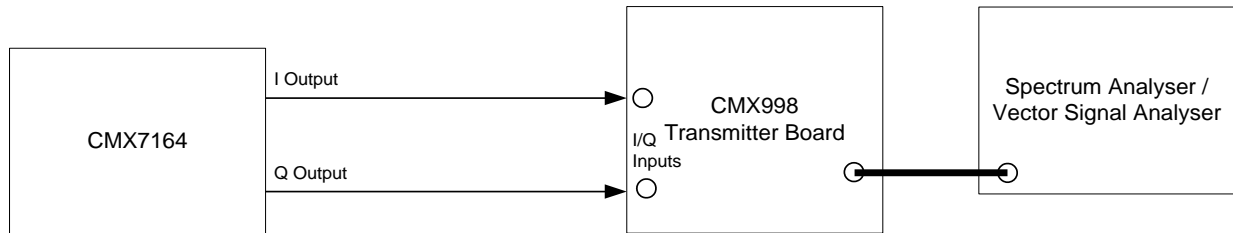
Figure 87 Tx Spectrum and Modulation Measurement Configuration for I/Q Operation

Some typical results are shown in the following figures. The internal PRBS generator was used to generate the data in all the results shown. Two baud rates are demonstrated – 18ksymbols/s which is typical of a 25kHz channel and 9ksymbols/s which is typical of a 12.5kHz channel. In all cases the transmit filter selected had α=0.2. Depending on transmitter requirements (e.g. applicable standards) faster baud rates may be possible.
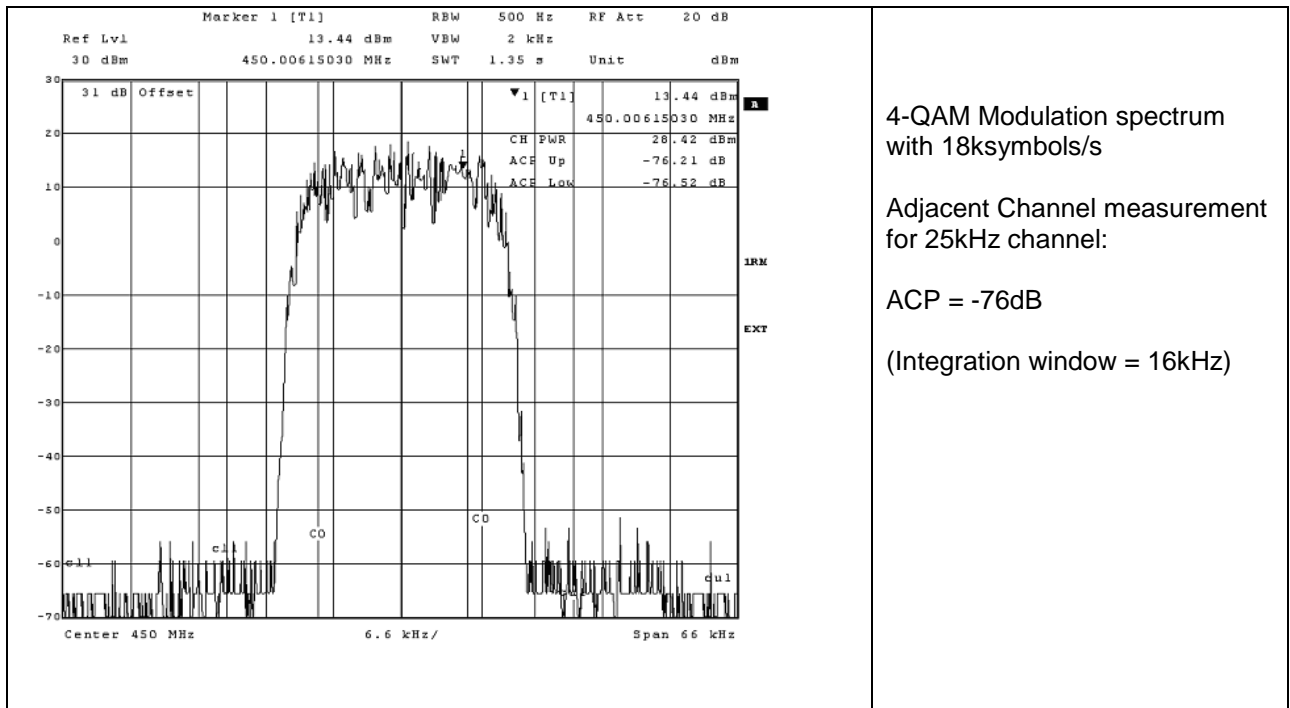
4-QAM Modulation spectrum with 18ksymbols/s

Adjacent Channel measurement for 25kHz channel:

ACP = -76dB

(Integration window = 16kHz)
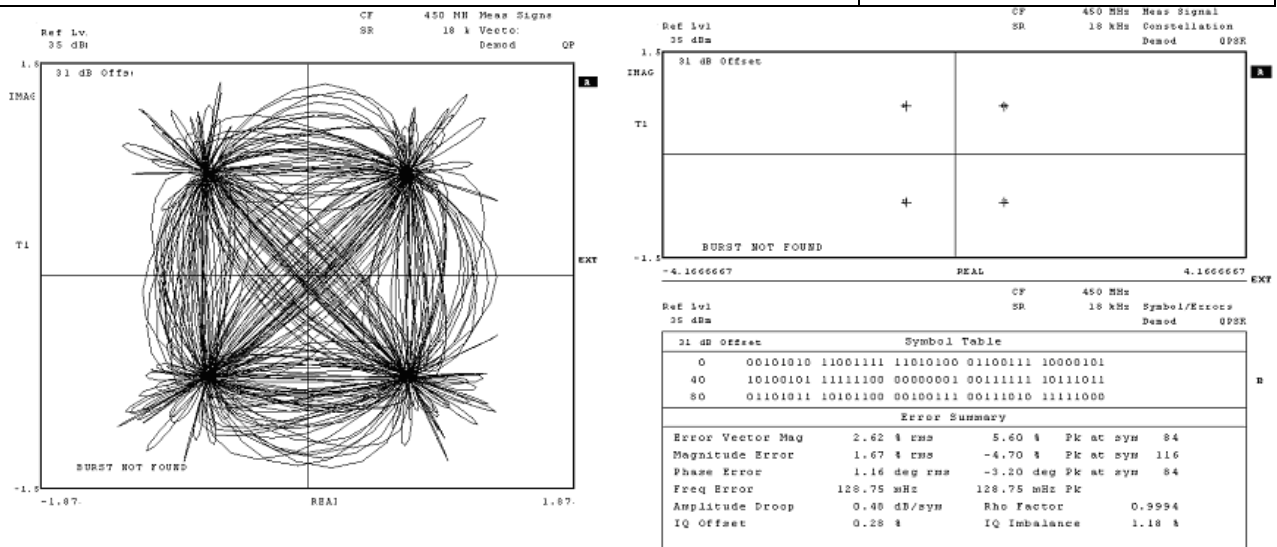
Constellation Diagram (Receiver filtered)   Error Vector

Figure 88 Tx Modulation Spectra (4-QAM), 18ksymbols/s I/Q Modulation into CMX998
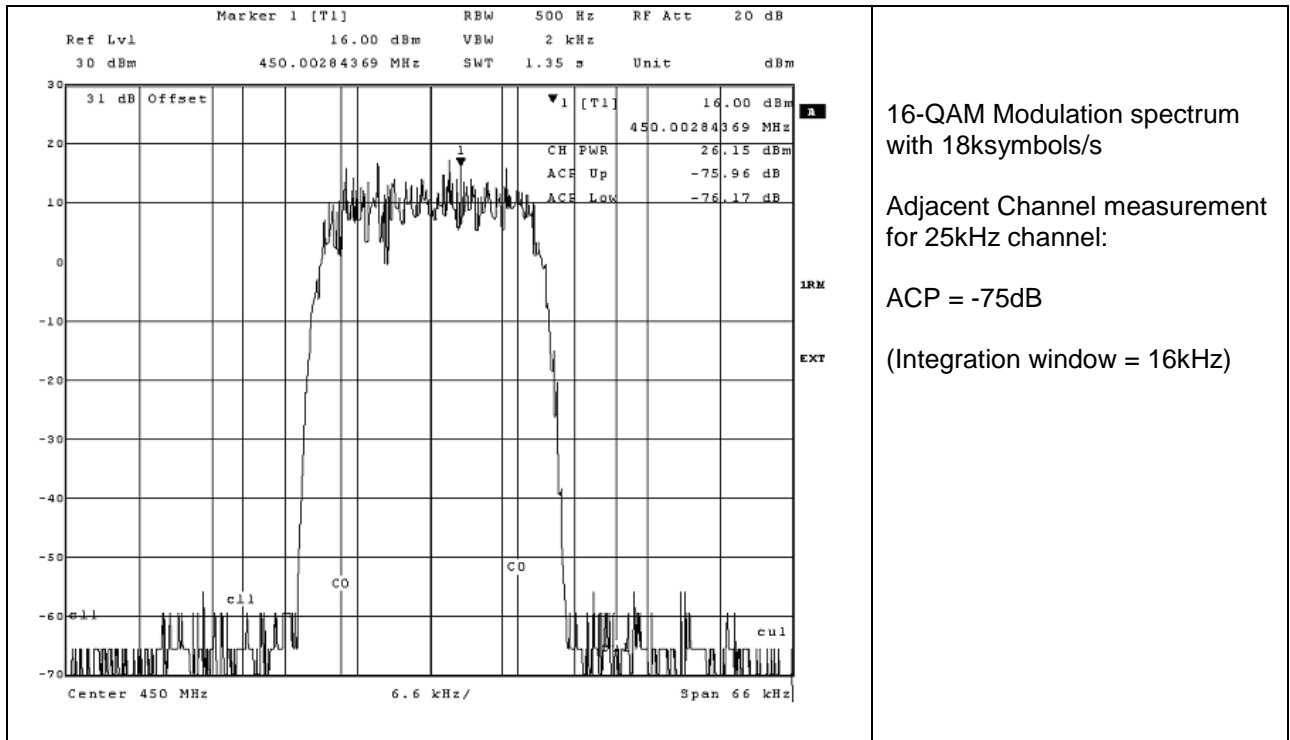
16-QAM Modulation spectrum with 18ksymbols/s

Adjacent Channel measurement for 25kHz channel:

ACP = -75dB

(Integration window = 16kHz)
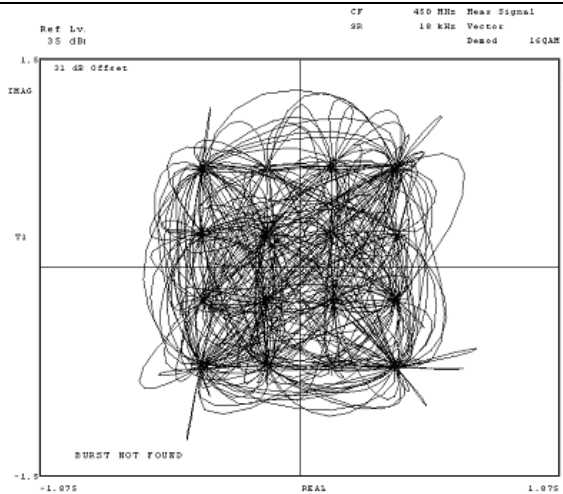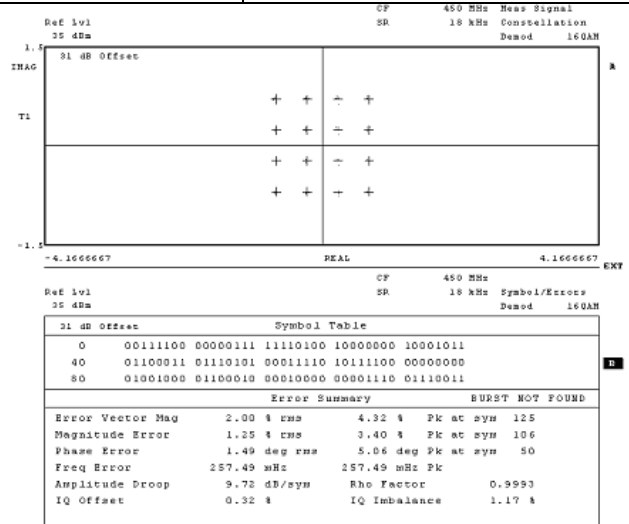
Constellation Diagram (Receiver filtered)   Error Vector

Figure 89 Tx Modulation Spectra (16-QAM), 18ksymbols/s I/Q Modulation into CMX998
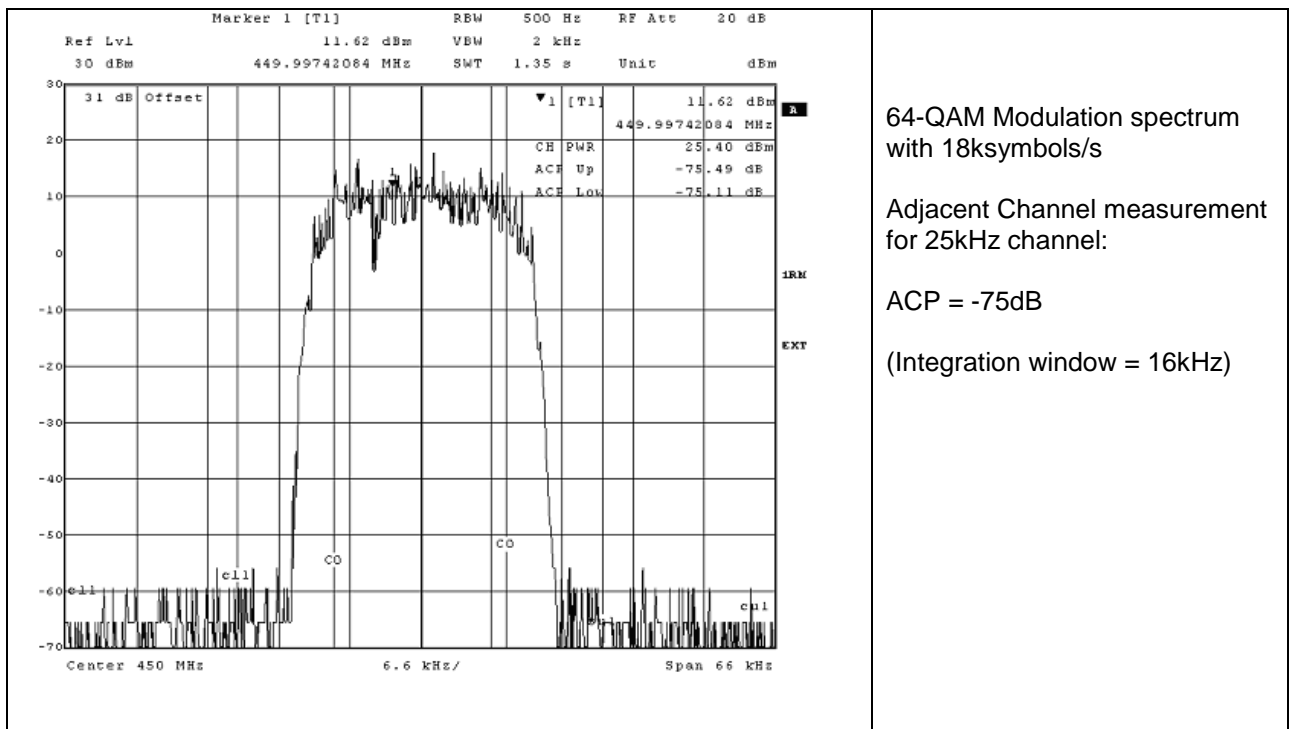
64-QAM Modulation spectrum with 18ksymbols/s

Adjacent Channel measurement for 25kHz channel:

ACP = -75dB

(Integration window = 16kHz)

Figure 90 Tx Modulation Spectra (64-QAM), 18ksymbols/s I/Q Modulation into CMX998

For a particular baud rate we can see that the spectral shape, and adjacent channel power measurements for each QAM type are almost identical. This is to be expected, as each is generated using the same filters. The average power generated will vary though, as each type of QAM used has a different peak–to-mean ratio and the CMX7164 transmits each with the same peak power.

16-QAM Modulation spectrum with 9ksymbols/s

Adjacent Channel measurement for 12.5kHz channel:

ACP = -76dB

(Integration window = 8kHz)
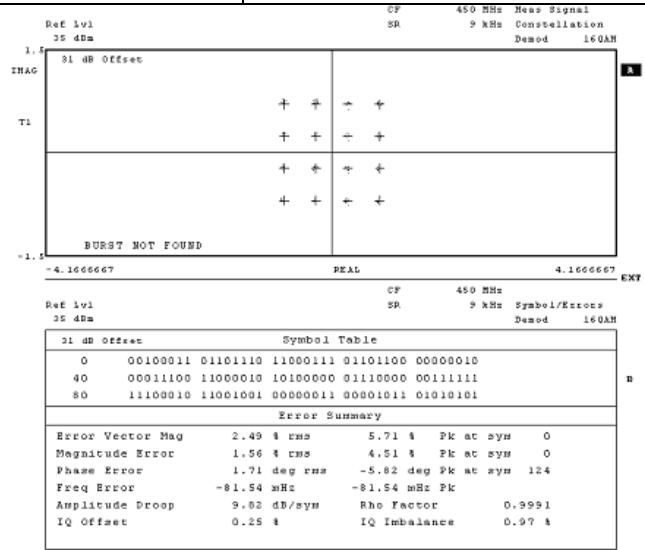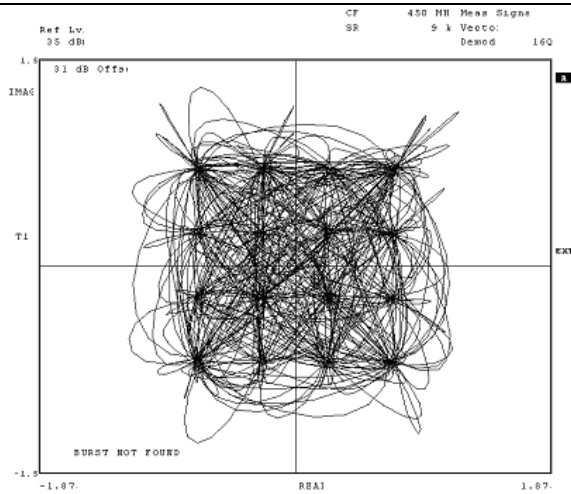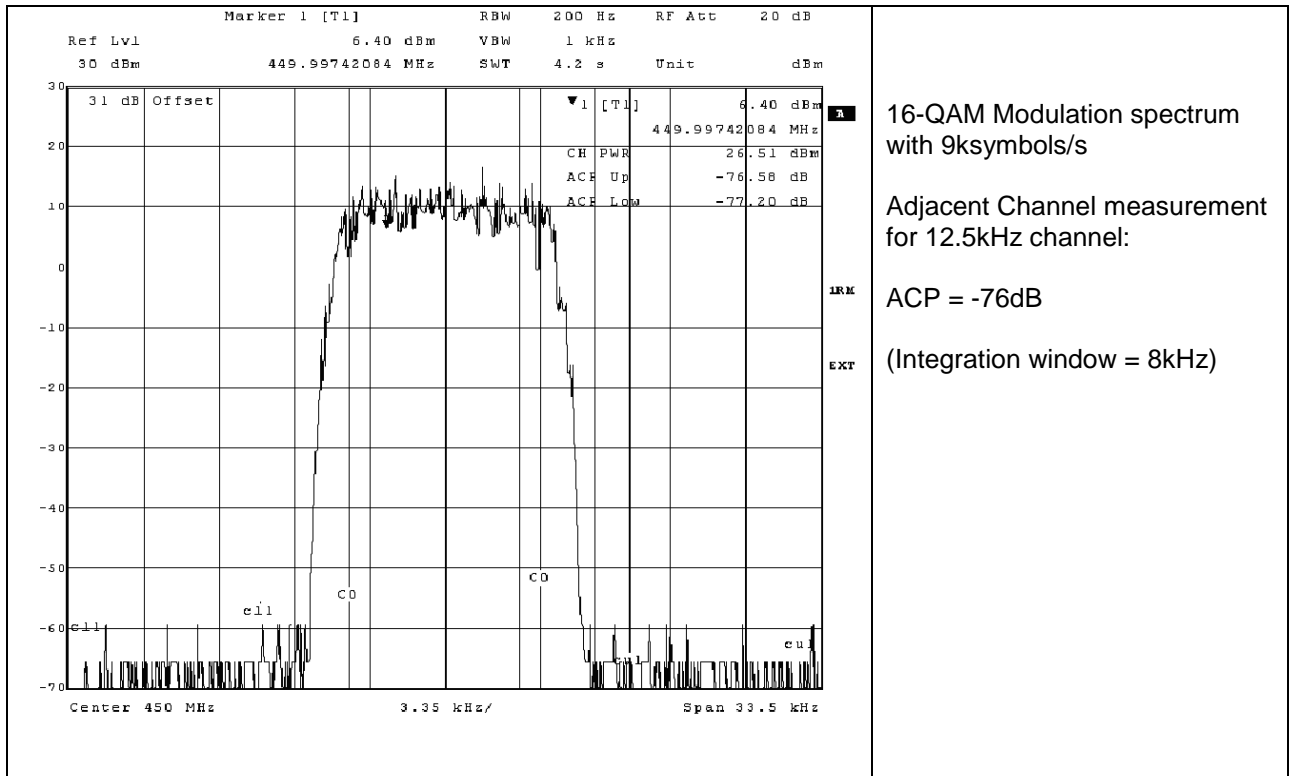
Constellation Diagram (Receiver filtered)   Error Vector

Figure 91 Tx Modulation Spectra (16-QAM), 9ksymbols/s I/Q Modulation into CMX998

Comparing Figure 89 and Figure 91 demonstrates that changing baud rate simply scales the transmitted spectrum – halving baud rate will halve the bandwidth occupied. This relationship can be used to select the maximum baud rate for a given channel bandwidth.

10.6 7164FI-4.x Typical Receive Performance

10.6.1   Signal-to-Noise and Co-channel Performance
The performance of the 7164FI-4.x when receiving is shown in the following graphs. It should be noted that error rate performance depends on the modulation rate; whether 4-QAM, 16-QAM, 32-QAM or 64-QAM is in use; the coding type selected and the block size. The 7164FI-4.x supports multiple combinations of these factors and it is beyond the scope of this document to provide data for every combination, however graphs are provided showing a selection of representative cases ranging from best case performance (maximum coding and block size) to worst case where no coding is used (raw mode). Formatted block types 0, 6 and 7 (see Table 6 and section 10.3 7164FI-4.x Formatted Data, for details) show different levels of error correction performance, formatted block type 7 giving the best performance (see Table 6).

In all of the following graphs (Figure 92 - Figure 101) the data rate is 18ksymbols/s, which is typical of the rate that may be achieved in a 25kHz RF channel. The selected transmit and receive filters had α=0.2. The signal-to-noise ratio is calculated as:

> SNR = Mean signal power -174 + NF + 10 $\log_{10}$(RxBW)

Where:

> NF = receiver noise figure in dB
> RxBW = receiver noise bandwidth, which in Figure 92 - Figure 101 is 18kHz
> Mean signal power is in dBm
> SNR = Signal-to-Noise Ratio in dB.

Note that the curves shown do not use the equaliser function but assume that the signal path filtering achieves a flat pass-band response. Note also that 32-QAM operation has been added to 7164FI-4.x after initial product launch so the 32-QAM data was measured at a different time to the other modulations - this may give rise to minor variations in the relative performance.
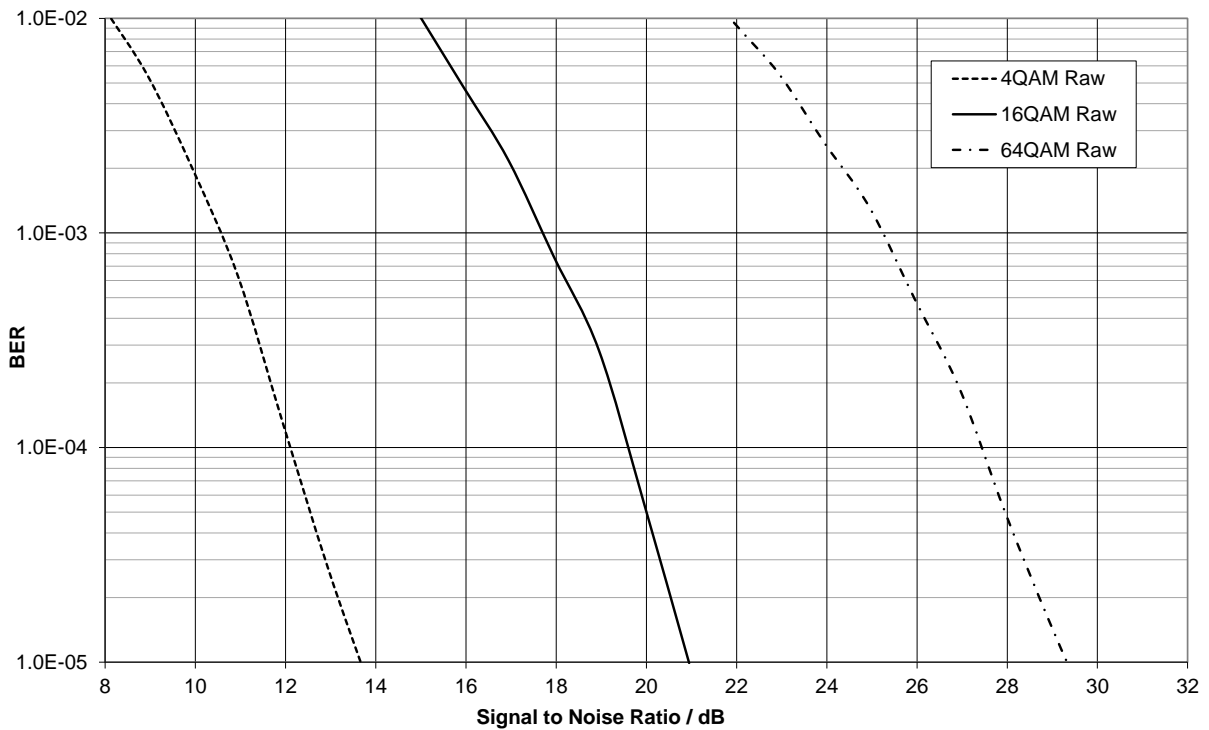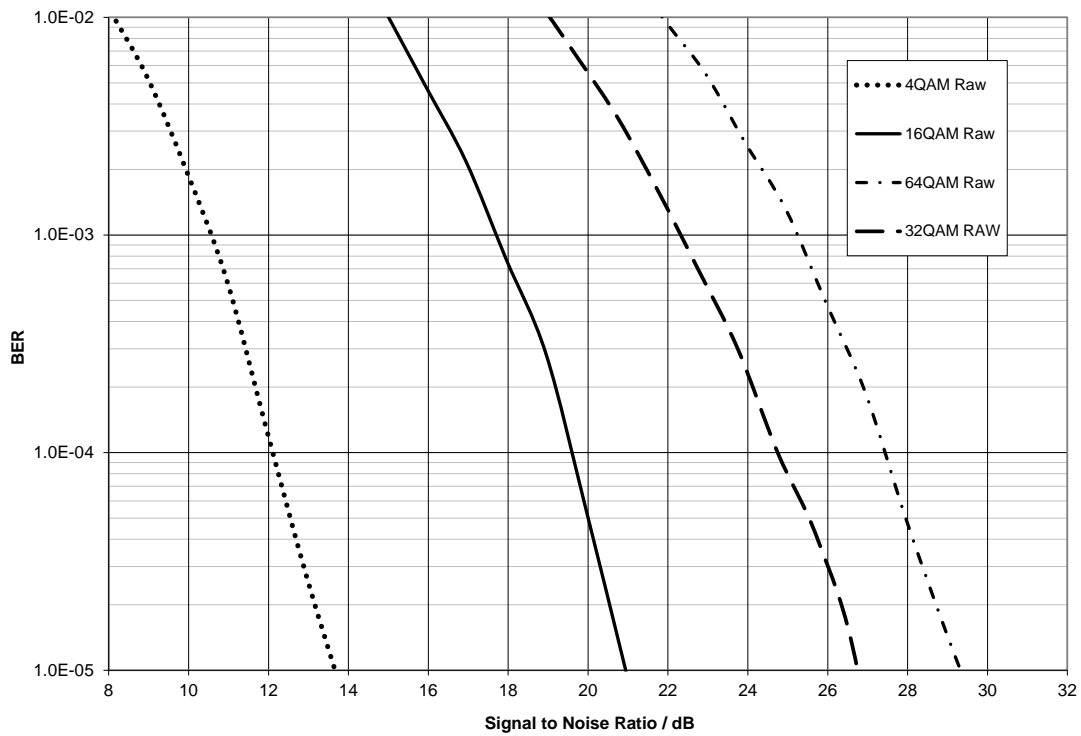
Figure 92 Modem Sensitivity Performance

The co-channel rejection ratio (Figure 93) is measured with an interferer modulated with 400Hz FM and having a deviation of 3kHz; which is 12% of the nominal 25kHz channel bandwidth. This particular interfering signal is used as it is specified in ETSI standard EN 300 113 for co-channel tests. The

measurement is taken at approximately 20dB above sensitivity and although this is not in line with EN 300 113, it means that the data presented here gives a true representation of the performance of the 7164FI-4.x modem rather than being partially influenced by the thermal noise level. The methodology is in line with standards for 6.25kHz channel spaced systems (EN 301 166).
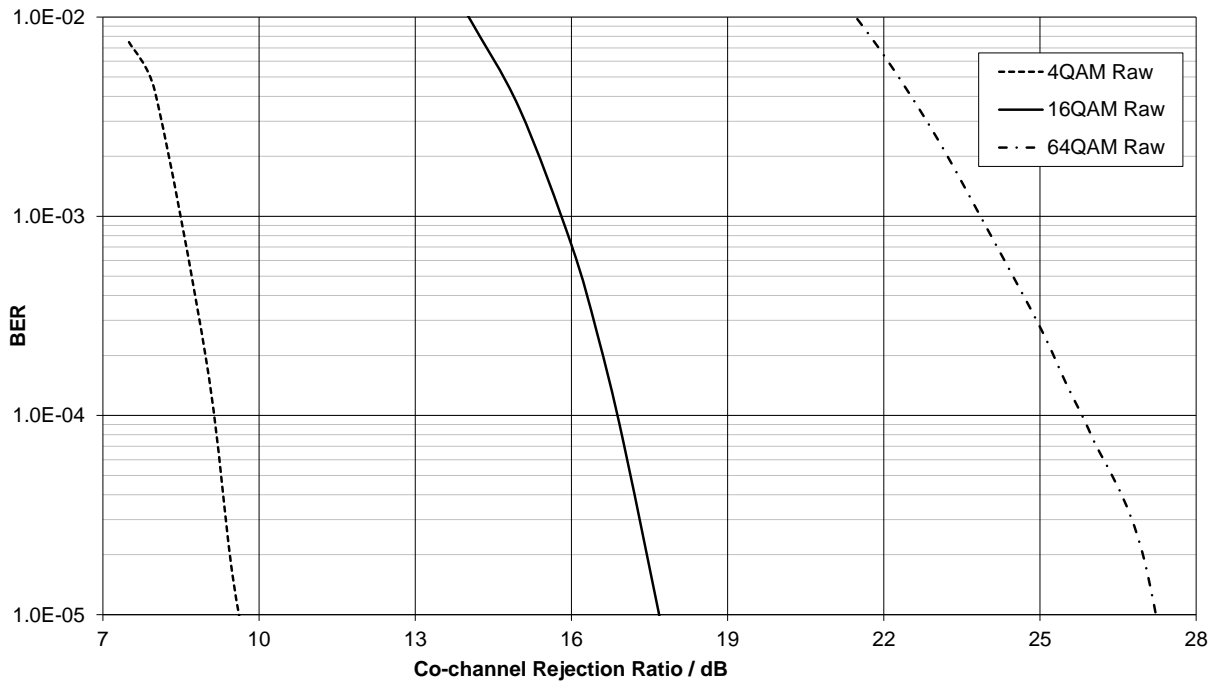
Figure 93 Modem Co-channel Rejection with FM Interferer (as EN 300 113)
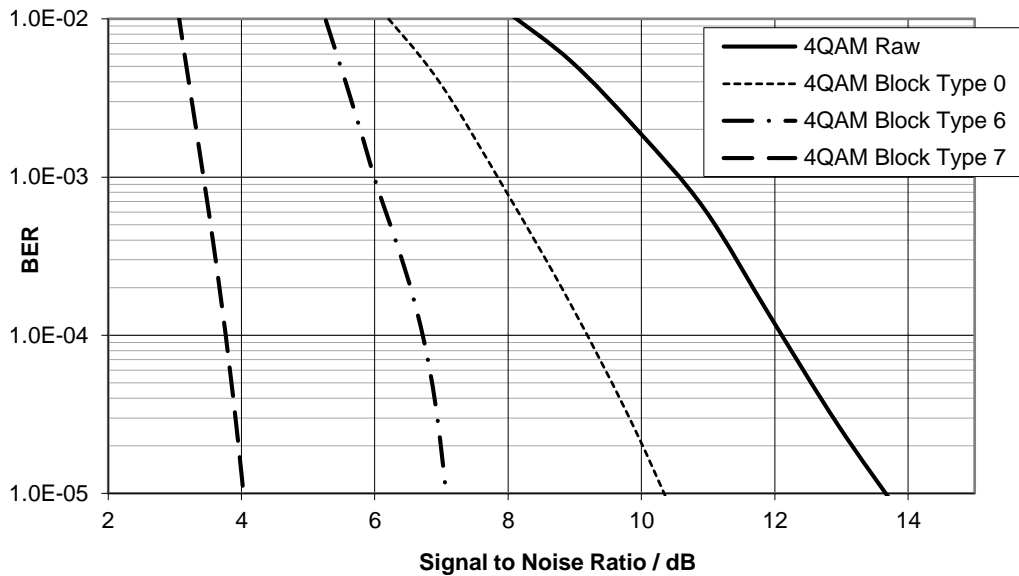
Figure 94 4-QAM Performance with Different Coding Schemes
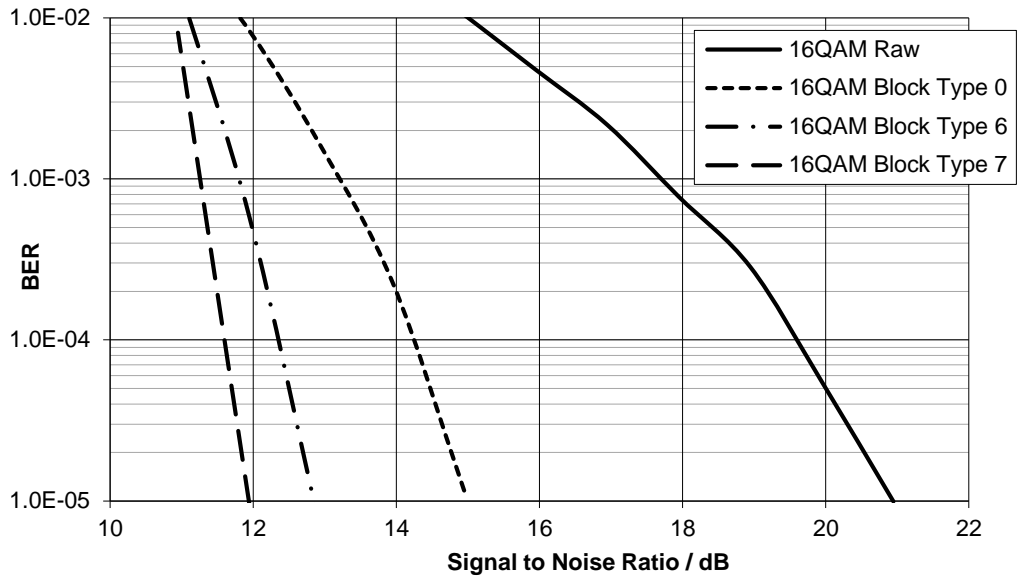
Figure 95 16-QAM Performance with Different Coding Schemes
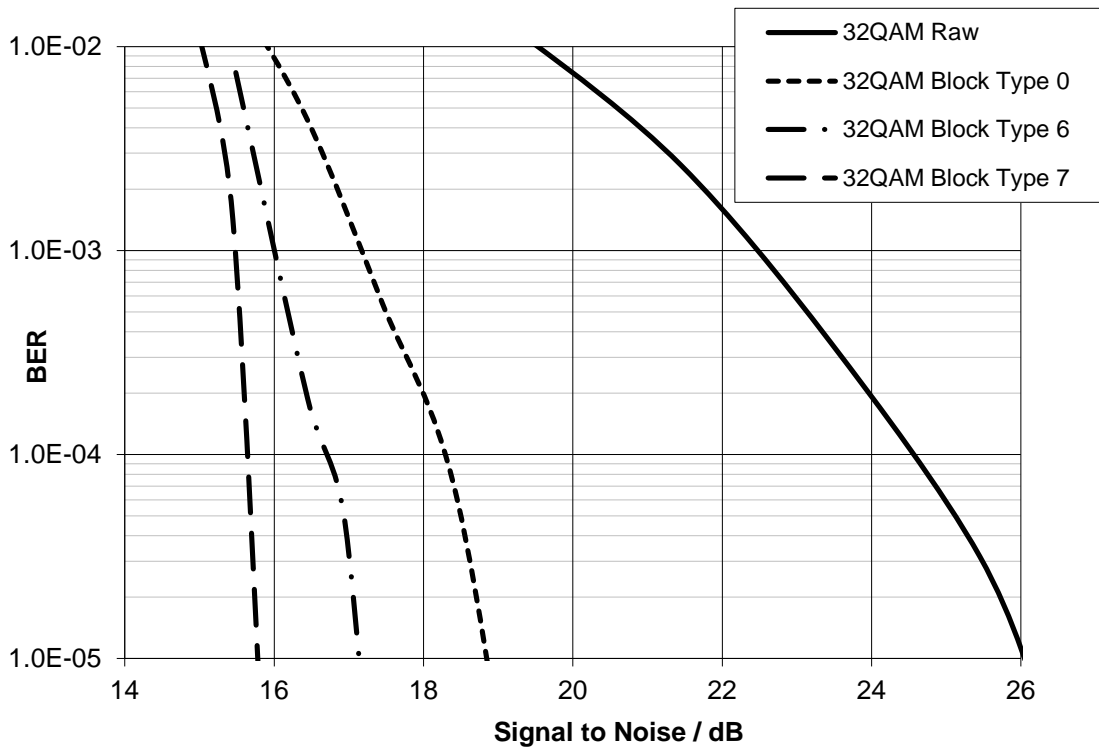
Figure 96 32-QAM Performance with Different Coding Schemes
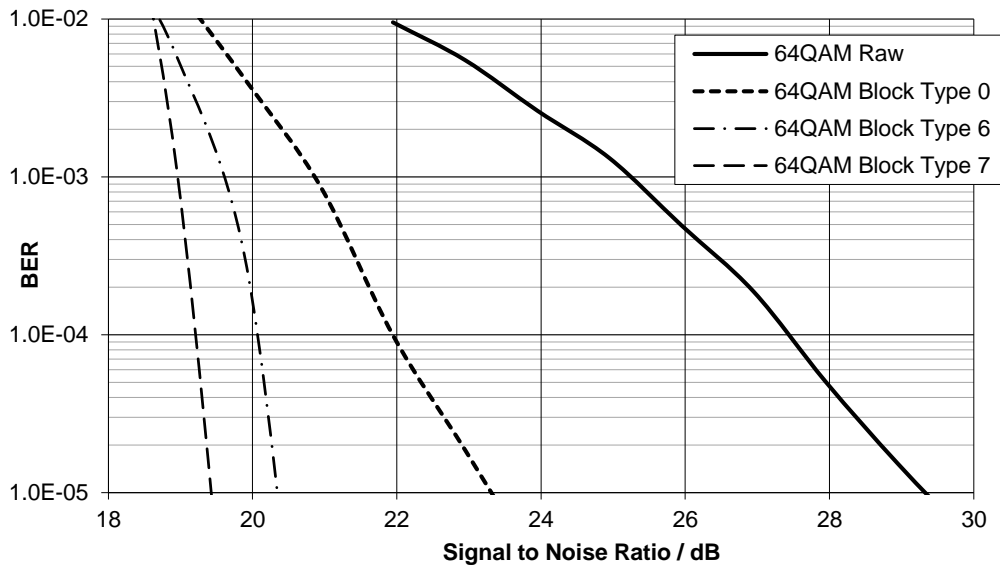
Figure 97 64-QAM Performance with Different Coding Schemes

The required performance of a modem may be assessed in terms of either Bit Error Rate (BER) or Packet Error Rate (PER). The performance of both measures is affected by coding type and block size but the PER also depends on the size of the packet. Short packets with strong coding will exhibit a much lower PER then a long packet with no coding. A comparison of PER vs BER for 4-QAM modulation is shown in Figure 98 based on packets of 182 bytes. The same comparisons for 16-QAM and 64-QAM are shown in Figure 99 and Figure 101 respectively.

Regulatory standards for radio modem designs using the 7164FI-4.x commonly use either BER or PER to assess the receiver performance. Typical BER assessment values are 5%, 1% or 0.1% whereas PER is most often assessed at 20%. It will be observed from Figure 98 that a 4-QAM modem using no coding (raw mode) with 182-byte packets will achieve 20% PER at just over 13dB SNR while 1% BER is achieved at 9.5dB SNR. With formatted block type 6 (see Table 6), approximately 7dB SNR gives 1% BER and 20% PER.

It is recommended that designers assess the performance of the 7164FI-4.x with the correct bit rate, coding, packet size etc. for their particular application having in mind the regulatory requirements that may apply and paying careful attention to the test methods that will be used.
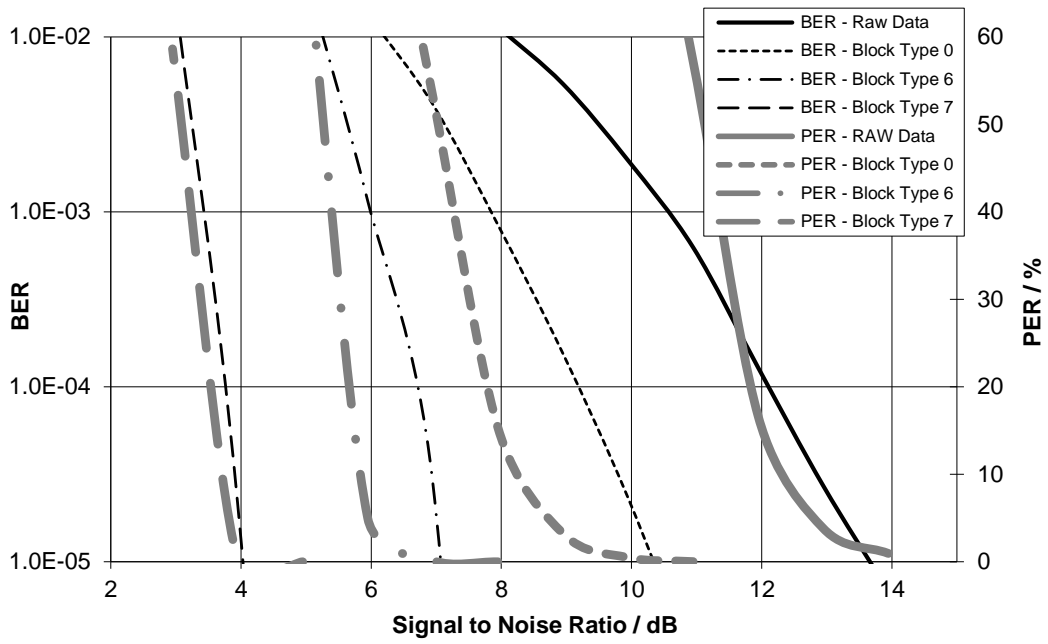
Figure 98 Comparison of BER and PER for 4-QAM Modulation
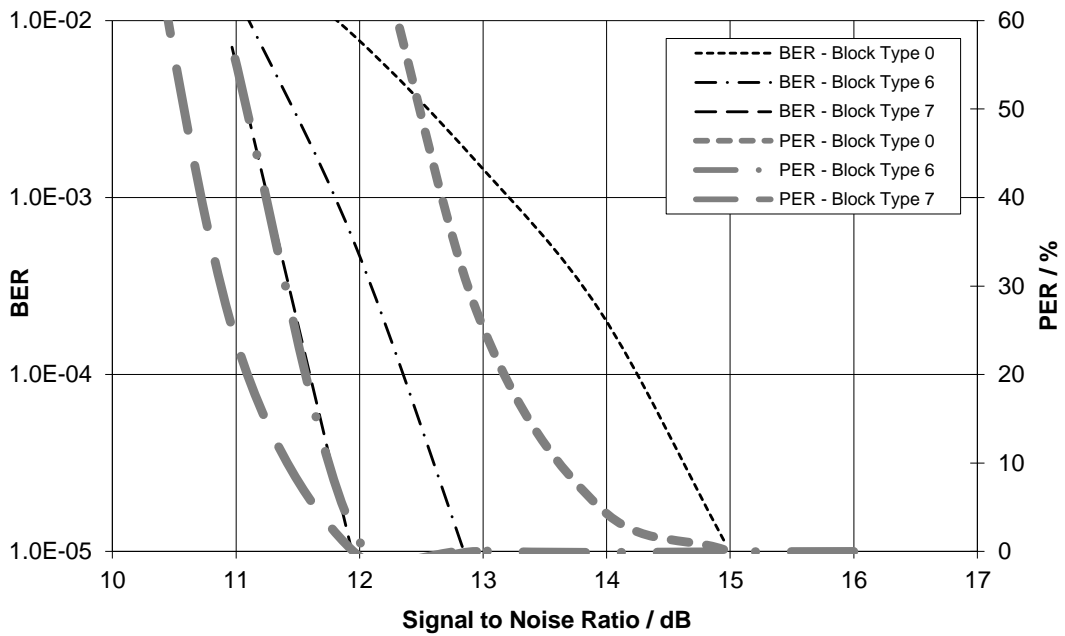
Figure 99 Comparison of BER and PER for 16-QAM Modulation
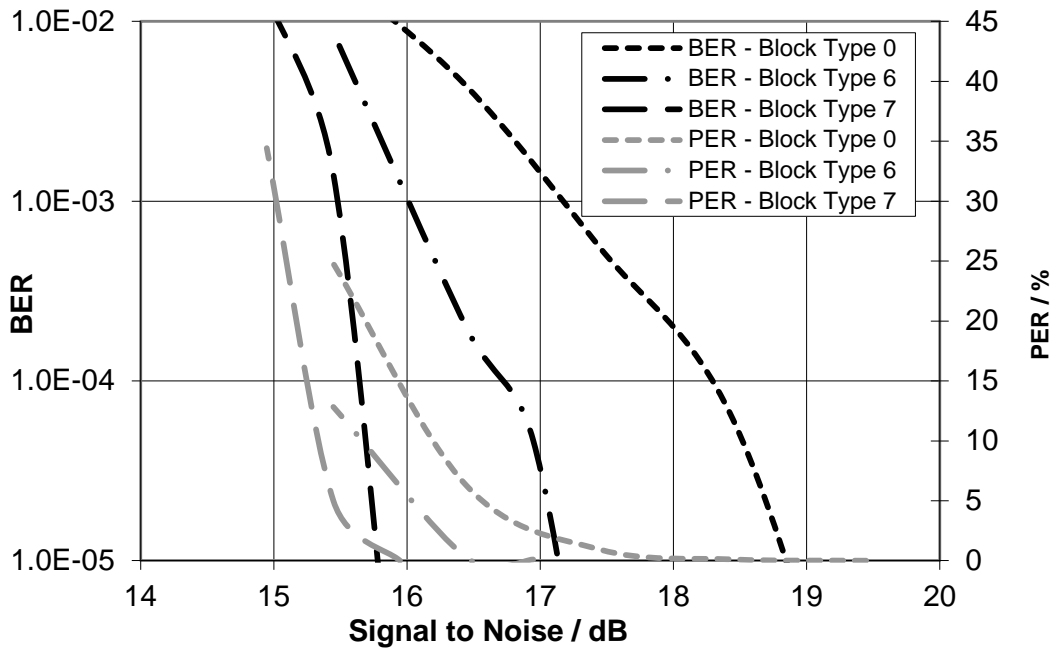
Figure 100 Comparison of BER and PER for 32-QAM Modulation
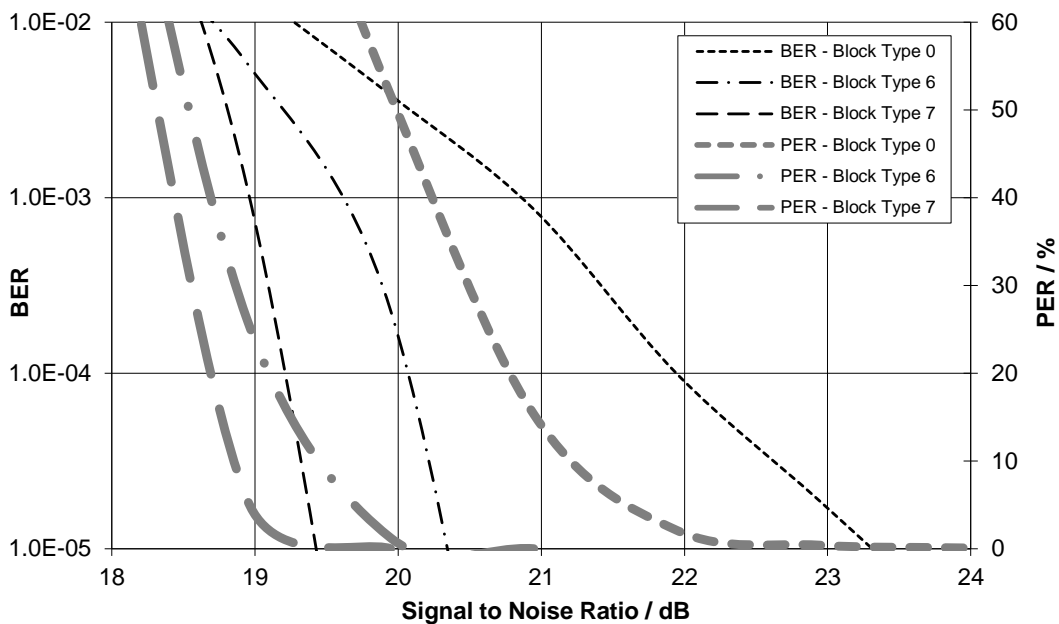
Figure 101 Comparison of BER and PER for 64-QAM Modulation

10.6.2 Adjacent Channel Performance

The 7164FI-4.x provides excellent rejection of adjacent signals present on the I/Q inputs. Assessment of the adjacent channel rejection (ACR) performance of the modem is normally made in terms of BER or PER for a given ratio between the wanted signal (on channel) and larger interferer on the adjacent

channel. Detailed measurement methods vary depending on the standards in use, in particular whether the wanted signal is raised above the sensitivity limit and where the reference is taken. The figures quoted here are based on the measurement method from EN 300 113, which tends to give lower figures than some other methods. In these tests the adjacent channel signal is close to the maximum input signal amplitude allowed by the 7164FI-4.x. The figures quoted in Table 7 are based on the difference between the interferer (400Hz FM modulation, 3kHz deviation) and the mean power of the wanted signal for less than 20% PER (182 byte packets), for 18ksymbols/s.

It has been observed that adjacent channel rejection is limited by the headroom offered by the I/Q Inputs above the sensitivity level of the input signal. This means that when the adjacent channel interferer reaches the maximum allowed input level of the I/Q Inputs, a rapid transition from almost zero BER to a large BER is observed. Given the relative sensitivity levels of the 4-QAM, 16-QAM and 64-QAM signals the result is a measured adjacent channel rejection of:

Table 7 ACR Rejection Performance

	4-QAM	**16-QAM**	**64-QAM**
Raw Data	62dB (less than 1e-3 BER)	55dB (less than 1e-3 BER)	48dB (less than 1e-3 BER)
Formatted Block Type 0	65dB for 6% PER	62dB (0% PER)	58dB (19% PER)
Formatted Block Type 6	65dB for 0% PER	62dB (0% PER)	58dB (0% PER)
Formatted Block Type 7	65dB for 0% PER	62dB (0% PER)	58dB (0% PER)

The figures in Table 7 are typical of what may be achieved with 7164FI-4.x and a typical I/Q radio receiver with no adjacent channel selectivity in the radio circuits. In a more normal RF architecture some adjacent channel selectivity will be provided making system results better than the measured values for the 7164FI-4.x alone. Furthermore, the results observed are not necessarily the maximum that the CMX7164 can achieve but are limited by the practical dynamic range of the CMX7164 combined with the system gain and noise figure of the receiver used in these tests.

10.6.3 Receiver Dynamic Range
The adjacent channel rejection results in section 10.6.2 also indicate that a wanted signal can be successfully received over the dynamic range stated in Table 7 without any need for an AGC. Note that this is limited at the top end by the maximum allowed signal amplitude into the CMX7164, but performance at the bottom end is affected by noise added by the test receiver – so these figures are not the absolute limit of CMX7164 FI-1.x/2.x/4.x/6.x performance.

10.6.4 Receiver Response Equaliser Performance
The performance of the 7164FI-4.x when receiving a signal through a typical IF crystal filter as used in EV9910B/EV9920B[12] is shown in the following graphs. The nominal bandwidth of the filter is 15kHz, however its response within that bandwidth is not flat, both amplitude and group delay distortion is introduced into the signal.

The following tests were carried out using a 16ksymbols/s 4-QAM, 16-QAM or 64-QAM signal. Where the results are quoted as using no equalisation the Receiver Response Equaliser was disabled. Where the results are quoted as Equalised the Receiver Response Equaliser was provided a 4-QAM training sequence with level –70dBm which produced 400mV (differential) on the I and Q inputs. Equaliser gain was set to 3000 and training lasted for 800 symbol periods. While training the received signal had less than 100Hz frequency error. Once trained the resulting equaliser coefficients were used for the remaining tests.

Firstly the signal-to-noise performance of equalised and non equalised received signals are compared. The test is similar to that described in section 10.6.1 Signal-to-Noise and Co-channel Performance,

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[12] Evaluation card for CMX991 / CMX992 RF Quadrature Transceiver / Receiver ICs.

except that as the baud rate is 16ksymbols/s the RxBW parameter is 16000. Applying this factor also means that the results in section 10.6.1 may be directly compared to those below in Figure 102.
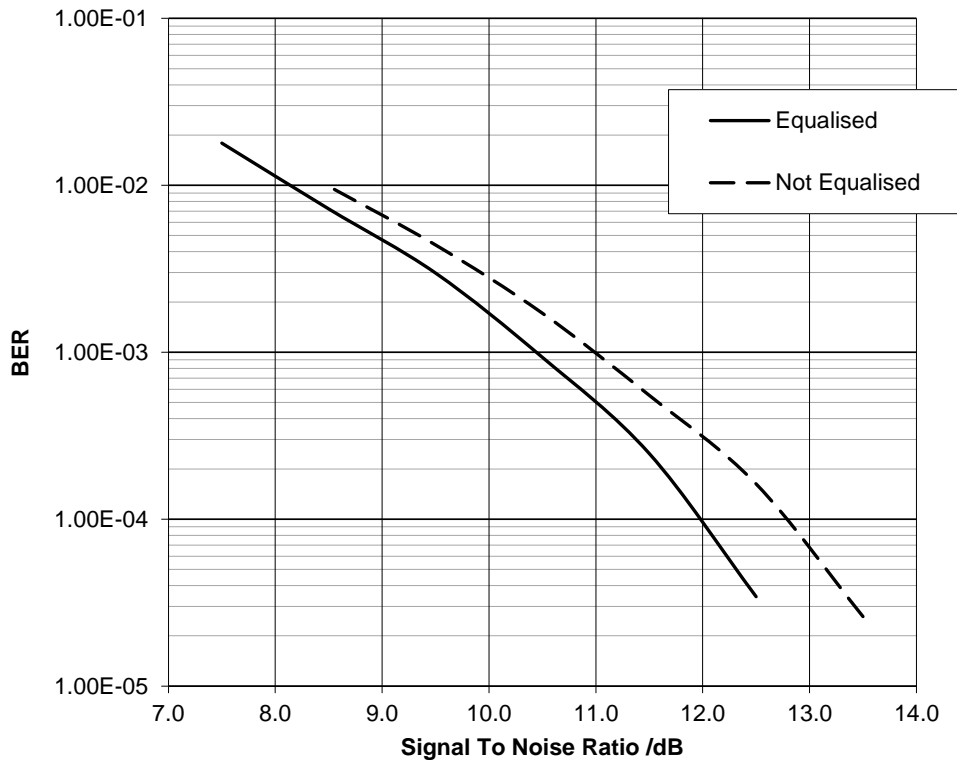
Figure 102 4-QAM Signal-to-Noise Performance, Equalised and Non-Equalised
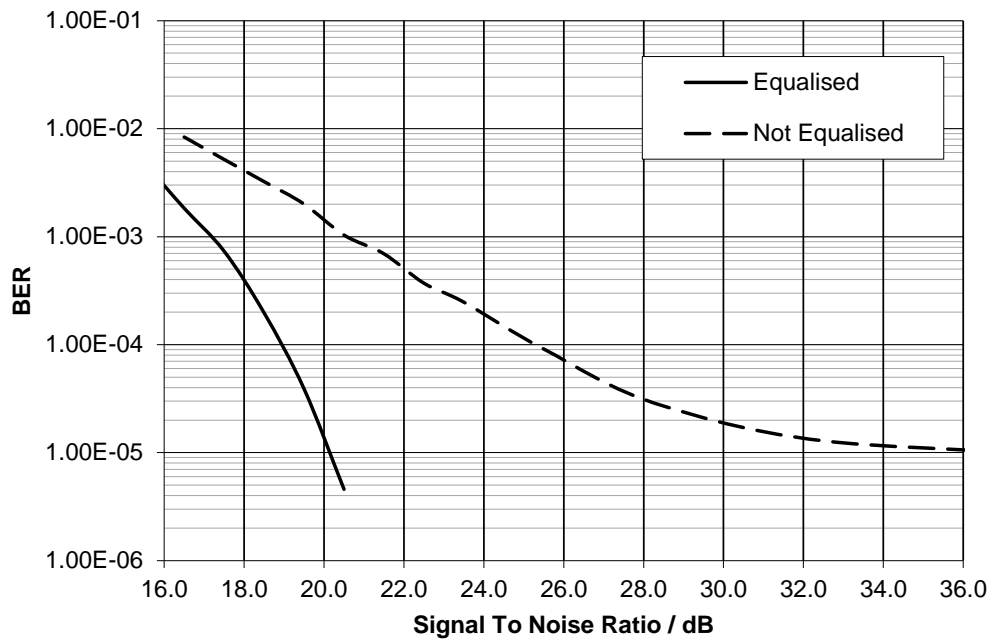
Figure 103 16-QAM Signal-to Noise Performance, Equalised and Non-Equalised
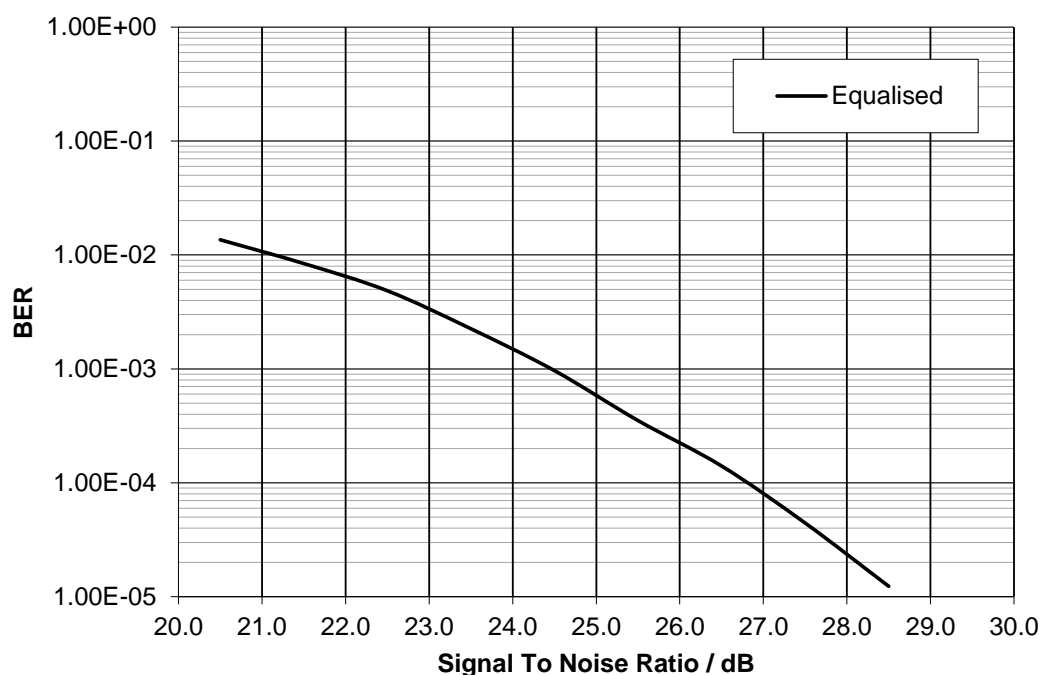
Figure 104 64-QAM Signal-to-Noise Performance, Equalised

Figure 102, Figure 103 and Figure 104 show that equaliser training improves the received signal performance in all cases: 4-QAM, 16-QAM and 64-QAM. We can see that without equalisation 16-QAM signals have a residual bit error rate even with a high signal level, as the non equalised curve flattens off. 64-QAM is unusable without equalisation producing a residual bit error rate of greater than 1e-2 regardless of signal-to-noise ratio. The 4-QAM curves show that 4-QAM is less affected by the receiver response, therefore the improvement made by equalisation is less. Once equalisation is present the measured figures compare well to the results (with no crystal filter in the receive path) in section 10.6.1 Signal-to-Noise and Co-channel Performance.

The response of crystal filters varies with temperature. This will affect the ability of an equaliser which is trained at room temperature to compensate effectively for crystal filter distortions at a different temperature. Other types of filter may be more stable with temperature, for example the baseband filters in the CMX994/A/E[13]. Measurements showing the degradation in signal-to-noise performance over temperature when the equaliser was trained at room temperature are shown in plots Figure 105 to Figure 108.

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[13] Direct Conversion Receiver IC.
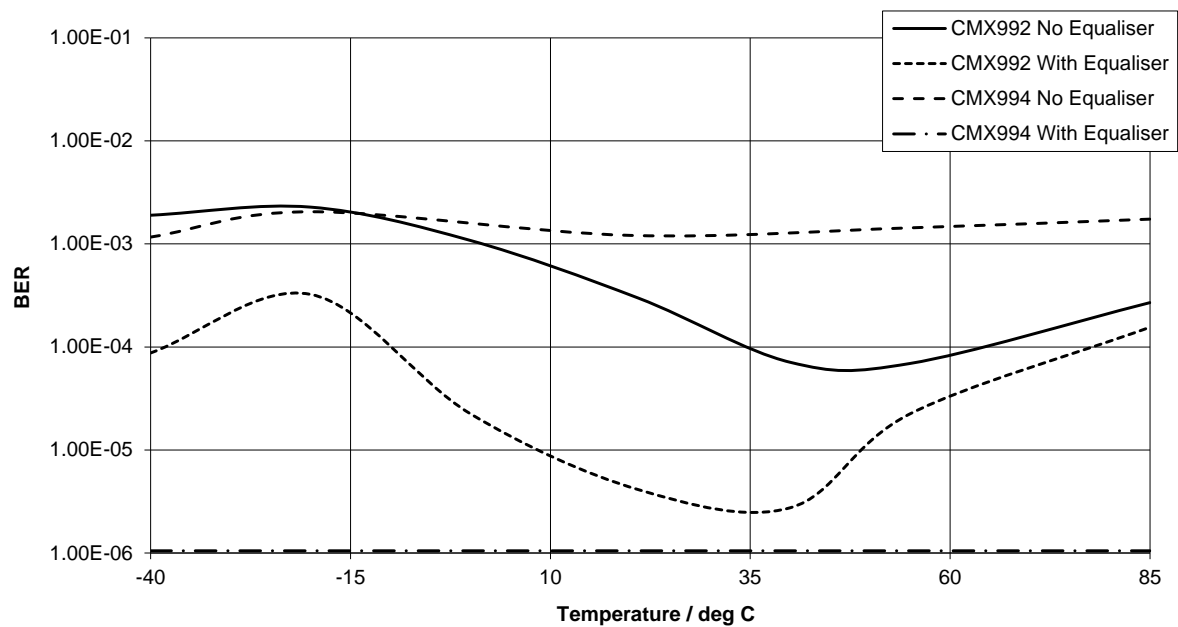
Figure 105 Performance of 16-QAM Equalised Signals with Temperature Variation

Tests were carried out using 16-QAM modulation with a signal level of -103dBm (Figure 105) and a signal level of –95dBm for 64-QAM (Figure 106), using the EV9910B[14] (CMX991 with GMCF-45 45G15B1 crystal filter) and the EV9942 (CMX994/A/E with temperature compensated baseband filter). BER performance was measured with and without equalisation being applied then the temperature was varied and the equalised and non-equalised bit error rate measurements repeated.

The results are shown in Figure 105 and Figure 106. The results show that with a crystal filter equalisation is most effective at the temperature at which calibration was carried out and that performance degrades away from this temperature. In contrast it will be observed that with the CMX994/A/E equaliser performance is maintained across the full operating temperature range. For all results a frequency error between transmitter and receiver of less than 100Hz.

As the crystal filter was used in EV9910B/EV9920B we should note that its specified range of operation is -20 to +55 deg C. It was also observed that a re-calibration at a given temperature would result in equalisation coefficients capable of producing a much improved BER at that temperature.

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[14] Evaluation card for CMX991 / CMX992 RF Quadrature Transceiver / Receiver ICs.
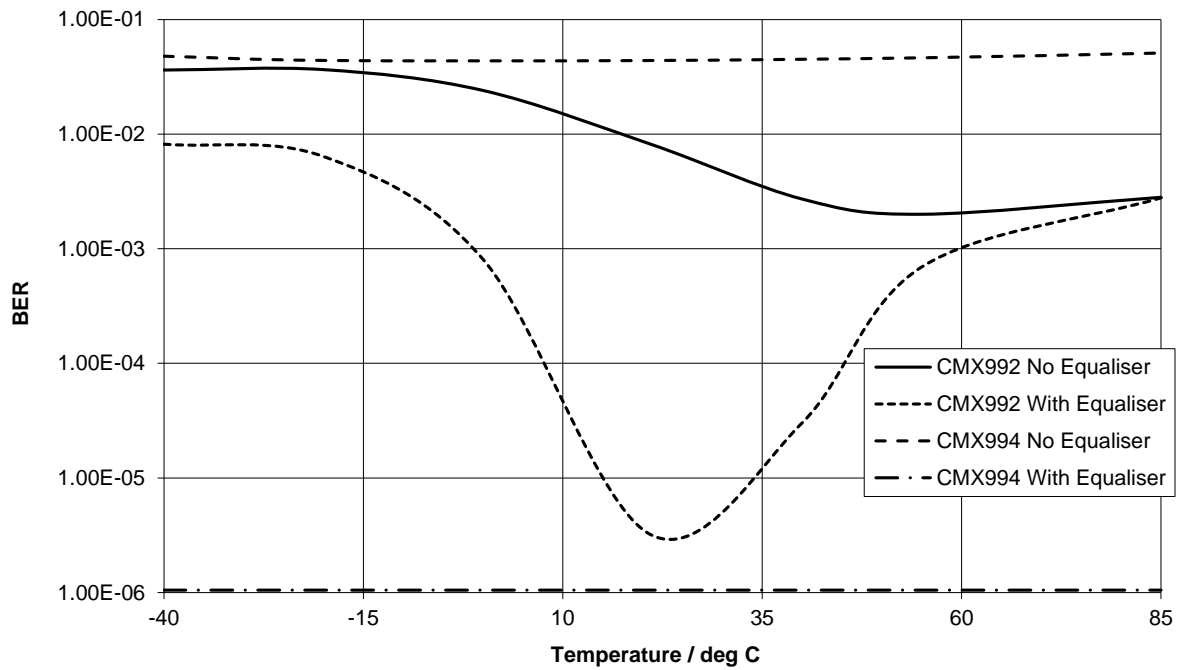
Figure 106 Performance of 64-QAM Equalised Signals with Temperature Variation

Because of the different sensitivities of the EV9910B and EV9942 further plots are shown (Figure 107 and Figure 108) where a constant signal to noise is used.
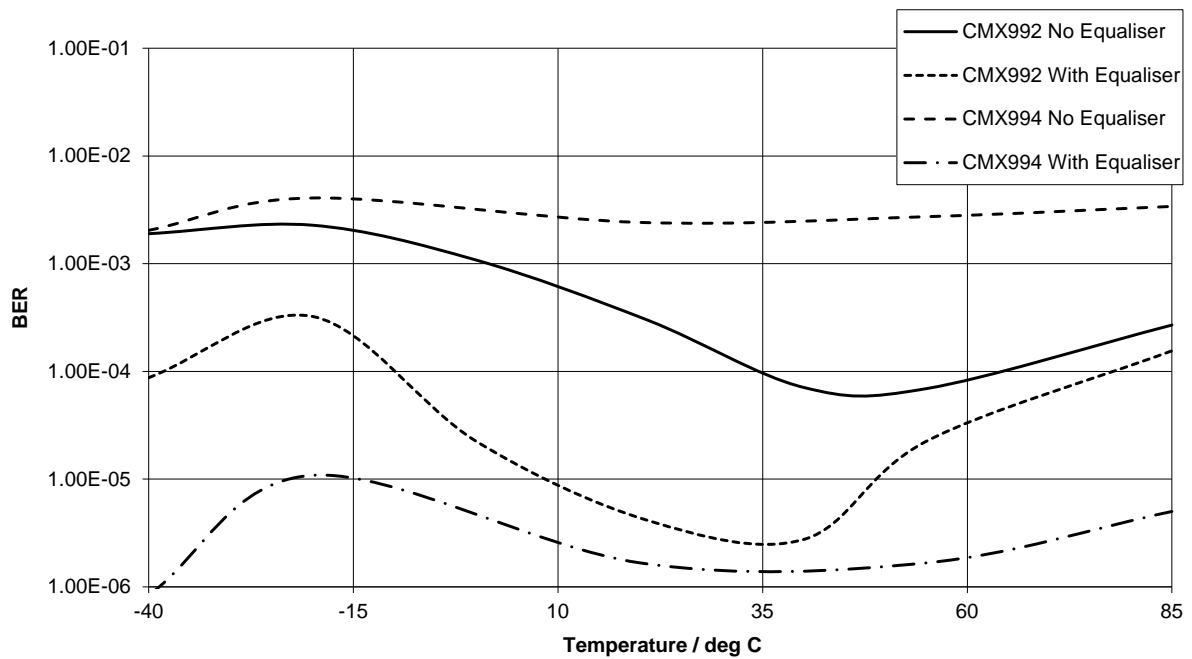
Figure 107 Performance of 16-QAM Equalised Signals with Temperature Variation and Constant Signal-to-Noise Ratio
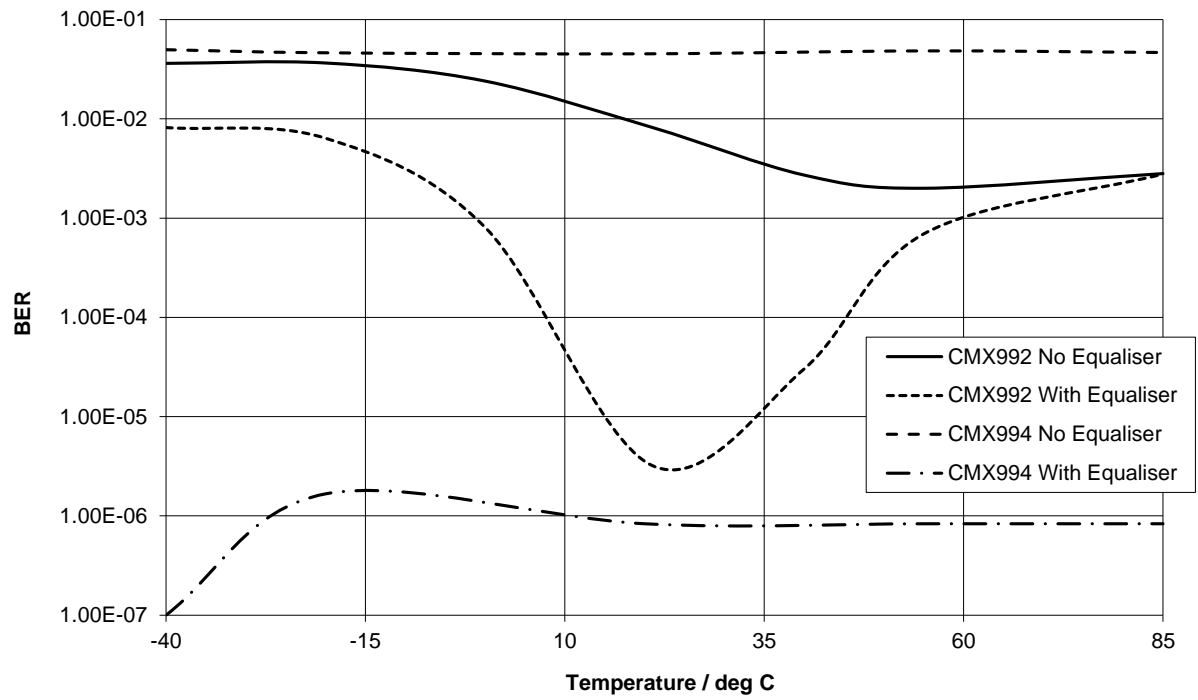
Figure 108 Performance of 64-QAM Equalised Signals with Temperature Variation and Constant Signal-to-Noise Ratio

11 7164FI-6.x Features

The 7164FI-6.x uses an FSK modulation scheme compatible with ITU-T V.23 with an over-air bit rate of 1200bps or 300bps. Raw and formatted data can be transferred. Formatting adds start, stop and parity bits.

11.1 7164FI-6.x Modulation

The modulation bandwidth is dependent on the peak frequency deviation of the modulating signal. The user can set the deviation in order to meet the requirements of a particular application.

11.2 7164FI-6.x Radio Interface

The transmit radio interface of 7164FI-6.x can be set to two-point modulation or I/Q. When the 7164FI-6.x is in two-point modulation mode, the I Output is used as 'Mod 1' and the Q Output is used as 'Mod 2'. The 7164FI-6.x receive input signal must come from a zero-IF I/Q radio receiver.

11.2.1 I/Q Transmit and I/Q Receive Interfaces

The 7164FI-6.x can produce a zero-IF modulated I/Q Tx output signal of user-configured deviation.

In receive, the 7164FI-6.x accepts a zero-IF I/Q input signal and provides significant digital channel filtering. It frequency demodulates the resulting signal, which is then treated internally in the same manner as a limiter discriminator output signal.

Note that the transmit and receive interfaces are identical to those used by other CMX7164 FIs.

Use of I/Q receive mode introduces the issue of I/Q dc offsets. These are dc offsets caused by the radio receiver – resulting in the signal into the CMX7164 having a dc offset other than that present on the VBIAS pin. The offsets need to be removed prior to demodulation. Offsets typically remain constant for a particular radio frequency selected, but will vary if that frequency is changed. Gain within the radio receiver may also affect the dc offset seen by the CMX7164.

I/Q dc offset effects are a radio issue which is beyond the control of the CMX7164, however, the CMX7164 does provide dc offset calculation and removal. This is described in Section 14 (Application Notes).

11.3 7164FI-6.x Formatted Data

The 7164FI-6.x supports formatted data. In this mode, the CMX7164 will automatically add start, stop and (optionally) parity bits to bytes in Tx and also check and remove start, stop and parity bits in Rx. Formatted data can be transferred in blocks of 1 to 8 bytes. When receiving formatted data, the CMX7164 will indicate errors in received data.

11.4 7164FI-6.x Typical Transmit Performance

Using the test system shown in Figure 109, the 7164FI-6.x internal PRBS generator is used to modulate the RF vector signal generator. Some typical results are shown in the following figures. The desired deviation is achieved by adjusting the CMX7164 peak deviation via register $61.
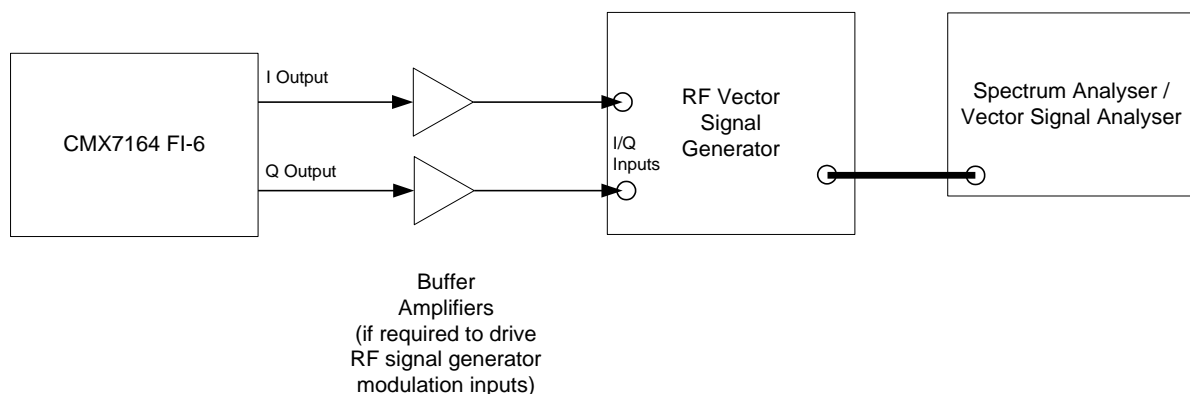
Figure 109 Tx Spectrum and Modulation Measurement Configuration for I/Q Operation

Modulation Spectrum (Peak deviation = 1.5kHz)
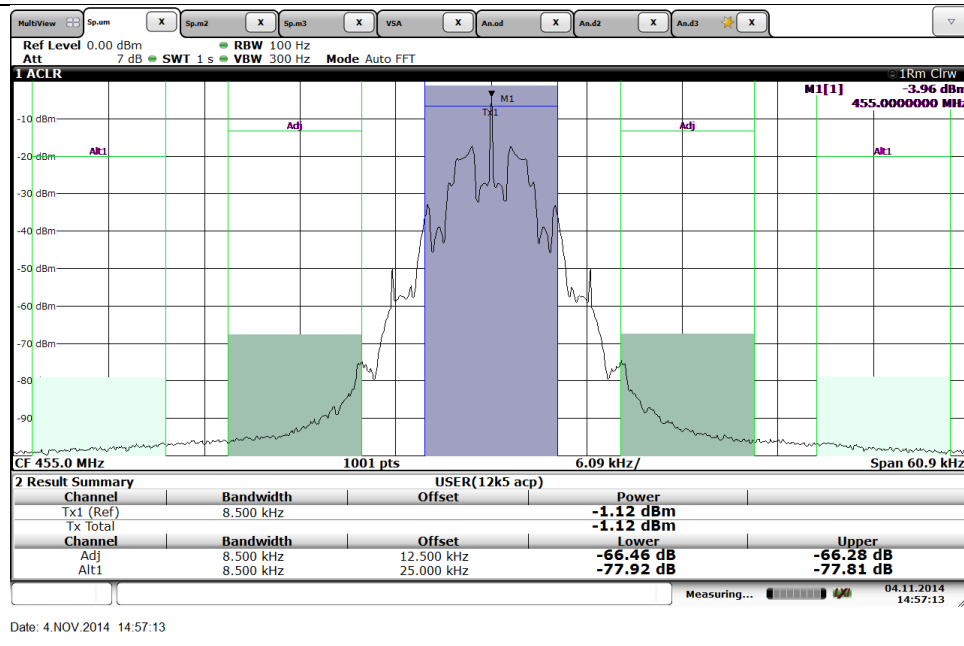
Modulation Spectrum

EN 300 113 Adjacent Channel measurement for 12.5kHz channel:

ACP < -66dB (limit is –60dB)

(Measurement bandwidth = 8.5kHz)
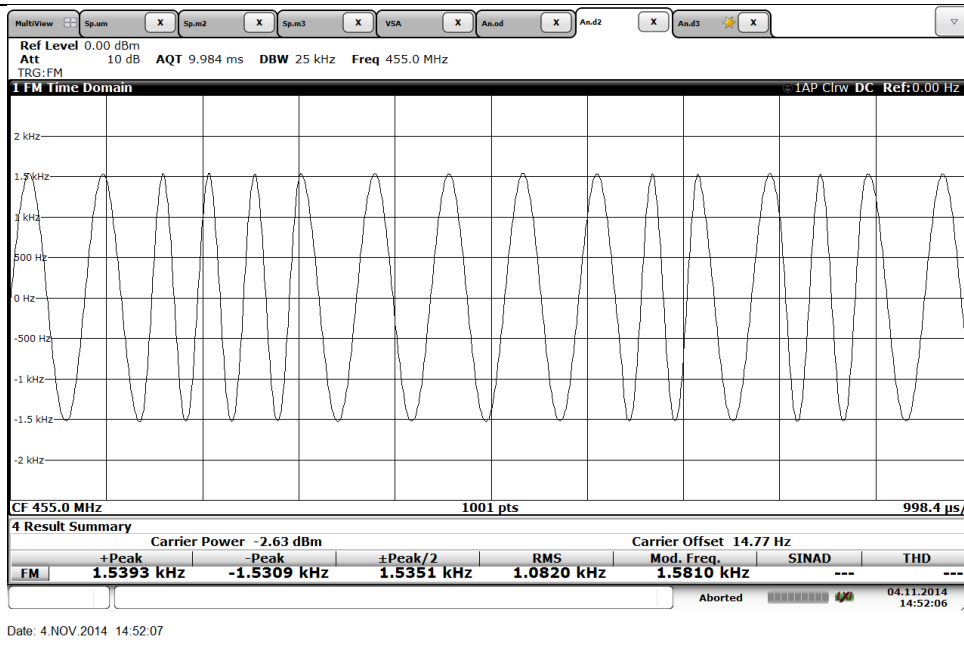
Figure 110 Tx Modulation V.23, 1200bps, I/Q Modulation

Modulation Spectrum (Peak deviation = 3.0 kHz)
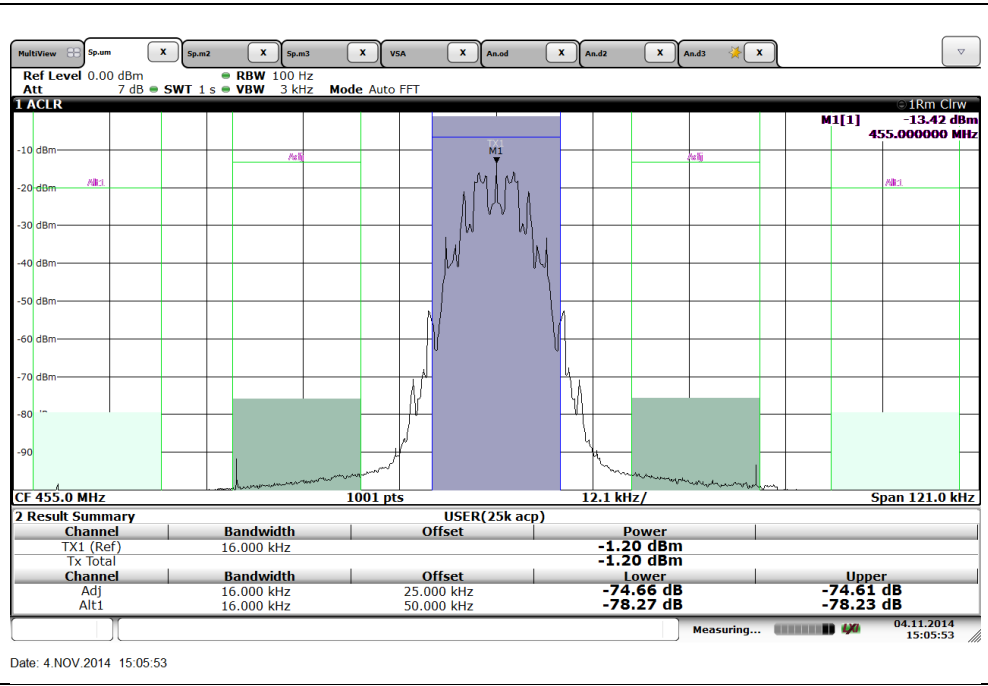
Modulation Spectrum

EN 300 113 Adjacent Channel measurement for 25kHz channel:

ACP < -74dB (limit is –70dB)

(Measurement bandwidth = 16kHz)

Date: 4.NOV.2014 15:05:53

Date: 4.NOV.2014 14:58:31
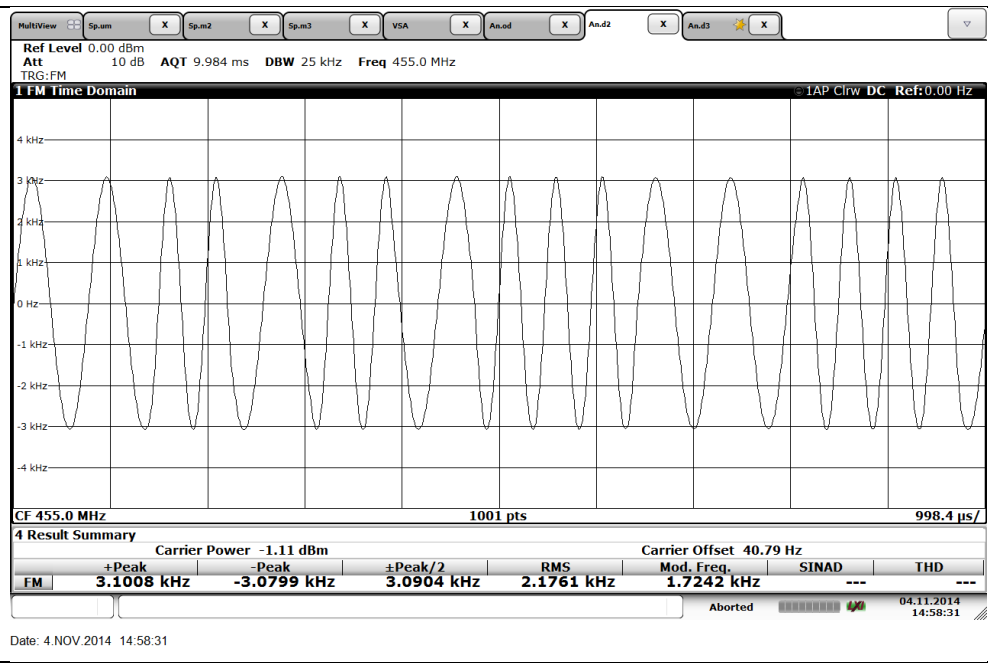
Figure 111 Tx Modulation V.23, 1200bps, I/Q Modulation

11.5 7164FI-6.x Typical Receive Performance

11.5.1 Signal-to-Noise Performance

Signal-to-noise performance was measured by sending 200 bursts of a known PRBS sequence. Each burst contained 800 bytes, for a total of 160,000 bytes, or 1,280,000 bits. Bit errors were detected by comparing with the known sequence. A CMX994/A/E-based receiver was used for this test. Tx Deviation was ±1.5kHz and the default, narrow channel filter was used.
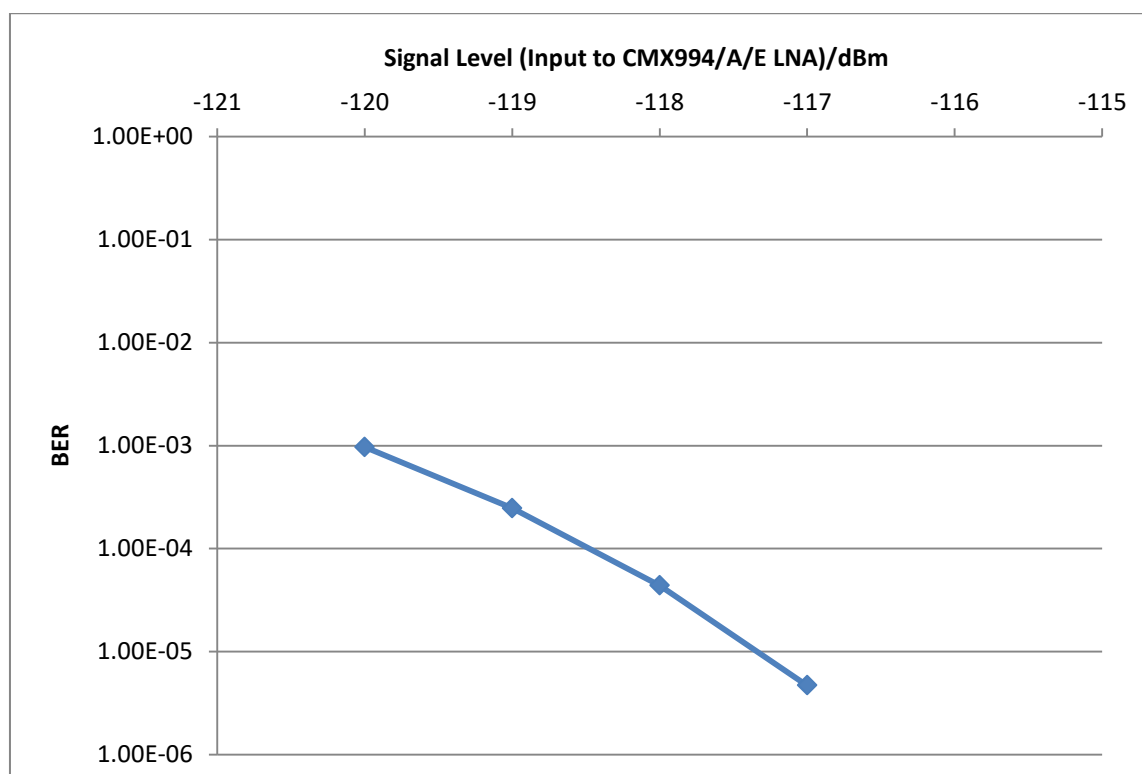
Figure 112 Signal Level vs BER

11.5.2 Adjacent Channel Performance

Assessment of the adjacent channel rejection (ACR) performance of the modem is normally made in terms of BER or PER for a given ratio between the wanted signal (on channel) and larger interferer on the adjacent channel. Detailed measurement methods vary depending on the standards in use, in particular whether the wanted signal is raised above the sensitivity limit and where the reference is taken. The figures quoted here are based on the measurement method from EN 300 113. The results are based on the difference between the interferer (400Hz FM modulation, 1.5kHz deviation) and the power of the wanted signal for 1.2ksymbols/s.

Channel bandwidth	Adjacent Channel rejection	BER
12.5kHz	60dB	<1%
25kHz	70dB	<1%

The results shown here are typical of what may be achieved with 7164FI-6.x and a typical I/Q radio receiver with no adjacent channel selectivity provided by receiver RF circuits. Genuine RF receivers typically provide some adjacent channel selectivity that would make system performance better than the measured values for the 7164FI-6.x alone. Furthermore, the results observed are not necessarily the

maximum that the CMX7164 can achieve but are limited by the practical dynamic range of the CMX7164 combined with the system gain and noise figure of the receiver used in these tests.

12 Performance Specification

12.1 Electrical Performance

12.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Power Supplies			
DV_{DD} - DV_{SS}	-0.3	4.0	V
DV_{CORE} - DV_{SS}	-0.3	2.16	V
AV_{DD} - AV_{SS}	-0.3	4.0	V
Voltage on any pin to V_{SS}	-0.3	IOV_{DD} + 0.3	V
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

L9 Package (64-pin LQFP)	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25ºC		1690	mW
Derating		16.9	mW/ºC
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	ºC

Q1 Package (64-pin VQFN)	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25ºC		3500	mW
Derating		35.0	mW/ºC
Storage Temperature	-55	+125	ºC
Operating Temperature	-40	+85	ºC

12.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ	Max.	Units
DV_{DD} - DV_{SS}	3.0	3.3	3.6	V
DV_{CORE} - DV_{SS}	1.7	1.8	1.9	V
AV_{DD} - AV_{SS}	3.0	3.3	3.6	V
Voltage differential between power supplies:				
DV_{DD} and AV_{DD}	0	–	0.3	V
DV_{SS} and AV_{SS}	0	–	50	mV
Operating Temperature	-40	–	+85	°C
Xtal Frequency	3.0	–	12.288	MHz
External Clock Frequency	3.0	–	25.000	MHz

12.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
External components as recommended in Section 5, External Components.

Maximum load on digital outputs = 30pF.

Xtal Frequency = 9.6MHz$\pm$0.002% (20ppm); T_{AMB} = -40°C to +85°C.

AV_{DD} = DV_{DD} = 3.0V to 3.6V.

Current consumption figures quoted in this section apply to the device when loaded with FI-1.x/2.x/4.x/6.x only. Current consumption may vary with other valid Function Images™.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current (see also section 12.1.5)	11				
All Powersaved					
AI_{DD} + DI_{DD}	10,15	–	1.0	–	µA
Idle Mode	12,15				
DI_{DD}	13	–	550	–	µA
AI_{DD}		–	17	–	µA
Additional Current for One Auxiliary System Clock (output running at 5MHz – SYSCLKPLL active)	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	900	–	µA
Additional Current for one Auxiliary System Clock (output running at 4.8MHz – SYSCLKPLL not required)	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	675	–	µA
Additional Current for Each Auxiliary ADC	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	190	–	µA
Additional Current for Each Auxiliary DAC	14,15				
AI_{DD} (AV_{DD} = 3.3V)		–	210 to 370	–	µA

Notes: 10 Idle mode with V_{BIAS} disabled.

11 T_{AMB} = 25°C, not including any current drawn from the device pins by external circuitry.

12 System Clocks, Auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled and V_{BIAS} enabled.

13 Using a 19.2MHz external clock input, Xtal oscillator circuit powered down.

14 A lower current is measured when outputting the smallest possible dc level from an AuxDAC, a higher current is measured when outputting the largest possible dc value.

15 Using a 19.2MHz external clock input.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK	20				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		−40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')	11	−1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current	11	-1.0	–	1.0	µA
V_{BIAS}	21				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	50	–	kΩ

Notes: 20   Characteristics when driving the XTAL/CLK pin with an external clock source.
              21   Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor, as shown in section 4 PCB Layout Guidelines and Power Supply Decoupling.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' Pulse Width		30	15	–	–	ns
'Low' Pulse Width		30	15	–	–	ns
Input Impedance (at 9.6MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)			–	20	–	ms
SYSCLK1/2 Outputs						
SYSPLL Operating Frequency			38	–	250	MHz
SYSCLK1/2 Output Frequency			–	–	20	MHz
Rise Time			–	–	13.5	ns
Fall Time			–	–	6	ns
V$_{BIAS}$						
Start-up Time (from powersave)			–	30	–	ms
Differential I and Q Inputs						
Input Impedance, Enabled		31	10	–	140	kΩ
Input Impedance, Muted or Powersaved				200		kΩ
Maximum Input Voltage Excursion		32	–	–	20 to 80	%AV$_{DD}$
Programmable Input Gain Stage						
Gain (at 0dB)		33	−0.5	0	+0.5	dB
Cumulative Gain Error	⎤					
(w.r.t. attenuation at 0dB)	⎦	33	−1.0	0	+1.0	dB

Notes:

	30	Timing for an external input to the XTAL/CLOCK pin.
	31	With no external components connected.
	32	For each input pin and for AV$_{DD}$ = 3.3V, the maximum allowed signal swing is: (3.3 x 0.8) - (3.3 x 0.2) = 2.0V.
	33	Design Value. Overall attenuation input to output has a design tolerance of 0dB ±1.0dB.

AC Parameters			Notes	Min.	Typ.	Max.	Unit
Modulator I/Q Outputs							
(I Output, Q Output)							
Power-up to Output Stable			40	–	50	100	µs
I/Q Output Coarse Gain Attenuators							
Attenuation (at 0dB)			42	−0.2	0	+0.2	dB
Cumulative Attenuation Error			42				
(w.r.t. attenuation at 0dB)				−0.6	0	+0.6	dB
Output Impedance		Enabled	41	–	600	–	Ω
		Disabled	41	–	>100	–	MΩ
Output Voltage Range			43, 44	0.3	–	AV_{DD}-0.3	V
Load Resistance				20	–	–	kΩ

Notes:
40 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

41 Small signal impedance, at AV_{DD} = 3.3V and T_{AMB} = 25°C.

42 Figures relate to attenuator block only. Design Value. Overall attenuation input to output has a design tolerance of 0dB ±1.0dB.

43 For each output pin. With respect to the output driving a 20kΩ load to AV_{DD}/2.

44 The levels of I/Q Output Fine Gain and Offset (registers $5D and $5E) should be adjusted so that the output voltage remains between 20% and 80% of AV_{DD} on each output pin (when 0dB of coarse output gain is used). This will produce the best performance when the device operates with AV_{DD} = 3.3V.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (AuxADC1-4)					
Source Output Impedance	50	–	–	24	kΩ
Auxiliary 10-Bit ADCs					
Resolution		–	10	–	Bits
Conversion Time	51	–	225	–	µs
Sample Rate		1	-	512	Hz
Input Impedance					
Resistance	56	–	26.5	30	kΩ
Capacitance	56	–	3	3.5	pF
Offset Error	54, 55	–	–	±18	mV
Integral Non-linearity	54, 55	–	–	±2	LSBs
Differential Non-linearity	52, 54	–	–	±1	LSBs
Auxiliary 10-Bit DACs					
Resolution		–	10	–	Bits
Conversion Time	51		60		µs
Settling Time to 0.5 LSB			10		µs
Offset Error	54, 55	–	–	±20	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity	54, 55	–	–	±4	LSBs
Differential Non-linearity	52, 54	–	–	±1	LSBs

Notes:

50	Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.
51	Typical – based on 9.6MHz Xtal or external oscillator
52	Guaranteed monotonic with no missing codes.
54	Specified between 2.5% and 97.5% of the full-scale range.
55	Calculated from the line of best fit of all the measured codes.
56	The input signal internally drives a S/H (sample and hold) circuit that is newly charged for one ADC conversion period on each ADC conversion. That circuit connects the input pin to an internal V_{DD}/2 voltage source via a series resistor-capacitor network. The S/H circuit's net time constant, including the external source impedance of any input signal, will determine the S/H settling time. Provided the external source impedance is of low value, the resultant settling time will be correspondingly small. Using the above figures and calculating time t = 9 time constants x R x C, the result would be 9 * 30kΩ * 3.5pF = 0.95µs.

12.1.4 7164FI-1.x Parametric Performance

For the following conditions unless otherwise specified:
External components as recommended in section 5.

Maximum load on digital outputs = 30pF.

Clock source = 19.2MHz $\pm$0.002% (20ppm) clock input; T_{AMB} = -40°C to +85°C.

AV_{DD} = DV_{DD} = 3.0V to 3.6V.

Reference signal level = 308mV rms at 1kHz with AV_{DD} = 3.3V

Signal levels track with supply voltage, so scale accordingly.

Signal-to-Noise Ratio (SNR) in bit rate bandwidth.

Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device when loaded with FI-1.x only. The use of other valid Function Images™, can modify the parametric performance of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current					
Rx Mode					
DI_{DD} (8ksymbols/s – search for FS)	61	–	10.3	–	mA
DI_{DD} (9.6ksymbols/s – search for FS)	61	–	10.8	–	mA
DI_{DD} (8ksymbols/s – FS found)	61	–	9.2	–	mA
DI_{DD} (9.6ksymbols/s – FS found)	61	–	9.4	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	8.7	–	mA
Tx Mode	60				
DI_{DD} (8ksymbols/s)		–	4.9	–	mA
DI_{DD} (9.6ksymbols/s)		–	5.0	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	7.7	–	mA

Notes:

60	Transmitting in I/Q mode, continuous GMSK/GFSK PRBS, all GPIOs and RAMDAC set to manual.
61	8ksymbols/s: 12.5kHz channel, BT=0.3; 9.6ksymbols/s: 25kHz channel, BT=0.5.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate		2 000		20 000	sym s^{-1}
Modulation			GMSK/ GFSK		
Filter BT			0.25, 0.27, 0.3 or 0.5		
Tx Bit-rate Accuracy	62		-		ppm
Tx Output Level (I Output, Q Output)	63				
FI-1.x I/Q modulation mode			2.6		Vp-p
FI-1.x Two-point modulation mode			3.3		Vp-p
Tx Adjacent Channel Power (I Output, Q Output, PRBS)	64	-	-	-	dB
Rx Frequency Error Tolerated	66		+/- 1.0		kHz
Rx Co-channel Rejection	65	-	-	-	dB
Rx Adjacent Channel Rejection	67	-	>63	-	dB

Notes:

62	Determined by the accuracy of the Xtal oscillator provided.
63	Transmitting continuous PRBS data. This is a differential voltage; I Output = IOUTPUTP-IOUTPUTN and Q Output = IOUTPUTP-IOUTPUTN.
64	See section 8.4
65	See section 8.5
66	Optimum performance is achieved with 0Hz frequency error. The figure quoted is for a symbol rate of 9.6ksymbols/s. The frequency error tolerated is proportional to the symbol rate.
67	Measured as per EN 300 113, offset = 12.5kHz. 8kbps, BT = 0.3

12.1.5 7164FI-2.x Parametric Performance

For the following conditions unless otherwise specified:
External components as recommended in section 5.

Maximum load on digital outputs = 30pF.

Clock source = 19.2MHz $\pm$0.002% (20ppm) clock input; T_{AMB} = $-40°C$ to +85°C.

AV_{DD} = DV_{DD} = 3.0V to 3.6V.

Reference signal level = 308mV rms at 1kHz with AV_{DD} = 3.3V

Signal levels track with supply voltage, so scale accordingly.

Signal-to-Noise Ratio (SNR) in bit rate bandwidth.

Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device when loaded with FI-2.x only. The use of other valid Function Images™, can modify the parametric performance of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current					
Rx Mode					
DI_{DD} (4.8ksymbols/s – search for FS)		–	12.9	–	mA
DI_{DD} (9.6ksymbols/s – search for FS)		–	20.2	–	mA
DI_{DD} (4.8ksymbols/s – FS found)		–	8.7	–	mA
DI_{DD} (9.6ksymbols/s – FS found)		–	11.6	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	7.7	–	mA
Tx Mode	69				
DI_{DD} (4.8ksymbols/s)		–	6.4	–	mA
DI_{DD} (9.6ksymbols/s)		–	9.2	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	8.0	–	mA

Notes:

69   Transmitting in I/Q mode, continuous 4-FSK PRBS, all GPIOs and RAMDAC set to manual.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate		2 000		10 000	sym s^{-1}
Modulation			2-FSK or		
Filter RRC Alpha			0.2		
Tx Bit-rate Accuracy	70		-		ppm
Tx Output Level (I Output, Q Output)	71				
FI-2.x I/Q modulation mode			2.6		Vp-p
FI-2.x Two-point modulation mode			4.1		Vp-p
Tx Adjacent Channel Power (I Output, Q Output, PRBS)	72	-	-	-	dB
Rx Frequency Error Tolerated	75		+/- 1.0		kHz
Rx Co-channel Rejection	73	-	-	-	dB
Rx Adjacent Channel Rejection	73	-	-	-	dB

Notes:

70	Determined by the accuracy of the Xtal oscillator provided.
71	Transmitting continuous PRBS data. This is a differential voltage; I Output = IOUTPUTP-IOUTPUTN and Q Output = IOUTPUTP-IOUTPUTN.
72	See section 9.5 7164FI-2.x Typical Transmit Performance
73	See section 9.6 7164FI-2.x Typical Receive Performance
75	Optimum performance is achieved with 0Hz frequency error. The figure quoted is for a symbol rate of 9.6ksymbols/s. The frequency error tolerated is proportional to the symbol rate.

12.1.6 7164FI-4.x Parametric Performance

For the following conditions unless otherwise specified:
External components as recommended in section 5.

      Maximum load on digital outputs = 30pF.

      Clock source = 19.2MHz $\pm$0.002% (20ppm) clock input; T_{AMB} = $-$40°C to +85°C.

      AV_{DD} = DV_{DD} = 3.0V to 3.6V.

      Reference signal level = 308mV rms at 1kHz with AV_{DD} = 3.3V

      Signal levels track with supply voltage, so scale accordingly.

      Signal-to-Noise Ratio (SNR) in bit rate bandwidth.

      Input stage gain = 0dB, Output stage attenuation = 0dB.

      All figures quoted in this section apply to the device when loaded with FI-4.x only. The use of other valid Function Images™, can modify the parametric performance of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current					
Rx Mode					
DI_{DD} (9.6ksymbols/s – search for FS)	80	–	15.7 to 21.0	–	mA
DI_{DD} (18ksymbols/s – search for FS)	80	–	24.1 to 34.1	–	mA
DI_{DD} (9.6ksymbols/s – FS found)		–	11.0	–	mA
DI_{DD} (18ksymbols/s – FS found)		–	15.4	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	7.7	–	mA
Tx Mode	81				
DI_{DD} (9.6ksymbols/s)		–	7.5	–	mA
DI_{DD} (18ksymbols/s)		–	11.1	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	8.0	–	mA

Notes:

80   A lower current is measured when searching for FrameSync1, a higher current is measured when doing automatic modulation detection.

81   Transmitting continuous 16-QAM PRBS, all GPIOs and RAMDAC set to manual.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate		2 000		20 000	sym s^{-1}
Modulation			QAM		
Filter RRC Alpha	96		0.2 or 0.35		
Tx Bit-rate Accuracy	90		-		ppm
Tx Output Level (I Output, Q Output)	91				
FI-4.x I/Q modulation mode			2.6		Vp-p
Tx Adjacent Channel Power (I Output, Q Output, PRBS)	92	-	-	-	dB
Rx Frequency Error Tolerated	95		+/- 1.0		kHz
Rx Co-channel Rejection	93	-	-	-	dB
Rx Adjacent Channel Rejection	93	-	-	-	dB

Notes:

90	Determined by the accuracy of the Xtal oscillator provided.
91	Transmitting continuous PRBS data. This is a differential voltage; I Output = IOUTPUTP-IOUTPUTN and Q Output = IOUTPUTP-IOUTPUTN.
92	See section 10.5 7164FI-4.x Typical Transmit Performance
93	See section 10.6 7164FI-4.x Typical Receive Performance
95	Optimum performance is achieved with 0Hz frequency error. The figure quoted is for a symbol rate of 18ksymbols/s. The frequency error tolerated is proportional to the symbol rate.
96	A user programmable filter option is also provided, allowing for compensation for external hardware and different α values than those provided.

12.1.7 7164FI-6.x Parametric Performance

For the following conditions unless otherwise specified:
External components as recommended in Section 5.

Maximum load on digital outputs = 30pF.
Clock source = 19.2MHz (clock input); T_{AMB} = $-40°C$ to $+85°C$.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.

All figures quoted in this section apply to the device when loaded with FI-6.x only. The use of other valid Function Images™, can modify the parametric performance of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current					
Rx Mode					
DI_{DD} (– search for FS)		–	1.4	–	mA
DI_{DD} (– FS found)		–	2.5	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	7.8	–	mA
Tx Mode	70				
DI_{DD} (1200symbols/s)		–	1.3	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	7.8	–	mA

Notes:

70   Transmitting in I/Q mode, continuous PRBS, all GPIOs and RAMDAC set to manual.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate			1200 or 300		sym s^{-1}
Modulation			V.23		
Tx Bit-rate Accuracy	72		-		Ppm
Tx Output Level (I Output, Q Output)	73		2.6		Vp-p
Tx Adjacent Channel Power (I Output, Q Output, PRBS)	74	-	-	-	dB
Rx Frequency Error Tolerated	76		+/- 2		kHz
Rx Co-channel Rejection		-	-	-	dB
Rx Adjacent Channel Rejection	75	-	-	-	dB

Notes:

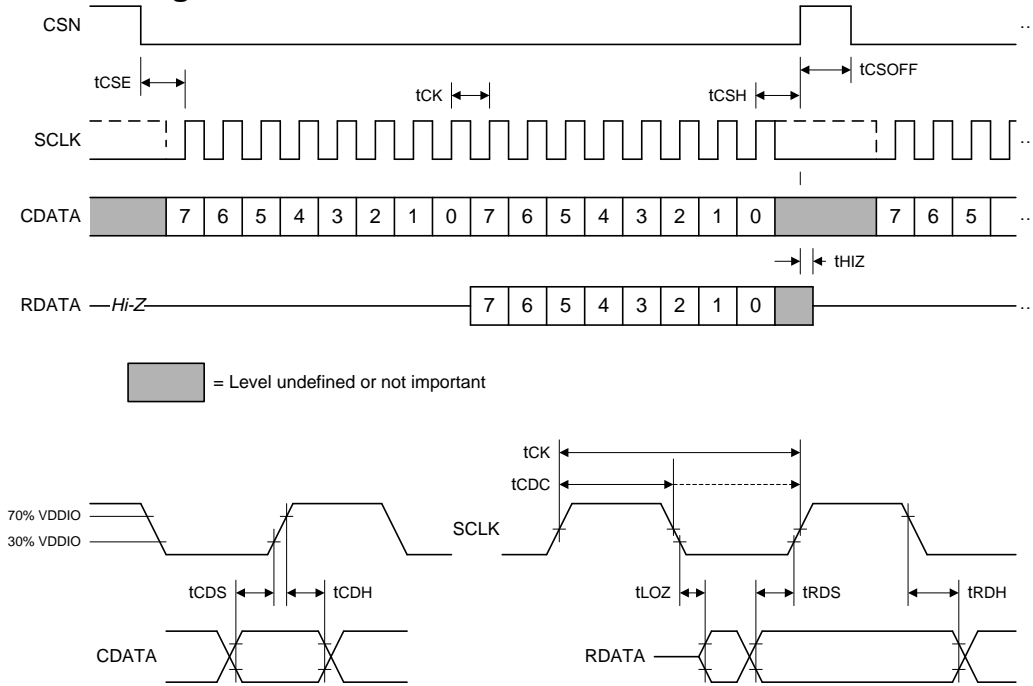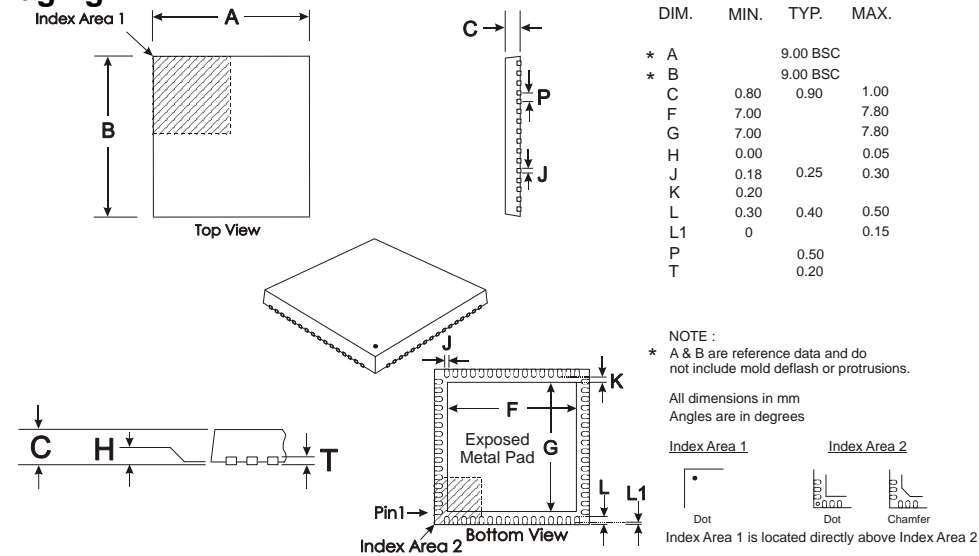|	
72	Determined primarily by the accuracy of the Xtal oscillator provided.
73	Transmitting continuous default preamble.
74	See Section 11.4
75	See Section 11.5
76	Optimum performance is achieved with 0Hz frequency error.

12.2 C-BUS Timing

Figure 113 C-BUS Timing

AC Parameters	Notes	Min.	Typ.	Max.	Unit
C-BUS Timing	1, 2				
Input pin rise/fall time (10% - 90% of VDDIO)		–	–	3	ns
Capacitive load on RDATA and IRQN		–	–	30	pF
tCSE CSN enable to SCLK high time		40	–	–	ns
tCSH Last SCLK high to CSN high time		40	–	–	ns
tLOZ SCLK low to RDATA output enable time		0	–	–	ns
tHIZ CSN high to RDATA high impedance		–	–	40	ns
tCSOFF CSN high time between transactions		50	–	–	ns
tCK SCLK cycle time		100	–	–	ns
tCDC SCLK duty cycle		40	–	60	%
tCDS CDATA setup time		25	–	–	ns
tCDH CDATA hold time		25	–	–	ns
tRDS RDATA setup time		25	–	–	ns
tRDH RDATA hold time		0	–	–	ns

Notes: 1.   Depending on the command, 1, 2 or more bytes of CDATA are sent to the peripheral MSB first, LSB (Bit 0) last. RDATA is read from the peripheral MSB first, LSB (Bit 0) last.
2.   Commands are acted upon between the last rising edge of SCLK of each command and the rising edge of the CSN signal.

12.3 Packaging

DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 114 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7164Q1

DIM.	MIN.	TYP.	MAX.
* A	9.80		10.20
* B	9.80		10.20
C	1.40		1.60
D	11.80		12.20
E	11.80		12.20
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
P		0.50	
T	0.09		0.20
X	0°		7°
Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
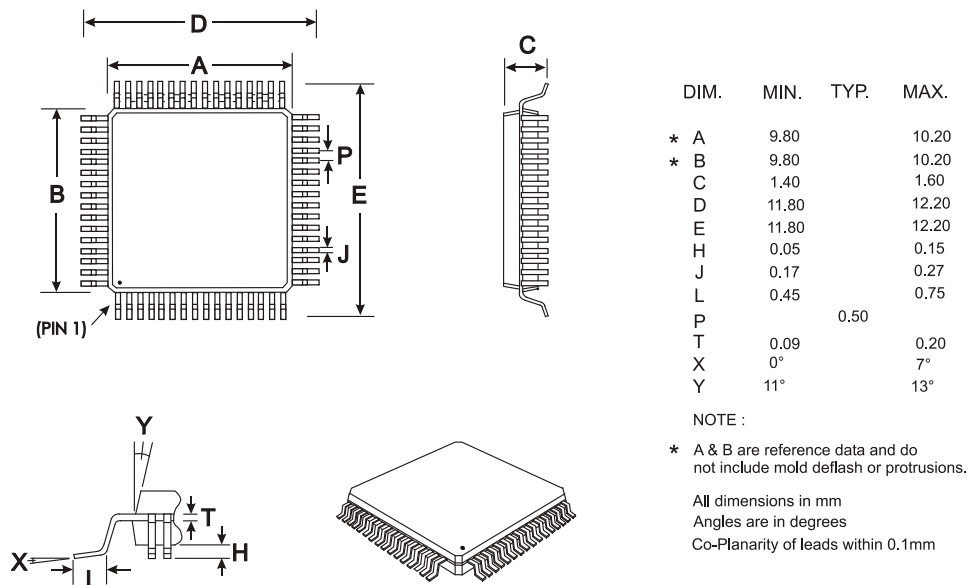Co-Planarity of leads within 0.1mm

Figure 115 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7164L9

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Design Support/Package Information page of the CML website: [www.cmlmicro.com].

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CML Microcircuits (UK) Ltd COMMUNICATION SEMICONDUCTORS	**CML Microcircuits (USA) Inc.** COMMUNICATION SEMICONDUCTORS	**CML Microcircuits (Singapore) Pte Ltd** COMMUNICATION SEMICONDUCTORS
Tel: +44 (0)1621 875500 **Fax:** +44 (0)1621 875600 **Sales:** sales@cmlmicro.com **Tech Support:** techsupport@cmlmicro.com	**Tel:** +1 336 744 5050 800 638 5577 **Fax:** +1 336 744 5054 **Sales:** us.sales@cmlmicro.com **Tech Support:** us.techsupport@cmlmicro.com	**Tel:** +65 62 888129 **Fax:** +65 62 888230 **Sales:** sg.sales@cmlmicro.com **Tech Support:** sg.techsupport@cmlmicro.com

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